MAX2682EUT
Rev. A

RELIABILITY REPORT

FOR

MAX2682EUT

PLASTIC ENCAPSULATED DEVICES

October 4, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2682 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2682 miniature, low-cost, low-noise downconverter mixer is designed for low-voltage operation and is ideal for use in portable communications equipment. Signals at the RF input port are mixed with signals at the local oscillator (LO) port using a double-balanced mixer. This downconverter mixer operates with RF input frequencies between 400MHz and 2500MHz, and downconvert to IF output frequencies between 10MHz and 500MHz.

The MAX2682 operates from a single +2.7V to +5.5V supply, allowing it to be powered directly from a 3-cell NiCd or a 1-cell Lithium battery. This device offers a wide range of supply currents and input intercept (IIP3) levels to optimize system performance. Additionally, this device features a low-power shutdown mode in which it typically draws less than 0.1µA of supply current. Consult the Selector Guide for various combinations of IIP3 and supply current.

The MAX2682 is manufactured on a high-frequency, low-noise, advanced silicon-germanium process and is offered in the space-saving 6-pin SOT23 package.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6.0V
RFIN Input Power (50½Source)	+10dBm
LO Input Power (50½Source)	+10dBm
SHDN, IFOUT, RFIN to GND	-0.3V to (VCC + 0.3V)
LO to GND	(VCC - 1V) to (VCC + 0.3V)
Continuous Power Dissipation (TA = +70°C)	
SOT23-6 (derate 8.7mW/°C above +70°C)	696mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°

II. Manufacturing Information

A. Description/Function: 400MHz to 2.5GHz, Low-Noise, SiGe Downconverter Mixers

B. Process: GST33

C. Number of Device Transistors: 83

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia or Thailand

F. Date of Initial Production: October, 1998

III. Packaging Information

A. Package Type: 6-Pin SOT

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-7001-0322

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 36 x 33 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: Metal1: 1.2; Metal2: 1.2; Metal3: 2.8; Metal4: 5.6 microns (as drawn)

F. Minimum Metal Spacing: Metal1: 1.3; Metal2: 1.4; Metal3: 2.6; Metal4: 2.6 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.78 \times 10^{-8}$ λ = 10.78 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The aBurn-In Schematic shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR22-2 die type has been found to have all pins able to withstand a transient pulse of <250V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX2682EUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

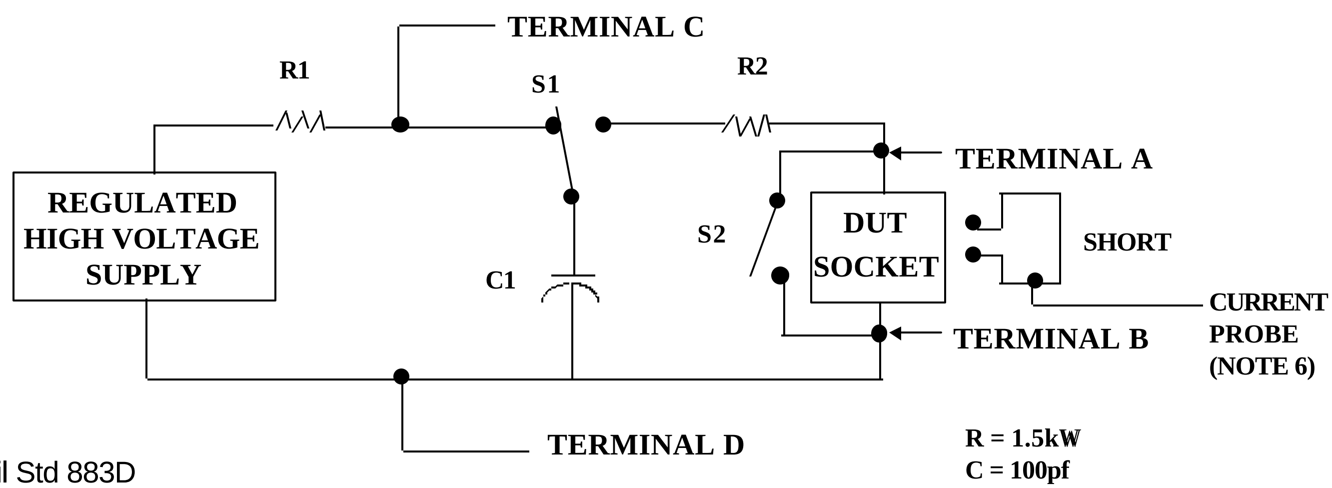
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

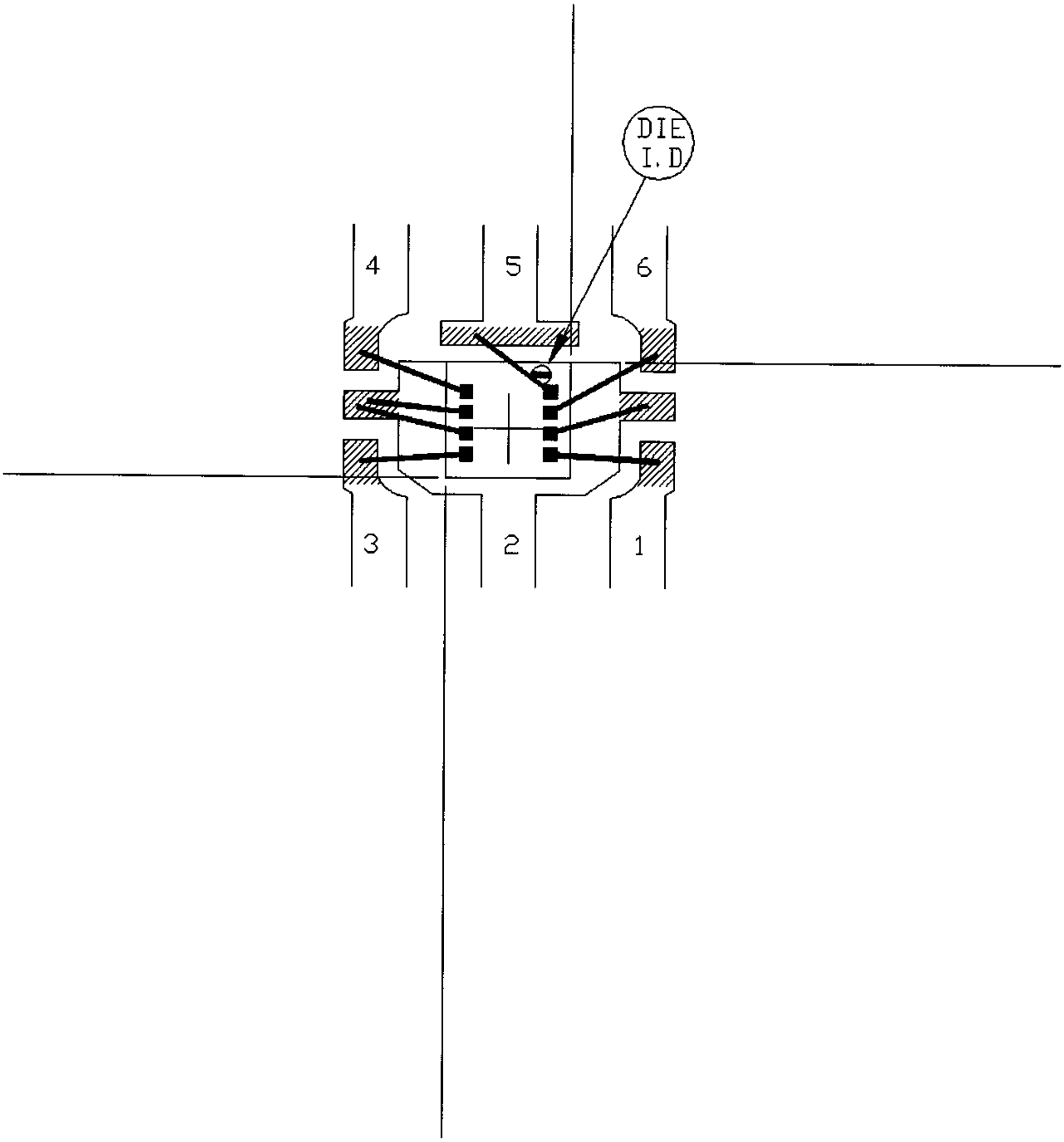
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: U6-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64x38	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0322 / REV.: C