

## MAX232E Dual RS-232 Driver and Receiver With IEC61000-4-2 Protection

### 1 Features

- Meets or Exceeds TIA/RS-232-F and ITU Recommendation V.28
- ESD Protection for RS-232 Bus Pins
  - ±15-kV Human-Body Model (HBM)
  - ±8-kV IEC61000-4-2, Contact Discharge
  - ±15-kV IEC61000-4-2, Air-Gap Discharge
- Operates From a Single 5-V Power Supply With 1-μF Charge-Pump Capacitors
- Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- Low Supply Current: 8 mA Typical

### 2 Applications

- TIA/RS-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

### 3 Description

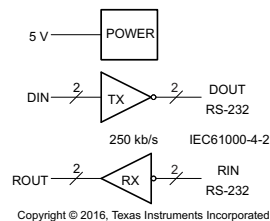
The MAX232E is a dual driver and receiver that includes a capacitive voltage generator to supply RS-232-F compliant voltage levels from a single 5-V supply. Each receiver converts RS-232 inputs to 5-V TTL/CMOS levels. This receiver has a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/RS-232-F levels.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
MAX232ECD MAX232EID	SOIC (16)	9.90 mm × 3.91 mm
MAX232ECDW MAX232EIDW	SOIC WIDE (16)	10.30 mm × 7.50 mm
MAX232ECN MAX232EIN	PDIP (16)	19.30 mm × 6.35 mm
MAX232ECPW MAX232EIPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.1 Overview .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	8.3 Feature Description .....	<b>9</b>
<b>4 Revision History</b> .....	<b>2</b>	8.4 Device Functional Modes .....	<b>10</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Applications and Implementation</b> .....	<b>11</b>
<b>6 Specifications</b> .....	<b>4</b>	9.1 Application Information .....	<b>11</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	9.2 Typical Application .....	<b>11</b>
6.2 ESD Ratings .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>13</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	<b>11 Layout</b> .....	<b>13</b>
6.4 Thermal Information .....	<b>4</b>	11.1 Layout Guidelines .....	<b>13</b>
6.5 Electrical Characteristics .....	<b>5</b>	11.2 Layout Example .....	<b>13</b>
6.6 Electrical Characteristics: Driver .....	<b>5</b>	<b>12 Device and Documentation Support</b> .....	<b>14</b>
6.7 Electrical Characteristics: Receiver .....	<b>5</b>	12.1 Receiving Notification of Documentation Updates .....	<b>14</b>
6.8 Switching Characteristics: Driver .....	<b>5</b>	12.2 Community Resources .....	<b>14</b>
6.9 Switching Characteristics: Receiver .....	<b>6</b>	12.3 Trademarks .....	<b>14</b>
6.10 Typical Characteristics .....	<b>6</b>	12.4 Electrostatic Discharge Caution .....	<b>14</b>
<b>7 Parameter Measurement Information</b> .....	<b>7</b>	12.5 Glossary .....	<b>14</b>
<b>8 Detailed Description</b> .....	<b>9</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>14</b>

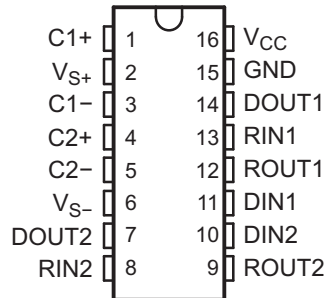
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (November 2009) to Revision C</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Deleted "±30-V Input Levels" from <i>Features</i> .....	<b>1</b>
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet .....	<b>1</b>
• Added MIN value ±3 to "Receiver input voltage (RIN1, RIN2) row in <i>Recommended Operating Conditions</i> .....	<b>4</b>
• Changed R <sub>θJA</sub> values in <i>Thermal Information</i> .....	<b>4</b>
• Deleted table note 3 from <i>Receiver Section Electrical Characteristics</i> .....	<b>5</b>
• Added a new row to the <i>Function Table for Each Receiver</i> .....	<b>10</b>

## 5 Pin Configuration and Functions

D, DW, N, or PW Package  
Add 16-Pin SOIC, PDIP, or TSSOP  
Top View



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	C1+	—	Positive lead of C1 capacitor
2	VS+	O	Positive charge pump output for storage capacitor only
3	C1-	—	Negative lead of C1 capacitor
4	C2+	—	Positive lead of C2 capacitor
5	C2-	—	Negative lead of C2 capacitor
6	VS-	O	Negative charge pump output for storage capacitor only
7	DOUT2	O	RS-232 line data output (to remote RS-232 system)
8	RIN2	I	RS-232 line data input (from remote RS-232 system)
9	ROUT2	O	Logic data output (to UART)
10	DIN2	I	Logic data input (from UART)
11	DIN1	I	Logic data input (from UART)
12	ROUT1	O	Logic data output (to UART)
13	RIN1	I	RS-232 line data input (from remote RS-232 system)
14	DOUT1	O	RS-232 line data output (to remote RS-232 system)
15	GND	—	Ground
16	VCC	—	Supply voltage—connect to external 5-V power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Input supply voltage <sup>(2)</sup>	-0.3	6	V
V <sub>S+</sub>	Positive output supply voltage	V <sub>CC</sub> - 0.3	15	V
V <sub>S-</sub>	Negative output supply voltage	-0.3	-15	V
V <sub>I</sub>	Input voltage	Driver	V <sub>CC</sub> + 0.3	V
		Receiver	±30	
V <sub>O</sub>	Output voltage	DOUT	V <sub>S-</sub> - 0.3 V <sub>S+</sub> + 0.3	V
		ROUT	-0.3 V <sub>CC</sub> + 0.3	
	Short-circuit duration	DOUT		Unlimited
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Pins 7, 8, 13, and 14	±15000	V
			Other pins	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	All pins	±1500	
			IEC61000-4-2, air-gap discharge	Pins 7, 8, 13, and 14	
		IEC61000-4-2, contact discharge		±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage (DIN1, DIN2)	2			V
V <sub>IL</sub>	Low-level input voltage (DIN1, DIN2)			0.8	V
	Receiver input voltage (RIN1, RIN2)	±3		±30	V
T <sub>A</sub>	Operating free-air temperature	MAX232EC	0	70	°C
		MAX232EI	-40	85	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)(2)(3)</sup>		MAX232E				UNIT
		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	73.8	73.4	43.3	101.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	33.4	35.1	30	29.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	31.4	38.3	23.3	47.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Thermal Information (continued)

THERMAL METRIC <sup>(1)(2)(3)</sup>		MAX232E				UNIT
		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$\Psi_{JT}$	Junction-to-top characterization parameter	5.8	9.4	14.4	1.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	31.1	37.7	23.2	46.6	°C/W

## 6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 10](#))

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$I_{CC}$	Supply current	$V_{CC} = 5.5\text{ V}$	All outputs open, $T_A = 25^\circ\text{C}$		8	10	mA

(1) Test conditions are  $C1 - C4 = 1\ \mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

## 6.6 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	DOUT	$R_L = 3\text{ k}\Omega$ to GND	5	7		V
$V_{OL}$	Low-level output voltage <sup>(3)</sup>	DOUT	$R_L = 3\text{ k}\Omega$ to GND		-7	-5	V
$r_o$	Output resistance	DOUT	$V_{S+} = V_{S-} = 0$ , $V_O = \pm 2\text{ V}$	300			$\Omega$
$I_{OS}$ <sup>(4)</sup>	Short-circuit output current	DOUT	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$		$\pm 10$		mA
$I_{IS}$	Short-circuit input current	DIN	$V_I = 0$			200	$\mu\text{A}$

(1) Test conditions are  $C1 - C4 = 1\ \mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

(4) Not more than one output should be shorted at a time.

## 6.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	ROUT	$I_{OH} = -1\text{ mA}$	3.5			V
$V_{OL}$	Low-level output voltage	ROUT	$I_{OL} = 3.2\text{ mA}$			0.4	V
$V_{IT+}$	Receiver positive-going input threshold voltage	RIN	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		1.7	2.4	V
$V_{IT-}$	Receiver negative-going input threshold voltage	RIN	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$	0.8	1.2		V
$V_{hys}$	Input hysteresis voltage	RIN	$V_{CC} = 5\text{ V}$	0.2	0.5	1	V
$r_i$	Receiver input resistance	RIN	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$	3	5	7	k $\Omega$

(1) Test conditions are  $C1 - C4 = 1\ \mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

## 6.8 Switching Characteristics: Driver

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT
SR	Driver slew rate	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See <a href="#">Figure 6</a>				30	V/ $\mu\text{s}$
SR(t)	Driver transition region slew rate	$R_L = 3\text{ k}\Omega$ , $C_L = 2.5\text{ nF}$ See <a href="#">Figure 7</a>			3		V/ $\mu\text{s}$
	Data rate	One DOUT switching			250		kbit/s

(1) Test conditions are  $C1 - C4 = 1\ \mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

### 6.9 Switching Characteristics: Receiver

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 5)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TYP	UNIT
$t_{PLH(R)}$ Receiver propagation delay time, low- to high-level output	$C_L = 50\text{ pF}$	500	ns
$t_{PHL(R)}$ Receiver propagation delay time, high- to low-level output	$C_L = 5\text{ 0pF}$	500	ns

(1) Test conditions are  $C_1 - C_4 = 1\text{ }\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

### 6.10 Typical Characteristics

$T_A = 25^\circ\text{C}$

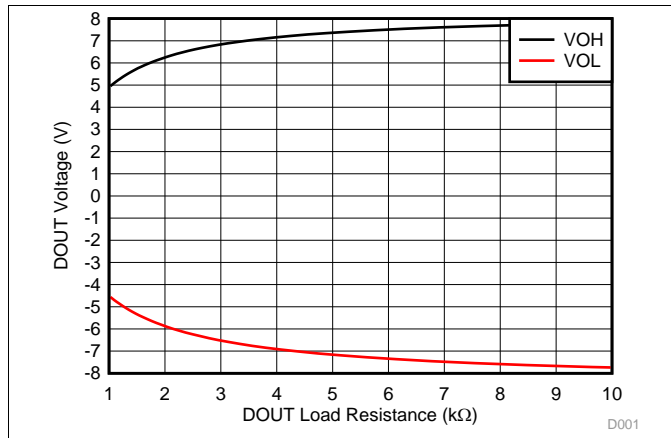


Figure 1. Driver Output Voltage vs Load Resistance

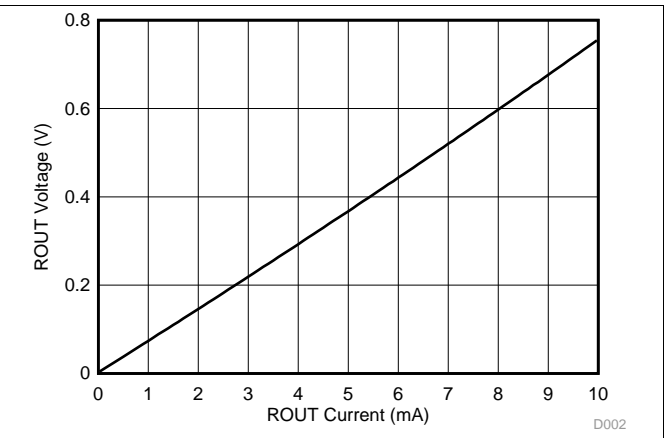


Figure 2. Receiver Low Output Voltage vs Load Current

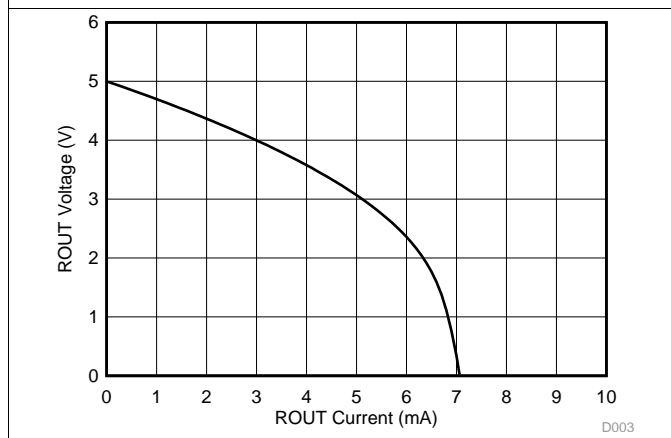


Figure 3. Receiver High Output Voltage vs Load Current

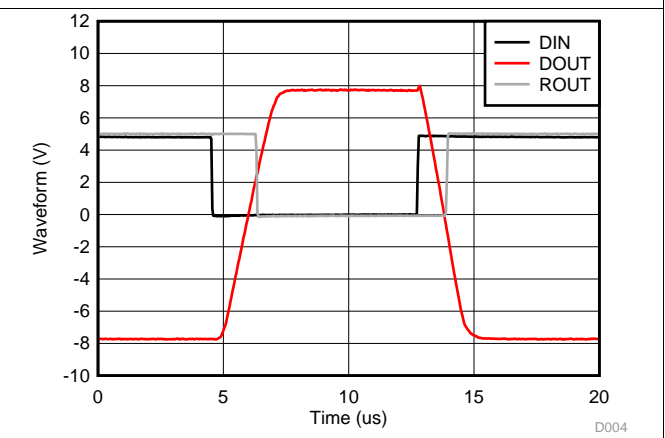
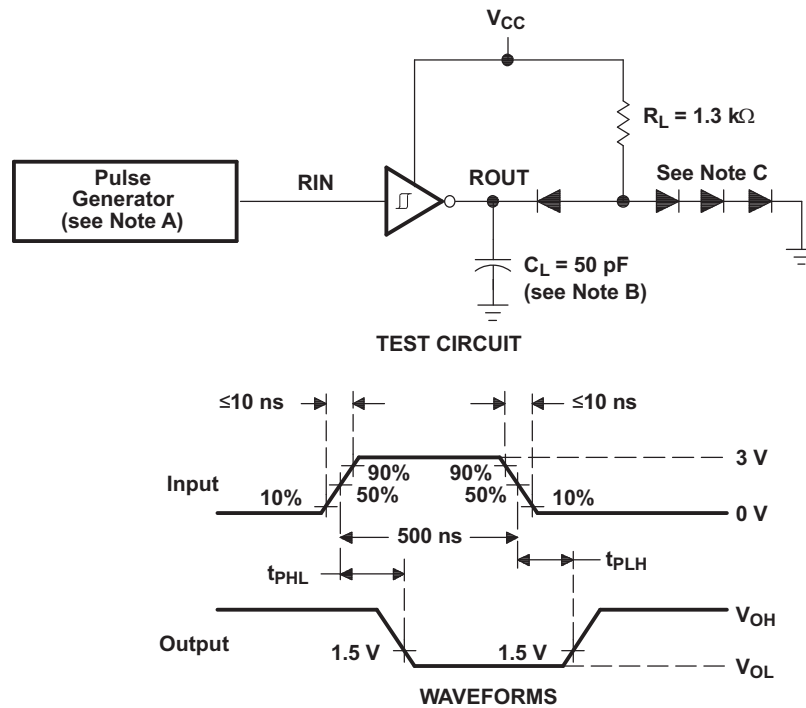


Figure 4. Loopback Waveforms  
Data Rate 120 kbit/s

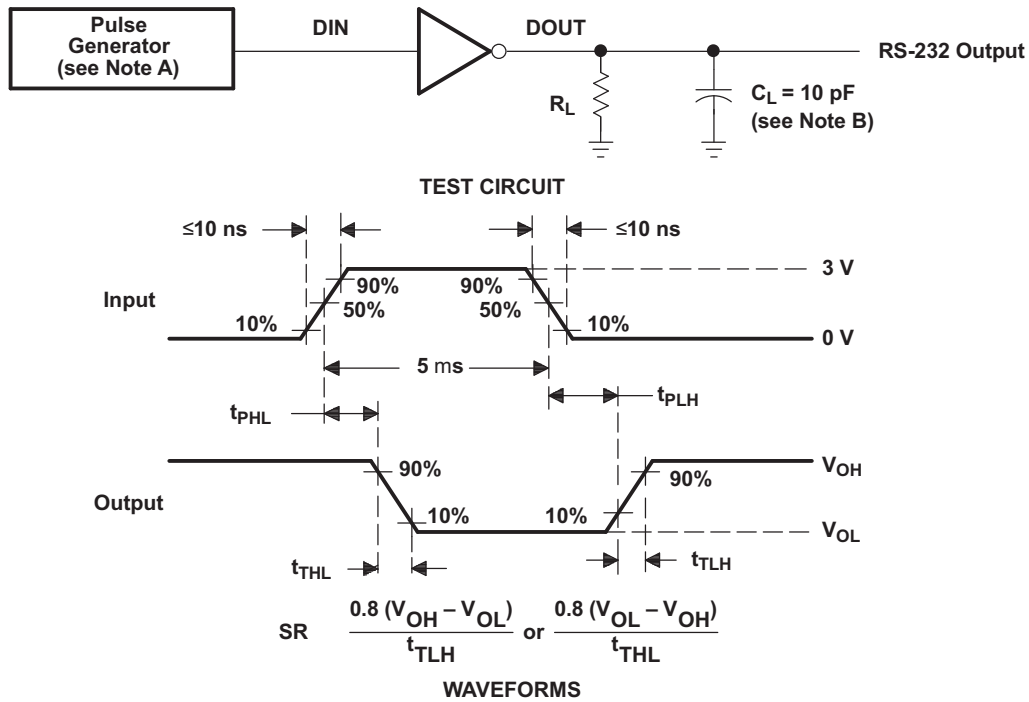
## 7 Parameter Measurement Information



- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

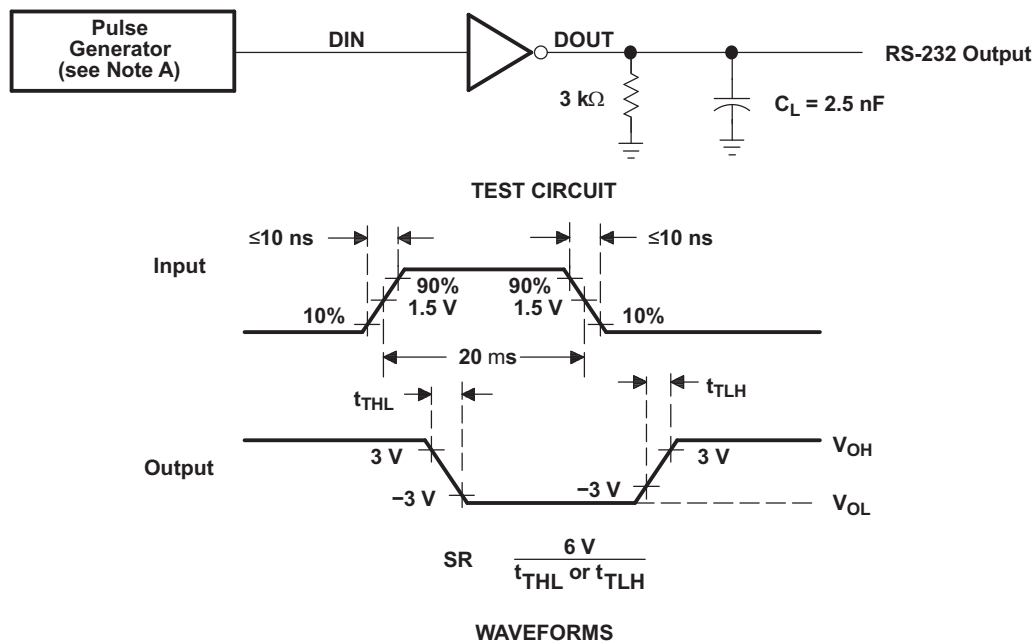
**Figure 5. Receiver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements**

Parameter Measurement Information (continued)



- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 6. Driver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements (5- $\mu\text{s}$  Input)



- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .

Figure 7. Test Circuit and Waveforms for  $t_{THL}$  and  $t_{TLH}$  Measurements (20- $\mu\text{s}$  Input)



## 8 Detailed Description

### 8.1 Overview

The MAX232E device is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. All RS-232 pins have 15-kV HBM and IEC61000-4-2 Air-Gap discharge protection. RS-232 pins also have 8-kV IEC61000-4-2 contact discharge protection. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to  $\pm 30$ -V inputs and decode inputs as low as  $\pm 3$  V. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

### 8.2 Functional Block Diagram

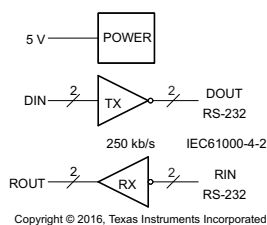


Figure 8. Logic Diagram (Positive Logic)

### 8.3 Feature Description

#### 8.3.1 Power

The power block increases and inverts the 5-V supply for the RS-232 driver using a charge pump that requires four 1- $\mu$ F external capacitors.

#### 8.3.2 RS-232 Driver

Two drivers interface standard logic level to RS-232 levels. Internal pullup resistors on DIN inputs ensures a high input when the line is high impedance.

#### 8.3.3 RS-232 Receiver

Two receivers interface RS-232 levels to standard logic levels. An open or shorted to ground input results in a high output on ROUT.

## 8.4 Device Functional Modes

### 8.4.1 $V_{CC}$ Powered by 5 V

The device is in normal operation.

### 8.4.2 $V_{CC}$ Unpowered

When MAX232E is unpowered, it can be safely connected to an active remote RS-232 device.

### 8.4.3 Truth Tables

[Table 1](#) and [Table 2](#) list the functions of this device.

**Table 1. Function Table for Each Driver<sup>(1)</sup>**

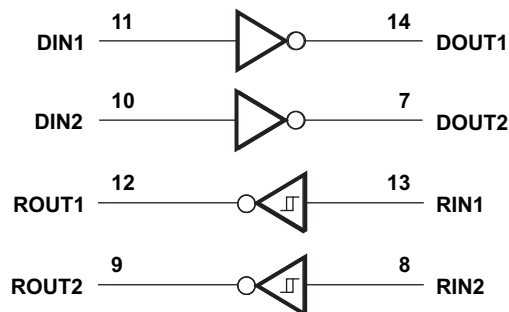
INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

**Table 2. Function Table for Each Receiver<sup>(1)</sup>**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off



**Figure 9. Logic Diagram (Positive Logic)**

## 9 Applications and Implementation

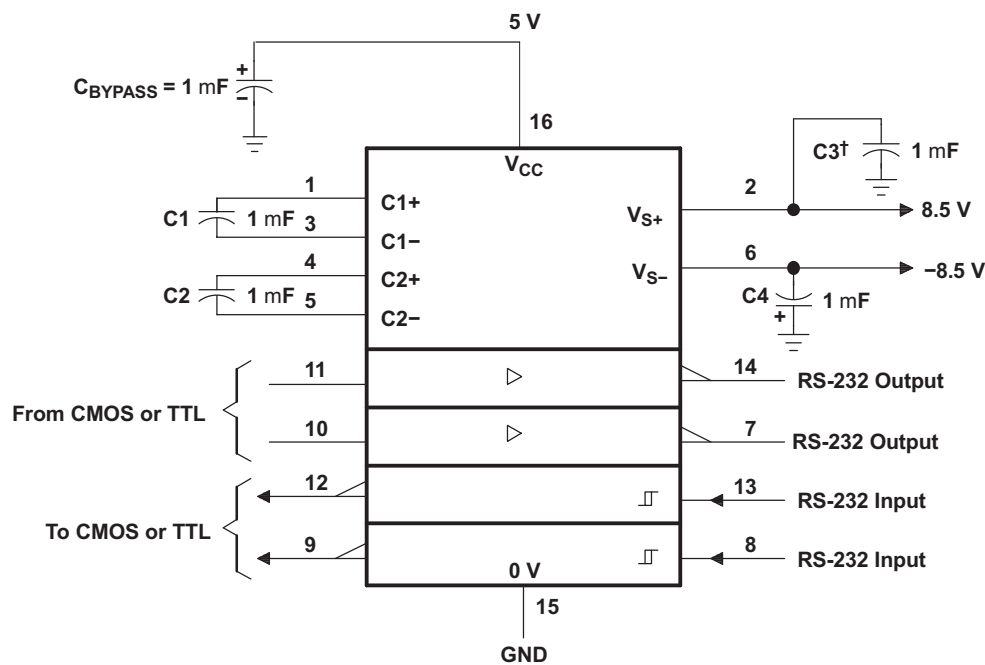
### NOTE

Information in the following applications and implementation sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

For proper operation add capacitors as shown in Figure 10. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

### 9.2 Typical Application



† C3 can be connected to  $V_{CC}$  or GND.

Copyright © 2016, Texas Instruments Incorporated

Resistor values shown are nominal.

Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 10. Typical Operating Circuit

#### 9.2.1 Design Requirements

- $V_{CC}$  minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 250 kbit/s.

#### 9.2.2 Detailed Design Procedure

The capacitor type used for C1–C4 is not critical for proper operation. The MAX232E requires 1- $\mu$ F capacitors, although capacitors up to 10  $\mu$ F can be used without harm. Ceramic dielectrics are suggested for capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on  $V+$  and  $V-$ .

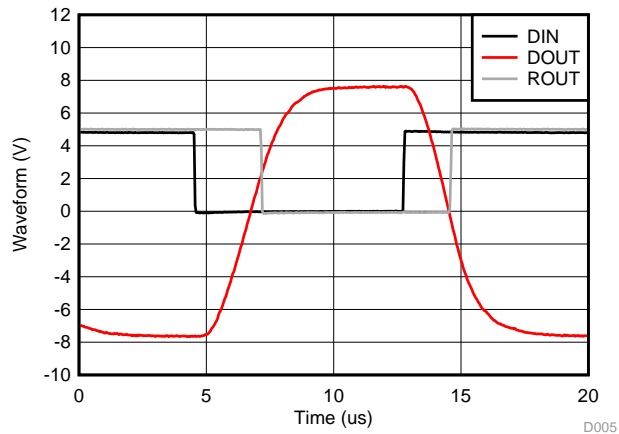
## Typical Application (continued)

Use larger capacitors (up to 10  $\mu\text{F}$ ) to reduce the output impedance at  $V_{S+}$  and  $V_{S-}$ .

Bypass  $V_{CC}$  to ground with at least 1  $\mu\text{F}$ . In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{CC}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

### 9.2.3 Application Curve

Loopback waveform connects DOUT to RIN.



Date Rate = 120 kbit/s,  $C_L = 1 \text{ nF}$

**Figure 11. Loopback Waveforms**

## 10 Power Supply Recommendations

The  $V_{CC}$  voltage should be connected to the same power source used for logic device connected to DIN and ROUT pins.  $V_{CC}$  should be between 4.5 V and 5.5 V.

## 11 Layout

### 11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX232E ground pin and circuit board's ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

### 11.2 Layout Example

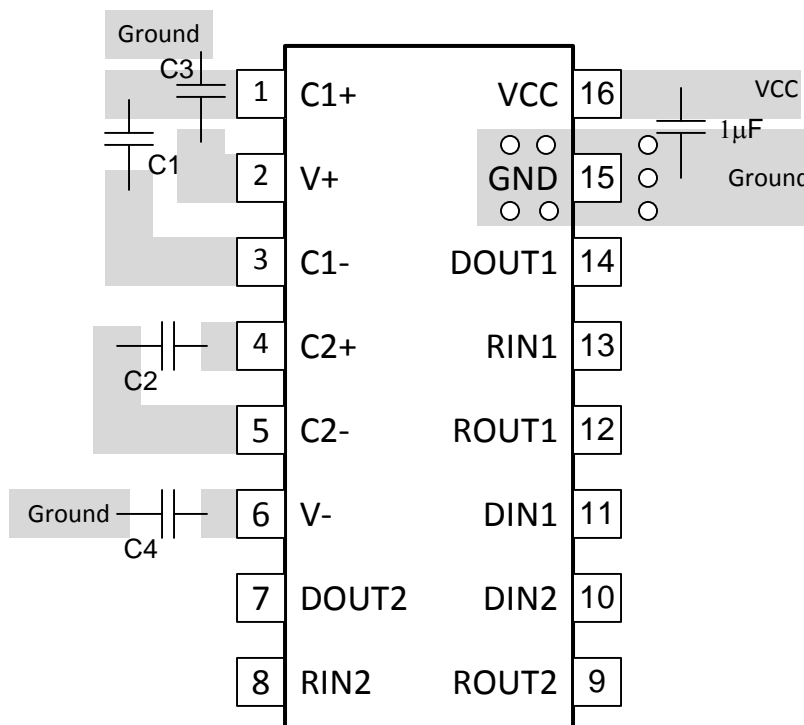


Figure 12. MAX232E Layout

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX232ECD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	<a href="#">Samples</a>
MAX232ECDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	<a href="#">Samples</a>
MAX232ECDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	<a href="#">Samples</a>
MAX232ECDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	MAX232EC	<a href="#">Samples</a>
MAX232ECDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	<a href="#">Samples</a>
MAX232ECDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX232EC	<a href="#">Samples</a>
MAX232ECN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MAX232ECN	<a href="#">Samples</a>
MAX232ECNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MAX232ECN	<a href="#">Samples</a>
MAX232ECPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA232EC	<a href="#">Samples</a>
MAX232ECPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	0 to 70	MA232EC	<a href="#">Samples</a>
MAX232ECPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA232EC	<a href="#">Samples</a>
MAX232EID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>
MAX232EIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>
MAX232EIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>
MAX232EIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>
MAX232EIDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>
MAX232EIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX232EIDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX232EI	<a href="#">Samples</a>
MAX232EIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	MAX232EIN	<a href="#">Samples</a>
MAX232EINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	MAX232EIN	<a href="#">Samples</a>
MAX232EIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI	<a href="#">Samples</a>
MAX232EIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI	<a href="#">Samples</a>
MAX232EIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB232EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232ECDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232ECPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX232ECDR	SOIC	D	16	2500	367.0	367.0	38.0
MAX232ECDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232ECDWRG4	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232ECPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
MAX232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX232ECPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX232EIDR	SOIC	D	16	2500	367.0	367.0	38.0
MAX232EIDWR	SOIC	DW	16	2000	367.0	367.0	38.0
MAX232EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

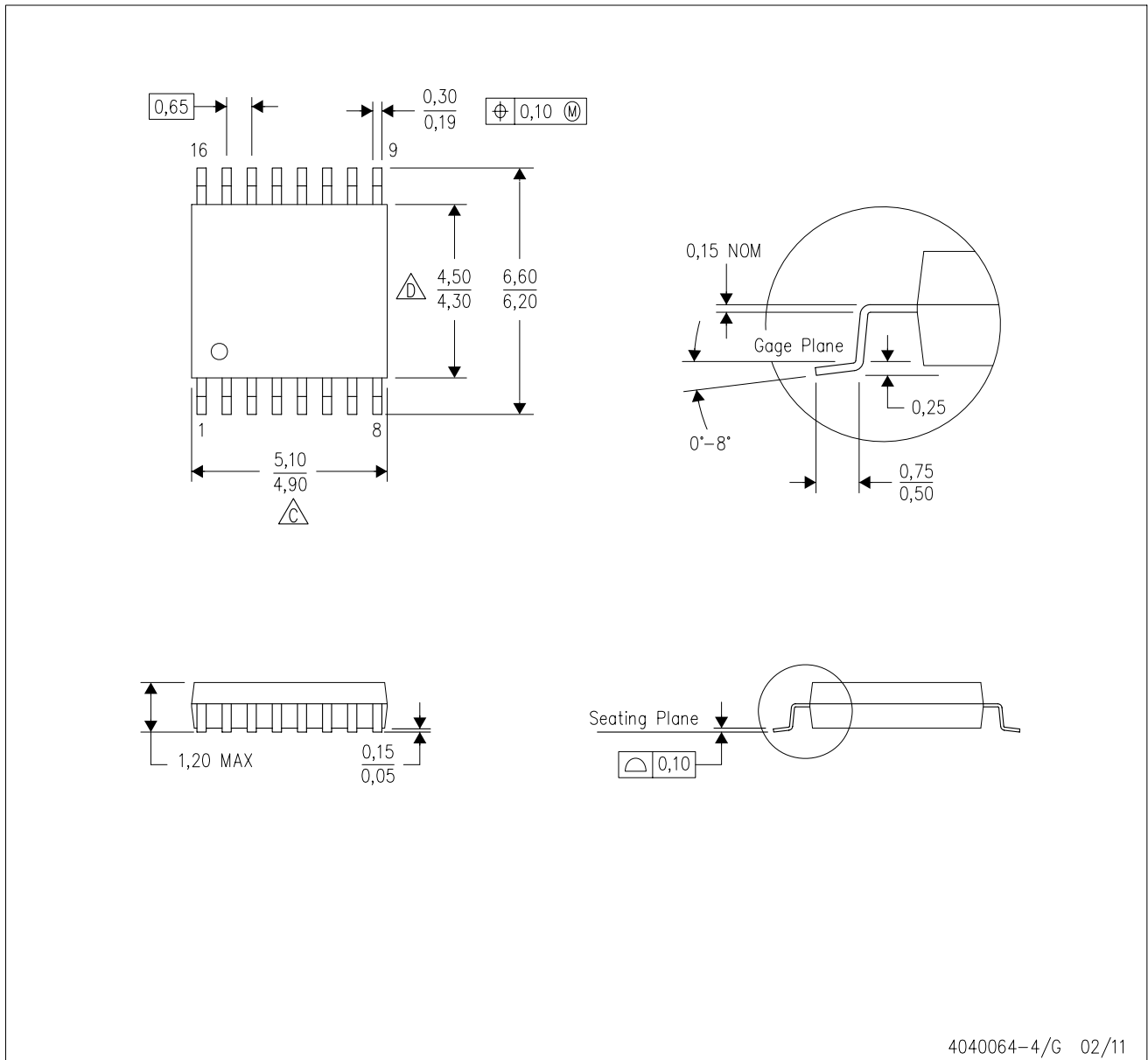


4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

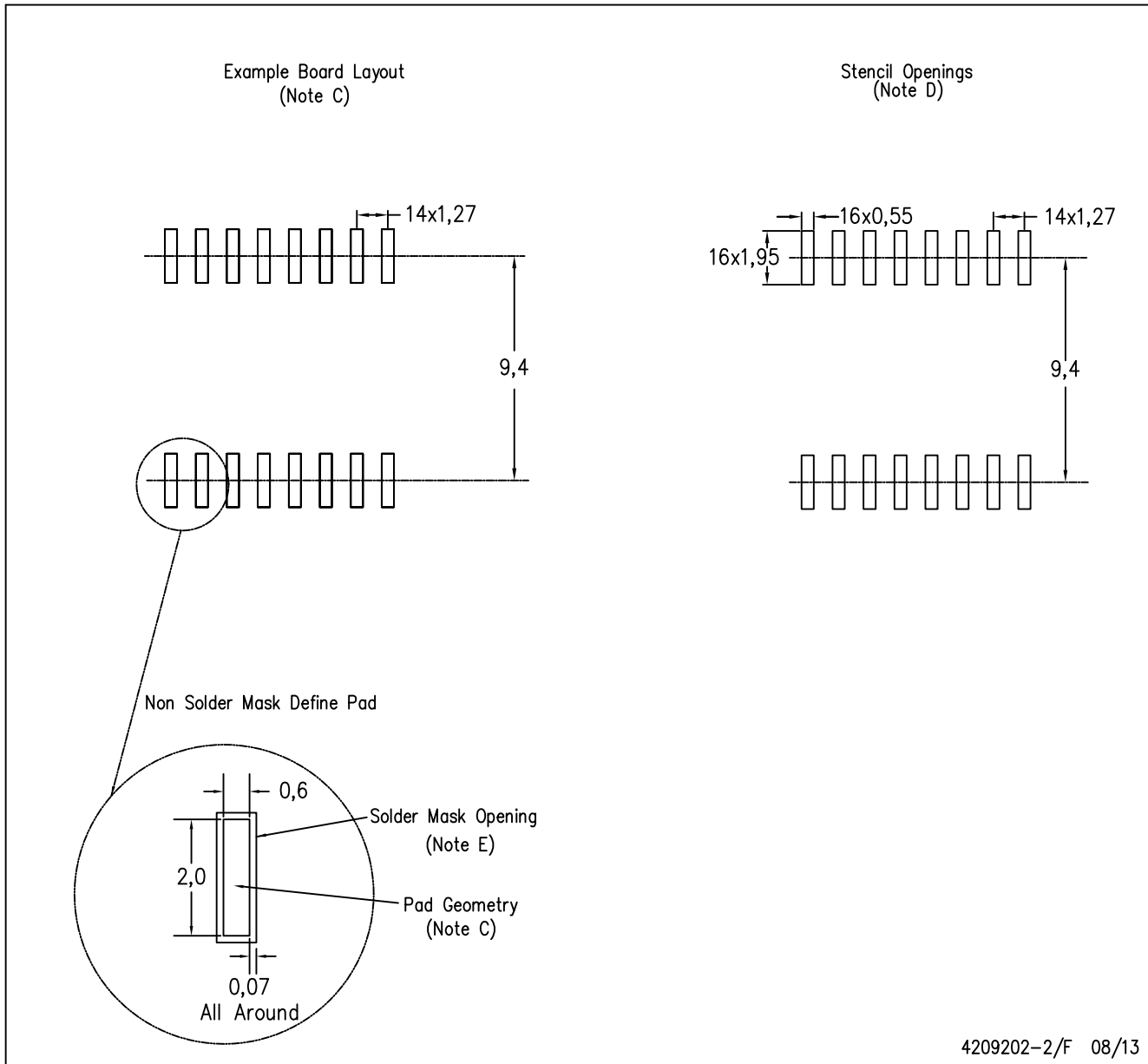
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)