MAX14736/MAX14737

Precision, Ultra-Fast, Low Supply Current, Bidirectional Overvoltage Protector

General Description

The MAX14736/MAX14737 overvoltage-protection (OVP) devices guard battery-powered modules in portable devices against overvoltage faults. The low 15mΩ (typ) on-resistance, as well as the low 13µA (typ) quiescent supply current of the devices, minimize power consumption, making them an ideal choice for low-power systems. Additionally, the devices feature a precision overvoltage-lockout (OVLO) threshold, ultra-fast response time, and surge suppression to ±35V, which serve to provide excellent protection against even high slew-rate, high-voltage transients.

The integrated power transistor in the devices is a p-channel device, but the intrinsic body diode from OUT to IN is removed through appropriate design techniques. Consequently, when the switch is in the off state, reverse-current blocking that is inherent to the devices. The MAX14736/MAX14737 feature a push-pull POK output, which is driven low if either an overvoltage, undervoltage, or thermal fault is detected; or if the device is placed into shutdown mode.

The MAX14736 has an active-low enable pin ($\overline{EN}$), while the enable pin (EN) on the MAX14737 is active high.

When the enable pin is driven to the active state, the device is enabled. When driven to the inactive state, the device is placed in a low-power shutdown mode and the switch is kept in the off state.

The MAX14736/MAX14737 are offered in a small, 9-bump (1.34mm x 1.36mm) wafer-level package (WLP) and operate over the -40°C to +85°C extended temperature range.

Benefits and Features

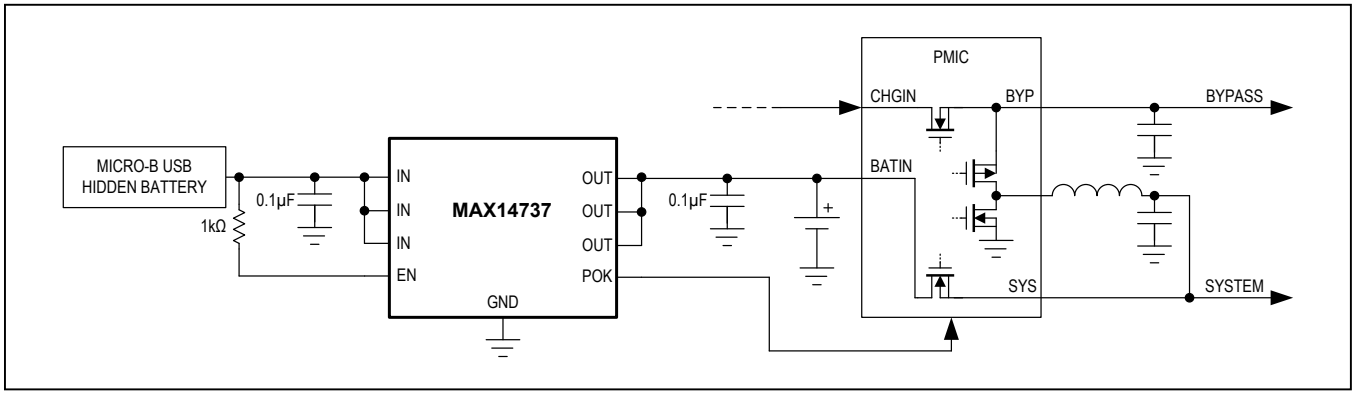
- Protects Battery-Connected Modules with Minimal Power Consumption
  - Wide Operating Input Voltage: +2.1V to +5.5V
  - 4.5A Continuous Current Capability
  - Integrated 15mΩ (typ) pFET
  - Ultra-Low Supply Current: 13µA (typ)
- Allows Precise Design in OVLO Implementation
  - Preset Accurate Internal OVP Thresholds
    - MAX14736: 4.7V ±2.0%
    - MAX14737: 5.2V ±2.0%
- Increases System Reliability Through Premium Security
  - Surge Immunity to ±35V
  - Soft-Start to Minimize Inrush Current
  - Output Hot Plug-In Protection
  - Thermal Shutdown
  - Ultra-Fast OVP Response Time: 200ns (typ)
- Minimizes Board Space by Compact WLP
  - 9-Bump 1.34mm x 1.36mm WLP

Applications

- Smartphones
- Tablet PCs
- e-Readers

Ordering Information ***appears at end of data sheet.***

Typical Application Circuit



19-7517; Rev 0; 5/15

Absolute Maximum Ratings

(All voltages referenced to GND.)
IN (Note 1), OUT, EN, $\overline{EN}$ .....-0.3V to +6V
POK.....-0.3V to max (IN,OUT) + 0.3V
Maximum Current into IN (DC) (Note 2) 4.5A
Peak Current into IN (10ms) 8A

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 11.9mW/°C above +70°C).....952mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 3)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....83.98°C/W

Note 1: Survives burst pulse up to ±40V with 2Ω minimum source resistance.
Note 2: Limited by thermal design.
Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = +2.1V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 4.3V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN, OUT							
Input Voltage Range	V_{IN}			2.1		5.5	V
Supply Current	I_{IN}	V_{IN} = 4.3V, no load			13	30	µA
IN Shutdown Current	I_{IN_Q}	Device disabled, V_{IN} = 4.3V, V_{OUT} = 0V			2	6	µA
OUT Shutdown Current		Device disabled, V_{OUT} = 5V, V_{IN} = 0V			2	6	µA
OVP							
On-Resistance (IN to OUT)	R_{ON}	V_{IN} = 4.3V, I_{OUT} = 100mA,			15	22	mΩ
Overvoltage Trip-Level Threshold	V_{OVLO}	V_{IN} rising	MAX14736	4.600	4.700	4.800	V
			MAX14737	5.095	5.200	5.305	V
Overvoltage Trip-Level Hysteresis	$V_{OVLO\_}$				100		mV
Undervoltage Trip-Level Threshold	V_{UVLO}				2.015		V
Undervoltage Trip-Level Hysteresis	$V_{UVLO\_}$				80		mV
OUT Load Capacitance	C_{OUT}				100		µF
DIGITAL OUTPUT (POK)							
Output Voltage Low	V_{OL}	I_{SINK} = 100µA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 100µA		1.4			V

Electrical Characteristics (continued)

(V_{IN} = +2.1V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = 4.3V, T_A = +25ºC, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE INPUT (EN, $\overline{EN}$) (FIGURE 1)						
EN, $\overline{EN}$ Input High Current	I_{EN_H}	V_{IN} = 5.5V, V_{EN} = 3.0V, $V_{\overline{EN}}$ = 3.0V (internal 650kΩ connected to GND)		4.6		µA
EN, $\overline{EN}$ Input Low Current	I_{EN_L}	V_{EN} = 0V, $V_{\overline{EN}}$ = 0V	-0.1		+0.1	µA
EN, $\overline{EN}$ Input Voltage High	V_{IH}		1.6			V
EN, $\overline{EN}$ Input Voltage Low	V_{IL}				0.4	V
TIMING CHARACTERISTICS (NOTE 5)						
Debounce Time	t_{DEB}	From V_{EN} = 3.0V, $V_{\overline{EN}}$ = 0V to when POK goes high		15		ms
Soft-Start Time	t_{SS}			30		ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_L = 100Ω, C_L = 100µF, V_{OUT} = 10% to 90% of V_{IN}		4		ms
Switch Turn-Off Response Time	t_{OFF_RES}	V_{IN} = $V_{OVLO(MIN)}$; V_{IN} rising at 2V/µs until V_{OUT} stops rising, R_L =		200		ns
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			150		°C
Thermal Hysteresis	T_{HYS}			20		°C
ESD PROTECTION						
Human Body Model		All pins		±2		kV
		IN pin, with 0.1µF bypass capacitor		±15		kV

Note 4: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 5: All timing characteristics are measured using 20% to 80% levels, unless otherwise noted.

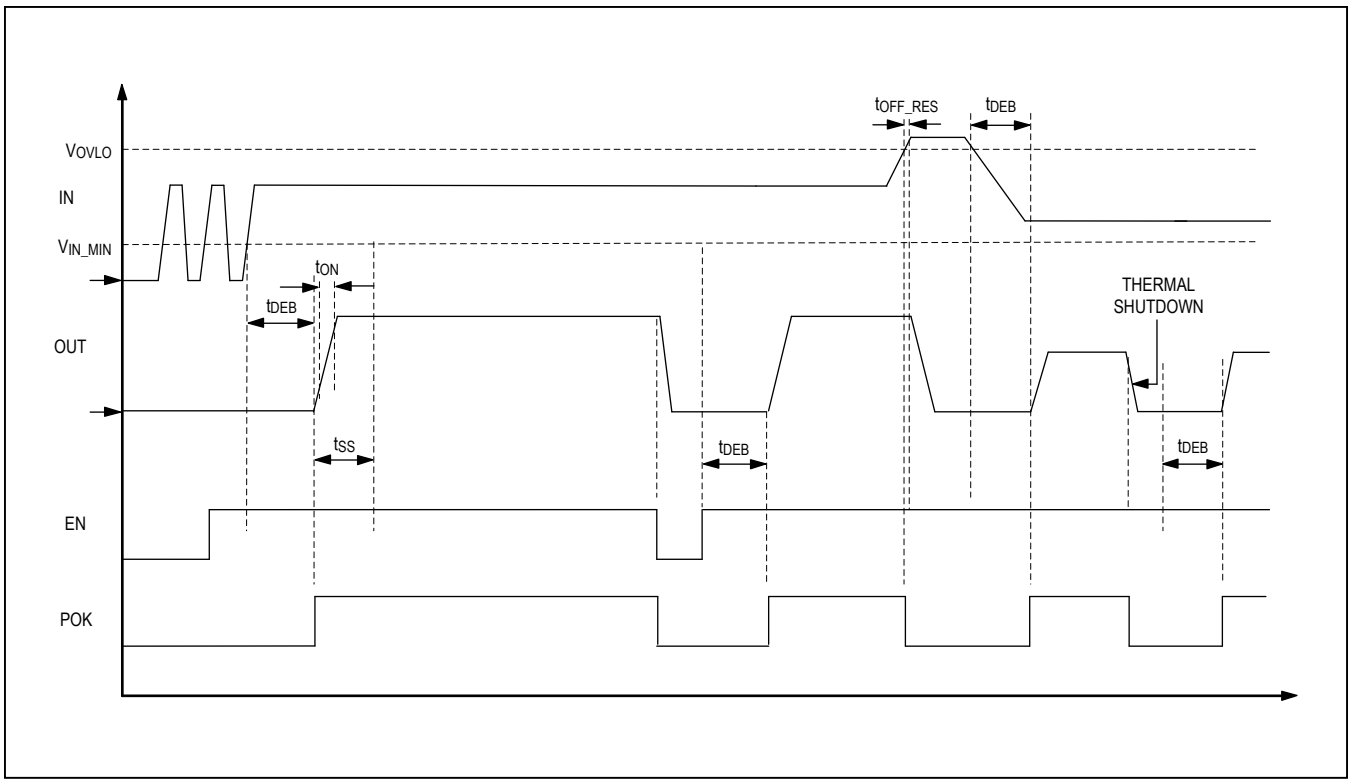
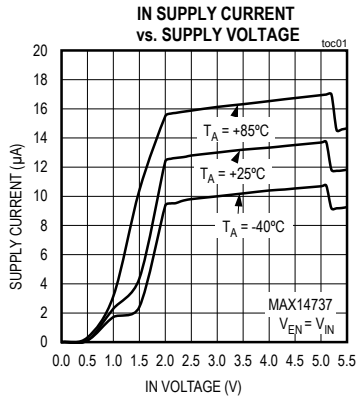
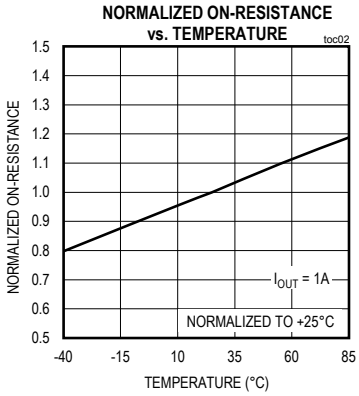


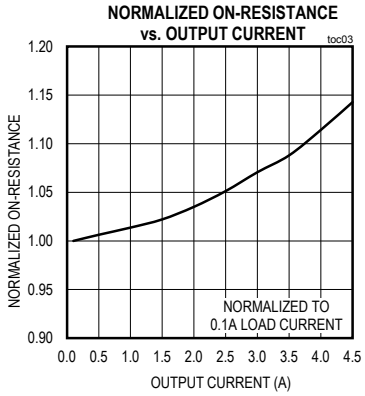
Figure 1. Timing Diagram

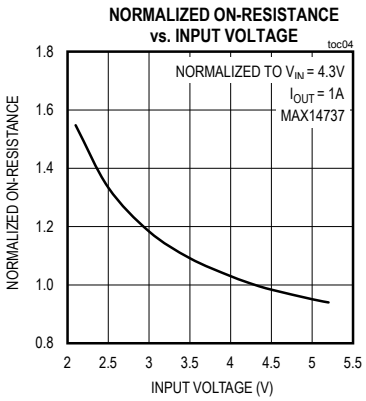
Typical Operating Characteristics

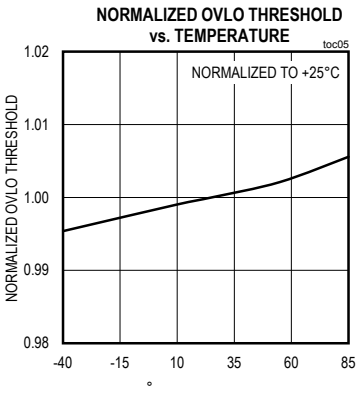
(V_{IN} = 4.3V, T_A = +25ºC, unless otherwise noted.)

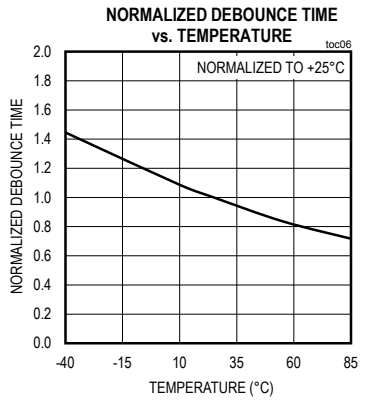








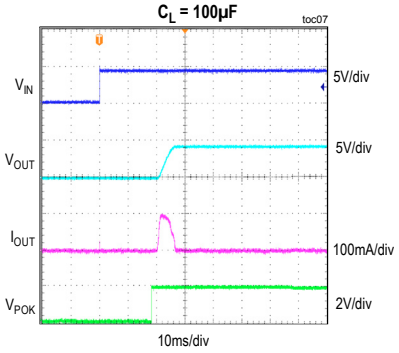




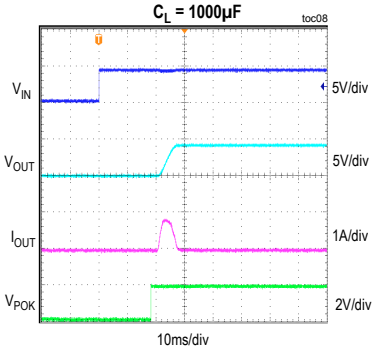
Typical Operating Characteristics (continued)

(V_{IN} = 4.3V, T_A = +25ºC, unless otherwise noted.)

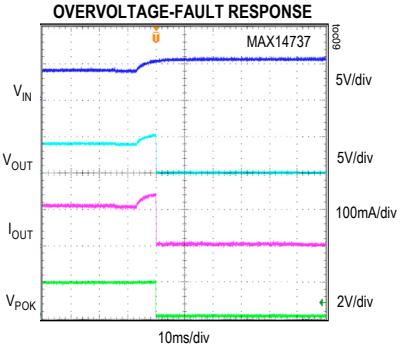
POWER-UP RESPONSE
C_L = 100µF



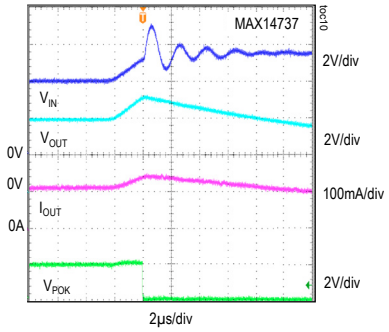
POWER-UP RESPONSE
C_L = 1000µF



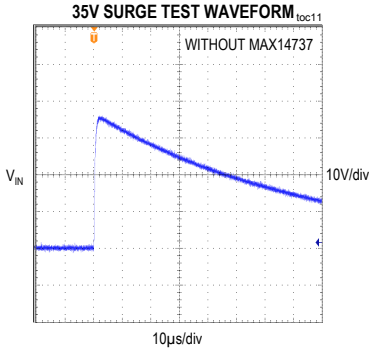
OVERVOLTAGE-FAULT RESPONSE



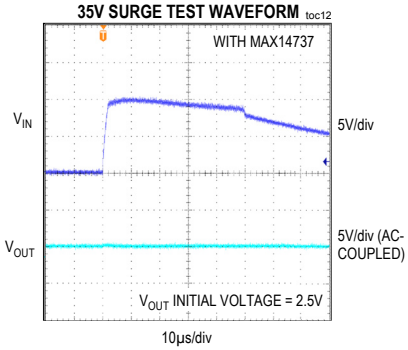
OVERVOLTAGE-FAULT RESPONSE



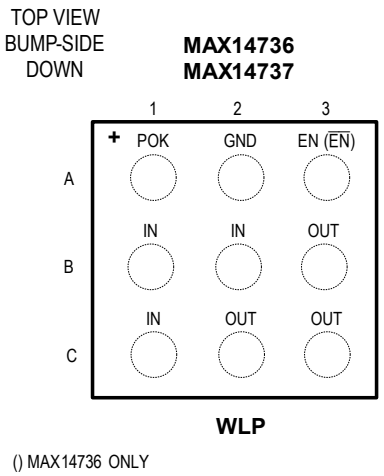
35V SURGE TEST WAVEFORM



35V SURGE TEST WAVEFORM



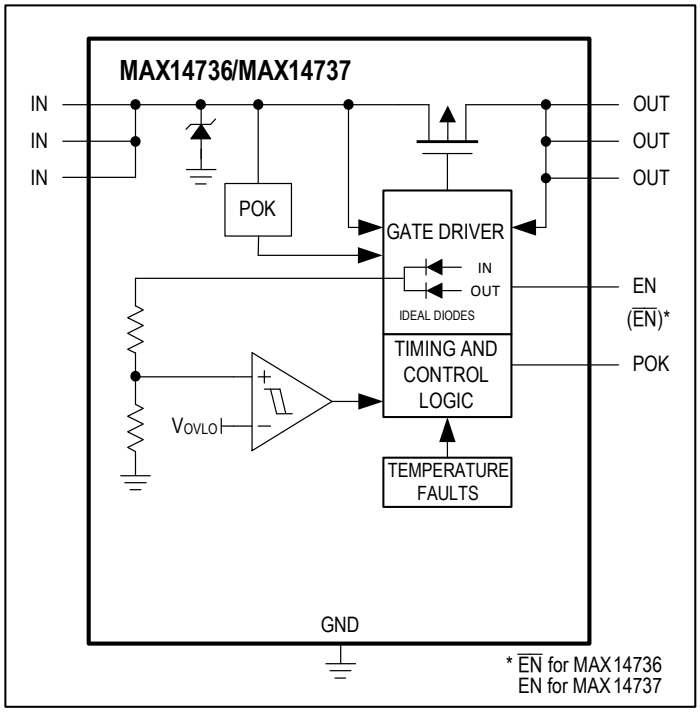
Bump Configuration



Bump Description

BUMP		NAME	FUNCTION
MAX14736	MAX14737		
A1	A1	POK	Push-Pull Power-Okay Output. When the POK output is low, an OVLO, UVLO, or thermal fault has been detected, or the device has been placed into shutdown mode.
A2	A2	GND	Ground
A3	—	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ high to place the device in shutdown mode (power switch is open). Drive $\overline{EN}$ low to place the device in normal operating mode.
—	A3	EN	Active-High Enable Input. Drive EN low to place the device in shutdown mode (power switch is open). Drive EN high to place the device in normal operating mode.
B1, B2, C1	B1, B2, C1	IN	Overvoltage-Protection Input. Bypass IN with a 0.1µF ceramic capacitor for ±15kV Human Body Model (HBM) ESD protection. No capacitor is required for ±2kV HBM ESD protection. Externally connect all the IN pins together.
B3, C2, C3	B3, C2, C3	OUT	Overvoltage-Protection Output. Bypass OUT with at least a 1µF ceramic capacitor. Externally connect all the OUT pins together.

Functional Diagram



Detailed Description

The MAX14736/MAX14737 overvoltage-protection (OVP) devices guard battery-powered modules in portable devices against overvoltage faults. The low, 15mΩ (typ) on-resistance, as well as the low 13µA (typ) quiescent supply current of the devices minimize power consumption, making them an excellent choice for low-power systems. Additionally, the devices feature a precision overvoltage-lockout (OVLO) threshold, ultra-fast response time, and surge suppression to ±35V, which serve to provide excellent protection against even high-slew rate, high-voltage transients.

The integrated power transistor in the devices is a p-channel device, but the intrinsic body diode from OUT to IN is removed through appropriate design techniques. Consequently, when the switch is in the off state, reverse-current blocking is inherent to the devices. The devices feature a push-pull POK output that is driven low if either an overvoltage, undervoltage, or thermal fault is detected; or if the device is placed into shutdown mode.

The MAX14736 has an active-low enable pin ($\overline{EN}$), while the enable pin (EN) on MAX14737 is active-high. When driven to the active state, the device is enabled. When driven to the inactive state, the device is placed in a low-power shutdown mode and the switch is kept in the off state.

Device Operation

The devices contain timing logic that controls the turn-on of the internal FET. When the device is enabled and $V_{UVLO} < V_{INT}* < V_{OVLO}$, the internal gate-driver circuitry is powered. After 15ms of debounce time, which prevents false turn-on of the FET during startup, the soft-start function limits inrush current through the FET for 30ms (typ). At any time, if $V_{INT}*$ rises above V_{OLVO}, or falls below V_{UVLO}, the FET is turned off and OUT is consequently disconnected from IN.

$$*V_{INT} = \max(V_{IN}, V_{OUT})$$

Overvoltage Lockout

The MAX14736 offers a 4.7V (typ) precision overvoltage threshold, while the overvoltage threshold for MAX14737 is 5.2V (typ). When IN or OUT rise above the overvoltage-lockout threshold (V_{OVLO}), OUT is disconnected from IN. When V_{INT}* drops by the OVLO falling hysteresis (V_{OVLO_HYS}), OUT and IN are reconnected.

Shutdown Mode

The devices feature a low-power shutdown mode, which disconnects OUT from IN and reduces current consumption to 2µA (typ). To enter shutdown mode, drive $\overline{EN}$ high on the MAX14736 or EN low on the MAX14737. The POK output is driven low when the device is in shutdown mode.

For MAX14737, EN has an internal pulldown resistor. The MAX14737 is placed in shutdown mode by leaving EN unconnected.

Thermal-Shutdown Protection

The devices contain internal thermal-shutdown circuitry necessary to protect the devices. The internal FET turns off, and POK is driven low, when the junction temperature exceeds +150°C (typ). The devices exit thermal shutdown after the junction temperature cools by 20°C (typ).

POK Output

The push-pull POK output on the devices assert high when they are enabled and when OVLO, UVLO, or thermal fault is not present. Table 1 shows the truth table for the POK output.

Table 1. POK Truth Table

V_{INT}*	$\overline{EN}$ (MAX14736)	EN (MAX14737)	THERMAL SHUTDOWN	POK
$V_{UVLO} < V_{INT} < V_{OVLO}$	HIGH	LOW	NO FAULT	LOW
			FAULT	LOW
	LOW	HIGH	NO FAULT	HIGH (AFTER t_{DEB})
			FAULT	LOW
$V_{INT} < V_{UVLO}$ OR $V_{INT} > V_{OVLO}$	HIGH	LOW	NO FAULT	LOW
			FAULT	LOW
	LOW	HIGH	NO FAULT	LOW
			FAULT	LOW

*$V_{INT} = max(V_{IN}, V_{OUT})$

Applications Information

IN Bypass Capacitor

The MAX14736/MAX14737 do not require an input capacitor, though it is generally recommended to bypass IN to GND with a 0.1µF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length or other non-ideal layout conditions, the device clamps the overshoot due to the LC tank circuit.

Output Capacitor

The soft-start functionality included in the MAX14736/MAX14737 limits inrush current for 30ms (typ), allowing the devices to charge capacitances over 1000µF.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX14736/MAX14737 are specified for ±2kV (HBM) typical ESD resistance on all pins and ±15kV (HBM) typical ESD resistance on IN with a 0.1µF bypass capacitor.

HBM ESD Protection

Figure 2 shows the Human Body Model, while Figure 3 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

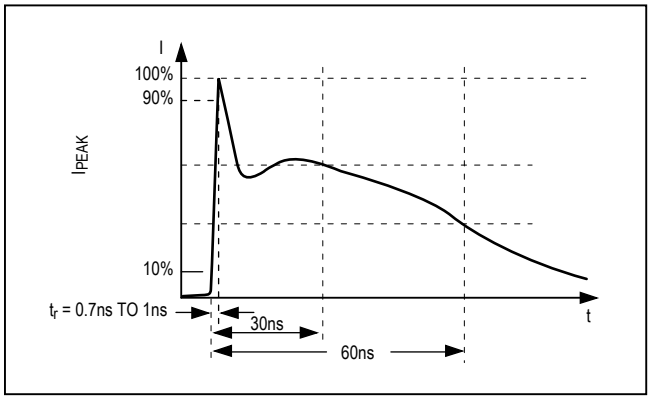


Figure 2. Human Body ESD Test Model

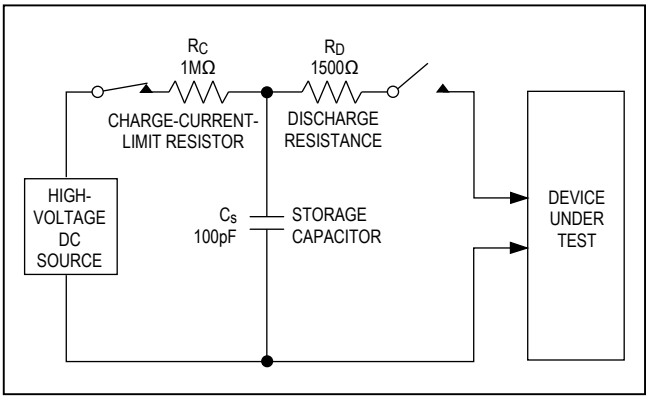


Figure 3. Human Body Current Waveform

Ordering Information

PART	ENABLE POLARITY	OVLO (V)	TOP MARK	PIN-PACKAGE
MAX14736EWL+T	$\overline{EN}$	4.7	AKQ	9 WLP
MAX14737EWL+T	EN	5.2	AKR	9 WLP

Note: *All devices are specified over the -40°C to +85°C extended temperature range.*

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "**#**", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91K1+1	**21-0760**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/15	Initial release	—