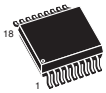
M41T93

Serial SPI bus RTC with battery switchover

Features

- Ultra-low battery supply current of 365 nA
- Factory calibrated accuracy ±5 ppm guaranteed after 2 reflows (SOX18)
  - Much better accuracies achievable using built-in programmable analog and digital calibration circuits
- 2.0 V to 5.5 V clock operating voltage
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- Automatic switchover and reset output circuitry (fixed reference)
  - M41T93S: V_{CC} = 3.0 V to 5.5 V (2.85 V ≤ V_{RST} ≤ 3.00 V)
  - M41T93R: V_{CC} = 2.7 V to 5.5 V (2.55 V ≤ V_{RST} ≤ 2.70 V)
  - M41T93Z: V_{CC} = 2.38 V to 5.50 V (2.25 V ≤ V_{RST} ≤ 2.38 V)
- Compatible with SPI bus serial interface (supports SPI mode 0 [CPOL = 0, CPHA = 0])
- Programmable alarm with interrupt function (valid even during battery back-up mode)
- Optional 2nd programmable alarm available
- Square wave output (defaults to 32 kHz on power-up)
- RESET ($\overline{RST}$) output
- Watchdog timer
- Programmable 8-bit counter/timer
- 7 bytes of battery-backed user SRAM
- Battery low flag
- Power-down time stamp (HT bit)
- Low operating current of 80 µA
- Oscillator stop detection
- Battery or SuperCap™ backup
- Operating temperature of –40°C to +85°C

QFN16, 4 mm x 4 mm (QA)



SOX18 (MY, 18-pin, 300 mil SOIC with embedded crystal)

- Package options include:
  - a 16-lead QFN or an 18-lead embedded crystal SOIC
- RoHS compliance: lead-free components are compliant with the RoHS directive

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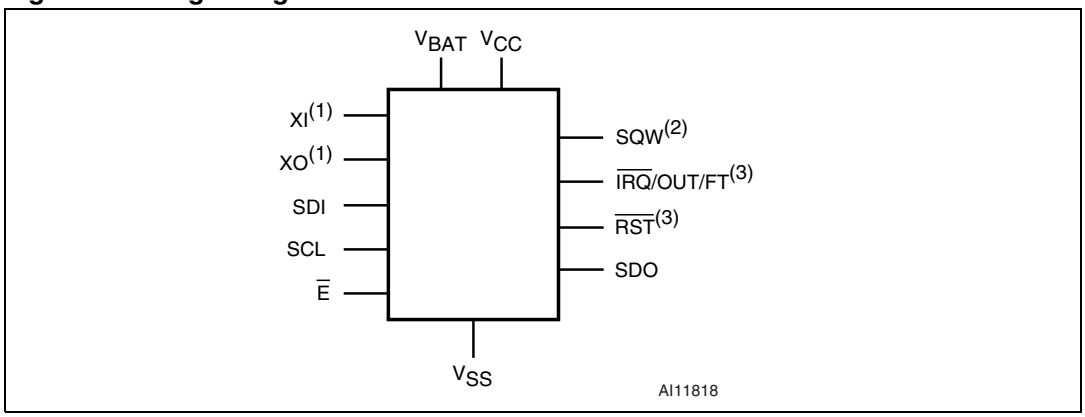
1 Description

The M41T93 is a low-power serial SPI bus real-time clock with a built-in 32.768 kHz oscillator (external crystal-controlled for the QFN16 package, and embedded crystal for the SOX18 package). Eight bytes of the register map (see *Table 3 on page 18*) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 17 bytes of the register map provide status/control of the two alarms, watchdog, 8-bit counter, and square wave functions. An additional seven bytes are made available as user SRAM.

Addresses and data are transferred serially via a serial SPI bus-compatible interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41T93 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button battery when a power failure occurs.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupt, watchdog timer, programmable 8-bit counter, and square wave outputs. The eight clock address locations contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. The M41T93 is supplied in either a QFN16 or an SOX18 (MY), 300mil SOIC which includes an embedded 32 kHz crystal. The SOX18 package requires only a user-supplied battery to provide non-volatile operation.

Figure 1. Logic diagram



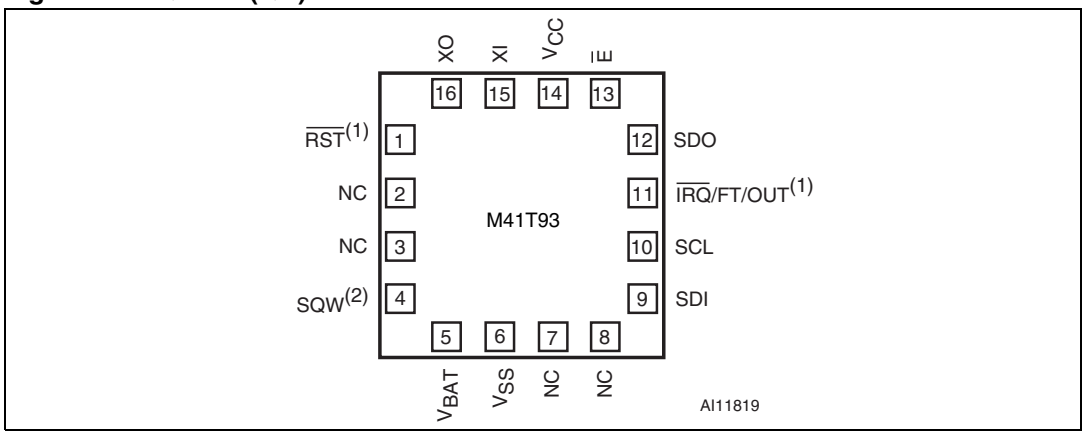
1. For QFN16 package only
2. Defaults to 32 kHz on power-up
3. Open drain

Table 1. Signal name

Symbol	Description
$XI^{(1)}$	32 kHz oscillator input
$XO^{(1)}$	32 kHz oscillator output
$\overline{IRQ}$/FT/OUT	Interrupt /frequency test/output driver (open drain)
$SQW^{(2)}$	32 kHz programmable square wave output
$\overline{RST}$	Power-on reset output (open drain)
$\overline{E}$	Chip enable
SDI	Serial data address input
SDO	Serial data address output
SCL	Serial clock input
V_{BAT}	Battery supply voltage (Tie V_{BAT} to V_{SS} if no battery is connected.)
$DU^{(3)}$	Do not use
V_{CC}	Supply voltage
V_{SS}	Ground

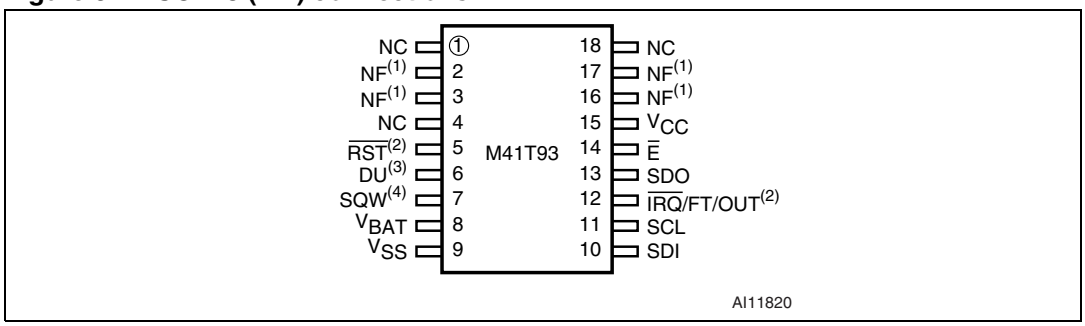
1. For QFN16 package only
2. Defaults to 32 kHz on power-up
3. Do not use (must be tied to V_{CC})

Figure 2. QFN16 (QA) connections



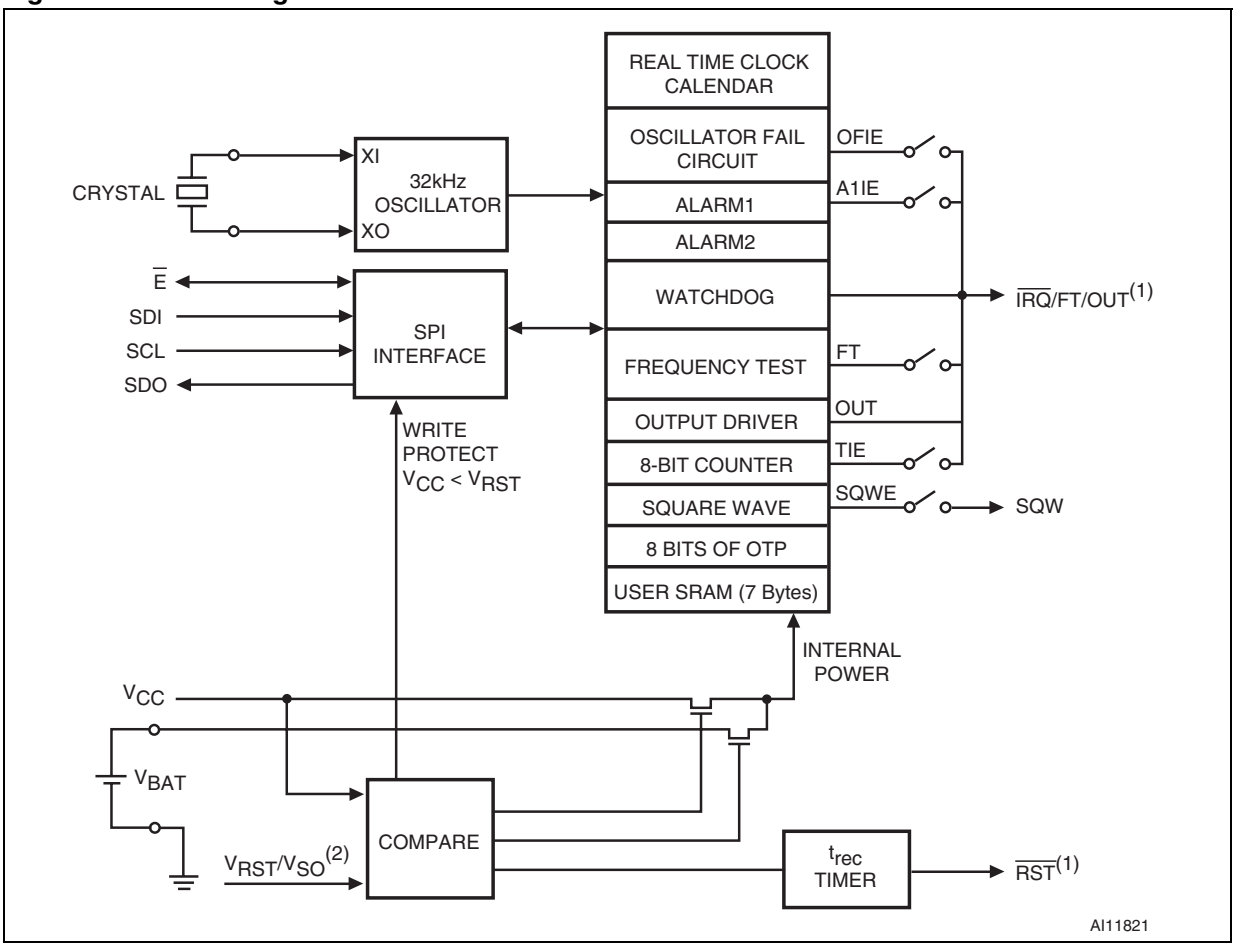
1. Open drain output
2. Defaults to 32 kHz on power-up

Figure 3. SOX18 (MY) connections



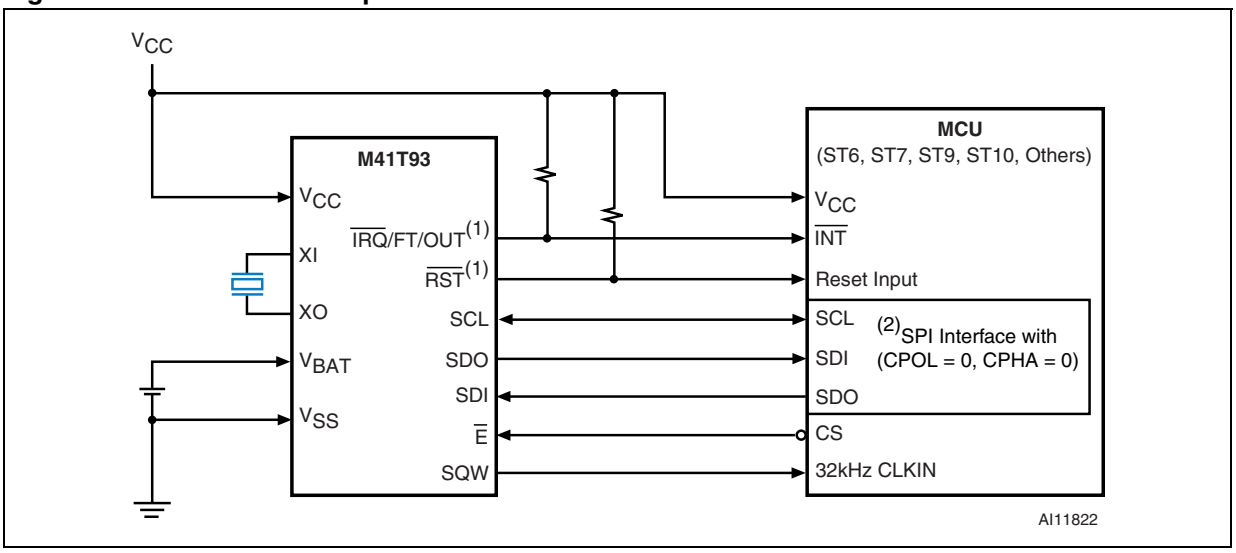
1. NF pins must be tied to V_{SS}. Pins 2 and 3, and 16 and 17 are internally shorted together.
2. Open drain output
3. Do not use (must be tied to V_{CC})
4. Defaults to 32kHz on power-up

Figure 4. Block diagram



1. Open drain output
2. $V_{RST} = V_{SO}$ = 2.93 V (S), 2.63 V (R), and 2.32 V (Z)

Figure 5. Hardware hookup



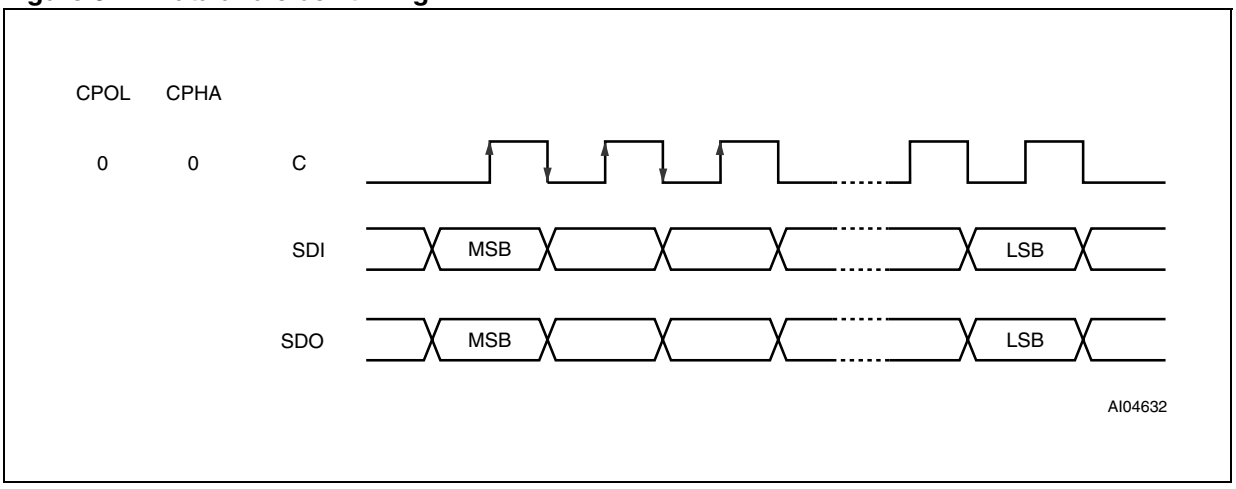
1. Open drain output
2. CPOL (clock polarity) and CPHA (clock phase) are bits that may be set in the SPI control register of the MCU.

Table 2. Function table

Mode	E	SCL	SDI	SDO
Disable reset	H	Input disabled	Input disabled	High Z
WRITE	L		Data bit latch	High Z
READ	L		X	Next data bit shift(1)

1. SDO remains at High Z until eight bits of data are ready to be shifted out during a READ.

Figure 6. Data and clock timing



Note: Supports SPI mode 0 (CPOL = 0, CPHA = 0) only.

1.1 SPI signal description

1.1.1 Serial data output (SDO)

The output pin is used to transfer data serially out of the memory. Data is shifted out on the falling edge of the serial clock.

1.1.2 Serial data input (SDI)

The input pin is used to transfer data serially into the device. Instructions, addresses, and the data to be written, are each received this way. Input is latched on the rising edge of the serial clock.

1.1.3 Serial clock (SCL)

The serial clock provides the timing for the serial interface (as shown in *Figure 19 on page 41* and *Figure 20 on page 41*). The W/R bit, addresses, or data are latched, from the input pin, on the rising edge of the clock input. The output data on the SDO pin changes state after the falling edge of the clock input.

The M41T93 can be driven by a microcontroller with its SPI peripheral running in only mode 0: (CPOL, CPHA) = (0,0).

For this mode, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL (see *Table 2 on page 10* and *Figure 6 on page 10*).

1.1.4 Chip enable ($\overline{E}$)

When $\overline{E}$ is high, the memory device is deselected, and the SDO output pin is held in its high impedance state.

After power-on, a high-to-low transition on $\overline{E}$ is required prior to the start of any operation.

2 Operation

The M41T93 clock operates as a slave device on the SPI serial bus. Each memory device is accessed by a simple serial interface that is SPI bus-compatible. The bus signals are SCL, SDI, and SDO (see *Table 1 on page 7* and *Figure 5 on page 10*). The device is selected when the chip enable input ($\overline{E}$) is held low. All instructions, addresses and data are shifted serially in and out of the chip. The most significant bit is presented first, with the data input (SDI) sampled on the first rising edge of the clock (SCL) after the chip enable ($\overline{E}$) goes low. The 32 bytes contained in the device can then be accessed sequentially in the following order:

1	Tenths/hundredths of a second register
2	Seconds register
3	Minutes register
4	Century/hours register
5	Day register
6	Date register
7	Month register
8	Year register
9	Digital calibration register
10	Watchdog register
11-15	Alarm1 registers
16	Flags register
17	Timer value register
18	Timer control register
19	Analog calibration register
20	Square wave register
21-25	Alarm2 registers
26-32	User RAM

The M41T93 clock continually monitors V_{CC} for an out-of tolerance condition. Should V_{CC} fall below V_{RST}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system.

The power input will also be switched from the V_{CC} pin to the external battery when V_{CC} falls below the battery back-up switchover voltage ($V_{SO} = V_{RST}$). At this time the clock registers will be maintained by the battery supply. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{REC} (min). For more information on battery storage life refer to application note AN1012.

2.1 SPI bus characteristics

The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. It consists of four signal lines: serial data input (SDI), serial data output (SDO), serial clock (SCL) and a chip enable ($\overline{E}$).

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

The $\overline{E}$ input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master (micro) and the slave (M41T93) device.

The SCL input, which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus (see *Figure 5 on page 10*).

The M41T93 can be driven by a microcontroller with its SPI peripheral running in only mode 0: (CPOL, CPHA) = (0,0).

For this mode, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL (see *Table 2* and *Figure 6 on page 10*).

There is one clock for each bit transferred. Address and data bits are transferred in groups of eight bits. Due to memory size the second most significant address bit is a “don’t care” (address bit 6).

2.2 Read and write cycles

Address and data are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any data transfer considers the first bit to define whether a READ or WRITE will occur. This is followed by seven bits defining the address to be read or written. Data is transferred out of the SDO for a READ operation and into the SDI for a WRITE operation. The address is always the second through the eighth bit written after the enable ($\overline{E}$) pin goes low. If the first bit is a '1,' one or more WRITE cycles will occur. If the first bit is a '0,' one or more READ cycles will occur (see *Figure 7* and *Figure 8 on page 14*).

Data transfers can occur one byte at a time or in multiple byte burst mode, during which the address pointer will be automatically incremented. For a single byte transfer, one byte is read or written and then $\overline{E}$ is driven high. For a multiple byte transfer all that is required is that $\overline{E}$ continue to remain low. Under this condition, the address pointer will continue to increment as stated previously. Incrementing will continue until the device is deselected by taking $\overline{E}$ high. The address will wrap to 00h after incrementing to 3Fh.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). Although the clock continues to maintain the correct time, this will prevent updates of time and date during either a READ or WRITE of these address locations by the user. The update will resume either due to a deselect condition or when the pointer increments to an non-clock or RAM address (08h to 1Fh).

Note: This is true both in READ and WRITE mode.

Figure 7. Read mode sequence

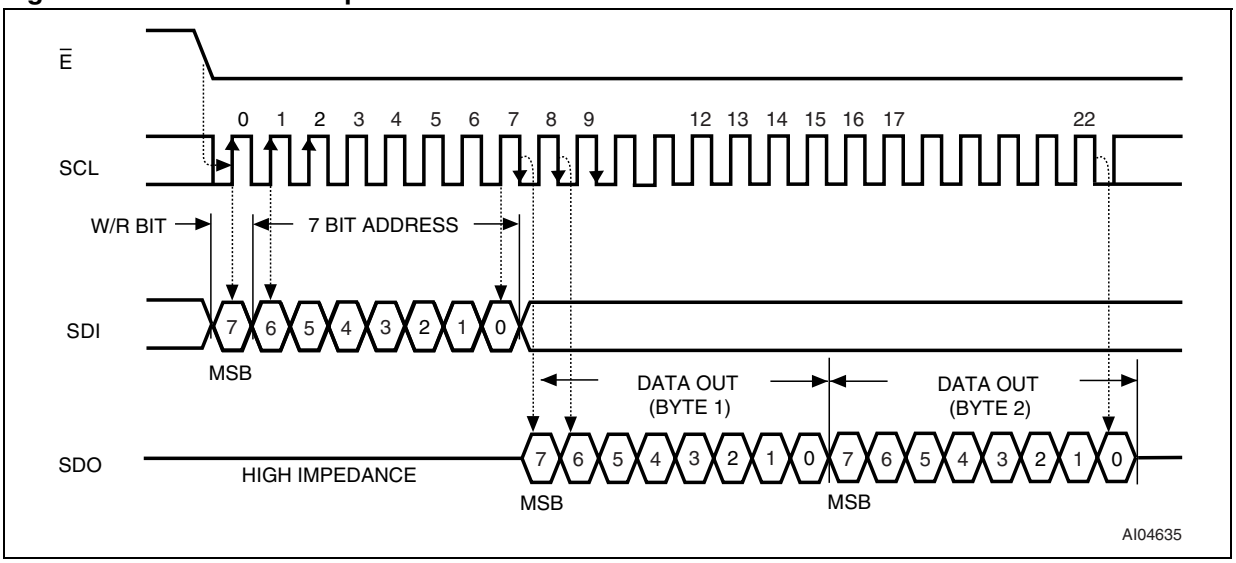
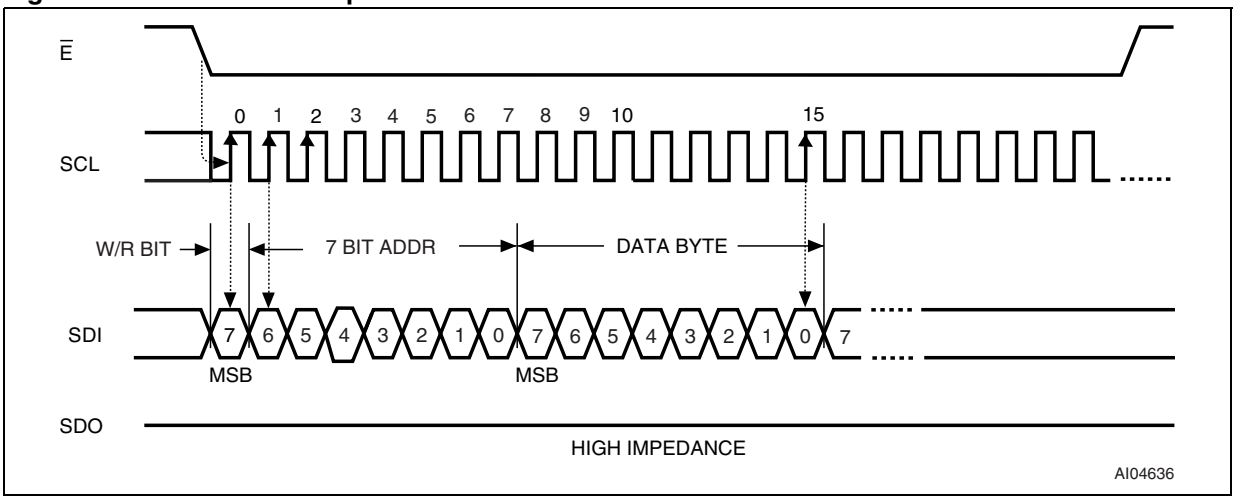


Figure 8. Write mode sequence



2.3 Data retention and battery switchover ($V_{SO} = V_{RST}$)

Once V_{CC} falls below the switchover voltage ($V_{SO} = V_{RST}$), the device automatically switches over to the battery and powers down into an ultra low current mode of operation to preserve battery life. If V_{BAT} is less than, or greater than V_{RST}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{RST} (see *Figure 18 on page 40*). At this time the clock registers and user RAM will be maintained by the attached battery supply.

When it is powered back up, the device switches back from battery to V_{CC} at V_{SO} + hysteresis. When V_{CC} rises above V_{RST}, it will recognize the inputs. For more information on battery storage life refer to application note AN1012.

2.4 Power-on reset (t_{rec})

The M41T93 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ output pulls low (open drain) and remains low after power-up for t_{rec} (210ms typical) after V_{CC} rises above V_{RST} (max).

Note: The t_{rec} period does not affect the RTC operation. Write protect only occurs when V_{CC} is below V_{RST}. When V_{CC} rises above V_{RST}, the RTC will be selectable immediately. Only the $\overline{RST}$ output is affected by the t_{rec} period.

The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

3 Clock operation

The M41T93 is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The 8-byte clock register (see *Table 3 on page 18*) is used to both set the clock and to read the date and time from the clock, in binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Note: Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to '0.' This provides an additional "kick-start" to the oscillator circuit.

Bits D6 and D7 of clock register 03h (century/ hours register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1). Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the digital calibration register, while the analog calibration register is found at address 12h (these are both described in the clock calibration section). Bit D7 of register 09h (watchdog register) contains the oscillator fail interrupt enable bit (OFIE). When the user sets this bit to '1,' any condition which sets the oscillator fail bit (OF) (see *Oscillator fail detection on page 34*) will also generate an interrupt output.

Note: A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the ST bit and CB0-CB1 bits will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The eight clock registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 Power-down time-stamp

When a power failure occurs, the halt update bit (HT) will automatically be set to a "1". This will prevent the clock from updating the clock/control registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a "0" will allow the clock to update the clock/registers with the current time. For more information, see application note AN1572.

3.2 Clock/control register map

The M41T93 offers 32 internal registers which contain clock, calibration (digital and analog), alarm 1 and 2, watchdog, flags, timer, and square wave. The clock registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER® cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the

completion of a WRITE to any clock address (00h to 07h). The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a stop condition or when the pointer increments to a non-clock address. Clock and alarm registers store data in BCD format. Calibration, timer, watchdog, and square wave bits are written in a binary format.

Table 3. Clock/control register map (32 bytes)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				Seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CB1	CB0	10 hours		Hours (24-hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	A1IE	SQWE	ABE	AI1 10M	Alarm1month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2[1]	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	TI/TP	TIE	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	RS3	RS2	RS1	RS0	0	0	AL2E	OTP	SQW	
14h	0	0	0	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 month				SRAM/AI2 date	01-31
16h	RPT23	0	AI2 10 hour		Alarm2 date				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. AF2 will always read '0' if the AL2E bit is set to '0'.

0 = Must be set to zero
ABE = Alarm in battery backup enable bit
A1IE = Alarm1 interrupt enable bit
AC0-AC6 = analog calibration bits
ACS = analog calibration sign bit
AF1, AF2 = Alarm flag
AL2E = Alarm 2 enable bit
BL = Battery low bit
BMB0-BMB4 = Watchdog multiplier bits
CB0, CB1 = Century bits
DC0-DC4 = Digital calibration bits
DCS = Digital calibration sign bit
FT = Frequency test bit
HT = Halt update bit
OF = Oscillator fail bit
OUT= Output level
OFIE = Oscillator fail interrupt enable
OTP = OTP control bit
RB0-RB2 = Watchdog resolution bits
RPT11-RPT15 = Alarm 1 repeat mode bits
RPT21-RPT25 = Alarm 2 repeat mode bits
RS0-RS3 = SQW frequency
SQWE = Square wave enable
SRAM/$\overline{ALM2}$ = SRAM/Alarm 2 bit
ST = Stop bit
TD0, TD1 = Timer frequency bits
TE = Timer enable bit
TF = Timer flag
$\overline{TI}$/TP = Timer interrupt or pulse
TIE = Timer interrupt enable
WDF = Watchdog flag

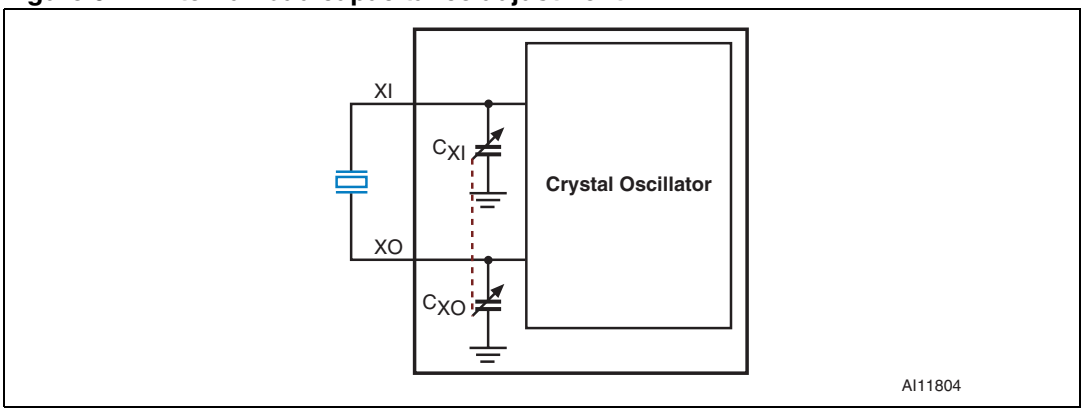
3.3 Real-time clock accuracy

The M41T93 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The accuracy of the real-time clock is dependent upon the accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Temperature also affects the crystal frequency, causing additional error (see *Figure 10 on page 23*).

The M41T93 provides the option of clock correction through either manufacturing calibration or in-application calibration. The total possible compensation is typically –93 ppm to +156 ppm. The two compensation circuits that are available are:

1. An analog calibration register (12h) can be used to adjust internal (on-chip) load capacitors for oscillator capacitance trimming. The individual load capacitors C_{XI} and C_{XO} (see *Figure 9*), are selectable from a range of –18 pF to +9.75 pF in steps of 0.25pF. This translates to a calculated compensation of approximately ±30 ppm (see *Analog calibration (programmable load capacitance) on page 22*).
2. A digital calibration register (08h) can also be used to adjust the clock counter by adding or subtracting a pulse at the 512 Hz divider stage. This approach provides periodic compensation of approximately –63 ppm to +126 ppm (see *Digital calibration (periodic counter correction) on page 20*).

Figure 9. Internal load capacitance adjustment



3.4 Clock calibration

The M41T93 oscillator is designed for use with a 12.5 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±1 ppm at 25°C.

The M41T93 design provides the following two methods for clock error correction.

3.4.1 Digital calibration (periodic counter correction)

This method employs the use of periodic counter correction by adjusting the ratio of the 100 Hz divider stage to the 512 Hz divider stage. Under normal operation, the 100Hz divider stage outputs precisely 100 pulses for every 512 pulses of the 512 Hz input stage to provide the input frequency to the fraction of seconds clock register. By adjusting the number of 512 Hz input pulses used to generate 100 output pulses, the clock can be sped up or slowed down, as shown in *Figure 12 on page 26*.

When a non-zero value is loaded into the five calibration bits (DC4 – DC0) found in the digital calibration register (08h) and the sign bit is ‘1,’ (indicating positive calibration), the 100 Hz stage outputs 100 pulses for every 511 input pulses instead of the normal 512. Since the 100 pulses are now being output in a shorter window, this has the effect of speeding up the clock by 1/512 seconds for each second the circuit is active. Similarly, when the sign bit is ‘0,’ indicating negative calibration, the block outputs 100 pulses for every 513 input pulses. Since the 100 pulses are then being output in a longer window, this has the effect of slowing down the clock by 1/512 seconds for each second the circuit is active.

The amount of calibration is controlled by using the value in the calibration register (N) to generate the adjustment in one second increments. This is done for the first N seconds once every *eight* minutes for positive calibration, and for N seconds once every *sixteen* minutes for negative calibration (see *Table 4 on page 21*).

For example, if the calibration register is set to '100010,' then the adjustment will occur for two seconds in every minute. Similarly, if the calibration register is set to '000011,' then the adjustment will occur for 3 seconds in every alternating minute.

The digital calibration bits (DC4 – DC0) occupy the five lower order bits in the digital calibration register (08h). These bits can be set to represent any value between 0 and 31 in binary form. The sixth bit (DCS) is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within an 8-minute (positive) or 16-minute (negative) cycle. Therefore, each calibration step has an effect on clock accuracy of +4.068 or –2.034 ppm. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month, which corresponds to a total range of +5.5 or –2.75 minutes per month.

Note: 1 The modified pulses are not observable on the frequency test (FT) output, nor will the effect of the calibration be measurable real-time, due to the periodic nature of the error compensation.

2 Positive digital calibration is performed on an eight minute cycle, therefore the value in the calibration register should not be modified more frequently than once every eight minutes for positive values of calibration. Negative digital calibration is performed on a sixteen minute cycle, therefore negative values in the calibration register should not be modified more frequently than once every sixteen minutes.

Table 4. Digital calibration values

Calibration value (binary)	Calibration value rounded to the nearest ppm	
DC4 – DC0	Negative calibration (DCS = 0)	Positive calibration (DCS = 1)
0 (00000)	0	0
1 (00001)	–2	4
2 (00010)	–4	8
3 (00011)	–6	12
4 (00100)	–8	16
5 (00101)	–10	20
6 (00110)	–12	24
7 (00111)	–14	28
8 (01000)	–16	33
9 (01001)	–18	37
10 (01010)	–20	41
11 (01011)	–22	45
12 (01100)	–24	49
13 (01101)	–26	53
14 (01110)	–28	57
15 (01111)	–31	61
16 (10000)	–33	65
17 (10001)	–35	69
18 (10010)	–37	73
19 (10011)	–39	77
20 (10100)	–41	81
21 (10101)	–43	85
22 (10110)	–45	90
23 (10111)	–47	94
24 (11000)	–49	98
25 (11001)	–51	102
26 (11010)	–53	106
27 (11011)	–55	110
28 (11100)	–57	114
29 (11101)	–59	118
30 (11110)	–61	122
31 (11111)	–63	126
N	N/491520 (per minute)	N/245760 (per minute)

3.4.2 Analog calibration (programmable load capacitance)

A second method of calibration employs the use of programmable internal load capacitors to adjust (or trim) the oscillator frequency.

By design, the oscillator is intended to be 0 ppm ± crystal accuracy at room temperature (25°C, see *Figure 10 on page 23*). For a 12.5 pF crystal, the default loading on each side of the crystal will be 25 pF. For incrementing or decrementing the calibration value, capacitance will be added or removed in increments of 0.25 pF to each side of the crystal.

Internally, C_{LOAD} of the oscillator is changed via two digitally controlled capacitors, C_{XI} and C_{XO}, connected from the XI and XO pins to ground (see *Figure 9 on page 19*). The effective on-chip series load capacitance, C_{LOAD}, ranges from 3.5 pF to 17.4 pF, with a nominal value of 12.5 pF (AC0-AC6 = '0').

The effective series load capacitance (C_{LOAD}) is the combination of C_{XI} and C_{XO}:

$$C_{LOAD} = 1/(1/C_{XI} + 1/C_{XO})$$

Seven analog calibration bits, AC0 to AC6, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. An analog calibration sign (ACS) bit determines if capacitance is added (ACS bit = '0,' negative calibration) or removed (ACS bit = '1,' positive calibration). The majority of the calibration adjustment is positive (i.e. to increase the oscillator frequency by removing capacitance) due to the typical characteristic of quartz crystals to slow down due to changes in temperature, but negative calibration is also available.

Since the analog calibration register adjustment is essentially "pulling" the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern this mechanism indicate that smaller capacitor values of analog calibration adjustment will provide larger increments. Thus, the larger values of analog calibration adjustment will produce smaller incremental frequency changes. These values typically vary from 6-10 ppm/bit at the low end to <1 ppm/bit at the highest capacitance settings. The range provided by the analog calibration register adjustment with a typical surface mount crystal is approximately ±30 ppm around the AC6-AC0 = 0 default setting because of this property (see *Table 5 on page 23*).

Figure 10. Crystal accuracy across temperature

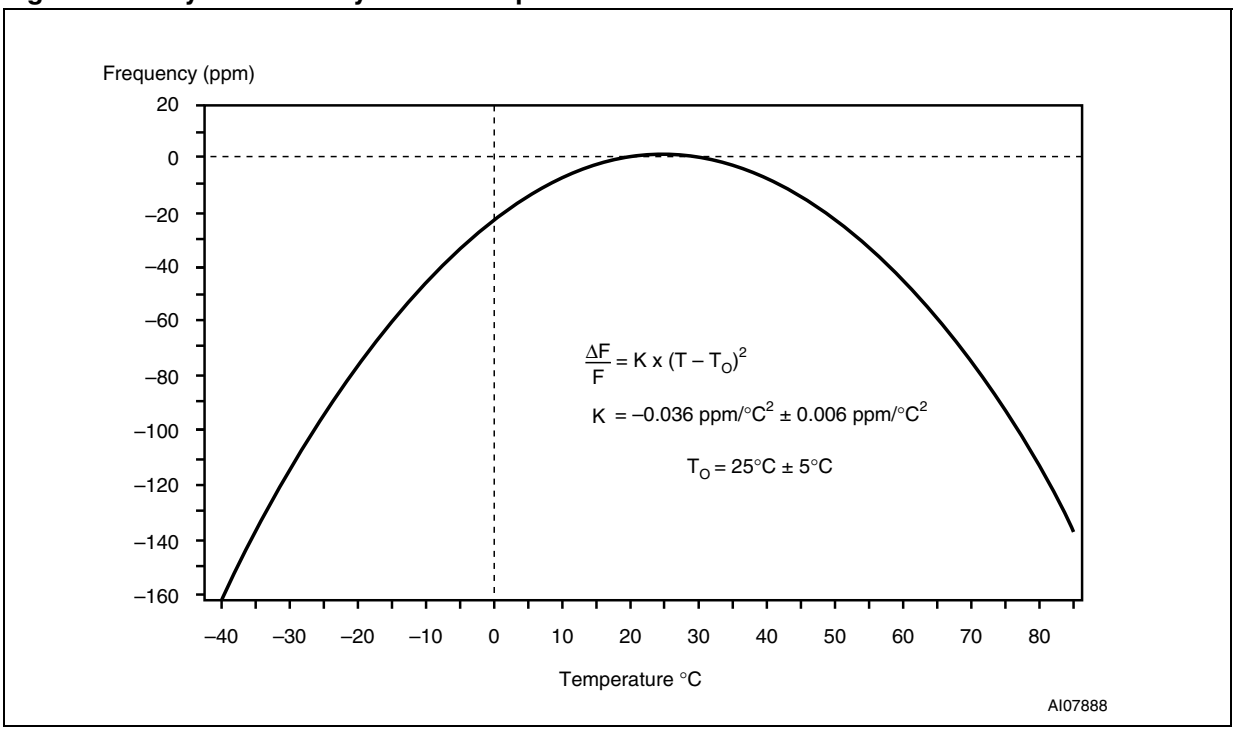


Table 5. Analog calibration values

Addr	Analog calibration value	D7	D6	D5	D4	D3	D2	D1	D0	C_{XI}, C_{XO}	C_{LOAD}(1)
		ACS (±)	AC6 (16 pF)	AC5 (8 pF)	AC4 (4 pF)	AC3 (2 pF)	AC2 (1pF)	AC1 (0.5 pF)	AC0 (0.25 pF)		
12h	0 pF	x	0	0	0	0	0	0	0	25 pF	12.5 pF
	3 pF	0	0	0	0	1	1	0	0	28 pF	14 pF
	5 pF	0	0	0	1	0	1	0	0	30 pF	15 pF
	–7 pF	1	0	0	1	1	1	0	0	18 pF	9 pF
	9.75 pF(2)	0	0	1	0	0	1	1	1	34.75 pF	17.4 pF
	–18 pF(3)	1	1	0	0	1	0	0	0	7 pF	3.5 pF

1. $C_{LOAD} = 1/(1/C_{XI} + 1/C_{XO})$
2. Maximum negative calibration value
3. Maximum positive calibration value

The on-chip capacitance can be calculated as follows:

$$C_{LOAD} = [(AC6-AC0\ value,\ decimal) \times 0.25pF] + 7pF$$

For example:

C_{LOAD} (12h = x0000000) = 12.5 pF

C_{LOAD} (12h =11001000) = 3.5 pF and

C_{LOAD} (12h = 00100111) = 17.4 pF

The oscillator sees a minimum of 3.5 pF with no programmable load capacitance selected.

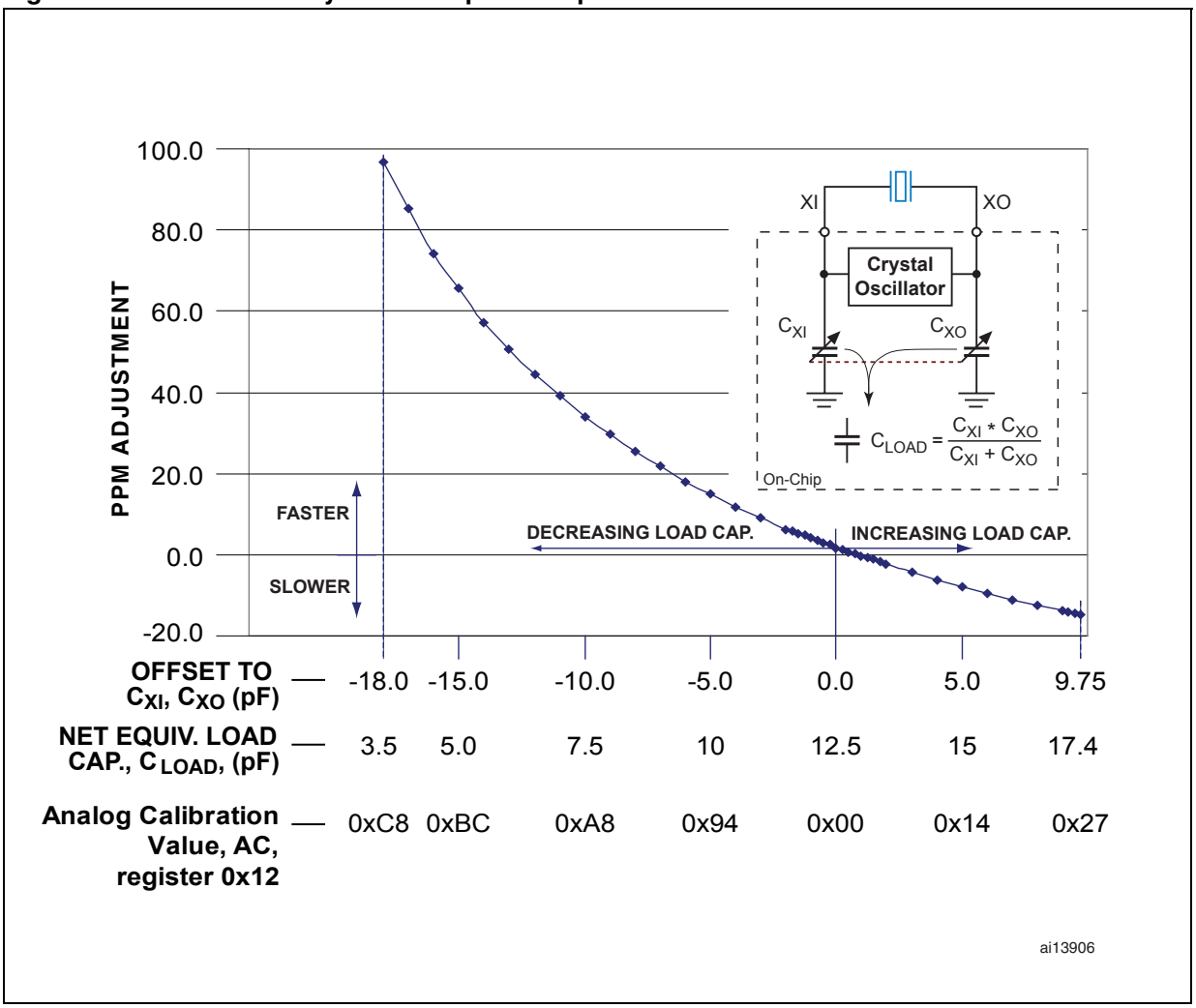
Note: These are typical values, and the total load capacitance seen by the crystal will include approximately 1-2 pF of package and board capacitance in addition to the analog calibration register value.

Any invalid value of analog calibration will result in the default capacitance of 25 pF.

The combination of analog and digital trimming can give up to –93 to +156 ppm of the total adjustment.

Figure 11 on page 25 represents a typical curve of clock ppm adjustment versus the Analog Calibration value. This curve may vary with different crystals, so it is good practice to evaluate the crystal to be used with an M41T93 device before establishing the adjustment values for the application in question.

Figure 11. Clock accuracy vs. on-chip load capacitors



Two methods are available for ascertaining how much calibration a given M41T93 may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses either or both of the calibration bytes.
- The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT/OUT pin. The $\overline{IRQ}$/FT/ OUT pin will toggle at 512 Hz when FT and OUT bits = '1' and ST = '0.' Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring either a –10 (xx001010) to be loaded into the digital calibration byte, or +6 pF (00011000) into the analog calibration byte for correction.

Note: Setting or changing the digital calibration byte does not affect the frequency test, square wave, or watchdog timer frequency, but changing the analog calibration byte DOES affect all functions derived from the low current oscillator (see Figure 12).

Figure 12. Clock divider chain and calibration circuits

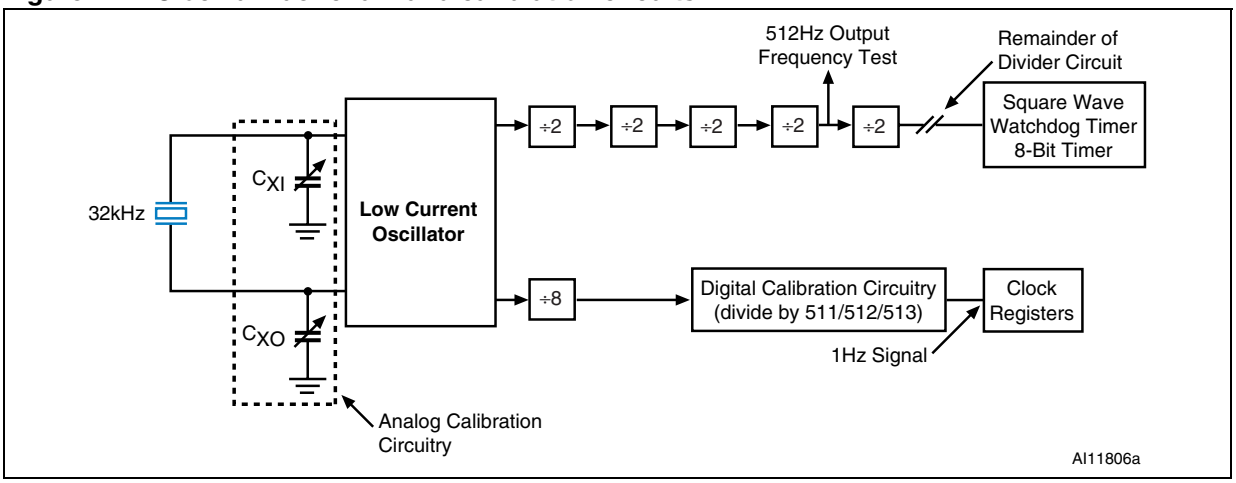
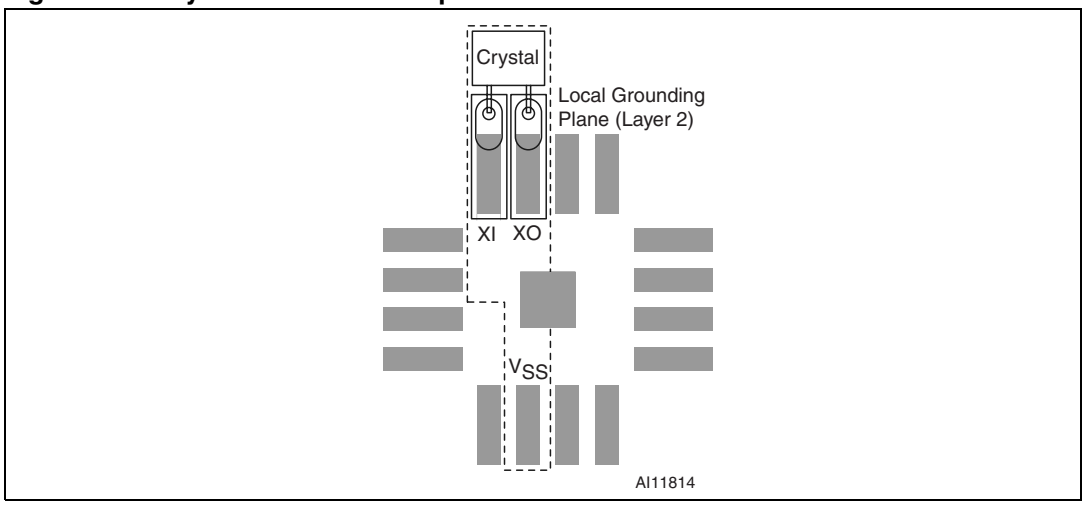


Figure 13. Crystal isolation example



Note: The substrate pad should be tied to V_{SS}.

3.5 Setting the alarm clock registers

Address locations 0Ah-0Eh (alarm 1) and 14h-18h (alarm 2) contain the alarm settings. Either alarm can be configured independently to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. Bits RPT15–RPT11 and RPT25-RPT21 put the alarms in the repeat mode of operation. *Table 6 on page 28* shows the possible bit configurations.

Codes not listed in the table default to the once-per-second mode to quickly alert the user of an incorrect alarm setting. When the clock information matches the alarm clock settings based on the match criteria defined by RPT15–RPT11 and/or RPT25-RPT21, AF1 (alarm 1 flag) or AF2 (alarm 2 flag) is set. If A1IE (alarm 1 interrupt enable) is set, the alarm condition activates the $\overline{IRQ}$/FT/OUT output pin. To disable either of the alarms, write a '0' to the alarm date registers and to the RPTx5–RPTx1 bits.

Note: If the address pointer is allowed to increment to the flag register address, or the last address written is "Alarm Seconds," the address pointer will increment to the flag address, and an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address.

The $\overline{IRQ}$ output is cleared by a READ to the flags register (0Fh) as shown in *Figure 14*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'.

The $\overline{IRQ}$/FT/OUT pin can also be activated in the battery backup mode (see *Figure 15 on page 28*).

3.6 Optional second programmable alarm

When the alarm 2 enable (AL2E) bit (D1 of address 13h) is set to a logic ‘1,’ registers 14h through 18h provide control for a second programmable alarm which operates in the same manner as the alarm function described above.

The AL2E bit defaults on initial power-up to a logic ‘0’ (alarm 2 disabled). In this mode, the five address bytes (14h-18h) function as additional user SRAM, for a total of 12 bytes of user SRAM.

Figure 14. Alarm interrupt reset waveform

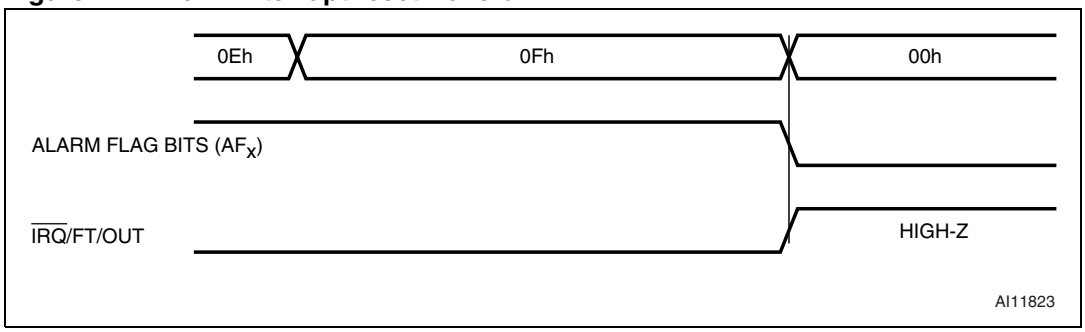
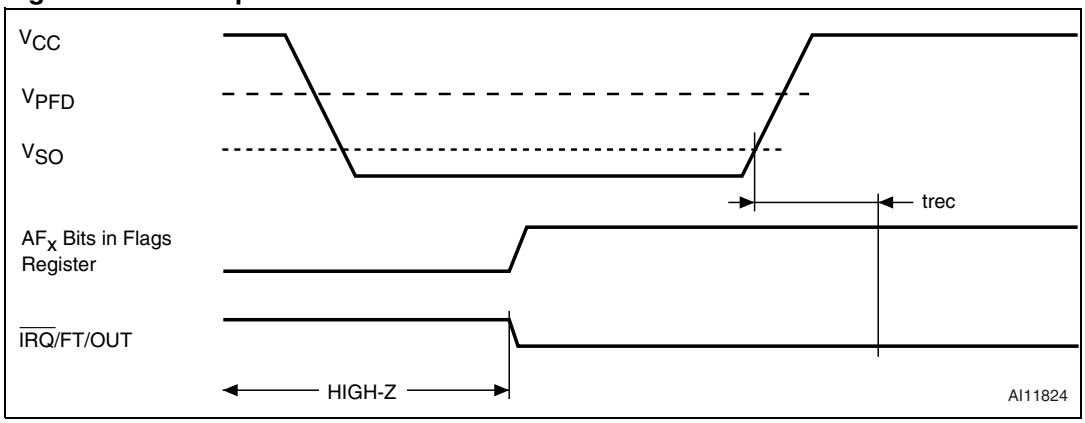


Figure 15. Backup mode alarm waveform



Note: ABE and A1IE bits = 1.

Table 6. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

3.7 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1, or 3 seconds). If the processor does not reset the timer within the specified period, the M41T93 sets the WDF (watchdog flag) and generates a watchdog interrupt.

The watchdog timer can be reset by having the microprocessor perform a WRITE of the watchdog register. The time-out period then starts over.

Should the watchdog timer time-out, a value of 00h needs to be written to the watchdog register in order to clear the $\overline{IRQ}$/FT/OUT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh).

The watchdog function is automatically disabled upon power-up and the watchdog register is cleared. If the watchdog function is set, the frequency test function is activated, and the SQWE bit is '0,' the watchdog function prevails and the frequency test function is denied.

3.8 8-bit (countdown) timer

The timer value register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register (11h) TE bit. Other timer properties such as the source clock, or interrupt generation are also selected in the timer control register (see *Table 7*). For accurate read back of the countdown value, the serial clock (SCL) must be operating at a frequency of at least twice the selected timer clock.

The timer control register selects one of four source clock frequencies for the timer (4096, 64, 1, or 1/60 Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag (TF) bit. The TF bit can only be cleared by software. When asserted, the timer flag (TF) can also be used to generate an interrupt ($\overline{IRQ}$/FT/OUT) on the M41T93. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. The timer interrupt/timer pulse ($\overline{TI}$/TP) bit is used to control this mode selection. When reading the timer, the current countdown value is returned.

Table 7. Timer control register map

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function
0Fh	WDF	AF1	AF2	BL	TF	OF	0	0	Flags
10h	Timer countdown value								Timer value
11h	TE	$\overline{TI}$/TP	TIE	0	0	0	TD1	TD0	Timer control

Note: Bit positions labeled with '0' should always be written with logic '0.'

3.8.1 $\overline{TI}$/TP

- $\overline{TI}$/TP = 0

  $\overline{IRQ}$/FT/OUT is active when TF is logic '1' (subject to the status of the timer interrupt enable bit (TIE).
- $\overline{TI}$/TP = 1

  $\overline{IRQ}$/FT/OUT pulses active according to *Table 8* (subject to the status of the TIE bit).

Note: If an alarm condition, watchdog time-out, oscillator failure, or OUT = 0 cause $\overline{IRQ}$/FT/OUT to be asserted low, then $\overline{IRQ}$/FT/OUT will remain asserted even if $\overline{TI}$/TP is set to '1.' When in pulse mode ($\overline{TI}$/TP = 1), clearing the TF bit will not stop the pulses on $\overline{IRQ}$/FT/OUT. The output pulses will only stop if TE, TIE, or $\overline{TI}$/TP are reset to '0.'

Table 8. Interrupt operation (bit $\overline{TI}$/TP = 1)

Source clock (Hz)	$\overline{IRQ}$[1] period(s)	
	n[2] = 1	n > 1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

1. TF and $\overline{IRQ}$/FT/OUT become active simultaneously.
2. n = loaded countdown timer value. The timer is stopped when n = 0.

3.8.2 TF

At the end of a timer countdown, TF is set to logic '1.' If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading the flag bits. The timer will auto-reload and continue to count down regardless of the state of TF bit (or $\overline{TI}$/TP bit). The TF bit is cleared by reading the flags register.

3.8.3 TIE

In level mode ($\overline{TI}$/TP = 0), when TF is asserted, the interrupt is asserted (if TIE = 1). To clear the interrupt, the TF bit or the TIE bit must be reset.

3.8.4 TE

- TE = 0

  When the timer register (10h) is set to ‘0,’ the timer is disabled.
- TE = 1

  The timer is enabled. TE is reset (disabled) on power-down. When re-enabled, the counter will begin from the same value as when it was disabled.

3.8.5 TD1/0

These are the timer source clock frequency selection bits (see *Table 9*). These bits determine the source clock for the countdown timer (see *Table 10*). When not in use, the TD1 and TD0 bits should be set to '11' (1/60 Hz) for power saving.

Table 9. Timer source clock frequency selection (244.1 µs to 4.25 hrs)

TD1	TD0	Timer source clock frequency (Hz)
0	0	4096 (244.1 µs)
0	1	64 (15.6 ms)
1	0	1 (1 s)
1	1	1/60 (60 s)

Table 10. Timer countdown value register bits (addr 11h)

Bit	Symbol	Description
7 - 0	<timer countdown value>	This register holds the loaded countdown value 'n.'
		Countdown period = n / source clock frequency

Note: Writing to the timer register will not reset the TF bit or clear the interrupt.

3.9 Square wave output

The M41T93 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 11*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

Note: If the SQWE bit is set to '1', and V_{CC} falls below the switchover (V_{SO}) voltage, the squarewave output will be disabled.

Table 11. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.10 Battery low warning

The M41T93 automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5 V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity. Clock data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery backup mode, the battery should be replaced.

The M41T93 only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery backup mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.11 Century bits

These two bits will increment in a binary fashion at the turn of the century, and handle all leap years correctly. See *Table 12* for additional explanation.

Table 12. Century bits examples

CB0	CB1	Leap Year?	Example(1)
0	0	Yes	2000
0	1	No	2100
1	0	No	2200
1	1	No	2300

1. Leap year occurs every four years (for years evenly divisible by four), except for years evenly divisible by 100. The only exceptions are those years evenly divisible by 400 (the year 2000 was a leap year, year 2100 is not).

3.12 Output driver pin

When the OFIE bit, A1IE bit, and watchdog register are not set to generate an interrupt, the $\overline{IRQ}$/FT/OUT pin becomes an output driver that reflects the contents of D7 of register 08h. In other words, when D7 (OUT bit) is a '0,' then the $\overline{IRQ}$/FT/OUT pin will be driven low.

Note: The $\overline{IRQ}$/FT/OUT pin is an open drain which requires an external pull-up resistor.

3.13 Oscillator fail detection

If the oscillator fail (OF) bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.' This will restart the oscillator. The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).

Note: If the OF bit cannot be written to '1' four seconds after the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.'

- The voltage present on V_{CC} or battery is insufficient to support oscillation
- The ST Bit is set to '1.'
- External interference of the crystal

For the M41T93, if the oscillator fail interrupt enable bit (OFIE) is set to a '1,' the $\overline{IRQ}$/FT/OUT pin will also be activated. The $\overline{IRQ}$/FT/OUT output is cleared by resetting the OFIE or OF bit to '0' (NOT by reading the flag register).

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to '0.' If the trigger event occurs during a power down condition, this bit will be set correctly.

3.14 Oscillator fail interrupt enable

If the oscillator fail interrupt bit (OFIE) is set to a '1,' the $\overline{IRQ}$/FT/OUT pin will also be activated. The $\overline{IRQ}$/FT/OUT output is cleared by resetting the OFIE or OF bit to '0' (not be reading the flags register).

3.15 Initial power-on defaults

Upon initial application of power to the device, the register bits will initially power-on in the state indicated in *Table 13* and *Table 14*.

Table 13. Initial power-on default values (part 1)

Condition[1]	ST	CB1	CB0	OUT	FT	DCS ACS	Digital calib.	Analog calib.	OFIE	Watchdog[2]	A1IE	SQWE	ABE
Initial power-up	0	0	0	1	0	0	0	0	0	0	0	1	0
Subsequent power-up[3][4]	UC	UC	UC	UC	0	UC	UC	UC	UC	0	UC	UC	UC

1. All other control bits power-up in an undetermined state
2. BMB0-BMB4, RB0, RB1
3. With battery backup
4. UC = Unchanged

Table 14. Initial power-up default values (part 2)

Condition[1]	RPT11-15	HT	OF	TE	$\overline{TI}$/TP	TIE	TD1	TD0	RS0	RS1-3	OTP	RPT21-25	AL2E
Initial power-up	0	1	1	0	0	0	1	1	1	0	0	0	0
Subsequent power-up [2][3]	UC	1	UC	0	UC	UC	UC	UC	UC	UC	UC	UC	UC

1. All other control bits power-up in an undetermined state
2. With battery backup
3. UC = Unchanged

3.16 OTP bit operation (SOX18 package only)

When the OTP (one time programmable) bit is set to a '1,' the value in the internal OTP registers will be transferred to the analog calibration register (12h) and are “read only.” The OTP value is programmed by the manufacturer, and will contain the calibration value necessary to achieve ±5 ppm at room temperature after two SMT reflows. This clock accuracy can be guaranteed to drift no more than ±3 ppm the first year, and ±1 ppm for each following year due to crystal aging.

If the OTP bit is set to '0,' the analog calibration register will become a WRITE/READ register and function like standard SRAM memory cells, allowing the user to implement any desired value of analog calibration.

When the user sets the OTP bit, they need to wait for approximately 8 ms before the analog registers transfer the value from the OTP to the analog registers due to the OTP read operation.

4 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 15. Absolute maximum ratings

Symbol	Parameter		Value(1)	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 7.0	V
T_{SLD}(2)	Lead solder temperature for 10 seconds	QFN16	260	°C
		SOX18	245	°C
V_{IO}	Input or output voltages		–0.2 to Vcc+0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. Data based on characterization results, not tested in production.
2. Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 16. Operating and AC measurement conditions

Parameter	M41T93
Supply voltage (V_{CC})	2.38 V to 5.5 V
Ambient operating temperature (T_A)	–40 to +85°C
Load capacitance (C_L, typical)	30 pF
Input rise and fall times	≤ 50 ns
Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and output timing ref. voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 16. Measurement AC I/O waveform

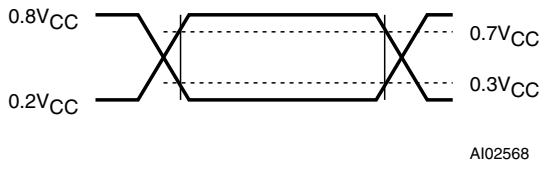


Table 17. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{OUT}[3]	Output capacitance		10	pF

1. Effective capacitance measured with power supply at 3.6 V; sampled only, not 100% tested
2. At 25°C, f = 1 MHz
3. Outputs deselected

Table 18. DC characteristics

Sym	Parameter	Test condition(1)		Min	Typ	Max	Unit
V_{CC}	Operating voltage (S)	–40 to 85°C		3.00		5.50	V
	Operating voltage (R)	–40 to 85°C		2.70		5.50	V
	Operating voltage (Z)	–40 to 85°C		2.38		5.50	V
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$				±1	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$				±1	µA
I_{CC1}	Supply current SCL = $0.1V_{CC}/0.9V_{CC}$ SDO = open	f_{SCL} = 2 MHz				0.5	mA
		f_{SCL} = 5 MHz				1.0	mA
		f_{SCL} = 10 MHz				2.0	mA
I_{CC2}	Supply current (standby)	$\overline{E} = V_{CC}$; All inputs $\ge V_{CC} - 0.2$ V; $\le V_{SS} + 0.2$ V	5.5 V		8	10	µA
			3.0 V		6.5		µA
V_{IL}	Input low voltage			–0.3		$0.3V_{CC}$	V
V_{IH}	Input high voltage			$0.7V_{CC}$		V_{CC}+0.3	V
V_{OL}	Output low voltage	$\overline{RST}$, FT/$\overline{RST}$	V_{CC}/V_{BAT} = 3.0 V, I_{OL} = 1.0 mA			0.4	V
		SQW, $\overline{IRQ}$/FT/OUT	V_{CC} = 3.0 V, I_{OL} = 1.0 mA			0.4	V
		SDO	V_{CC} = 3.0 V, I_{OL} = 3.0 mA			0.4	V
V_{OH}	Output high voltage	V_{CC} = 3.0 V, I_{OH} = –1.0 mA (push-pull)		2.4			V
	Pull-up supply voltage (open drain)	$\overline{IRQ}$/FT/OUT				5.5	V
V_{BAT}	Backup supply voltage			1.8		5.5	V
I_{BAT}	Battery supply current	25°C; V_{CC} = 0 V; OSC on; V_{BAT} = 3 V; 32 kHz off			365	450	nA

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.38 V to 5.5 V (except where noted)

Figure 17. I_{CC2} vs. temperature

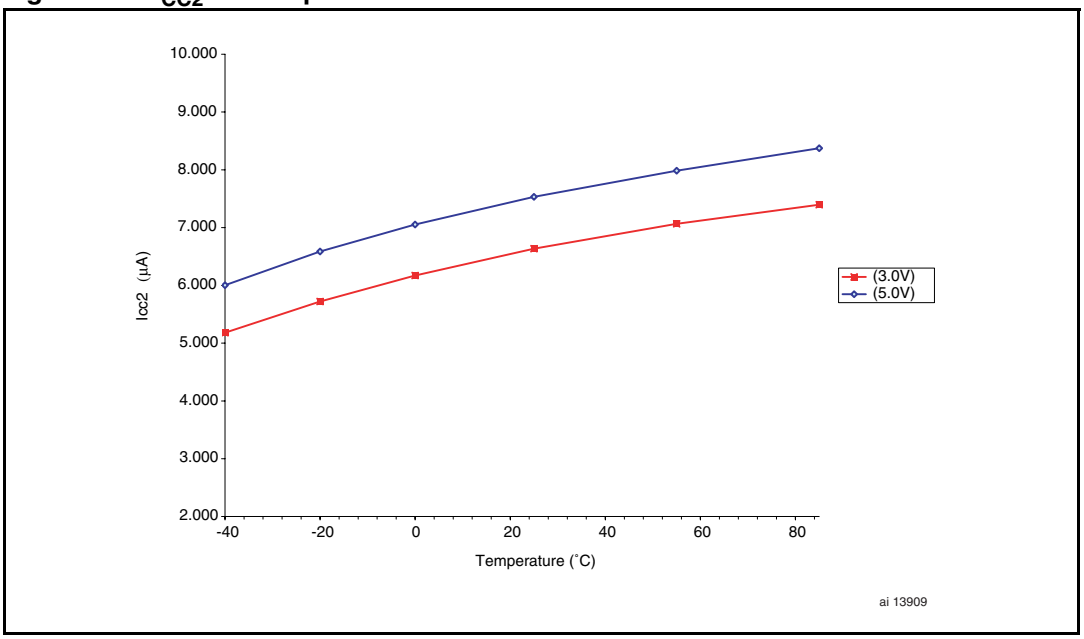


Table 19. Crystal electrical characteristics

Symbol	Parameter[1][2]	Min	Typ	Max	Units
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			65[3]	kΩ
C_L	Load capacitance		12.5		pF

1. Externally supplied if using the QFN16 package. STMicroelectronics recommends the Citizen CFS-145 (1.5 x 5 mm) and the KDS DT-38 (3 x 8 mm) for thru-hole, or the KDS DMX-26S (3.2 x 8 mm) or Micro Crystal MS3V-T1R (1.5 x 5 mm) for surface-mount, tuning fork-type quartz crystals. For contact information, see *Section 8: References on page 49*.
2. Load capacitors are integrated within the M41T93. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. Guaranteed by design.

Table 20. Oscillator characteristics

Symbol	Parameter[1][2]	Conditions	Min	Typ	Max	Units
V_{STA}	Oscillator start voltage	≤4 s	2.0			V
t_{STA}	Oscillator start time	$V_{CC} = V_{SO}$			1	s
C_{XI}, C_{XO}[1]	Capacitor input, capacitor output			25		pF
	IC-to-IC frequency variation[2][3]		–10		+10	ppm

1. With default analog calibration value (= 0)
2. Reference value
3. T_A = 25°C, V_{CC} = 5.0 V

Figure 18. Power down/up mode AC waveforms

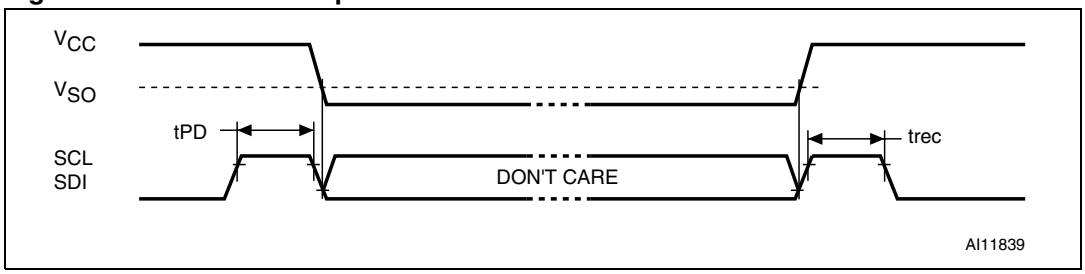


Table 21. Power down/up trip points DC characteristics

Sym	Parameter[1][2]		Min	Typ	Max	Unit
V_{RST}	Reset threshold voltage	S	2.85	2.93	3.0	V
		R	2.55	2.63	2.7	V
		Z	2.25	2.32	2.38	V
V_{SO}	Battery backup switchover		V_{RST}			V
	Hysteresis		25			mV
t_{rec}	Reset pulse width (V_{CC} rising)		140		280	ms
	V_{CC} to reset delay, V_{CC} = (V_{RST} + 100 mV), falling to (V_{RST} – 100 mV; for V_{CC} slew rate of 10 mV/µs			2.5		µs

1. All voltages referenced to V_{SS}
2. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.38 to 5.5 V (except where noted)

Figure 19. Input timing requirements

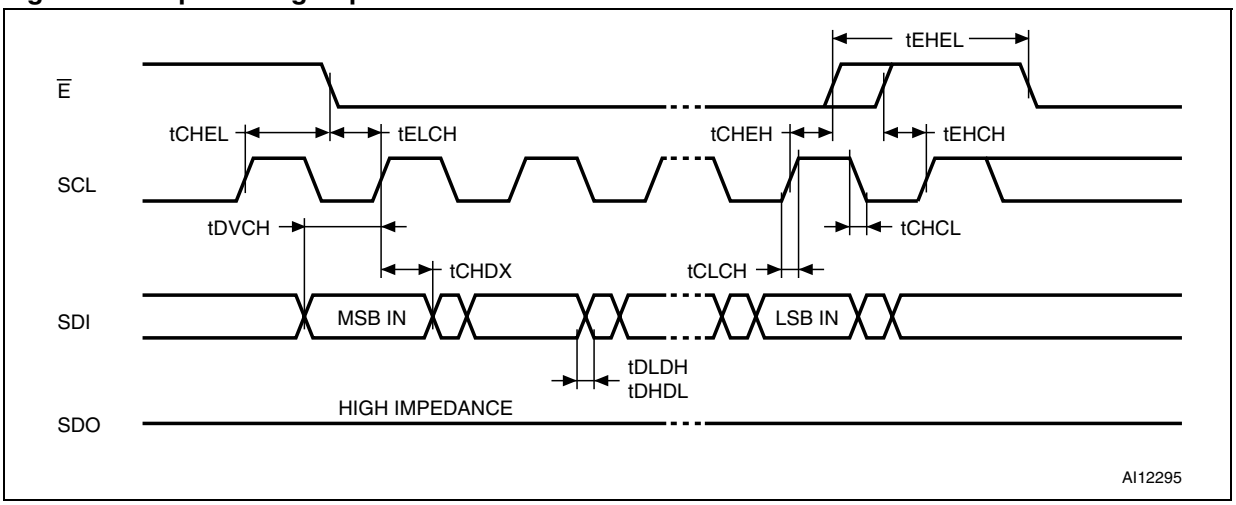


Figure 20. Output timing requirements

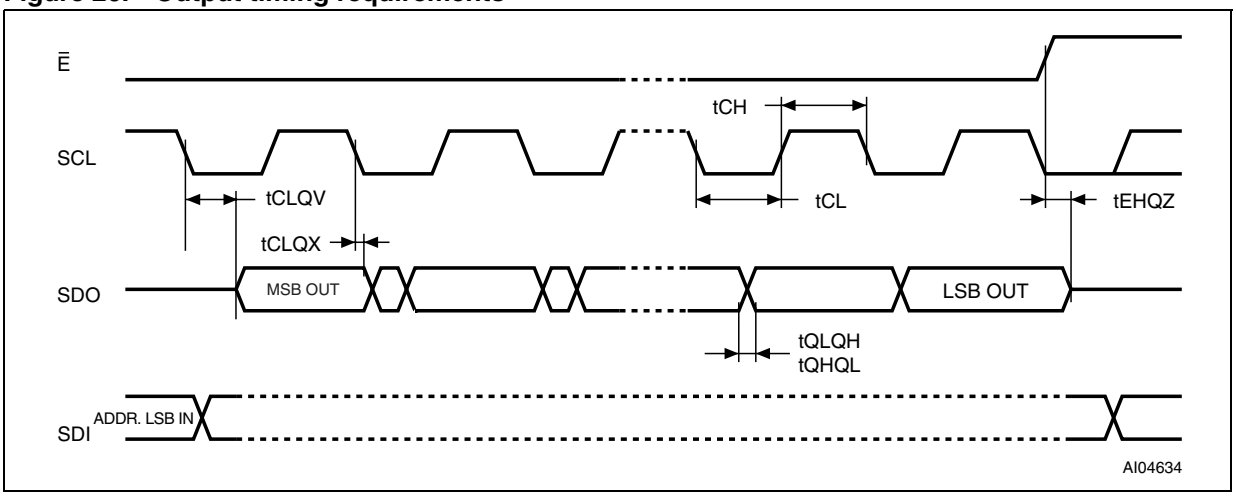


Table 22. AC characteristics

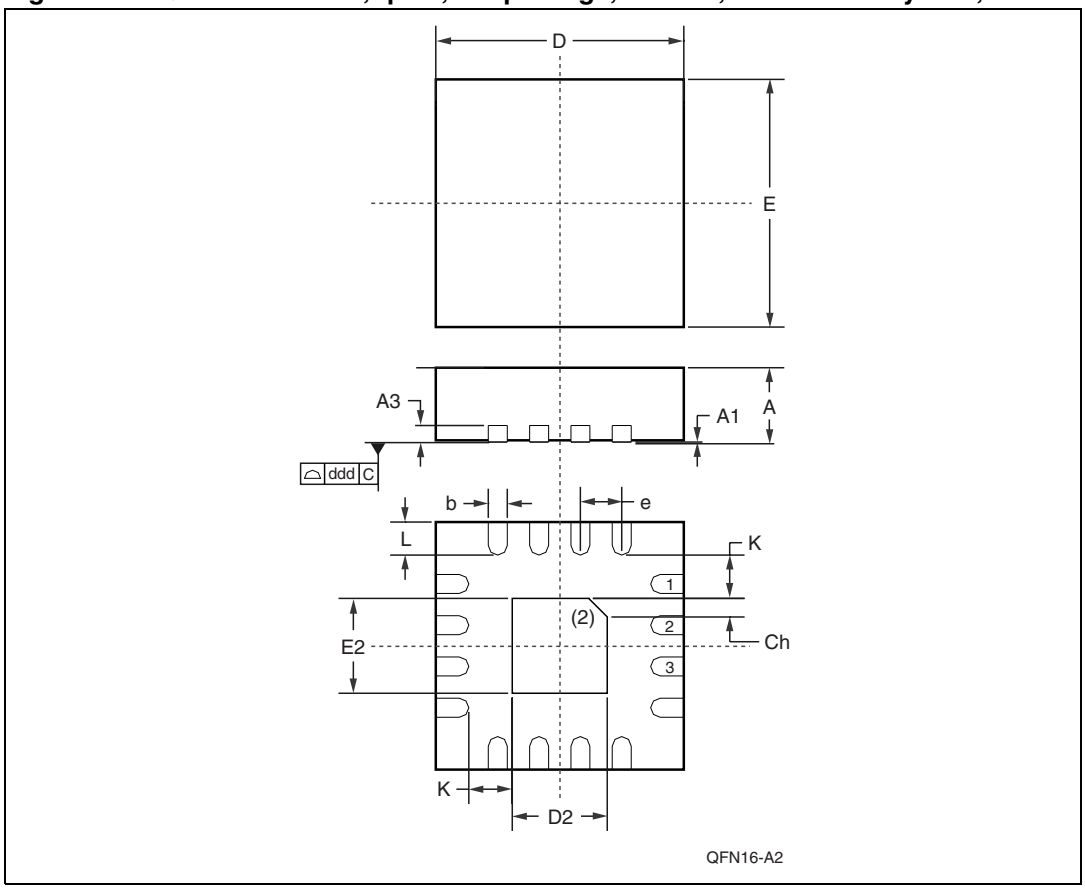
Sym	Parameter[1]	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	D.C.	5	D.C.	10	MHz
t_{ELCH}	$\overline{E}$ active setup time	90		30		ns
t_{EHCH}	$\overline{E}$ not active setup time	90		30		ns
t_{EHEL}	$\overline{E}$ deselect time	100		40		ns
t_{CHEH}	$\overline{E}$ active hold time	90		30		ns
t_{CHEL}	$\overline{E}$ not active hold time	90		30		ns
t_{CH}[2]	Clock high time	90		40		ns
t_{CL}[2]	Clock low time	90		40		ns
t_{CLCH}[3]	Clock rise time		1		2	µs
t_{CHCL}[3]	Clock fall time		1		2	µs
t_{DVCH}	Data in setup time	20		10		ns
t_{CHDX}	Data in hold time	30		10		ns
t_{EHQZ}[3]	Output disable time		100		40	ns
t_{CLQV}	Clock low to output valid		60		40	ns
t_{CLQX}	Output hold time	0		0		ns
t_{QLQH}[3]	Output rise time		50		40	ns
t_{QHQL}[3]	Output fall time		50		40	ns

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.38 to 5.5 V (except where noted)
2. t_{CH} and t_{CL} must never be lower than the shortest possible clock period, $1/f_{C(max)}$
3. Value guaranteed by characterization, not 100% tested in production

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at **www.st.com**.

Figure 21. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm body size, outline

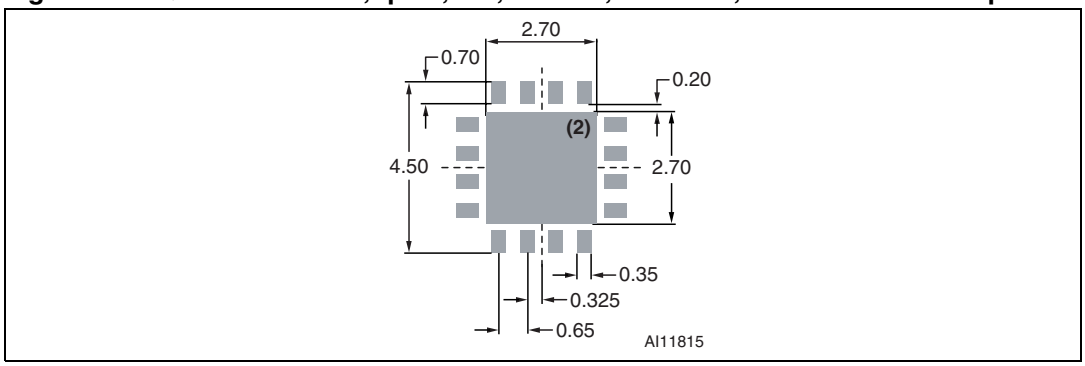


1. Drawing is not to scale
2. Substrate pad should be tied to V_{SS}

Table 23. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm body, mech. data

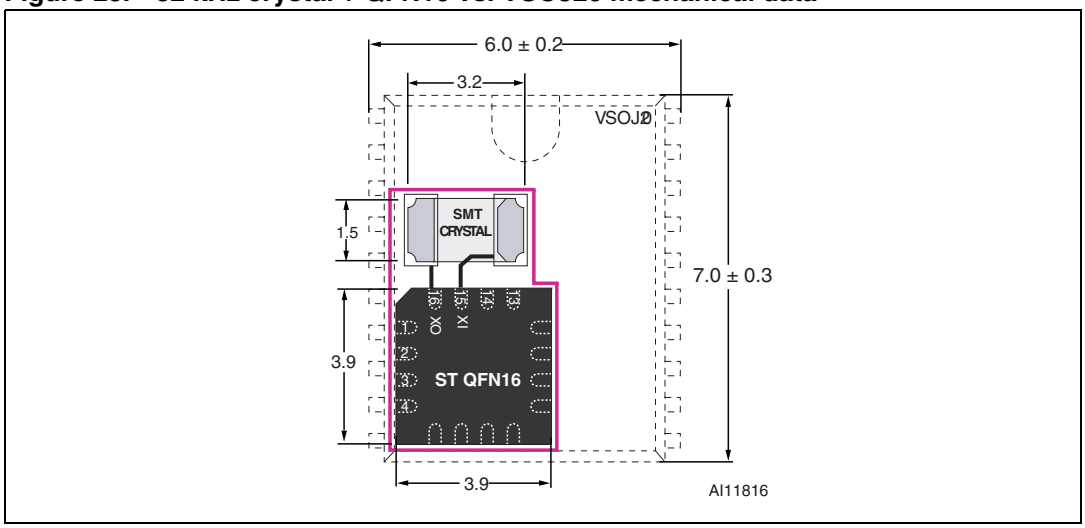
Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.90	0.80	1.00	0.035	0.032	0.039
A1	0.02	0.00	0.05	0.001	0.000	0.002
A3	0.20	–	–	0.008	–	–
b	0.30	0.25	0.35	0.010	0.007	0.012
D	4.00	3.90	4.10	0.118	0.114	0.122
D2	–	2.50	2.80	0.067	0.061	0.071
E	4.00	3.90	4.10	0.118	0.114	0.122
E2	–	2.50	2.80	0.067	0.061	0.071
e	0.65	–	–	0.020	–	–
K	0.20	–	–	0.008	–	–
L	0.40	0.30	0.50	0.016	0.012	0.020
ddd	–	0.08	–	–	0.003	–
Ch	–	0.33	–	–	0.013	–
N	16			16		

Figure 22. QFN16 – 16-lead, quad, flat, no lead, 4 x 4 mm, recommended footprint



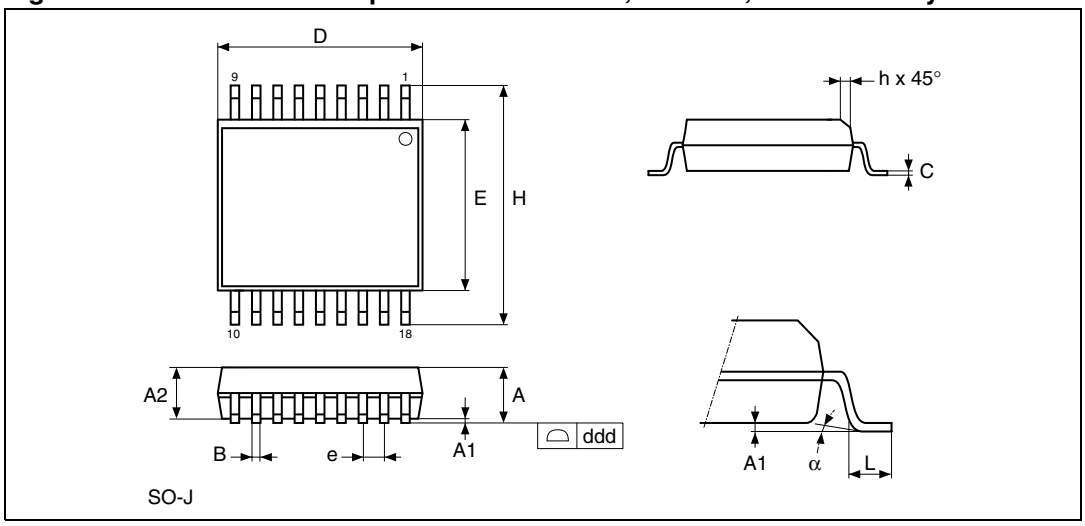
1. Dimensions shown are in millimeters (mm)
2. Substrate pad should be tied to V_{SS}

Figure 23. 32 kHz crystal + QFN16 vs. VSOJ20 mechanical data



Note: Dimensions shown are in millimeters (mm).

Figure 24. SOX18 – 18-lead plastic small outline, 300 mils, embedded crystal



Note: Drawing is not to scale.

Table 24. SOX18 – 18-lead plastic SO, 300 mils, embedded crystal, pkg. mech. data

Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	2.44	2.69	–	0.096	0.106
A1	–	0.15	0.31	–	0.006	0.012
A2	–	2.29	2.39	–	0.090	0.094
B	–	0.41	0.51	–	0.016	0.020
C	–	0.20	0.31	–	0.008	0.012
D	11.61	11.56	11.66	0.457	0.455	0.459
ddd	–	–	0.10	–	–	0.004
E	–	7.57	7.67	–	0.298	0.302
e	1.27	–	–	0.050	–	–
H	–	10.16	10.52	–	0.400	0.414
L	–	0.51	0.81	–	0.020	0.032
α	–	0°	8°	–	0°	8°
N	18			18		

7 Part numbering

Table 25. Ordering information

Example: M41T 93 S QA 6 E

Device family

M41T

Device type

93

Operating voltage

S = V_{CC} = 3.00 to 5.5 V

R = V_{CC} = 2.70 to 5.5 V

Z = V_{CC} = 2.38 to 5.5 V

Package

QA = QFN16 (4 mm x 4 mm)

MY(1) = SOX18

Temperature range

6 = –40°C to +85°C

Shipping method

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

1. The SOX18 package includes an embedded 32,768 Hz crystal. Contact local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 References

Below is a listing of the crystal component suppliers mentioned in this document.

- KDS can be contacted at **kouhou@kdsj.co.jp** or **http://www.kdsj.co.jp**.
- Citizen can be contacted at **csd@citizen-america.com** or **http://www.citizencrystal.com**.
- Micro Crystal can be contacted at **sales@microcrystal.ch** or **http://www.microcrystal.com**.

9 Revision history

Table 26. Document revision history

Date	Revision	Changes
07-Aug-2006	1	Initial release.
08-May-2007	2	Document status upgraded to full datasheet; updated *Figure 11: Clock accuracy vs. on-chip load capacitors*; *Section 3.16*; *Section 3.4.1*; *Table 1*, *15*, and *18*, *Figure 3* and *23*; added *Figure 17: I_{CC2} vs. temperature*. Micro Crystal information added (*Table 19*).
22-Oct-2007	3	Updated Features on cover page; minor formatting changes; modified footnote 1 in *Table 19*; added *Section 8: References*.
15-Aug-2008	4	Removed references to SPI bus mode 3 operation (updated cover page, *Figure 5*, *6*, *Section 1.1.3*, *Section 2.1*); minor formatting changes.

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