Push-Pull PWM Controller

FEATURES

- **High Efficiency Push-Pull PWM**
- **1.5A Sink, 1A Source Output Drivers**
- **Adjustable Push-Pull Dead-Time**
- **Adjustable System Undervoltage Lockout and Hysteresis**
- Adjustable Leading Edge Blanking
- Low Start-Up and Quiescent Currents
- Current Mode Operation
- Single Resistor Slope Compensation
- V_{CC} UVLO and 25mA Shunt Regulator
- Programmable Fixed Frequency Operation to 1MHz
- Soft-Start, Cycle-by-Cycle Current Limiting and Hiccup Mode Short-Circuit Protection
- 5V, 15mA Low Dropout Regulator
- 16-Pin SSOP and (4mm × 4mm) QFN Packages

APPLICATIONS

- Telecommunications, Infrastructure Power Systems
- Distributed Power Architectures
- Server Power Supplies
- High Density Power Modules

DESCRIPTION

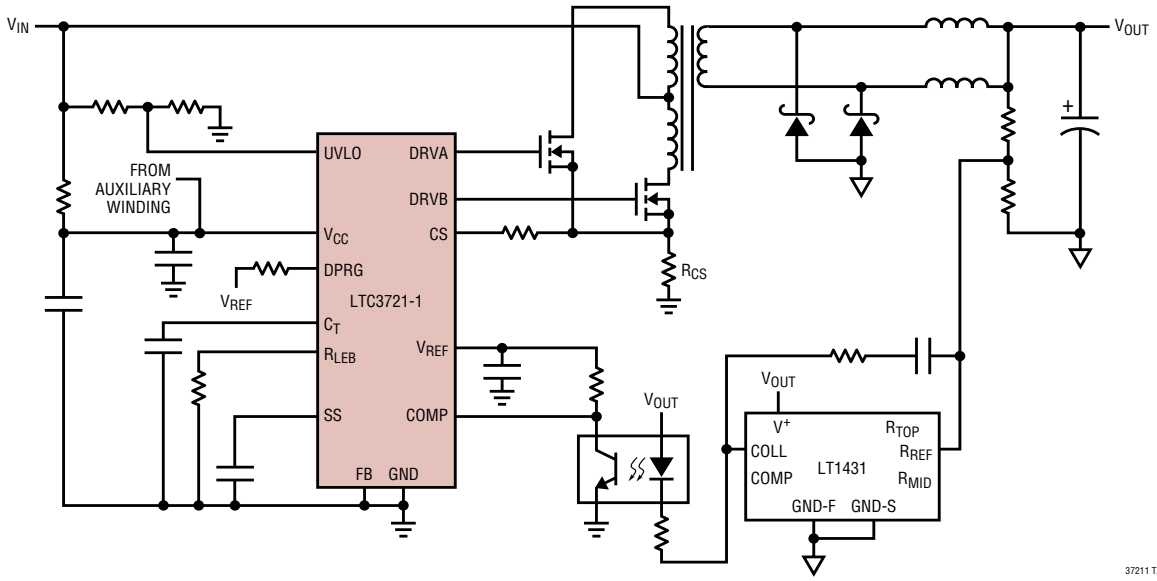
The LTC®3721-1 push-pull PWM controller provides all of the control and protection functions necessary for compact and highly efficient, isolated power converters. High integration minimizes external component count, while preserving design flexibility.

The robust push-pull output stages switch at half the oscillator frequency. Dead-time is independently programmed with an external resistor. A UVLO program input provides precise system turn-on and turn off voltages. The LTC3721-1 features peak current mode control with programmable slope compensation and leading edge blanking.

The LTC3721-1 features extremely low operating and start-up currents and reliable short-circuit and overtemperature protection. The LTC3721-1 is offered in 16-pin SSOP and (4mm × 4mm) QFN packages.

TYPICAL APPLICATION

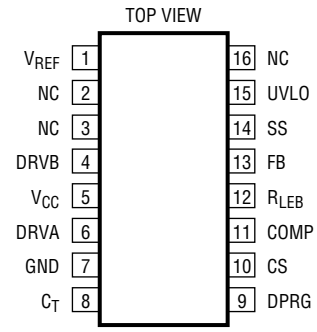
Isolated Push-Pull Converter



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND (Low Impedance Source) .....–0.3V to 10V
(Chip Self-Regulates at 10.3V)
UVLO to GND ..... –0.3V to V_{CC}
All Other Pins to GND
(Low Impedance Source) .....–0.3V to 5.5V
V_{CC} (Current Fed) 40mA
V_{REF} Output Current ..... Self-Regulated
Operating Temperature (Notes 5,6)
LTC3721-1 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (GN Package only)
(Soldering, 10sec) ..... 300°C

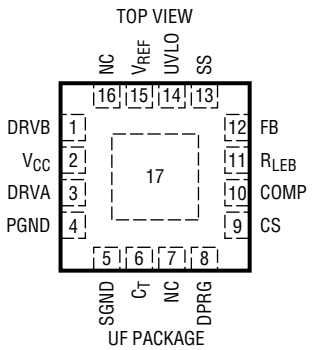
PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC3721EGN-1
GN PART MARKING
37211



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 100°C/W
EXPOSED PAD IS GND
(PIN17) MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3721EUF-1
UF PART MARKING
37211

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 9.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{CCUV}	V_{CC} Undervoltage Lockout	Measured on V_{CC}			10.25	10.7	V
V_{CCHY}	V_{CC} UVLO Hysteresis	Measured on V_{CC}		3.8	4.2		V
I_{CCST}	Start-Up Current	V_{CC} = V_{UVLO} – 0.3V	●		145	230	µA
I_{CCRN}	Operating Current	No Load on Outputs			3	6	mA
V_{SHUNT}	Shunt Regulator Voltage	Current into V_{CC} = 10mA			10.3	10.8	V
R_{SHUNT}	Shunt Resistance	Current into V_{CC} = 10mA to 17mA			1.4	3.5	Ω
SUVLO	System UVLO Threshold	Measured on UVLO Pin, 10mA into V_{CC}		4.8	5.0	5.2	V
SHYST	System UVLO Hysteresis Current	Current Flows Out of UVLO Pin, 10mA into V_{CC}		8.5	10	11.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 9.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Pulse Width Modulator							
ROS	Ramp Offset Voltage	Measured on COMP, CS = 0V			0.65		V
I_{RMP}	Ramp Discharge Current	CS = 1V, COMP = 0V, C_T = 4V			50		mA
I_{SLP}	Slope Compensation Current	Measured on CS, C_T = 1V C_T = 2.25V			30 68		µA µA
DCMAX	Maximum Duty Cycle	COMP = 4.5V	●	47	48.2	50	%
DCMIN	Minimum Duty Cycle	COMP = 0V	●		0		%
DTADJ	Dead-Time				130		ns
Oscillator							
OSCI	Initial Accuracy	T_A = 25°C, C_T = 270pF		220	250	280	kHz
OSCT	V_{CC} Variation	V_{CC} = 6.5V to 9.5V	●	–3		3	%
OSCV	C_T Ramp Amplitude	Measured on C_T			2.35		V
Error Amplifier							
V_{FB}	FB Input Voltage	COMP = 2.5V, (Note 3)		1.172	1.2	1.22	V
FB_I	FB Input Range	Measured on FB, (Note 4)		–0.3		2.5	V
AVOL	Open-Loop Gain	COMP = 1V to 3V, (Note 3)		70	90		dB
I_{IB}	Input Bias Current	COMP = 2.5V, (Note 3)			5	50	nA
V_{OH}	Output High	Load on COMP = –100µA		4.7	4.92		V
V_{OL}	Output Low	Load on COMP = 100µA			0.27	0.5	V
I_{SOURCE}	Output Source Current	COMP = 2.5V		400	700		µA
I_{SINK}	Output Sink Current	COMP = 2.5V		2	5		mA
Reference							
V_{REF}	Initial Accuracy	T_A = 25°C, Measured on V_{REF}		4.925	5.00	5.075	V
REFLD	Load Regulation	Load on V_{REF} = 100µA to 5mA			2	15	mV
REFLN	Line Regulation	V_{CC} = 6.5V to 9.5V			1	10	mV
REFTV	Total Variation	Line, Load and Temperature	●	4.900	5.000	5.100	V
REFSC	Short-Circuit Current	V_{REF} Shorted to GND		18	30	45	mA
Push-Pull Outputs							
DRVH(x)	Output High Voltage	$I_{OUT(x)}$ = –100mA			9.2		V
DRVL(x)	Output Low Voltage	$I_{OUT(x)}$ = 100mA			0.17		V
RDH(x)	Pull-Up Resistance	$I_{OUT(x)}$ = –10mA to –100mA			2.9		Ω
RDL(x)	Pull-Down Resistance	$I_{OUT(x)}$ = –10mA to –100mA			1.7		Ω
TDR(x)	Rise-Time	$C_{OUT(x)}$ = 1nF			10		ns
TDF(x)	Fall-Time	$C_{OUT(x)}$ = 1nF			10		ns
Current Limit and Shutdown							
CLPP	Pulse by Pulse Current Limit Threshold	Measured on CS		280	300	320	mV
CLSD	Shutdown Current Limit Threshold	Measured on CS		475	600	725	mV
CLDEL	Current Limit Delay to Output	100mV Overdrive on CS, (Note 2)			80		ns
SSI	Soft-Start Current	SS = 2.5V		10	13	16	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 9.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SSR	Soft-Start Reset Threshold	Measured on SS		0.7	0.4	0.1	V
FLT	Fault Reset Threshold	Measured on SS		4.5	4.2	3.5	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Includes leading edge blanking delay, R_{LEB} = 20k, not tested in production.

Note 3: FB is driven by a servo loop amplifier to control V_{COMP} for these tests.

Note 4: Set FB to –0.3V, 2.5V and insure that COMP does not phase invert.

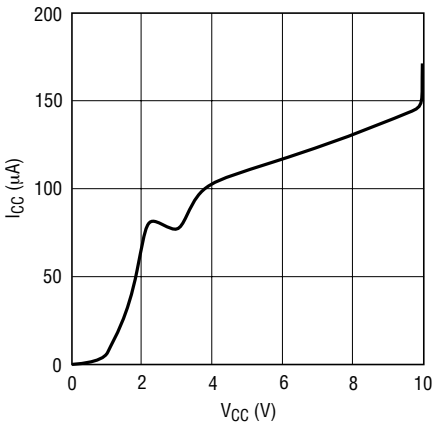
Note 5: The LTC3721–1 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

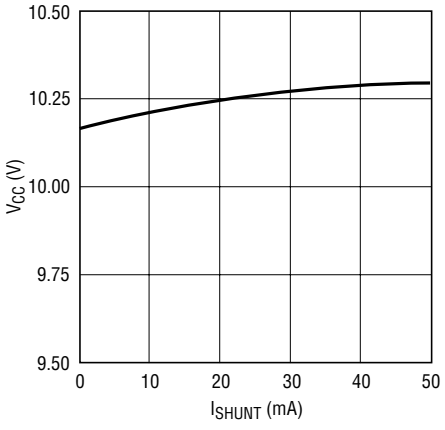
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

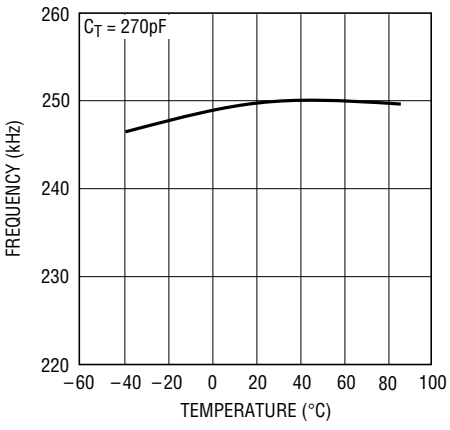
Start-Up I_{CC} vs V_{CC}



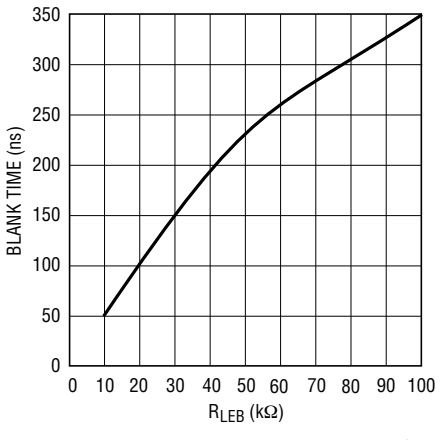
V_{CC} vs I_{SHUNT}



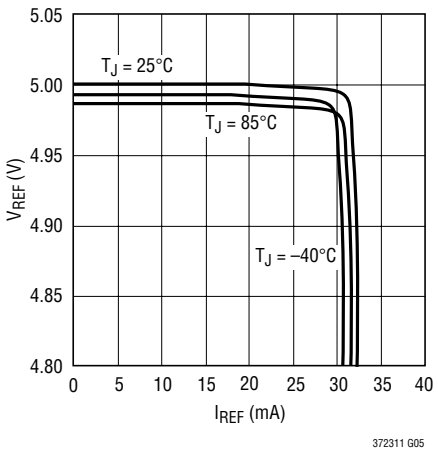
Oscillator Frequency vs Temperature



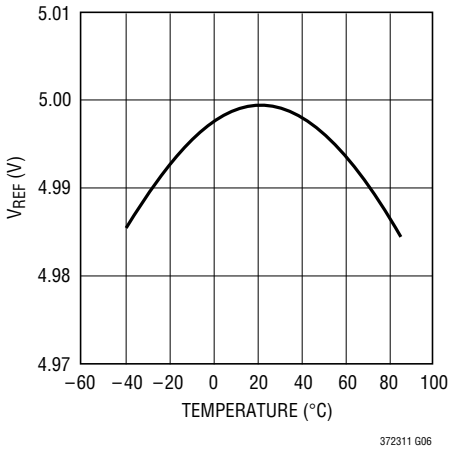
Leading Edge Blanking Time vs R_{LEB}



V_{REF} vs I_{REF}

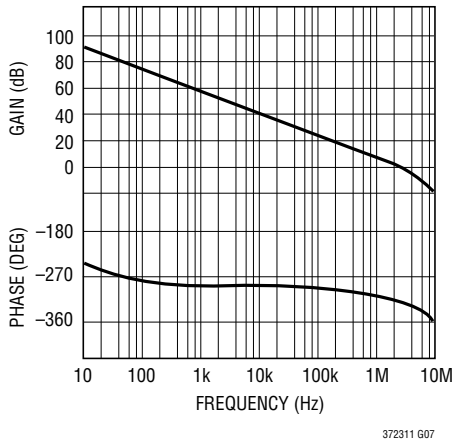


V_{REF} vs Temperature



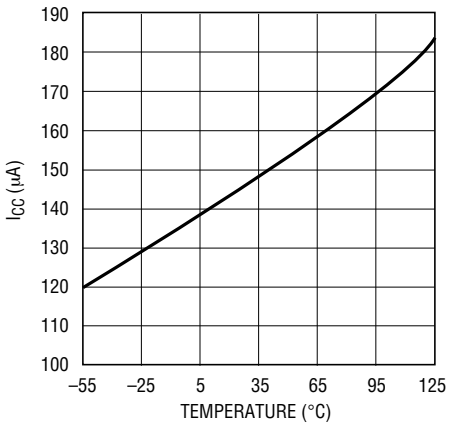
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Error Amplifier Gain/Phase



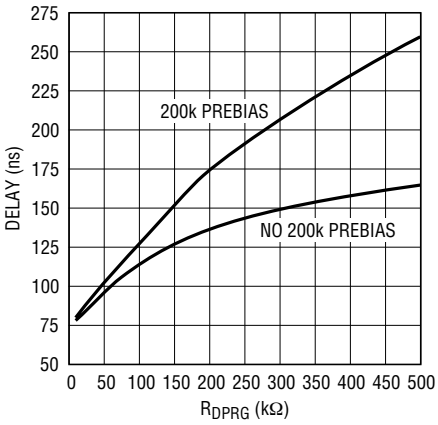
372311 G07

Start-Up I_{CC} vs Temperature



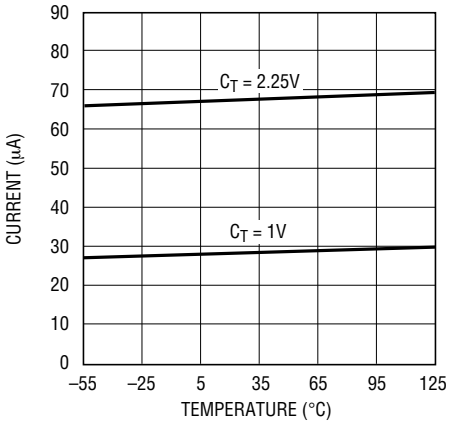
372311 G08

Deadtime vs R_{DPRG}



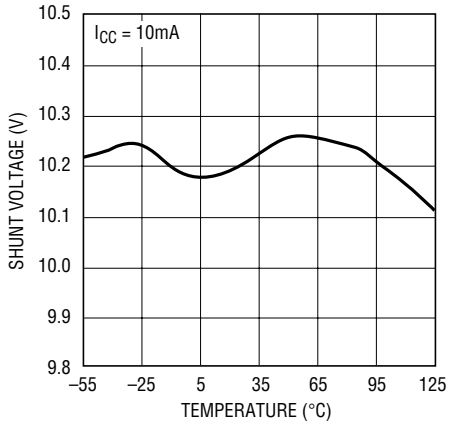
372311 G09

Slope Current vs Temperature



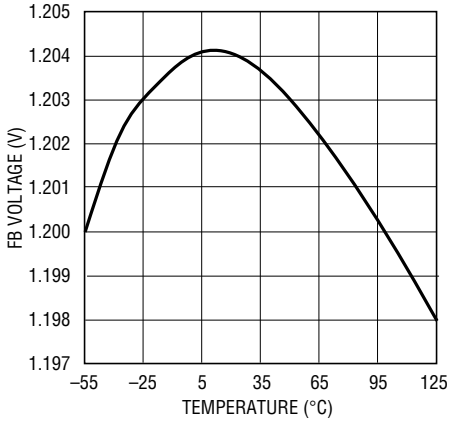
372311 G10

V_{CC} Shunt Voltage vs Temperature



372311 G11

FB Input Voltage vs Temperature



372311 G12

PIN DESCRIPTIONS (GN Package/UF Package)

V_{REF} (Pin 1/Pin 15): Output of the 5.0V Reference. V_{REF} is capable of supplying up to 18mA to external circuitry. V_{REF} should be decoupled to GND with a 1μF ceramic capacitor.

DRVB (Pin 4/Pin 1): High Speed 1.5A Sink, 1A Source Totem Pole MOSFET Driver. Connect to gate of external push-pull MOSFET with as short a PCB trace as practical to preserve drive signal integrity. A low value resistor connected between DRVA and the MOSFET gate is optional and will improve the gate drive signal quality if the PCB trace from the driver to the MOSFET cannot be made short.

V_{CC} (Pin 5/Pin 2): Supply Voltage Input to the LTC3721-1 and 10.25V Shunt Regulator. The chip is enabled after V_{CC} has risen high enough to allow the V_{CC} shunt regulator to conduct current and the UVLO comparator threshold is exceeded. Once the V_{CC} shunt regulator has turned on, V_{CC} can drop to as low as 6V (typical) and maintain operation. Bypass V_{CC} to GND with a high quality 1μF or larger ceramic capacitor to supply the transient currents caused by the high speed switching and capacitive loads presented by the on chip totem pole drivers.

DRVA (Pin 6/Pin 3): High Speed 1.5A Sink, 1A Source Totem Pole MOSFET Driver. Connect to gate of external push-pull MOSFET with as short a PCB trace as practical to preserve drive signal integrity. A low value resistor connected between DRVA and the MOSFET gate is optional and will improve the gate drive signal quality if the PCB trace from the driver to the MOSFET cannot be made short.

GND (Pin 7/Pin 4, Pin 5, Pin 17): All circuits in the LTC3721-1 are referenced to GND. Use of a ground plane is highly recommended. V_{IN} and V_{REF} bypass capacitors must be terminated with a star configuration as close to GND as practical for best performance. For the 4mm × 4mm QFN package only, the internal power (PGND) and signal (SGND) buses are connected separately to pins 4 and 5 respectively, and the exposed pad must be soldered to PCB ground.

C_T (Pin 8/Pin 6): Timing Capacitor for the Oscillator. Use a ±5% or better low ESR ceramic capacitor for best results. C_T ramp amplitude is 2.35V peak-to-peak (typical).

DPRG (Pin 9/Pin 8): Programming Input for Push-Pull Dead-Time. Connect a resistor between DPRG and V_{REF} to program the dead-time. The nominal voltage on DPRG is 2V.

CS (Pin 10/Pin 9): Input to Pulse-by-Pulse and Overload Current Limit Comparators, Output of Slope Compensation Circuitry. The pulse-by-pulse comparator has a nominal 300mV threshold, while the overload comparator has a nominal 600mV threshold. An internal switch discharges CS to GND after every timing period. Slope compensation current flows out of CS during the PWM period. An external resistor connected from CS to the external current sense resistor programs the amount of slope compensation.

COMP (Pin 11/Pin 10): Error Amplifier Output, Inverting Input to Phase Modulator.

R_{LEB} (Pin 12/Pin 11): Timing Resistor for Leading Edge Blanking. Use a 10k to 100k resistor connected between R_{LEB} and GND to program from 40ns to 310ns of leading edge blanking of the current sense signal on CS for the LTC3721-1. A ±1% tolerance resistor is recommended. The nominal voltage on R_{LEB} is 2V. If leading edge blanking is not required, tie R_{LEB} to V_{REF} to disable.

PIN DESCRIPTIONS (GN Package/UF Package)

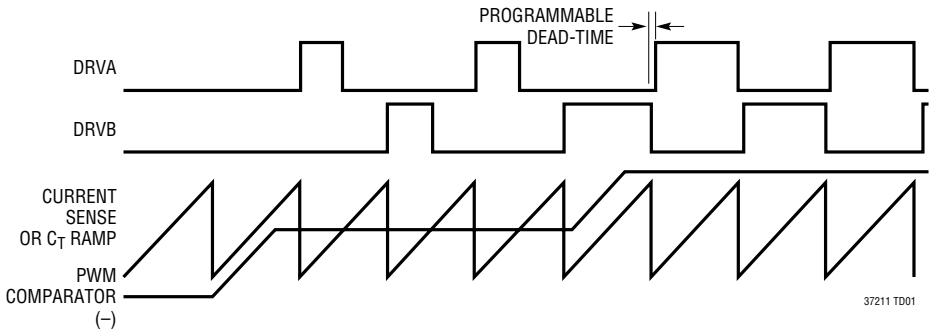
FB (Pin 13/Pin 12): Error Amplifier Inverting Input. This is the voltage feedback input for the LTC3721-1. The nominal regulation voltage at FB is 1.2V.

SS (Pin 14/Pin 13): Soft-Start/Restart Delay Circuitry Timing Capacitor. A capacitor from SS to GND provides a controlled ramp of the current command. During overload conditions, SS is discharged to ground initiating a soft-start cycle. SS charging current is approximately 13μA. SS will charge up to approximately 5V in normal operation. During a constant overload current fault, SS will oscillate at a low frequency between approximately 0.5V and 4V.

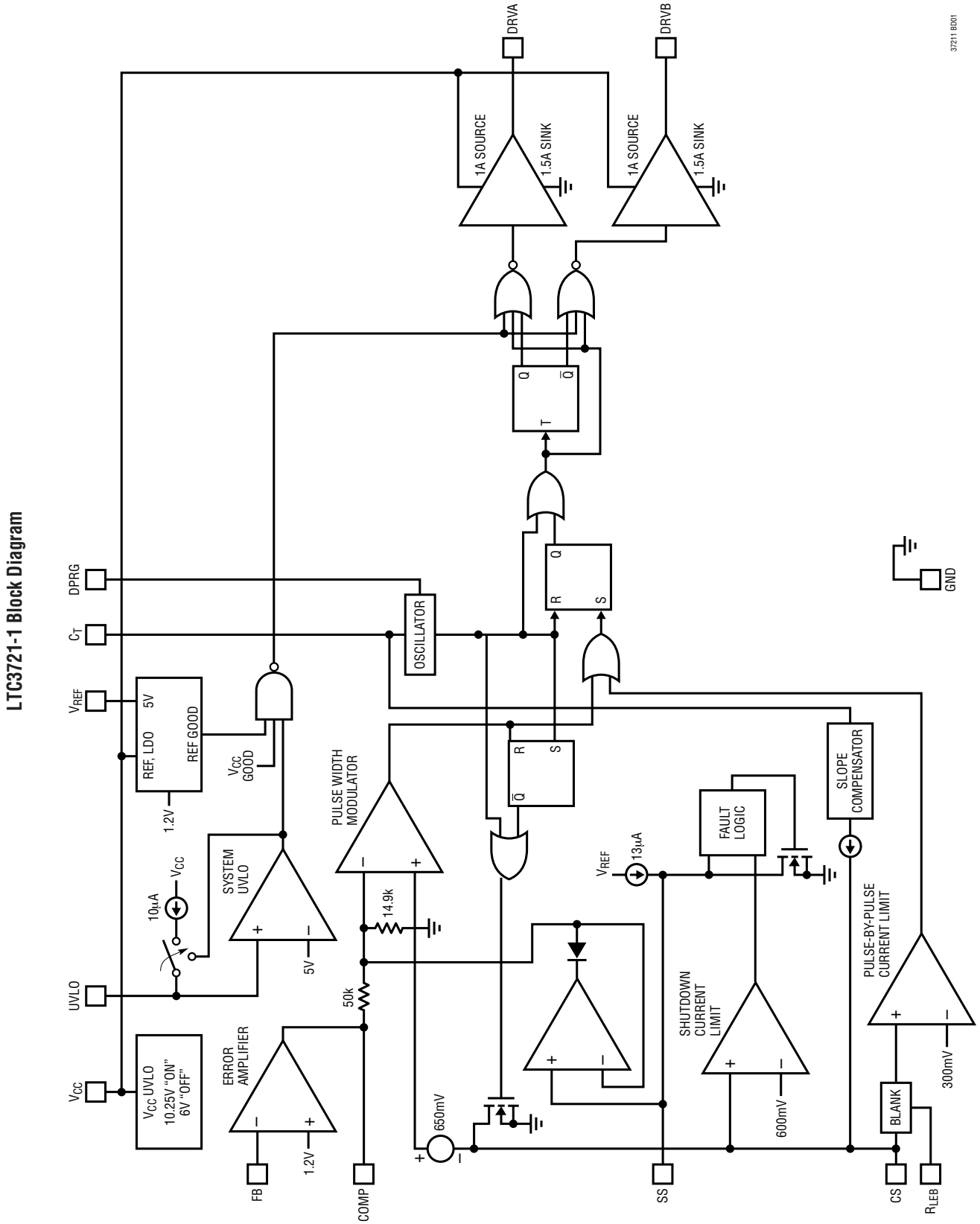
UVLO (Pin 15/Pin 14): Input to Program System Turn-On and Turn-Off Voltages. The nominal threshold of the UVLO comparator is 5.0V. UVLO is connected to the main DC system feed through a resistor divider. When the UVLO threshold is exceeded, the LTC3721-1 commences a soft-start cycle and a 10μA (nominal) current is fed out of UVLO to program the desired amount of system hysteresis. The hysteresis level can be adjusted by changing the resistance of the divider. UVLO can also be used to terminate all switching by pulling UVLO down to less than 4V. An open drain or collector switch can perform this function without changing the system turn on or turn off voltages.

NC (Pin 2, Pin 3, Pin 16/Pin 7, Pin 16): Not Connected.

TIMING DIAGRAM



BLOCK DIAGRAMS



OPERATION

Please refer to the detailed Block Diagram for this discussion. The LTC3721-1 is a PWM push-pull controller that operates with pulse-by-pulse peak current mode control. It is best suited for moderate to high power isolated power systems where small size and high efficiency are required. The push-pull topology delivers excellent transformer utilization and requires only two low side power MOSFET switches. The controller generates 180° out of phase 0% to <50% duty cycle drive signals on DRVA and DRVB. The external MOSFETs are driven directly by these powerful on-chip drivers. The external MOSFETs typically control opposite primary windings of a centertapped power transformer. The centertap primary winding is connected to the input DC feed. The secondary of the transformer can be configured in different synchronous or nonsynchronous configurations depending on the application needs.

The duty ratio is controlled by the voltage on COMP. A switching cycle commences with the falling edge of the internal oscillator clock pulse. The LTC3721-1 attenuates the voltage on COMP and compares it to the current sense signal to terminate the switching cycle. If the voltage on CS exceeds 300mV, the present cycle is terminated. If the voltage on CS exceeds 600mV, all switching stops and a soft-start sequence is initiated.

A host of other features including an error amplifier, system UVLO programming, adjustable leading edge blanking, slope compensation and programmable dead-time provide flexibility for a variety of applications.

Programming Driver Dead-Time

The LTC3721-1 includes a feature to program the minimum time between the output signals on DRVA and DRVB commonly referred to as the driver dead-time. This function will come into play if the controller is commanded for maximum duty cycle. The dead-time is set with an external resistor connected between DPRG and V_{REF} (see Figure 1). The nominal regulated voltage on DPRG is 2V. The external resistor programs a current which flows into DPRG. The dead-time can be adjusted from 90ns to 300ns with this resistor. The dead-time can also be modulated based on an external current source that feeds current into DPRG. Care must be taken to limit the current fed into DPRG to 350μA or less. An internal 10μA current source sets a maximum deadtime if DPRG is floated. The internal current source causes the programmed deadtime to vary non-linearly with increasing values of R_{DPRG} (see Typical Performance Characteristics). An external 200k resistor connected from DPRG to GND will compensate for the internal 10μA current source and linearize the deadtime delay vs R_{DPRG} characteristic.

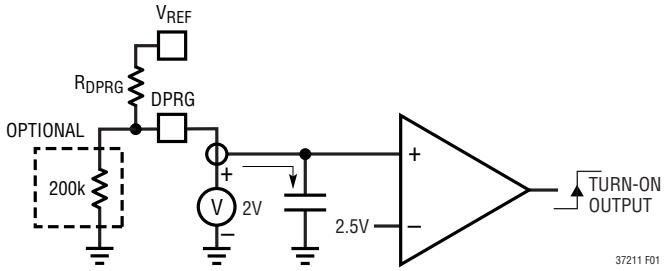


Figure 1. Deadtime Adjust

Powering the LTC3721-1

The LTC3721-1 utilizes an integrated V_{CC} shunt regulator to serve the dual purposes of limiting the voltage applied to V_{CC} as well as signaling that the chip's bias voltage is sufficient to begin switching operation (under voltage lockout). With its typical 10.2V turn-on voltage and 4.2V UVLO hysteresis, the LTC3721-1 is tolerant of loosely regulated input sources such as an auxiliary transformer winding. The V_{CC} shunt is capable of sinking up to 40mA of externally applied current. The UVLO turn-on and turn-off thresholds are derived from an internally trimmed reference making them extremely accurate. In addition, the LTC3721-1 exhibits very low (145μA typ) start-up current that allows the use of 1/8W to 1/4W trickle charge start-up resistors.

The trickle charge resistor should be selected as follows:

$$R_{START(MAX)} = V_{IN(MIN)} – 10.7V/250\mu A$$

Adding a small safety margin and choosing standard values yields:

APPLICATION	V_{IN} RANGE	R_{START}
DC/DC	36V to 72V	100k
Off-Line	85V to 270V_{RMS}	430k
PFC Preregulator	390V_{DC}	1.4M

OPERATION

V_{CC} should be bypassed with a 0.1µF to 1µF multilayer ceramic capacitor to decouple the fast transient currents demanded by the output drivers and a bulk tantalum or electrolytic capacitor to hold up the V_{CC} supply before the bootstrap winding, or an auxiliary regulator circuit takes over.

$C_{HOLDUP} = (I_{CC} + I_{DRIVE}) \bullet t_{DELAY}/3.8V$
(minimum UVLO hysteresis)

Regulated bias supplies as low as 7V can be utilized to provide bias to the LTC3721-1. Refer to Figure 2 for various bias supply configurations.

Programming Undervoltage Lockout

The LTC3721-1 provides undervoltage lockout (UVLO) control for the input DC voltage feed to the power converter in addition to the V_{CC} UVLO function described in the preceding section. Input DC feed UVLO is provided with the UVLO pin. A comparator on UVLO compares a divided down input DC feed voltage to the 5V precision reference. When the 5V level is exceeded on UVLO, the SS pin is released and output switching commences. At the same time a 10µA current is enabled which flows out of UVLO into the voltage divider connected to UVLO. The amount of DC feed hysteresis provided by this current is: 10µA • R_{TOP}, (Figure 3). The system UVLO threshold is: 5V • {(R_{TOP} + R_{BOTTOM})/R_{BOTTOM}}. If the voltage applied to UVLO is present and greater than 5V prior to the V_{CC} UVLO circuitry activation, then the internal UVLO logic will prevent output switching until the following three conditions are met: (1) V_{CC} UVLO is enabled, (2) V_{REF} is in regulation and (3) UVLO pin is greater than 5V.

UVLO can also be used to enable and disable the power converter. An open drain transistor connected to UVLO as shown in Figure 3 provides this capability.

Off-Line Bias Supply Generation

If a regulated bias supply is not available to provide V_{CC} voltage to the LTC3721-1 and supporting circuitry, one must be generated. Since the power requirement is small, approximately 1W, and the regulation is not critical, a simple open-loop method is usually the easiest and lowest cost approach. One method that works well is to add a winding to the main power transformer, and post regulate the resultant square wave with an L-C filter (see Figure 4a). The advantage of this approach is that it maintains decent regulation as the supply voltage varies, and it does not require full safety isolation from the input winding of the transformer. Some manufacturers include a primary winding for this purpose in their standard product offerings as well. A different approach is to add a winding to the output inductor and peak detect and filter the square wave signal (see Figure 4b). The polarity of this winding is designed so

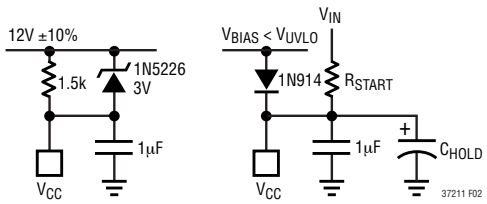


Figure 2. Bias Configurations

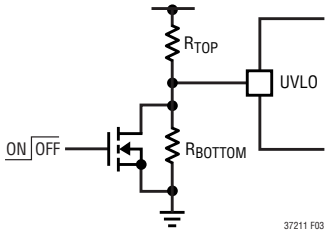


Figure 3. System UVLO Setup

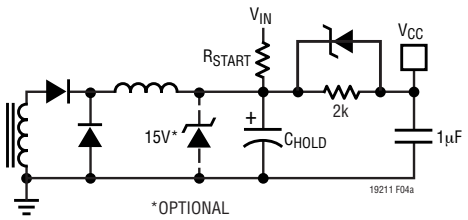


Figure 4a. Auxiliary Winding Bias Supply

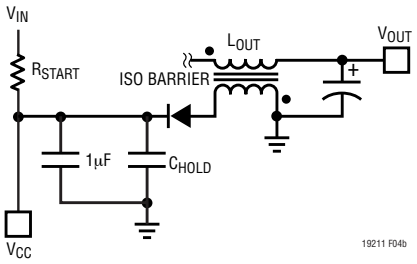


Figure 4b. Output Inductor Bias Supply

OPERATION

that the positive voltage square wave is produced while the output inductor is freewheeling. An advantage of this technique over the previous is that it does not require a separate filter inductor and since the voltage is derived from the well-regulated output voltage, it is also well controlled. One disadvantage is that this winding will require the same safety isolation that is required for the main transformer. Another disadvantage is that a much larger V_{CC} filter capacitor is needed, since it does not generate a voltage as the output is first starting up, or during short-circuit conditions.

Programming the LTC3721-1 Oscillator

The high accuracy LTC3721-1 oscillator circuit provides flexibility to program the switching frequency and slope compensation required for current mode control. The oscillator circuit produces a 2.35V peak-to-peak amplitude ramp waveform on C_T. Typical maximum duty cycles of 49% are possible. The oscillator is capable of operation up to 1MHz by the following equation:

$$C_T = 1/(14.8k \bullet F_{OSC})$$

Note that this is the frequency seen on C_T. The output drivers switch at 1/2 of this frequency. Also note that higher switching frequency and added driver dead-time via DPRG will reduce the maximum duty cycle.

The LTC3721-1 derives a compensating slope current from the oscillator ramp waveform and sources this current out of CS. The desired level of slope compensation is selected with an external resistor connected between CS and the external current sense resistor, (Figure 5).

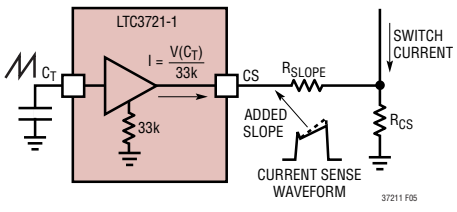


Figure 5. Slope Compensation Circuitry

Current Sensing and Overcurrent Protection

Current sensing provides feedback for the current mode control loop and protection from overload conditions. The LTC3721-1 is compatible with either resistive sensing or current transformer methods. Internally connected to CS are two comparators that provide pulse-by-pulse and overcurrent shutdown functions respectively, (Figure 6).

The pulse-by-pulse comparator has a 300mV nominal threshold. If the 300mV threshold is exceeded, the PWM cycle is terminated. The overcurrent comparator is set approximately 2x higher than the pulse-by-pulse level. If the current signal exceeds this level, the PWM cycle is terminated, the soft-start capacitor is quickly discharged and a soft-start cycle is initiated. If the overcurrent condition persists, the LTC3721-1 halts PWM operation and waits for the soft-start capacitor to charge up to approximately 4V before a retry is allowed. The soft-start capacitor is charged by an internal 13μA current source. If the fault condition has not cleared when soft-start reaches 4V, the soft-start pin is again discharged and a new cycle is initiated. This is referred to as hiccup mode operation. In normal operation and under most abnormal conditions, the pulse-by-pulse comparator is fast enough to prevent hiccup mode operation. In severe cases, however, with high input voltage, very low $R_{DS(ON)}$ MOSFETs and a shorted output, or with saturating magnetics, the overcurrent comparator provides a means of protecting the power converter.

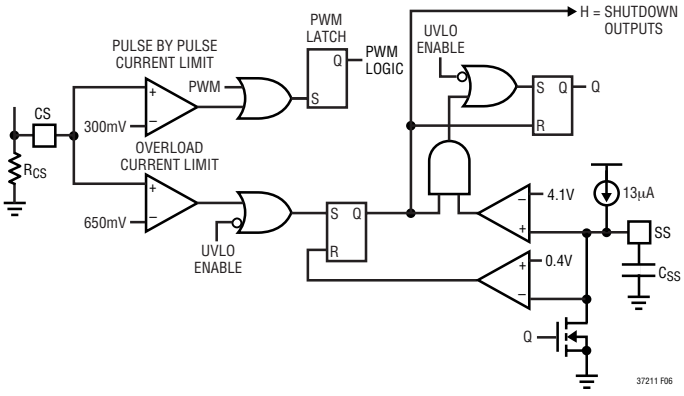


Figure 6. Current Sense/Fault Circuitry Detail

OPERATION

Leading Edge Blanking

The LTC3721-1 provides programmable leading edge blanking to prevent nuisance tripping of the current sense circuitry. Leading edge blanking relieves the filtering requirements for the CS pin, greatly improving the response to real overcurrent conditions. It also allows the use of a ground referenced current sense resistor or transformer(s), further simplifying the design. With a single 10k to 100k resistor from R_{LEB} to GND, blanking times of approximately 40ns to 320ns are programmed. If not required, connecting R_{LEB} to V_{REF} can disable leading edge blanking. Keep in mind that the use of leading edge blanking will slightly reduce the linear control range for the pulse width modulator.

High Current Drivers

The LTC3721-1 high current, high speed drivers provide direct drive of external power N-channel MOSFET switches. The drivers swing from rail to rail. Due to the high pulsed current nature of these drivers (1.5A sink, 1A source), care must be taken with the board layout to obtain advertised performance. Bypass V_{CC} with a 1µF minimum, low ESR, ESL ceramic capacitor. Connect this capacitor with minimal length PCB leads to both V_{CC} and GND. A ground plane is highly recommended. The driver output pins (DRVA, DRVB) connect to the gates of the external MOSFET switches. The PCB traces making these connections should also be as short as possible to minimize overshoot and undershoot of the drive signal.

Transformer Configurations

The LTC3721-1 used in a typical isolated push-pull converter application will need a transformer to provide the voltage translation and galvanic isolation. The push-pull transformer employs a center tapped primary winding configuration. The transformer secondary can be center tapped or a single winding depending on the configuration and application needs.

Center tapped secondary configurations apply alternating <50% duty cycle square waves to a single inductor/capacitor combination. This L-C circuit filters the square wave and produces the regulated output voltage. The secondary square wave amplitude is given by:

$V_{SEC} = V_{IN} \bullet N$, where N = Ns/Np, transformer turns ratio, # of secondary turns divided by # of primary turns.

OPERATION

The duty cycle of these square waves is guaranteed to never exceed 50% by the LTC3721-1. In steady state operation, the duty ratio is given by:

$$D = V_{OUT}/(2 \bullet V_{IN} \bullet N)$$

To calculate the transformer turns ratio, first determine the minimum input voltage ($V_{IN(MIN)}$) and the maximum duty ratio ($D_{(MAX)}$) of the controller IC. This will be the worst case condition. An example is provided below:

V_{IN} = 32V to 75V, use $V_{IN(MIN)}$ = 30V to account for system voltage drops.

V_{OUT} = 7V

Maximum duty cycle (D_{MAX}) = 47% (per datasheet), use 45% for margin.

The required transformer turns ratio is given by:

$$\text{Turns ratio (Ns/Np)} = V_{OUT}/(V_{IN(MIN)} \bullet 2 \bullet D_{(MAX)})$$

$$= 7V/(30V \bullet 2 \bullet 0.45)$$

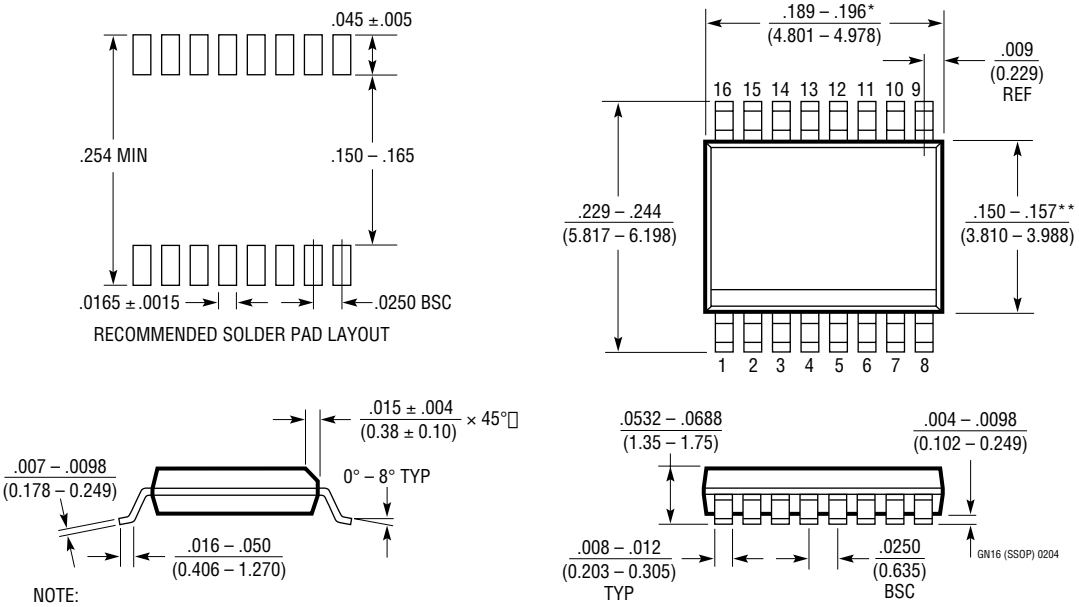
$$Ns/Np = (1/3.86)$$

Note that this is a simplified equation that does not take into account primary and secondary side voltage drops due to diodes, power MOSFETs, and resistive elements in the power paths. By margining down $V_{IN(MIN)}$ and D_{MAX} as suggested above, the equation becomes closer to reality.

An alternative secondary winding configuration uses a single non-center tapped winding and two filter inductors. Each end of the secondary winding alternately drives an inductor with <50% duty cycle square wave. The two inductors are connected together at the opposite ends to common output filter capacitor(s). This configuration is also called the current doubler rectifier. The current doubler utilizes half of the secondary windings compared to the center tapped case. The two out of phase inductors reduce the ripple current seen by the output and input capacitors, possibly allowing fewer capacitors in some applications. In addition, each output inductor carries half of the total load current, making them physically smaller, which can help to optimize the power stage layout. However, the total combined size may be slightly larger than the single inductor configuration.

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



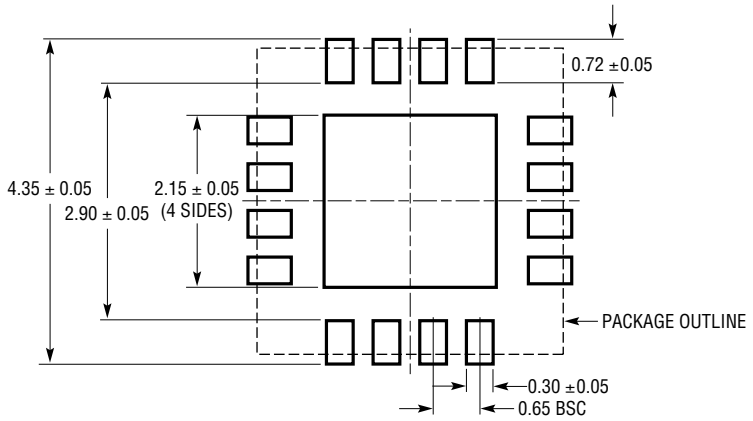
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

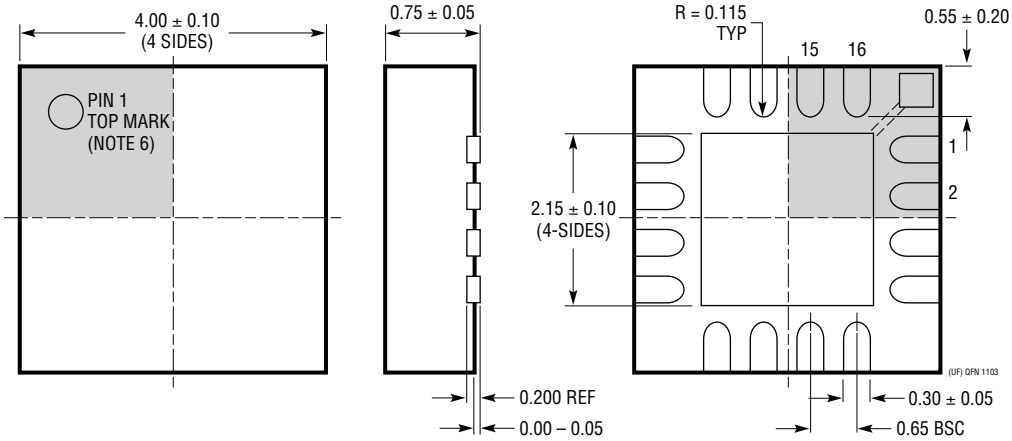
PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



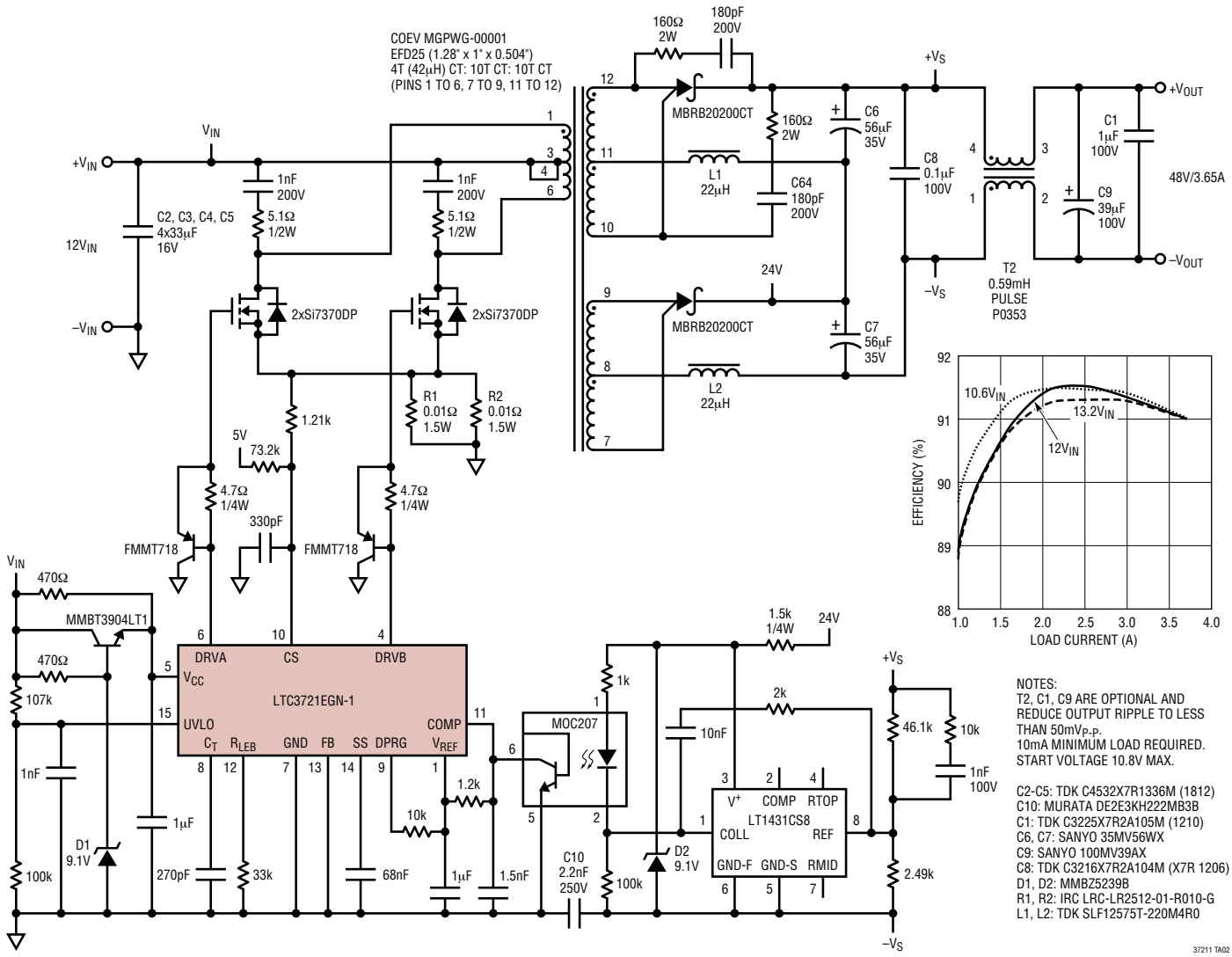
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION



NOTES:
T2, C1, C9 ARE OPTIONAL AND REDUCE OUTPUT RIPPLE TO LESS THAN 50mVP-P.
10mA MINIMUM LOAD REQUIRED.
START VOLTAGE 10.8V MAX.

C2-C5: TDK C4532X7R1336M (1812)
C10: MURATA DE2E3KH222MB3B
C1: TDK C3225X7R2A105M (1210)
C6, C7: SANYO 35MV56WX
C9: SANYO 100MV39AX
C8: TDK C3216X7R2A104M (X7R 1206)
D1, D2: MMBZ5239B
R1, R2: IRC LRC-LR2512-01-R010-G
L1, L2: TDK SLF12575T-220M4R0

37211 TA02

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1431	Reference and Opto-Driver	Drives Opto-Coupler
LT1681/LT3781	Synchronous Forward Controllers	High Efficiency 2-Switch Forward Control
LTC1693-1	Dual MOSFET Gate Drivers	High Speed MOSFET Gate Drivers
LT1950	Single Switch Forward Converter Controller	Auxillary Boost Converter, Programmable Volt-SPC Clamp
LTC3722-1/LTC3722-2	Dual Mode Phase Modulated Full-Bridge Controllers	ZVS Full-Bridge Controllers
LT3804	Secondary Side Dual Output Controller with Opto Driver	Regulates Two Secondary Outputs; Optocoupler Feedback Driver and Second Output Synchronous Driver Controller
LTC3901	Secondary Side Synchronous Driver for Push-Pull and Full Bridge Converters	Fault Timer, Reverse Current Sense, SO8
LTC3723-1/LTC3723-2	Synchronous Push-Pull Controllers	Highest Efficiency Push-Pull Controllers
LTC4440	100V High Side MOSFET Driver	SOT-23 and MSOP; 1.6Ω Pull-Down, 2.4A Pull-Up

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