Pin-Selectable, 2-Channel, 2-Wire Multiplexer with Bus Buffers

FEATURES

- **1:2 Multiplexer/Switch for 2-Wire Bus**
- **Bidirectional Buffer for SDA and SCL Lines**
- **High Noise Margin with $V_{IL} = 0.3 \bullet V_{CC}$**
- **ENABLE Pins Connect SDA and SCL Lines**
- **Selectable Rise Time Accelerator Current and Activation Voltage**
- Level Shift 1.5V, 1.8V, 2.5V, 3.3V and 5V Busses
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- Stuck Bus Disconnect and Recovery
- Compatible with I^2C, I^2C Fast Mode and SMBus
- ±4kV Human Body Model (HBM) ESD Ruggedness
- 14-Lead 4mm × 3mm DFN and 16-Lead MSOP Packages

APPLICATIONS

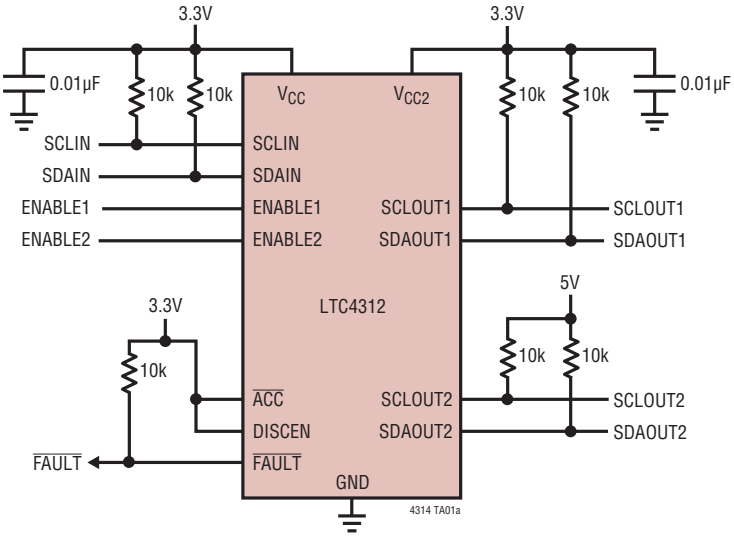
- Telecommunications Systems Including ATCA
- Address Expansion
- Level Translator
- Capacitance Buffers/Bus Extender
- Live Board Insertion
- PMBus

DESCRIPTION

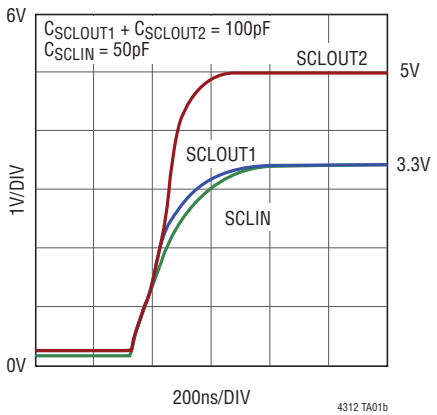
The LTC®4312 is a hot-swappable 2-channel 2-wire bus multiplexer that allows one upstream bus to connect to any combination of downstream busses or channels. An individual enable pin controls each connection. The LTC4312 provides bidirectional buffering, keeping the upstream bus capacitance isolated from the downstream bus capacitances. The high noise margin allows the LTC4312 to be interoperable with I^2C devices that drive a high V_{OL} (> 0.4V). The LTC4312 supports level translation between 1.5V, 1.8V, 2.5V, 3.3V and 5V busses. The hot-swappable nature of the LTC4312 allows I/O card insertion into, and removal from, a live backplane without corruption of the data and clock busses.

If both data and clock are not simultaneously high at least once in 45ms and DISCEN is high, a $\overline{\text{FAULT}}$ signal is generated indicating a stuck bus low condition, the input is disconnected from each enabled output channel and up to 16 clocks are generated on the enabled downstream busses. A three state $\overline{\text{ACC}}$ pin enables input and output side rise time accelerators of varying strengths and sets the $V_{IL,RISING}$ voltage.

TYPICAL APPLICATION



Rising Edge from Asserted Low with Level Translation



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage
- V_{CC}, V_{CC2} ..... –0.3V to 6V

Input Voltages
- $\overline{ACC}$, DISCEN, ENABLE1-2 ..... –0.3V to 6V

Input/Output Voltages
- SDAIN, SCLIN, SCLOUT1-2, SDAOUT1-2, $\overline{FAULT}$ ..... –0.3V to 6V

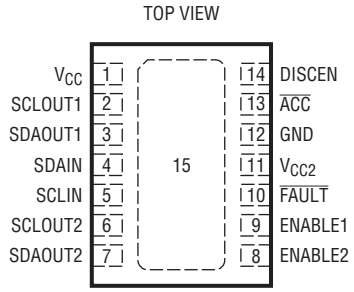
Output DC Sink Currents
- $\overline{FAULT}$ 50mA

Operating Ambient Temperature Range
- LTC4312C ..... 0°C to 70°C
- LTC4312I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

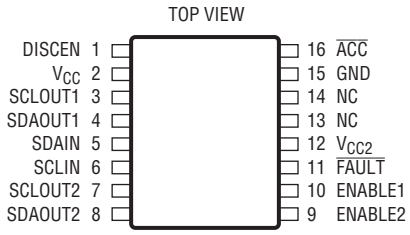
Lead Temperature (Soldering, 10 sec)
- MSOP ..... 300°C

PIN CONFIGURATION



DE14 PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN #15) PCB CONNECTION TO GND IS OPTIONAL



MS PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 120°C/W, θ_{JC} = 21°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4312IDE#PBF	LTC4312IDE#TRPBF	4312	14-Lead (4mm × 3mm) DFN	–40°C to 85°C
LTC4312IMS#PBF	LTC4312IMS#TRPBF	4312	16-Lead Plastic MSOP	–40°C to 85°C
LTC4312CDE#PBF	LTC4312CDE#TRPBF	4312	14-Lead (4mm × 3mm) DFN	0°C to 70°C
LTC4312CMS#PBF	LTC4312CMS#TRPBF	4312	16-Lead Plastic MSOP	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{CC2} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply/Start-Up							
V_{CC}	Input Supply Range		●	2.9		5.5	V
$V_{DD, BUS}$	2-Wire Bus Supply Voltage		●	2.25		5.5	V
V_{CC2}	Output Side Accelerator Supply Range		●	2.25		5.5	V
I_{CC}	Input Supply Current	One or Both $V_{ENABLE1-2}$ = V_{CC} = V_{CC2} = 5.5V (Note 3)	●	6.0	7.3	9	mA
$I_{CC(DISABLED)}$	Input Supply Current	$V_{ENABLE1-2}$ = 0V; V_{CC} = V_{CC2} = 5.5V (Note 3)	●	1.6	2.2	3.5	mA
I_{CC2}	V_{CC2} Supply Current	One or Both $V_{ENABLE1-2}$ = V_{CC} = V_{CC2} = 5.5V (Note 3)	●	0.35	0.5	0.6	mA
t_{UVLO}	UVLO Delay		●	60	110	200	µs
V_{TH_UVLO}	UVLO Threshold		●		2.3	2.6	V
$V_{CC\_UVLO(HYST)}$	UVLO Threshold Hysteresis Voltage				200		mV
Buffers							
$V_{OS1(SAT)}$	Buffer Offset Voltage	I_{OL} = 4mA, Driven $V_{SDAIN,SCLIN}$ = 50mV	●	130	220	280	mV
		I_{OL} = 500µA, Driven $V_{SDAIN,SCLIN}$ = 50mV	●	15	60	120	mV
$V_{OS2(SAT)}$	Buffer Offset Voltage	I_{OL} = 4mA, Driven $V_{SDAOUT,SCLOUT}$ = 50mV	●	90	190	260	mV
		I_{OL} = 500µA, Driven $V_{SDAOUT,SCLOUT}$ = 50mV	●	15	55	110	mV
V_{OS}	Buffer Offset Voltage	I_{OL} = 4mA, Driven $V_{SDAIN,SCLIN}$ = 200mV	●	50	130	195	mV
		I_{OL} = 500µA, Driven $V_{SDAIN,SCLIN}$ = 200mV	●	15	55	110	mV
V_{OS2}	Buffer Offset Voltage	I_{OL} = 4mA, Driven $V_{SDAOUT,SCLOUT}$ = 200mV	●	35	95	170	mV
		I_{OL} = 500µA, Driven $V_{SDAOUT,SCLOUT}$ = 200mV	●	15	50	100	mV
$V_{IL,FALLING}$	Buffer Input Logic Low Voltage	SDA, SCL Pins (Notes 4, 5)	●	0.3•V_{MIN}	0.33•V_{MIN}	0.36•V_{MIN}	V
$V_{IL,RISING}$	Buffer Input Logic Low Voltage	SDA, SCL Pins; $\overline{ACC}$ Grounded	●	0.5	0.6	0.7	V
		SDA, SCL Pins; $\overline{ACC}$ Open or High (Notes 4, 5)	●	0.3•V_{MIN}	0.33•V_{MIN}	0.36•V_{MIN}	V
I_{LEAK}	Input Leakage Current	SDA, SCL Pins; V_{CC}, V_{CC2} = 0V, 5.5V	●			±10	µA
C_{IN}	Input Capacitance	SDA, SCL Pins (Note 6)				<20	pF
Rise Time Accelerators							
dV/dt (RTA)	Minimum Slew Rate Requirement	SDA, SCL Pins; V_{CC} = V_{CC2} = 5V	●	0.1	0.2	0.4	V/µs
$V_{RTA(TH)}$	Rise Time Accelerator DC Threshold Voltage	SDA, SCL Pins; V_{CC} = V_{CC2} = 5V, $\overline{ACC}$ Grounded	●	0.7	0.8	0.9	V
		$\overline{ACC}$ Open or High, V_{CC} = V_{CC2} = 5V (Note 4)	●	0.36•V_{MIN}	0.4•V_{MIN}	0.44•V_{MIN}	V
$\Delta V_{\overline{ACC}}$	Buffers Off to Accelerator On Voltage	SDA, SCL Pins; V_{CC} = V_{CC2} = 5V, $\overline{ACC}$ Grounded	●	100	200		mV
		$\overline{ACC}$ Open, V_{CC} = V_{CC2} = 5V (Note 4)	●	0.05•V_{MIN}	0.07•V_{MIN}		mV
I_{RTA}	Rise Time Accelerator Pull-Up Current	SDA, SCL Pins; V_{CC} = V_{CC2} = 5V, $\overline{ACC}$ Grounded (Note 7)	●	20	35	45	mA
		$\overline{ACC}$ Open, V_{CC} = V_{CC2} = 5V (Note 7)	●	1.5	3	4	mA
Enable/Control							
$V_{DISCEN(TH)}$	DISCEN Threshold Voltage		●	0.8	1.4	2	V
$\Delta V_{DISCEN(HYST)}$	DISCEN Hysteresis Voltage				20		mV
$V_{EN(TH)}$	ENABLE1-2 Threshold Voltage		●	0.8	1.4	2	V
$\Delta V_{EN(HYST)}$	ENABLE1-2 Hysteresis Voltage				20		mV
t_{LH_EN}	ENABLE1-2 High to Buffer Active				0.56	1	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{CC2} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LEAK}	Input Leakage Current	DISCEN = ENABLE1-2 = 5.5V	●		0.1	±10	µA
$I_{\overline{ACC}(IN, HL)}$	$\overline{ACC}$ High, Low Input Current	V_{CC} = 5V, $V_{\overline{ACC}}$ = 5V, 0V	●		±23	±40	µA
$I_{\overline{ACC}(IN, Z)}$	Allowable Leakage Current in Open State	V_{CC} = 5V	●			±5	µA
$I_{\overline{ACC}(EN, Z)}$	$\overline{ACC}$ High Z Input Current	V_{CC} = 5V	●	±5			µA
$V_{\overline{ACC}(L, TH)}$	$\overline{ACC}$ Input Low Threshold Voltages	V_{CC} = 5V	●	0.2•V_{CC}	0.3•V_{CC}	0.4•V_{CC}	V
$V_{\overline{ACC}(H,TH)}$	$\overline{ACC}$ Input High Threshold Voltages	V_{CC} = 5V	●	0.7•V_{CC}	0.8•V_{CC}	0.9•V_{CC}	V
Stuck Low Timeout Circuitry							
$t_{TIMEOUT}$	Bus Stuck Low Timer	SDAOUT or SCLOUT < 0.3•V_{CC}	●	35	45	55	ms
$V_{\overline{FAULT}(OL)}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 3mA	●			0.4	V
$I_{\overline{FAULT}(OH)}$	$\overline{FAULT}$ Leakage Current		●		0.1	±5	µA
I^2C Interface Timing							
$f_{SCL(MAX)}$	I^2C Frequency Max	(Note 6)	●	400			kHz
t_{PDHL}	SDA, SCL Fall Delay	V_{CC} = 3V to 5.5V, C_{BUS} = 50pF, I_{BUS} = 1mA (Note 6)			60	100	ns
t_f	SDA, SCL Fall Times	V_{CC} = 3V to 5.5V, C_{BUS} = 50pF, I_{BUS} = 1mA (Note 6)			10		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive and all voltages are referenced to GND unless otherwise indicated.

Note 3: SDAIN, SCLIN pulled low.

Note 4: V_{MIN} = minimum of V_{CC} and V_{CC2} if V_{CC2} > 2.25V else V_{MIN} = V_{CC}.

Note 5: V_{IL} is tested for the following (V_{CC}, V_{CC2}) combinations: (2.9V, 5.5V), (5.5V, 2.25V), (3.3V, 3.3V) and (5V, 0V).

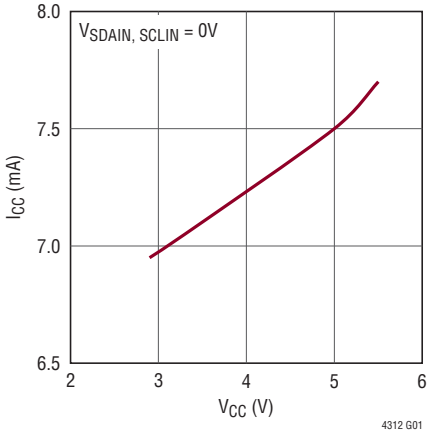
Note 6: Guaranteed by design and not tested.

Note 7: Measured in a special DC mode with $V_{SDA,SCL}$ = $V_{RTA(TH)}$ + 1V. The transient I_{RTA} seen during rising edges when $\overline{ACC}$ is low will depend on the bus loading condition and the slew rate of the bus. The LTC4312's internal slew rate control circuitry limits the maximum bus rise rate to 75V/µs by controlling the transient I_{RTA}.

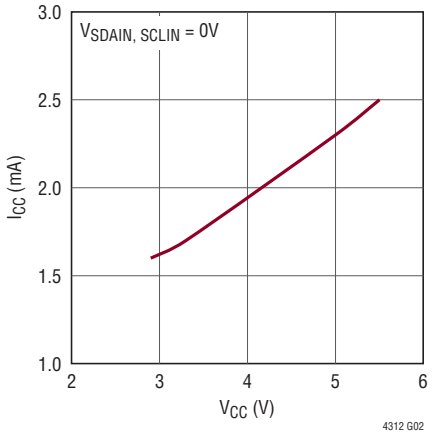
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

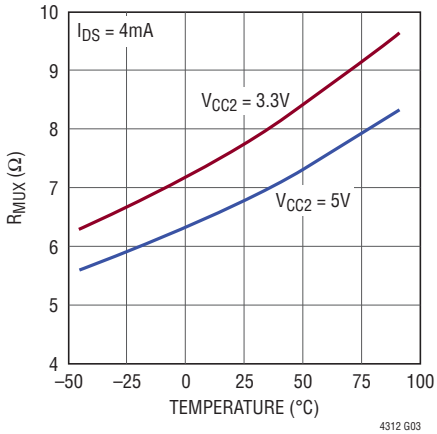
I_{CC} Enabled Current vs Supply Voltage



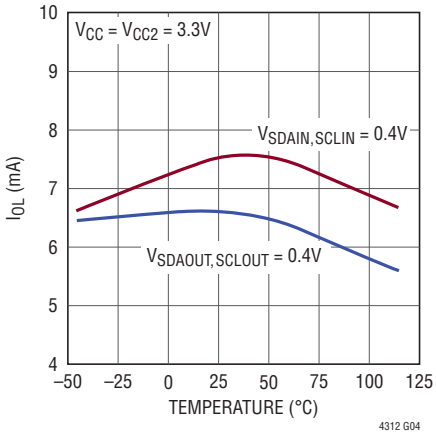
I_{CC} Disabled (ENABLE1-2 Low) Current vs Supply Voltage



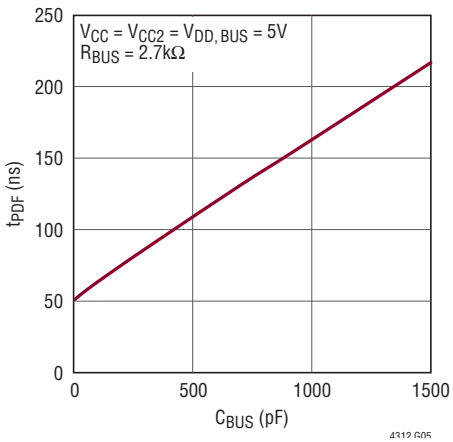
Multiplexer Switch Resistance R_{MUX} vs Temperature



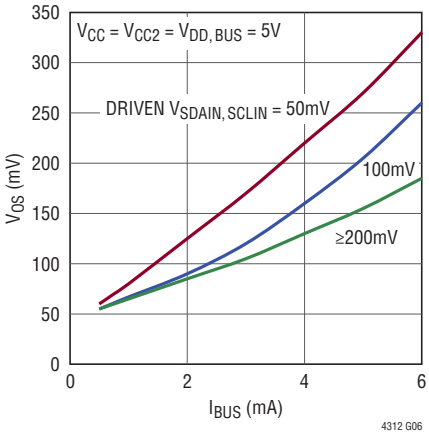
Buffer DC I_{OL} vs Temperature



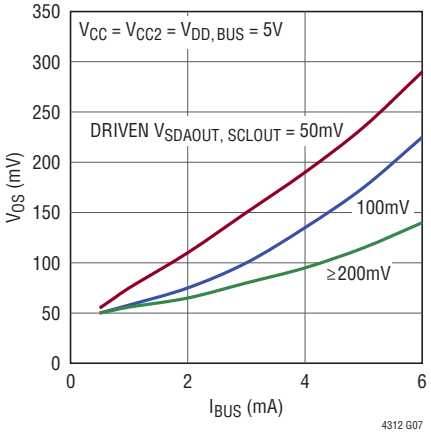
Buffer High to Low Propagation Delay vs Output Capacitance



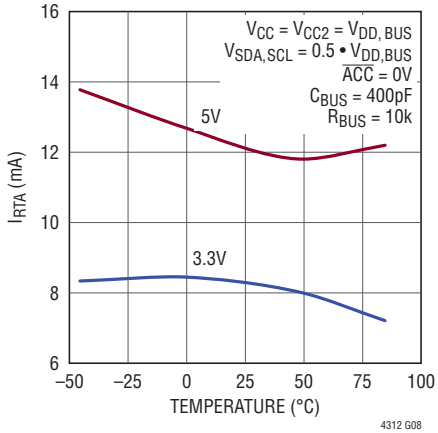
Input to Output Offset Voltage vs Bus Current for Different Driven Input Voltage Levels



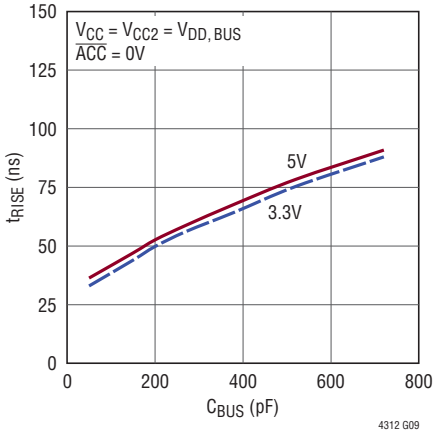
Output to Input Offset Voltage vs Bus Current for Different Driven Output Voltage Levels



Rise Time Accelerator Current vs Temperature



$t_{RISE(30\%–70\%)}$ vs C_{BUS}



PIN FUNCTIONS

$\overline{\text{ACC}}$: Three-State Acceleration and Buffer Mode Selector. This pin controls the turn on voltage of the rise time accelerators and their current strength on both the input and output sides. It also controls the turn-off voltage of the buffers. See Table 1 in the Applications Information section.

DISCEN: Disconnect Stuck Bus Enable Input. When this pin is high, stuck busses are automatically disconnected and $\overline{\text{FAULT}}$ is pulled low after a timeout period of 45ms. Up to sixteen clock pulses are subsequently applied to the stuck output channels. When DISCEN pin is low, stuck busses are neither disconnected nor clocked but $\overline{\text{FAULT}}$ is pulled low. Connect to GND if unused.

ENABLE1-ENABLE2: Connection Enable Inputs. These input pins enable or disable the corresponding output channel. Driving an ENABLE pin low isolates SDAIN and SCLIN from the corresponding SDAOUT and SCLOUT. Only enable and disable a channel when all busses are idle. During a bus stuck low fault condition, a falling edge on all ENABLE pins followed by a rising edge on one or more ENABLE pins forces a connection from SDAIN to the selected SDAOUT and SCLIN to the selected SCLOUT. Connect to GND if unused.

Exposed Pad (DFN Package Only): Exposed pad may be left open or connected to device ground.

$\overline{\text{FAULT}}$: Stuck Bus Fault Output. This open drain N-channel MOSFET output pulls low if a simultaneous high on the enabled SCLOUT and SDAOUT channels does not occur in 45ms. In normal operation $\overline{\text{FAULT}}$ is high. Connect a pull up resistor, typically 10k, from this pin to the bus pull-up supply. Leave open or tie to GND if unused.

GND: Device Ground.

SCLIN: Upstream Serial Bus Clock Input/Output. Connect this pin to the SCL line on the upstream bus. Connect an external pull-up resistor or current source between this pin and the bus supply. Do not leave open.

SCLOUT1-SCLOUT2: Downstream Serial Bus Clock Input/Output Channels 1-2. Connect pins SCLOUT1-SCLOUT2 to the SCL lines on the downstream channels 1-2, respectively. When in use, an external pull-up resistor or current source is required between the pin and the corresponding bus supply. Leave open or tie to GND and connect the corresponding ENABLE pin to GND, if unused.

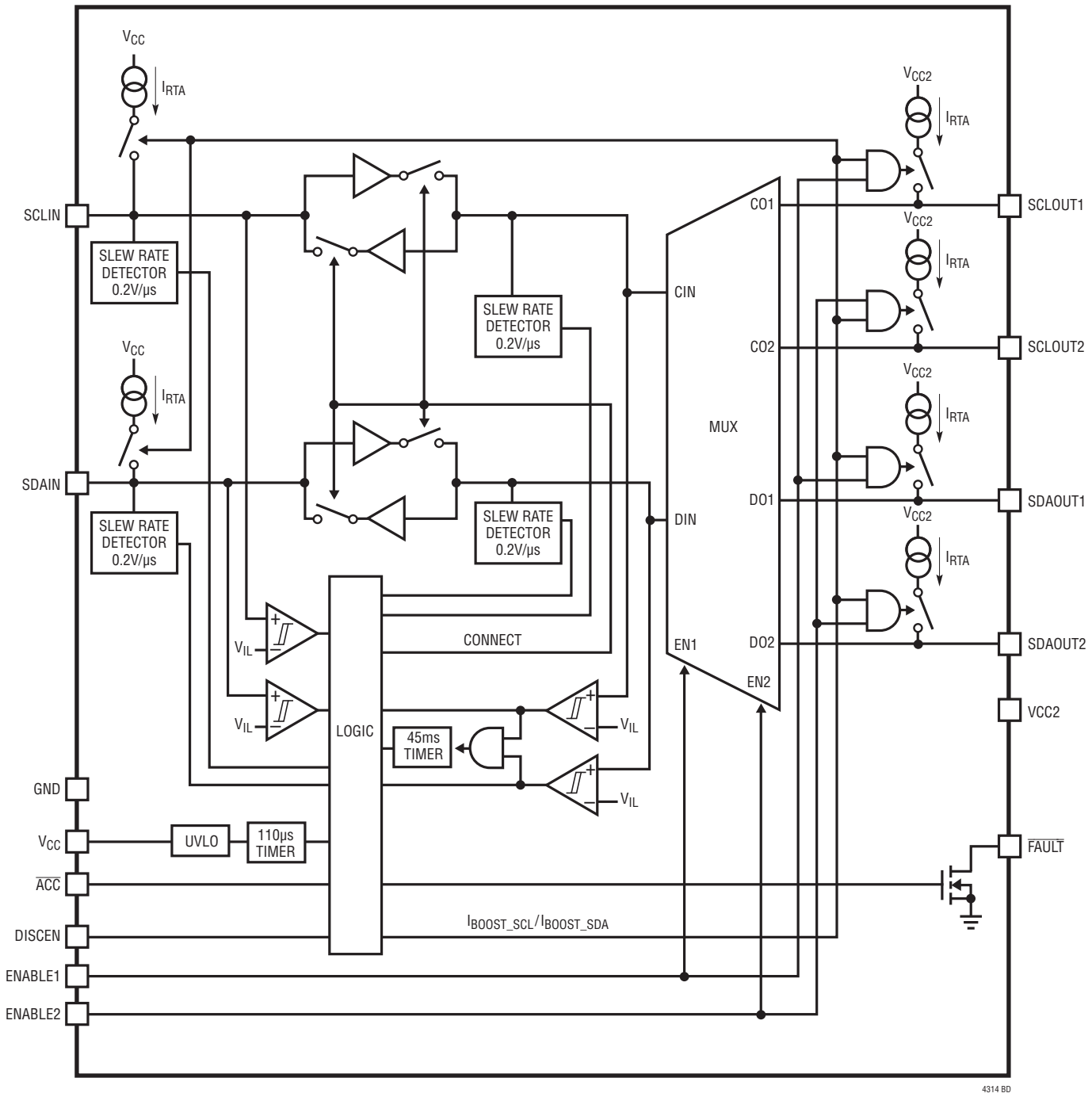
SDAIN: Upstream Serial Bus Data Input/Output. Connect this pin to the SDA line on the upstream bus. Connect an external pull-up resistor or current source between this pin and the bus supply. Do not leave open.

SDAOUT1-SDAOUT2: Downstream Serial Bus Data Input/Output Channels 1-2. Connect pins SDAOUT1-SDAOUT2 to the SDA lines on downstream channels 1-2, respectively. When in use, an external pull-up resistor or current source is required between the pin and the corresponding bus supply. Leave open or tie to GND and connect the corresponding ENABLE pin to GND, if unused.

V_{CC}: Power Supply Voltage. Power this pin from a supply between 2.9V and 5.5V. Bypass with at least 0.01µF to GND.

V_{CC2}: Output Side Rise Time Accelerator (RTA) Power Supply Voltage. When powering V_{CC2}, use a supply voltage ranging from 2.25V to 5.5V and bypass with at least 0.01µF to GND. If the downstream busses are powered from multiple supply voltages, power V_{CC2} from the lowest supply voltage. Output side RTAs are active if $V_{CC2} \geq$ 2.25V and $\overline{\text{ACC}}$ is low or open. Grounding V_{CC2} disables output side RTAs.

BLOCK DIAGRAM



OPERATION

The Block Diagram shows the major functional blocks of the LTC4312. The LTC4312 is a 1:2 multiplexer with capacitance buffering for I²C signals. Capacitance buffering is achieved by use of back to back buffers on the clock and data channels which isolate the SDAIN and SCLIN capacitances from the SDAOUT and SCLOUT capacitances respectively. All SDA and SCL pins are fully bidirectional. The high noise margin allows the LTC4312 to operate with I²C devices that drive a non-compliant high V_{OL}. Multiplexing is done using N-channel MOSFETs that are controlled by dedicated ENABLE pins. When enabled, rise time accelerator pull-up currents I_{RTA} turn on during rising edges to reduce system rise time. In a typical application the input side bus is pulled up to V_{CC} and the output side busses are pulled up to V_{CC2} although these are not requirements. V_{CC} is the primary power supply to the LTC4312. V_{CC} and V_{CC2} serve as the input and output side rise time accelerator supplies respectively. Grounding V_{CC2} disables the output side accelerators. The multiplexer N-channel MOSFET gates of the enabled channels are driven to V_{CC2} if V_{CC2} is > 1.8V, otherwise they are driven to V_{CC}.

When the LTC4312 first receives power on its V_{CC} pin, it starts out in an undervoltage lockout mode (UVLO) until 110µs after V_{CC} exceeds 2.3V. During this time, the buffers and rise time accelerators are disabled, the multiplexer gates are off and the LTC4312 ignores transitions on the clock and data pins independent of the state of the ENABLE pins. V_{CC2} transitions from a high to a low or vice-versa across a 1.8V threshold also cause the LTC4312 to disable the buffers, rise time accelerators and transmission gates and to ignore the clock and data pins until 110µs after that transition. Assuming that the LTC4312 is not in UVLO mode, when one or both ENABLEs are asserted, the LTC4312 activates the connection circuitry between the SDAIN/SCLIN inputs and selected output channels. The input rise time accelerators and the output rise time accelerators of the selected channels are also enabled at this time. When a SDA/SCL input pin or output pin on an enabled output channel is driven below the $V_{IL,FALLING}$ level of $0.33 \bullet V_{MIN}$, the buffers are turned on and the logic low level is propagated though the LTC4312 to the other side. For V_{CC2} > 1.8V, V_{MIN} is the lower of the V_{CC} and V_{CC2} voltages. For V_{CC2} < 1.8V, V_{MIN} is the V_{CC} voltage. The LTC4312 is designed to sink a minimum total bus current I_{OL} of 4mA while holding a V_{OL} of 0.4V. If multiple output channels are enabled, the bus current of all enabled channels needs to be summed to get the total bus current. See the Typical Performance Characteristics curves for I_{OL} as a function of temperature.

A high occurs when all devices on the input and output sides release high. Once the bus voltages rise above the $V_{IL,RISING}$ level, which is determined by the state of the $\overline{ACC}$ pin, the buffers are turned off. The rise time accelerators are turned on at a slightly higher voltage. The rise time accelerators accelerate the rising edges of the SDA/SCL inputs and selected outputs up to voltages of $0.9 \bullet V_{CC}$ and $0.8 \bullet V_{CC2}$ respectively, provided that the busses on their own are rising at a minimum rate of 0.2V/µs as determined by the slew rate detectors. $\overline{ACC}$ is a 3-state input that controls $V_{IL,RISING}$, the rise time accelerator turn-on voltage and the rise time accelerator pull-up strength.

The LTC4312 detects a bus stuck low (fault) condition when both clock and data busses are not simultaneously high at least once in 45ms. The voltage monitoring for a stuck low condition is done on the common internal node of the clock and data outputs. Hence a stuck low condition is detected only if it occurs on an enabled output channel. When a stuck bus occurs, the LTC4312 asserts the $\overline{FAULT}$ flag. If DISCEN is tied high, the LTC4312 also disconnects the input and output sides. After waiting at least 40µs, it generates up to sixteen 5.5kHz clock pulses on the enabled SCLOUT pins and a stop bit to attempt to free the stuck bus. If the bus recovers high before 16 clocks are issued, the LTC4312 ceases issuing clocks and generates a stop bit. If DISCEN is tied low, a stuck bus event only causes $\overline{FAULT}$ flag assertion. Disconnection of the input and output sides and clock generation do not occur. Once the stuck bus recovers and the fault has been cleared, in order for a connection to be established between the input and output sides, both ENABLE pins need to be driven low followed by the assertion high of the desired ENABLE pins. When powering into a stuck low condition, the LTC4312 upon exiting UVLO will connect the input and output sides for 45ms until a stuck bus timeout event is detected.

APPLICATIONS INFORMATION

The LTC4312 is a 1:2 pin selectable I²C multiplexer that provides a high noise margin, capacitance buffering and level translation capability on its clock and data pins. Rise time accelerators accelerate rising edges to enable operation at high frequencies with heavy loads. These features are illustrated in the following subsections.

Rise Time Accelerators and DC Hold-Off Voltage

Once the LTC4312 has exited UVLO and a connection has been established between the SDA and SCL inputs and outputs, the rise time accelerators on both the input and output sides of the SDA and SCL busses are activated based on the state of the $\overline{ACC}$ pin and the V_{CC2} supply voltage. During positive bus transitions of at least 0.2V/µs, the rise time accelerators provide pull-up currents to reduce rise time. Enabling the rise time accelerators allows users to choose larger bus pull-up resistors, reducing power consumption and improving logic low noise margins, to design with bus capacitances outside of the I²C specification or to switch at a higher clock frequency. The $\overline{ACC}$ pin sets the turn-off threshold voltage for the buffers, the turn-on voltage for the rise time accelerators, and the rise time accelerator pull-up current strength. The $\overline{ACC}$ functionality is shown in Table 1. Set $\overline{ACC}$ open or high when a high noise margin is required such as when the LTC4312 is used in a system having I²C devices with V_{OL} > 0.4V.

Table 1. $\overline{ACC}$ Control of the Rise Time Accelerator Current I_{RTA} and Buffer Turn-Off Voltage $V_{IL,RISING}$

$\overline{ACC}$	I_{RTA}	$V_{RTA(TH)}$	$V_{IL,RISING}$
Low	Strong	0.8V	0.6V
Open	3mA	0.4•V_{MIN}	0.33•V_{MIN}
High	None	N/A	0.33•V_{MIN}

The $\overline{ACC}$ pin has a resistive divider between V_{CC} and GND to set its voltage to 0.5•V_{CC} if left open. In the current source accelerator mode, the LTC4312 provides a 3mA constant current source pull-up. In the strong mode, the LTC4312 sources pull-up current to make the bus rise at 75V/µs (typical). The strong mode current is therefore directly proportional to the bus capacitance. The LTC4312 is capable of sourcing up to 45mA of current in the strong mode. The effect of the rise time accelerator strength is shown in the SDA waveforms in Figures 1 and 2 for identical bus loads for a single enabled output channel. The rise time accelerator supplies 3mA and 10mA of pull-up current (I_{RTA}) respectively in the current source and strong modes for the bus conditions shown in Figures 1 and 2. The rise time accelerator turn-on voltage in the strong mode is also lower as compared to the current source mode. For identical bus loading conditions, the bus returns high faster in Figure 1 compared to Figure 2 because of both the higher I_{RTA} and the lower turn-on voltage of the rise time accelerator. In each figure, note that the input and output rising waveforms are nearly coincident due to the input and output busses having nearly identical bus current and capacitance.

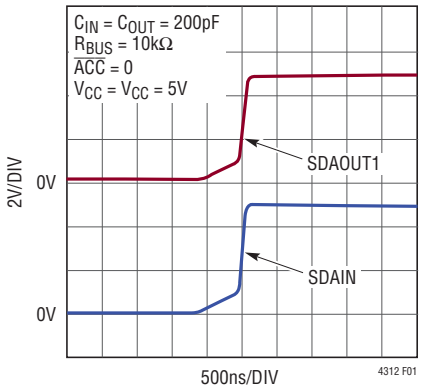


Figure 1. Bus Rising Edge for the Strong Accelerator Mode

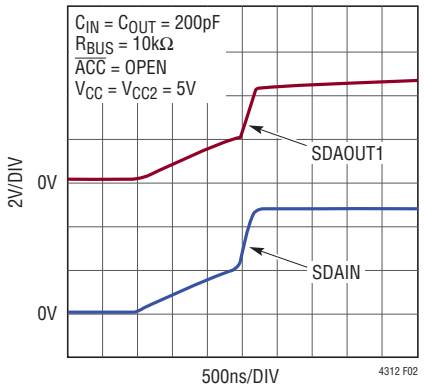


Figure 2. Bus Rising Edge for the Current Source Accelerator Mode

APPLICATIONS INFORMATION

If V_{CC2} is tied low, the output side rise time accelerators are disabled independent of the state of the $\overline{ACC}$ pin. $\overline{ACC}$ tied high disables input and output RTAs. Using a combination of the $\overline{ACC}$ pin and the V_{CC2} voltage allows the user independent control of the input and output side rise time accelerators. The rise time accelerators are also internally disabled during power-up and V_{CC2} transitions, as described in the Operation section, as well as during automatic clocking and stop bit generation for a bus stuck low recovery event.

The rise time accelerators when activated pull the bus up to 0.9•V_{CC} on the input side of the SDA and SCL lines. On the output side the SDAOUT and SCLOUT lines are pulled up by the rise time accelerators to 0.8•V_{CC2}. For V_{CC2} voltages approaching 2.3V, acceleration of the output bus may not be seen all the way to 0.8•V_{CC2} due to the threshold voltage of the NFET pass device.

Supply Voltage Considerations in Level Translation Applications

Care must be taken to ensure that the bus supply voltages on the input and output sides are greater than 0.9•V_{CC} and 0.8•V_{CC2}, respectively, to ensure that the bus is not driven above the bus supplies by the rise time accelerators. This is usually accomplished in a level shifting application by tying V_{CC} to the input bus supply and V_{CC2} to the minimum bus supply on the output side as shown in Figure 3.

If V_{CC2} is grounded, the multiplexer pass gates are powered from V_{CC}. In this case the minimum output bus supply of the enabled channels should be greater than or equal to V_{CC} to prevent cross-conduction between the enabled output channels. This is shown in Figure 4. Grounding V_{CC2} as shown in Figure 4 disables the output side rise time accelerators independent of the state of the $\overline{ACC}$ pin. The input rise time accelerators in this configuration continue to be controlled by the $\overline{ACC}$ pin and can be enabled independently. In Figure 4, $\overline{ACC}$ is left open to obtain a high V_{IL} and a 3mA rise time accelerator current on the input side.

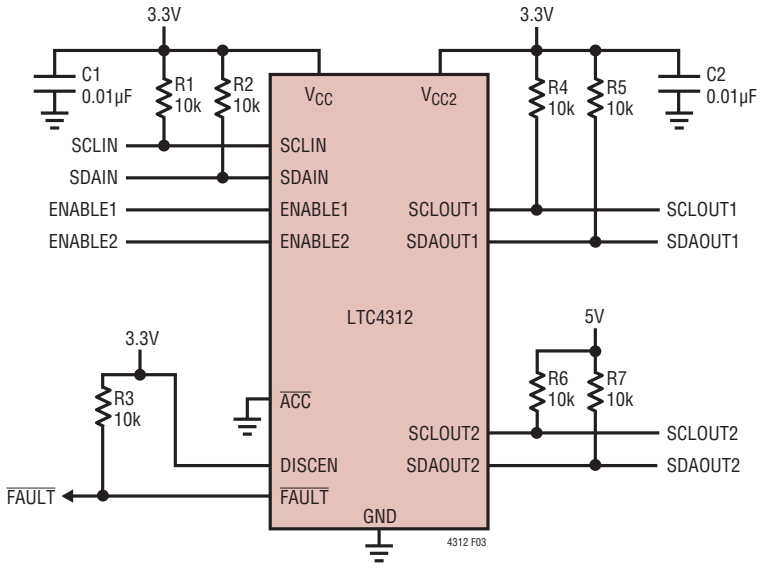


Figure 3. Connection of the LTC4312 in a Level Shift Application. V_{CC2} Is Less Than or Equal to the Minimum Bus Supply Voltage on the Output Side

APPLICATIONS INFORMATION

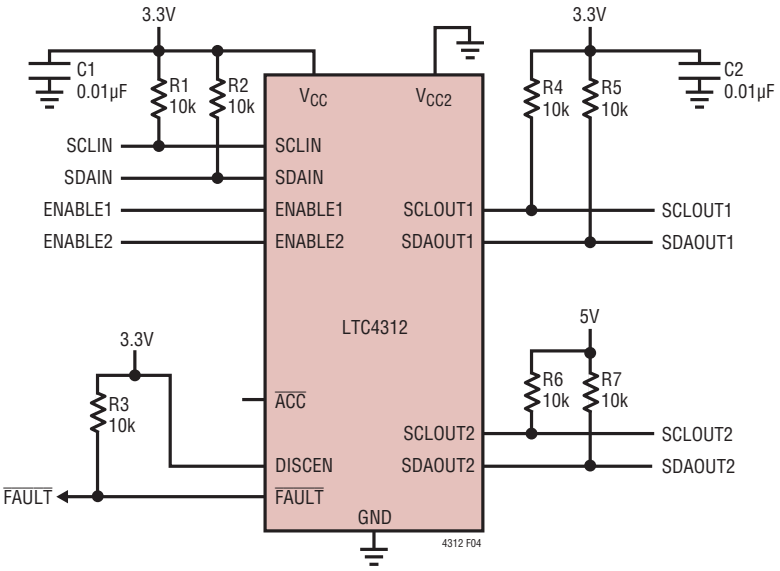


Figure 4. Connection of the LTC4312 in a Level Shift Application. V_{CC} Is Less Than or Equal to the Minimum Bus Supply Voltages on the Output Side. V_{CC2} Is Grounded to Disable Output Rise Time Accelerators

Pull-Up Resistor Value Selection

To guarantee that the rise time accelerators are activated during a rising edge, the bus must rise on its own with a positive slew rate of at least 0.4V/µs. To achieve this, choose a maximum R_{BUS} using equation 1:

$$R_{BUS}(\Omega) \leq \frac{\left(V_{DD,BUS(MIN)} - V_{RTA(TH)}\right)}{0.4\frac{V}{\mu s} \bullet C_{BUS}} \quad (1)$$

R_{BUS} is the bus pull-up resistor, $V_{DD,BUS(MIN)}$ the minimum bus pull-up supply voltage, $V_{RTA(TH)}$ the voltage at which the rise time accelerator turns on, which is a function of $\overline{ACC}$, and C_{BUS} the equivalent bus capacitance. R_{BUS} values on each output channel must also be chosen to ensure that when all the required output channels are enabled, the total bus current is ≤4mA. The bus current in each output channel can be 4mA if only one output channel is enabled at any given time. The R_{BUS} value on the input side must also be chosen to limit the bus current to be ≤4mA. The bus current for a single bus is determined by equation 2:

$$I_{BUS}(A) = \frac{V_{DD,BUS} - 0.4V}{R_{BUS}} \quad (2)$$

Input to Output Offset Voltage and Propagation Delay

The LTC4312 introduces both an offset as well as a propagation delay for falling edges between the input and output. When a logic low voltage of ≥200mV is driven on any of the LTC4312's data or clock pins, the LTC4312 regulates the voltage on the opposite side to a slightly higher value. When SCLIN or SDAIN is driven to a logic low voltage, SCLOUT or SDAOUT is driven to a slightly higher voltage as directed by equation 3 which uses SDA as an example:

$$V_{SDAOUT}(V) = V_{SDAIN} + 45mV + (10\Omega + R_{MUX}) \bullet \frac{V_{DD,BUS}}{R_{BUS}} \quad (3)$$

$V_{DD,BUS}$ is the output bus voltage, R_{BUS} the output bus pull-up resistance and R_{MUX} is the resistance of the channel transmission gate in the multiplexer shown in the block diagram. The offset is affected by the V_{CC2} voltage and bus current. A higher V_{CC2} voltage (V_{CC} if V_{CC2} is grounded) reduces R_{MUX} leading to a lower offset. See the Typical Performance Characteristics plots for the variation of R_{MUX} as a function of V_{CC2} and temperature. When SDAOUT or SCLOUT is driven to a logic low voltage ≥ 200mV, SCLIN

APPLICATIONS INFORMATION

or SDAIN is regulated to a logic low voltage as directed by equation 4 which uses SDA as an example:

$$V_{SDAIN}(V) = V_{SDAOUT} + 45mV + 10\Omega \bullet \frac{V_{DD,BUS}}{R_{BUS}} \quad (4)$$

The SCLOUT/SDAOUT to SCLIN/SDAIN offset is lower than the reverse case as the multiplexer transmission gate does not affect this offset. For driven logic low voltages <200mV, the above equations do not apply as the saturation voltage of the open collector output transistor results in a higher offset. However, the offset is guaranteed to be less than 400mV for a total bus pull-up current of 4mA under all conditions. See the Typical Performance Characteristics curves for the buffer offset voltage as a function of the driven logic low voltage and bus pull-up current.

The high-to-low propagation delay arises due to both the finite response time of the buffers and their finite current sink capability. See the Typical Performance Characteristics curves for the propagation delay as a function of the bus capacitance.

Cascading LTC4312 Devices and Other LTC Bus Buffers

Multiple LTC4312s can be cascaded or the LTC4312 may be cascaded with other LTC bus buffers as required by the application. This is shown for the data pathway in Figure 5 where an LTC4312 is cascaded with other LTC4312s and some select LTC bus buffers. The clock path is identical. When using such cascades, users should be aware of the additive logic low offset voltages (V_{OS}) when determining system noise margin. If the sum of the offsets (refer to Equations 3 and 4 and to the data sheets of the corresponding bus buffers) plus the worst-case driven logic low voltage across the cascade exceeds the buffer turn off voltage, signals will not be propagated across the cascade. Also the minimum rise time accelerator (RTA) turn-on voltage (wherever applicable) of each device in the cascade should also be greater than the maximum buffer turn-off voltage of all the devices in the cascade. This condition is required to prevent contention between one device's buffer and another's RTA. Based on this requirement,

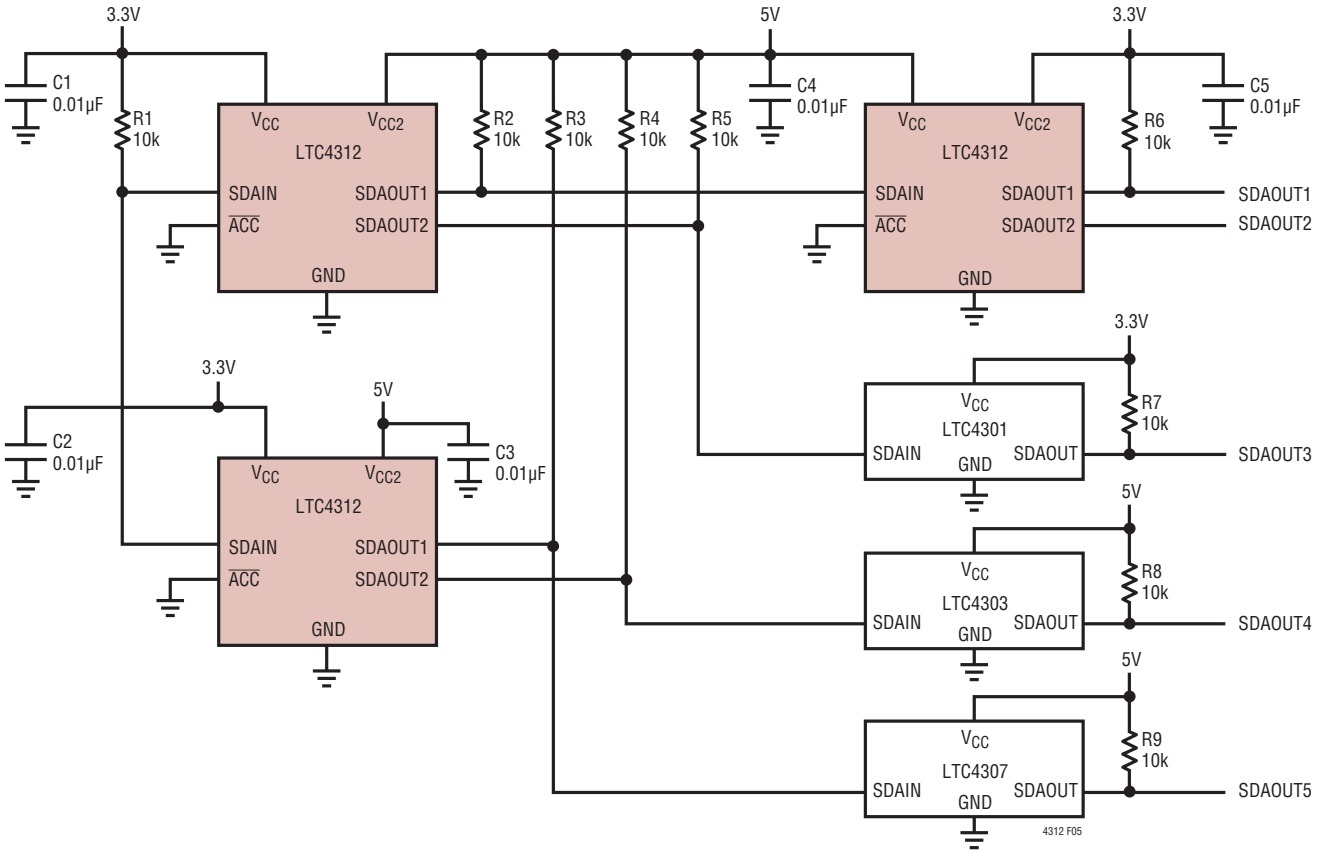


Figure 5. Cascading LTC4312s with Other LTC4312s and LTC Bus Buffers. Only the SDA Path Is Shown for Simplicity

APPLICATIONS INFORMATION

the LTC4312 can be cascaded with the LTC4303 and LTC4307 if the LTC4312's RTA turn-on voltage is set to be 0.8V ($\overline{ACC}$ low). The LTC4312 can be cascaded with the LTC4301 and LTC4301L under all $\overline{ACC}$ settings as these devices do not have RTAs. The LTC4312 can be cascaded with the LTC4302, LTC4304, LTC4305 and LTC4306 if the LTC4312's RTAs are set to turn on at 0.8V ($\overline{ACC}$ low) or under all $\overline{ACC}$ settings if the RTAs on the other bus buffers are disabled. Finally, two LTC4312s can be cascaded if their $\overline{ACC}$ pins are tied to the same state, HIGH, LOW or open or if the $\overline{ACC}$ pin of one LTC4312 is tied high and the other is left open.

Radial Telecommunications

Figure 6 shows the use of the LTC4312 in a radial telecommunications application. Two Shelf Managers are wired to communicate with slave I^2C devices for redundancy. Each Shelf Manager can have as many LTC4312s as required depending on the number of boards in the system and the desired radial/star configuration. The ENABLE pins of the LTC4312s inside only one Shelf Manager are asserted high at any time. For simplicity, in Figure 6 only the SDA pathway is shown. The SCL pathway is identical.

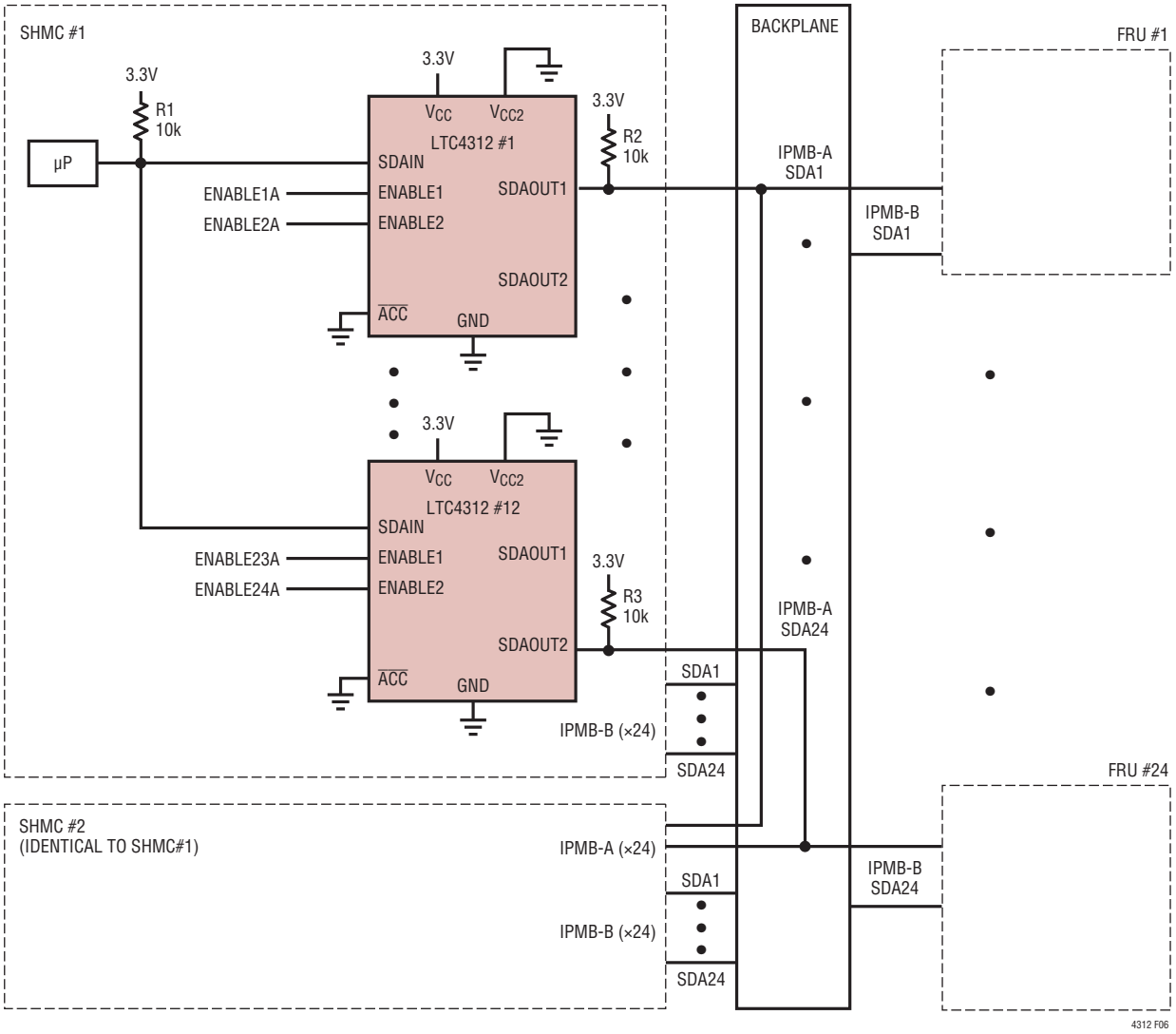


Figure 6. LTC4312s Configured for a Radially Connected Redundant Telecommunications Shelf Manager Application in a 12 × 2 Arrangement. The ENABLE Pins on Only One of the Shelf Managers Are High at Any Time. Only the SDA Path Is Shown for Simplicity

APPLICATIONS INFORMATION

Nested Addressing

The LTC4312 can provide nested addressing when its ENABLE pins are used as channel select bits. This is shown in Figure 7 where the master communicates with slave devices that have the same address by selectively enabling only one output channel at a time. Since slaves have the same address care must be taken that the master never enables both channels at the same time.

Stop Bit Generation and $\overline{\text{FAULT}}$ Clocking

If the output bus sticks low (SCLOUT or SDAOUT stuck low for at least 45ms) on one of the enabled channels and DISCEN is high, the LTC4312 attempts to unstick the bus by first breaking the connection between the input and output, asserting $\overline{\text{FAULT}}$ low and generating up to 16 clock pulses at 5.5kHz on the SCLOUT node common to the two channels. Should the stuck bus release high during this period, clock pulsing is stopped, a stop bit is generated and $\overline{\text{FAULT}}$ is cleared. In order for a connection to be established between the input and output, all ENABLEs have to be taken low followed by an assertion of the ENABLEs of the required channels.This process is illustrated in Figure 8 for the case where only channel 1 is active and SDAOUT1 starts out stuck low and then recovers. If DISCEN is tied low and a stuck low event occurs, the $\overline{\text{FAULT}}$ flag is driven low, but the connection between the input and output is not broken and clock generation is not done.

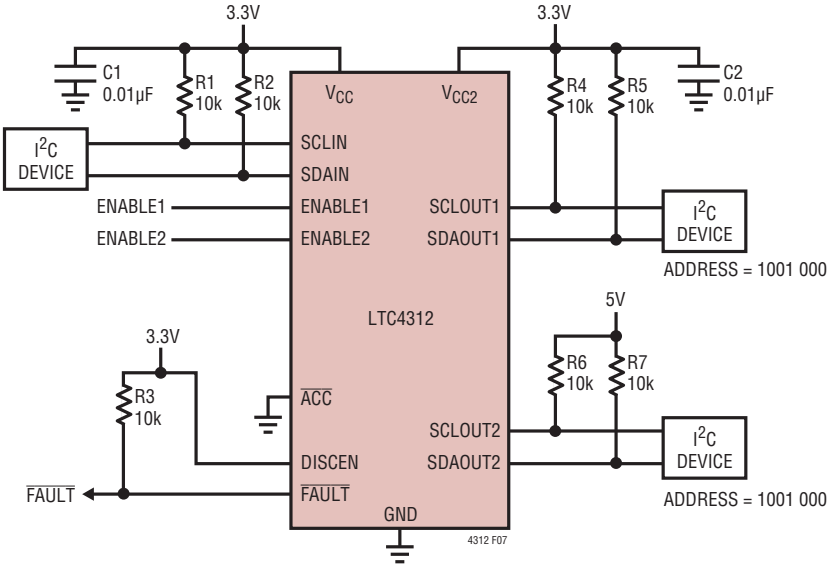


Figure 7. Nested Addressing

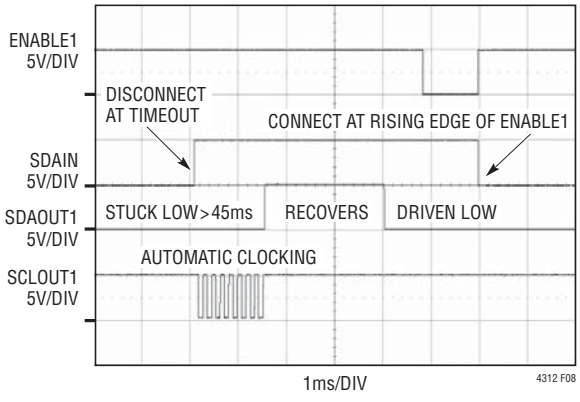


Figure 8.Bus Waveforms During a SDAOUT Stuck Low and Recovery Event

APPLICATIONS INFORMATION

Demultiplexer Function

Due to its bi-directional nature, the LTC4312 can be used as a demultiplexer. This is shown in Figure 9 where two channels are used to drive I²C data from the master side with redundancy to the slave side. In this application the SDAOUT/SCLOUT channels serve as the inputs while the SDAIN/SCLIN channel is the output. Redundancy on the master side provides protection against power supply failure. In Figure 9, if the 5V bus supply on channel 1 falls below 1.4V, channel 1 gets disabled as ENABLE1 is driven below its digital threshold. Simultaneously, the V_{BE} of the NPN pull-down device on ENABLE2 falls below 0.7V and it turns off. This causes ENABLE2 to be pulled up by R7 which in turn enables channel 2, causing control to be transferred to the backup I²C master device.

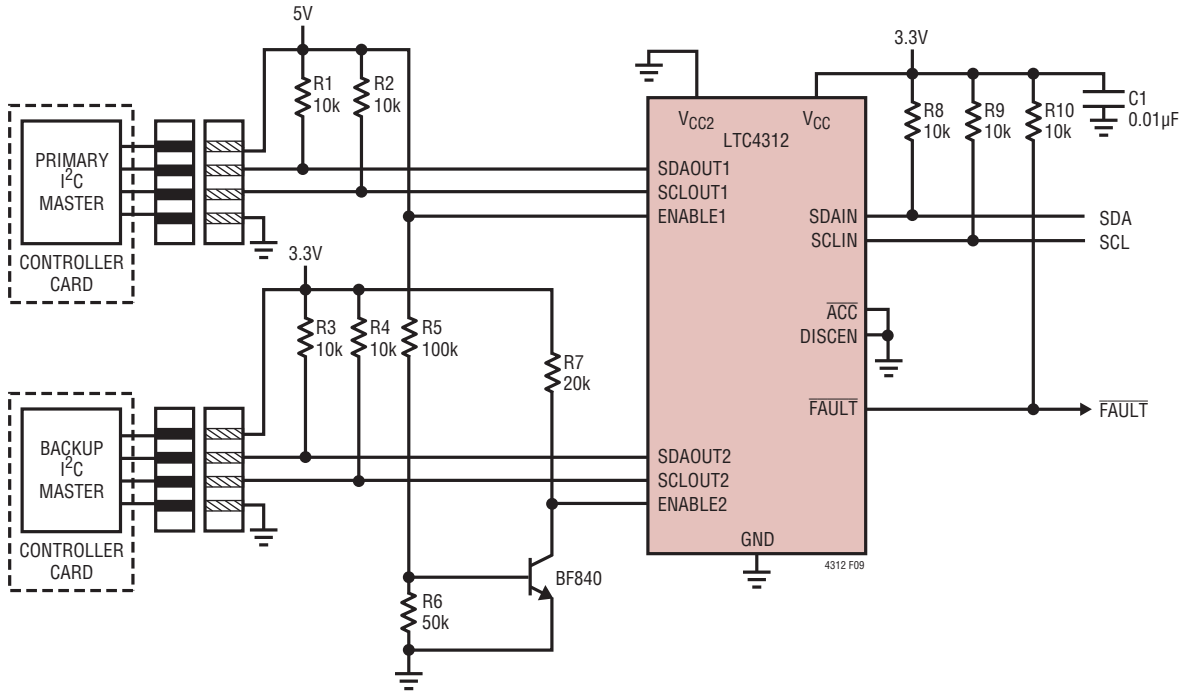


Figure 9. The LTC4312 Configured as a 2:1 Demultiplexer in a System with Redundancy

APPLICATIONS INFORMATION

Hot-Swapping

Figure 10 shows the LTC4312 in a typical hot-swapping application where the LTC4312 is on the backplane and I/O cards plug into the downstream channels. The outputs must idle high and the corresponding output channel must be disabled before an I/O card can be plugged or unplugged from an output channel. Figure 10 also shows the use of a non-compliant I^2C device with the LTC4312. The high noise margin of the LTC4312 supports logic low levels up to $0.3 \bullet V_{CC}$, allowing devices to drive greater than 0.4V logic low levels on the clock and data lines.

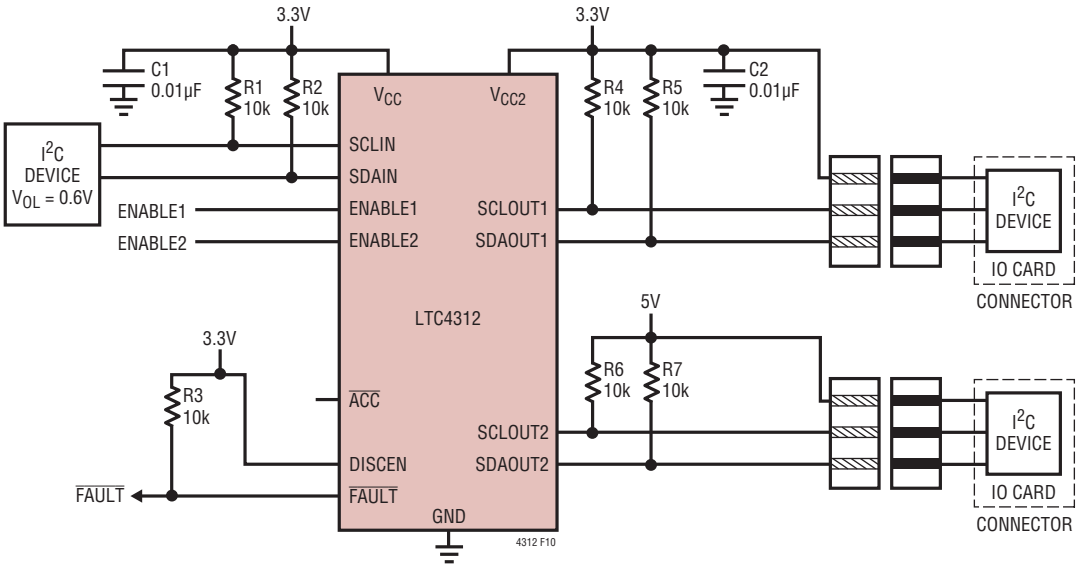


Figure 10. SDA, SCL Hot Swap™ and Operation with a Non-Compliant I^2C Device

APPLICATIONS INFORMATION

Level Translating to Bus Voltages < 2.25V

The LTC4312 can be used for level translation to bus voltages below 2.25V if certain conditions are met. In order to perform this level translation, RTAs on the low voltage side need to be disabled in order to prevent an over drive of the low voltage bus. If one of the output channels is pulled up to the low voltage bus supply, the other output channel needs to be disabled when this channel is active, in order to prevent cross conduction between the output channels. Since the buffer turn-on and turn-off voltages are $0.3 \bullet V_{MIN}$, the minimum bus supply voltage is determined by equation 5:

$$V_{DD,BUS(MIN)} \geq \frac{0.3 \bullet V_{MIN}}{0.7} \quad (5)$$

in order to meet the $V_{IH} = 0.7 \bullet V_{DD,BUS}$ requirement and not impact the high side noise margin. Users willing to live with a lower logic high noise margin can level translate down to 1.5V. An example of voltage level translation from 3.3V to 1.8V is illustrated in Figure 11, where a 3.3V input voltage level is translated to a 1.8V output voltage level on channel 1. Tying V_{CC} to 3.3V satisfies equation 5. Grounding V_{CC2} disables the RTA on the low voltage channel. V_{MIN} defaults to V_{CC} under these conditions, making the buffer turn off voltage 0.99V. Channel 2 must be disabled when channel 1 is enabled. A similar voltage translation can also be performed going from a 3.3V bus supply on the output side to a 1.8V bus supply on the input side if $\overline{ACC}$ is tied high to disable the input RTA and if V_{CC} and V_{CC2} are tied to the output side bus supply.

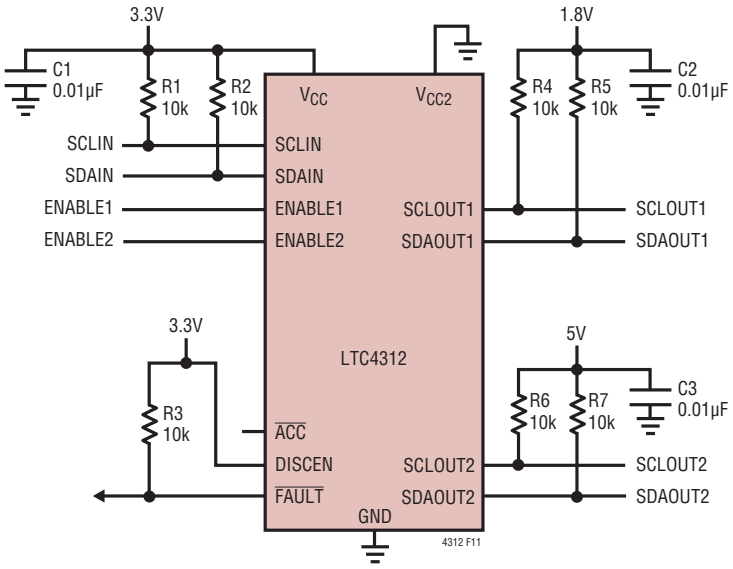
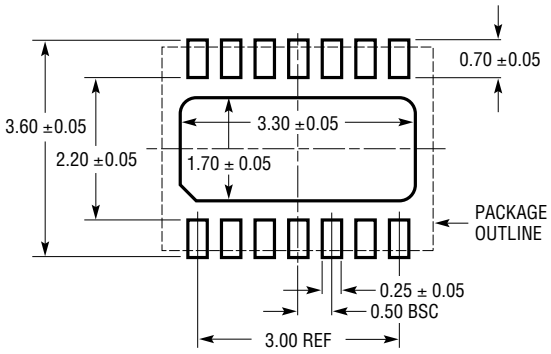


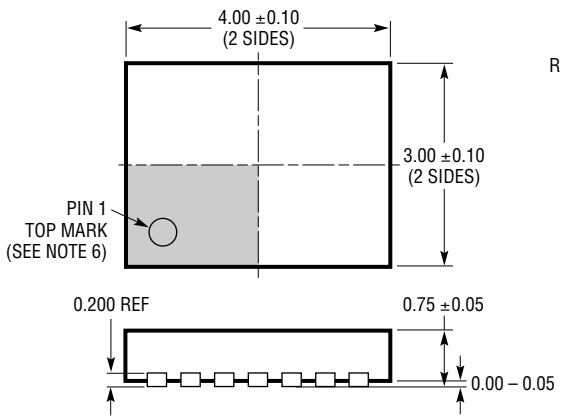
Figure 11. Level Shifting Down to 1.8V Using the LTC4312, V_{CC2} Is Grounded to Disable the Rise Time Accelerator on the Low Voltage Bus. ENABLE2 Must Be Low Whenever ENABLE1 Is High

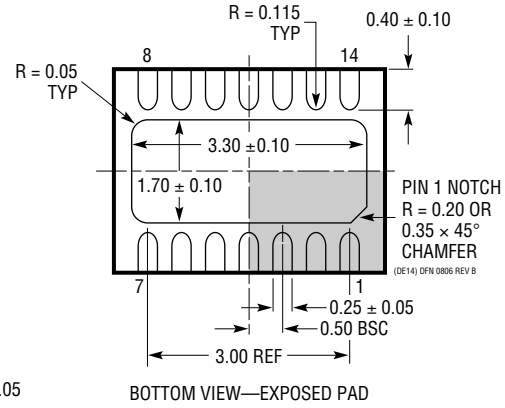
PACKAGE DESCRIPTION

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



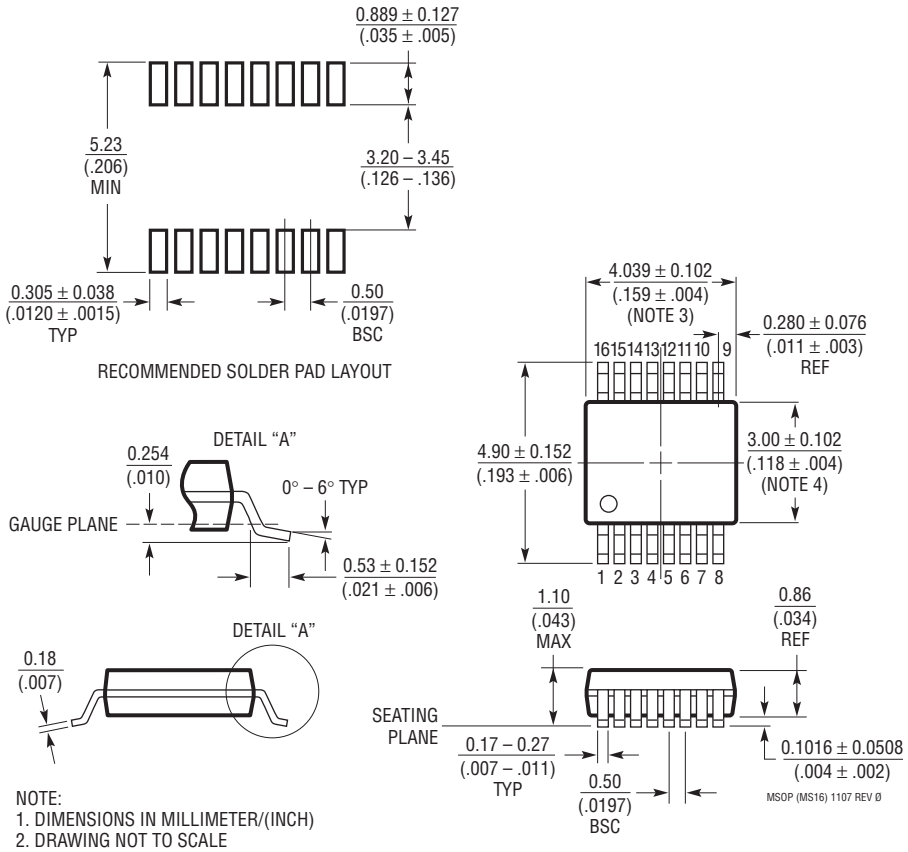


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

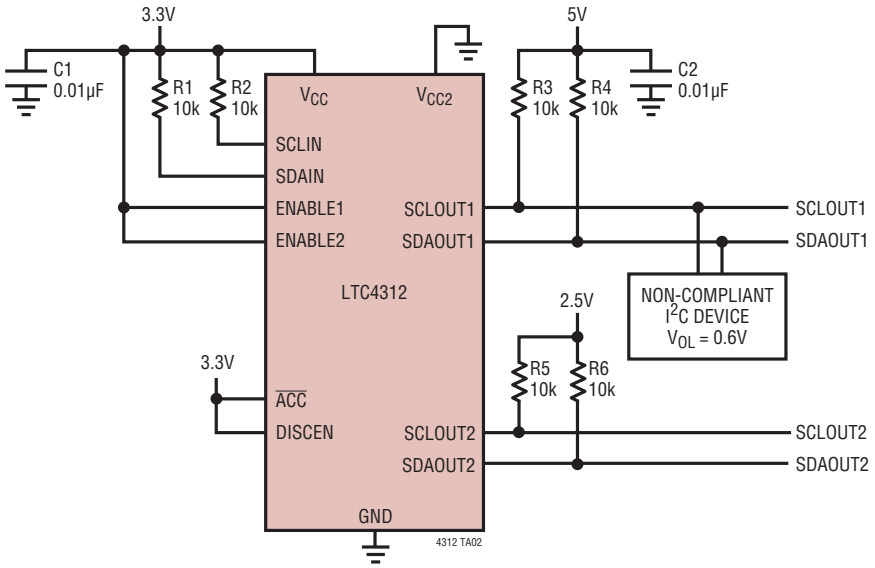
MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Level Translating 2.5V, 3.3V and 5V Busses and Operation with a Non-Compliant I²C Device



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4300A-1/ LTC4300A-2/ LTC4300A-3	Hot-Swappable 2-Wire Bus Buffers	-1: Bus Buffer with READY and ENABLE -2: Dual Supply Buffer with $\overline{ACC}$ -3: Dual Supply Buffer with ENABLE
LTC4302-1/ LTC4302-2	Addressable 2-Wire Bus Buffer	Address Expansion, GPIO, Software Controlled
LTC4303 LTC4304	Hot-Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	Provides Automatic Clocking to Free Stuck I²C Busses
LTC4305 LTC4306	2- or 4-Channel, 2-Wire Bus Multiplexers with Capacitance Buffering	2 or 4 Software Selectable Downstream Busses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±10kV HBM ESD Tolerance
LTC4307	Low Offset Hot-Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Bus Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ±5kV HBM ESD Tolerance
LTC4307-1	High Definition Multimedia Interface (HDMI) Level Shifting 2-Wire Bus Buffer	60mV Buffer Offset, 3.3V to 5V Level Shifting, ±5kV HBM ESD Tolerance
LTC4308	Low Voltage, Level Shifting Hot-Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	Bus Buffer with ENABLE and READY, Level Translation to 1V Busses, Output Side Rise Time Accelerators
LTC4309	Low Offset Hot-Swappable 2-Wire Bus Buffer with Stuck Bus Recovery	60mV Buffer Offset, 30ms Stuck Bus Disconnect and Recovery, Rise Time Accelerators, ±5kV HBM ESD Tolerance
LTC4310-1/ LTC4310-2	Hot-Swappable I²C Isolators	-1: 100kHz Bus -2: 400kHz Bus
LTC4311	Low Voltage I²C/SMBus Accelerator	Rise Time Acceleration with ENABLE and ±8kV HBM ESD Tolerance
LTC4314	Pin-Selectable, 4-Channel, 2-Wire Multiplexer with Bus Buffer	4 Pin-Selectable Downstream Busses, Stuck Bus Disconnect and Recovery, Selectable Rise Time Accelerator Current and Activation Voltage, ±4kV HBM ESD Tolerance
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Bus Buffer with 1V Pre-Charge, $\overline{CS}$ and READY
LTC4301L	Hot-Swappable 2-Wire Bus Buffer with Low Voltage Level Translation	Bus Buffer with $\overline{CS}$ and READY Allowing for Input Bus Voltages of Up to 1V
LTC1694-1	SMBus/I²C Accelerator	Rise Time Accelerator

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