Dual 12-Bit Rail-to-Rail Micropower DACs

FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 5V Operation, I_{CC}: 700μA Typ (LTC1454)
- 3V Operation, I_{CC}: 450μA Typ (LTC1454L)
- Built-In Reference: 2.048V (LTC1454)
  1.220V (LTC1454L)
- $\overline{CLR}$ Pin
- Power-On Reset
- **16-Lead SO Package**
- 3-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

The LTC®1454/LTC1454L are complete single supply, dual rail-to-rail voltage output, 12-bit digital-to-analog converters (DACs) in a 16-lead SO package. They include an output buffer amplifier with variable gain (×1 or ×2) and an easy-to-use 3-wire cascadable serial interface.

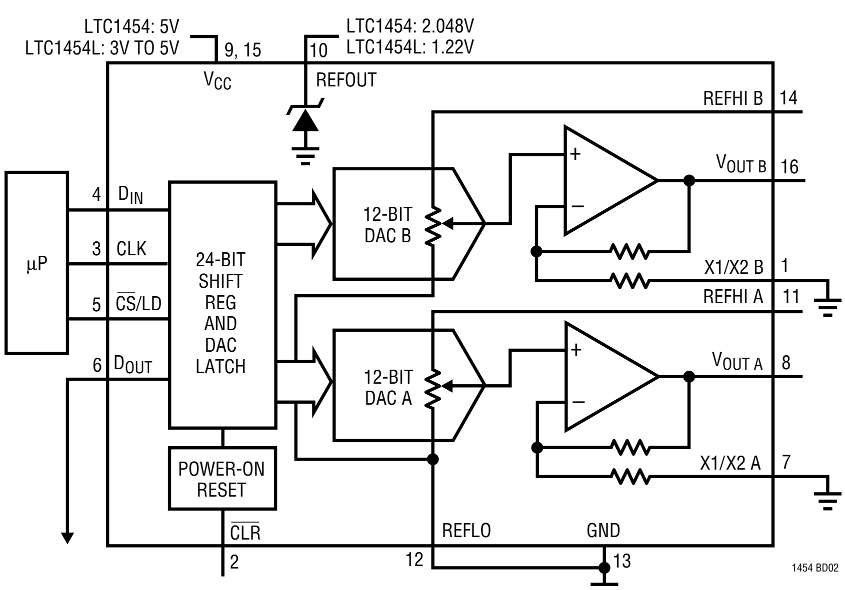
The LTC1454 has an onboard reference of 2.048V and a full-scale output of 4.095V in a ×2 gain configuration. It operates from a single 4.5V to 5.5V supply.

The LTC1454L has an onboard 1.22V reference and a full-scale output of 2.5V in a ×2 gain configuration. It operates from a single 2.7V to 5.5V supply.

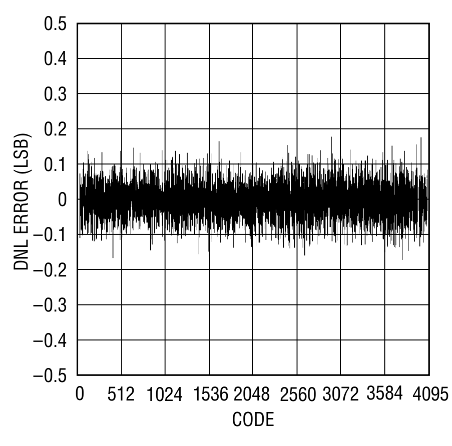
Low power supply current, excellent DNL and small size allow these parts to be used in a host of applications where size, DNL and single supply operation are important.

TYPICAL APPLICATION

Functional Block Diagram: Dual 12-Bit Rail-to-Rail DAC



Differential Nonlinearity vs Input Code

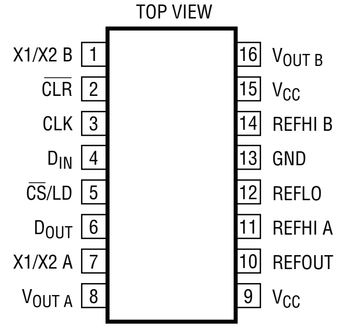


ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .... −0.5V to 7.5V
Logic Inputs to GND .... −0.5V to 7.5V
$V_{OUT\,A}$, $V_{OUT\,B}$, X1/X2 A,
X1/X2 B .... −0.5V to V_{CC} + 0.5V
REFHI A, REFHI B, REFLO .... −0.5V to V_{CC} + 0.5V
Maximum Junction Temperature .... 125°C
Operating Temperature Range
LTC1454C/LTC1454LC .... 0°C to 70°C
LTC1454I/LTC1454LI .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................. 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



N PACKAGE 16-LEAD PDIP
S PACKAGE 16-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LTC1454CN
LTC1454IN
LTC1454CS
LTC1454IS
LTC1454LCN
LTC1454LIN
LTC1454LCS
LTC1454LIS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1454), 2.7V to 5.5V (LTC1454L), X1/X2 = REFLO = GND, REFHI = REFOUT, V_{OUT} and REFOUT unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●			±0.5	LSB
INL	Integral Nonlinearity	T_A = 25°C			±2.0	±4.0	LSB
		(Note 1)	●		±2.5	±4.5	LSB
V_{OS}	Offset Error	T_A = 25°C			±2.0	±12	mV
			●		±4.0	±18	mV
$V_{OS}TC$	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	When Using Internal Reference, LTC1454, T_A = 25°C		4.065	4.095	4.125	V
		LTC1454	●	4.045	4.095	4.145	V
		When Using Internal Reference, LTC1454L, T_A = 25°C		2.470	2.500	2.530	V
		LTC1454L	●	2.460	2.500	2.540	V
$V_{FS}TC$	Full-Scale Voltage Temperature Coefficient	When Using Internal Reference			±24		ppm/°C
Reference							
	Reference Output Voltage	LTC1454	●	2.008	2.048	2.088	V
		LTC1454L	●	1.195	1.220	1.245	V
	Reference Output Temperature Coefficient				±20		ppm/°C
	Reference Line Regulation		●		0.7	±2.0	LSB/V
	Reference Load Regulation	0 ≤ I_{OUT} ≤ 100µA, LTC1454	●		0.2	1.5	LSB
		LTC1454L	●		0.6	3.0	LSB
	Reference Input Range	$V_{REFHI} \le V_{CC} - 1.5V$			$V_{CC}/2$		V
	Reference Input Resistance		●	15	24	40	kΩ
	Reference Input Capacitance				15		pF
	Short-Circuit Current	REFOUT Shorted to GND	●		40	120	mA

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1454), 2.7V to 5.5V (LTC1454L), X1/X2 = REFLO = GND, REFHI = REFOUT, V_{OUT} and REFOUT unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1454 LTC1454L	● ●	4.5 2.7		5.5 5.5	V V
I_{CC}	Supply Current	$4.5V \le V_{CC} \le 5.5V$ (Note 4), LTC1454 $2.7V \le V_{CC} \le 5.5V$ (Note 4), LTC1454L	● ●		700 450	1250 1100	µA µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		70	120	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		80	120	mA
	Output Impedance to GND	Input Code = 0	●		40		Ω
AC Performance							
	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0		V/µs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		µs
	Digital Feedthrough				0.3		nV•s
	AC Feedthrough	REFHI = 1kHz, $2V_{P-P}$, (Code: All 0s)			–95		dB
SINAD	Signal-to-Noise + Distortion	REFHI = 1kHz, $2V_{P-P}$, (Code: All 1s)			85		dB

V_{CC} = 5V (LTC1454), 3V (LTC1454L), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

				LTC1454			LTC1454L			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Digital I/O										
V_{IH}	Digital Input High Voltage		●	2.4			2.0			V
V_{IL}	Digital Input Low Voltage		●			0.8			0.6	V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA	●	V_{CC} – 1.0			V_{CC} – 0.7			V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA	●			0.4			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10			±10	µA
C_{IN}	Digital Input Capacitance	Guaranteed by Design	●			10			10	pF
Switching										
t_1	D_{IN} Valid to CLK Setup		●	40			60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			0			ns
t_3	CLK High Time		●	40			60			ns
t_4	CLK Low Time		●	40			60			ns
t_5	$\overline{CS}$/LD Pulse Width		●	50			80			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40			60			ns
t7	$\overline{CS}$/LD Low to CLK		●	20			30			ns
t_8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●			150			220	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	20			30			ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

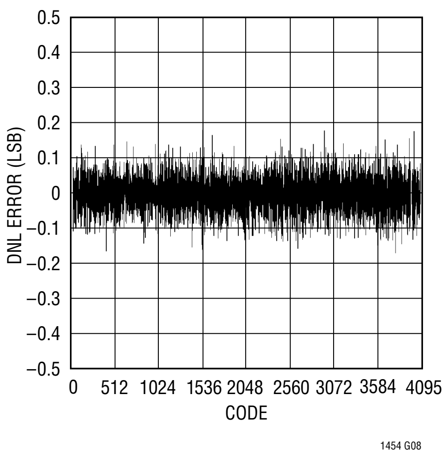
Note 2: Load is 5kΩ in parallel with 100pF.

Note 3: DAC switched between all 1s and the code corresponding to V_{OS} for the part.

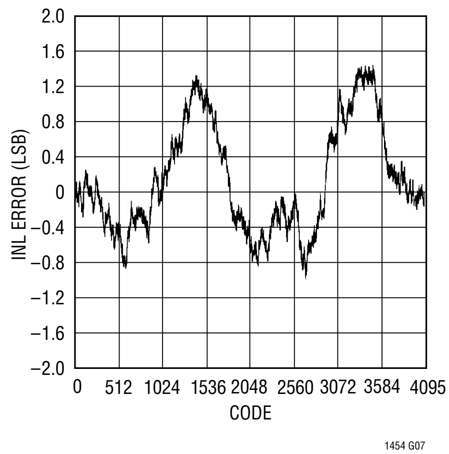
Note 4: Digital inputs at 0V or V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

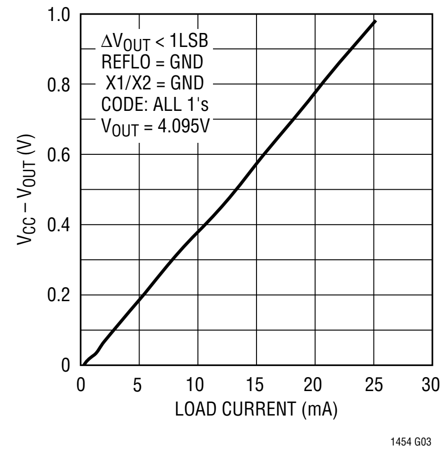
LTC1454 Differential Nonlinearity



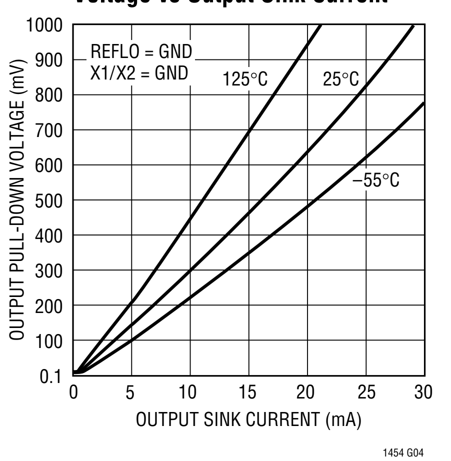
LTC1454 Integral Nonlinearity



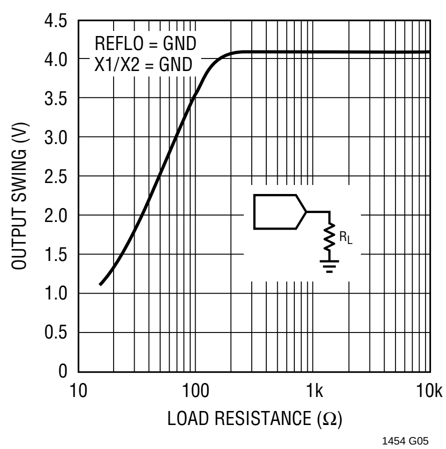
Minimum Supply Headroom for Full Output Swing vs Load Current



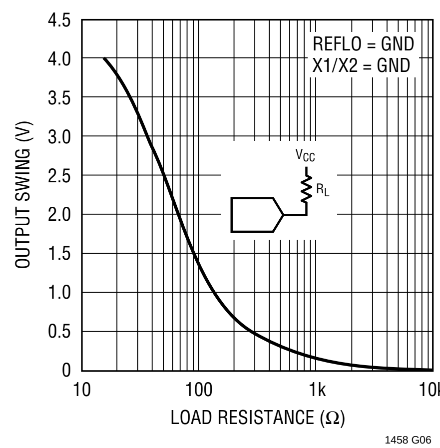
LTC1454 Minimum Output Voltage vs Output Sink Current



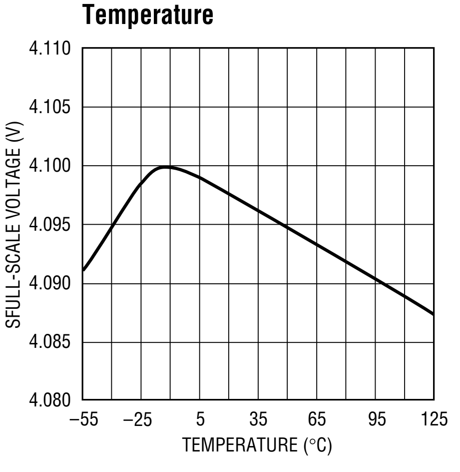
LTC1454 Output Swing vs Load Resistance



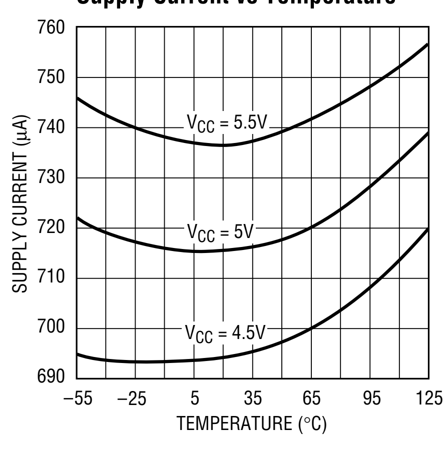
LTC1454 Output Swing vs Load Resistance



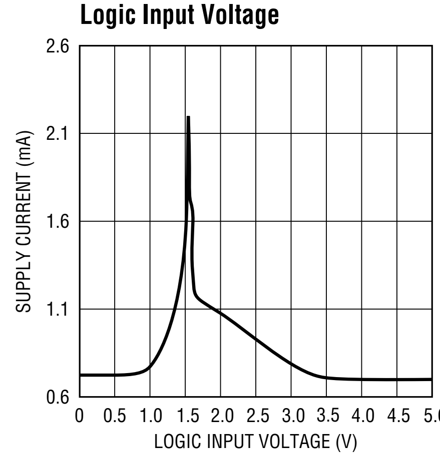
LTC1454 Full-Scale Voltage vs Temperature



LTC1454 Supply Current vs Temperature



LTC1454 Supply Current vs Logic Input Voltage



PIN FUNCTIONS

X1/X2 B, X1/X2 A (Pins 1, 7): The Input Pin that Sets the Gain for DAC A/B. When grounded the gain will be 2, i.e., output full scale will be ×2 REFHI. When connected to V_{OUT} the gain will be 1, i.e., output full scale will be equal to REFHI.

$\overline{\text{CLR}}$ (Pin 2): The Clear Pin for the DAC. Clears both DACs to zero scale when pulled low. This pin should be tied to V_{CC} for normal operation.

CLK (Pin 3): The Serial Interface Clock Input.

D_{IN} (Pin 4): The Serial Data Input. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock. Data is loaded as one 24-bit word. The first 12 bits are for DAC A, MSB-first and the second 12 bits are for DAC B, MSB-first.

$\overline{\text{CS}}$/LD (Pin 5): The Serial Interface Enable and Load Control Input. When $\overline{\text{CS}}$/LD is low the CLK signal is enabled so the data can be clocked in. When $\overline{\text{CS}}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT} (Pin 6): The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

$V_{OUT\ A}$, $V_{OUT\ B}$ (Pins 8, 16): The Buffered DAC Outputs.

V_{CC} (Pins 9, 15): The Positive Supply Input. $4.5 \le V_{CC} \le 5.5V$ (LTC1454), $2.7V \le V_{CC} \le 5.5V$ (LTC1454L). Requires a bypass capacitor to ground.

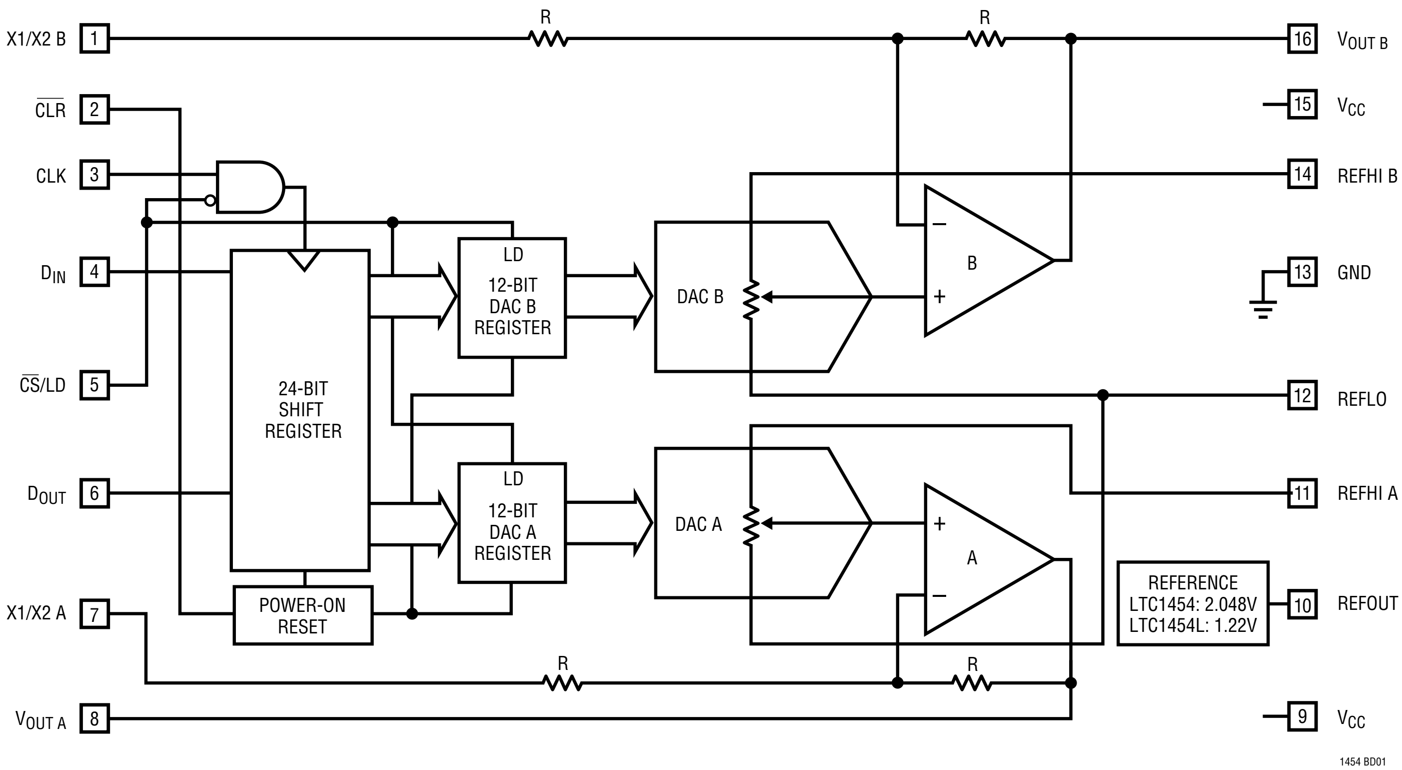
REFOUT (Pin 10): The Output of the Internal Reference.

REFHI A , REFHI B (Pins 11,14): The Inputs to the DAC Resistor Ladder for DAC A/B.

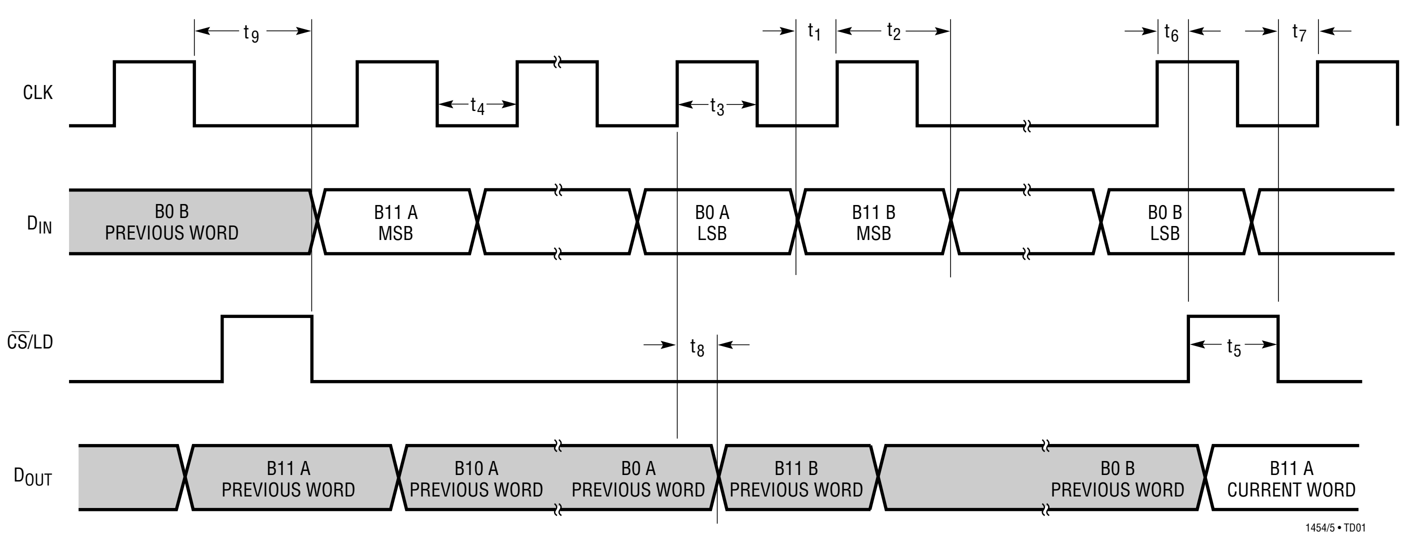
REFLO (Pin 12): The Bottom of the DAC Resistor Ladder for Both DACs. This can be used to offset zero-scale above ground. REFLO should be connected to ground when no offset is required.

GND (Pin 13): Ground.

BLOCK DIAGRAM



TIMING DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

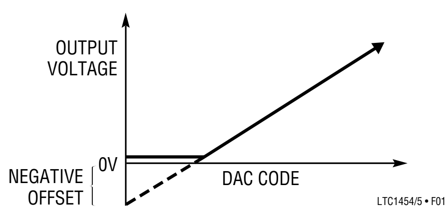


Figure 1. Effect of Negative Offset

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - (\text{Code})(V_{FS})/(2^n - 1)$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1454	LSB = 4.095V/4095 = 1mV
LTC1454L	LSB = 2.5V/4095 = 0.610mV

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(\text{Code}/4095)]/LSB$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 24-bit word, DAC A first, then DAC B. The MSB is loaded first for each DAC. The DAC registers load the data from the shift register when $\overline{CS}$/LD is pulled high. The CLK is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 24-bit shift register is available on the D_{OUT} pin which swings from ground to V_{CC}.

Multiple LTC1454/LTC1454Ls may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the CLK and $\overline{CS}$/LD signals remain common to all chips in the daisy-chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Reference

The LTC1454L has an internal reference of 1.22V with a full scale of 2.5V (gain of 2 configuration). The LTC1454 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2 configuration). When the buffer gain is 2, the external reference must be less than $V_{CC}/2$ and be capable of driving the 15k minimum DAC resistor ladder. With a gain of 1 configuration the external reference must be less than V_{CC} – 1.5V.

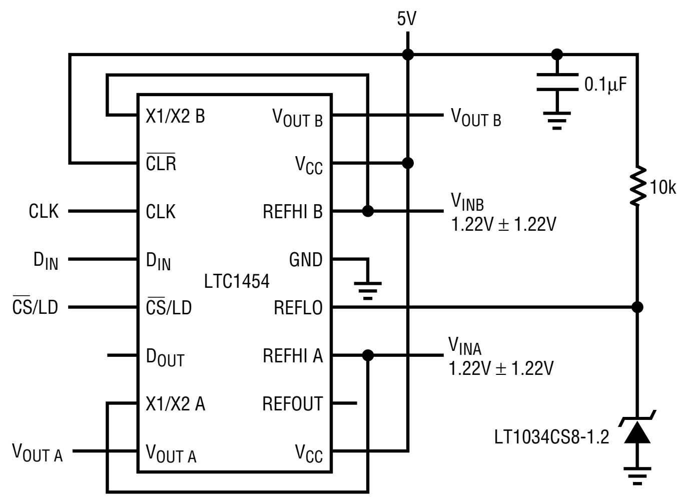
Voltage Output

The rail-to-rail buffered output of the LTC1454 family can source or sink 5mA when operating with a 5V supply while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

APPLICATIONS INFORMATION

A Single Supply, 4-Quadrant Multiplying DAC

The LTC1454 can also be used for 4-quadrant multiplying with an offset signal ground of 1.22V. This application is shown in Figure 2. The inputs are connected to REFHI B or REFHI A and have a 1.22V amplitude around a signal ground of 1.22V. The outputs will swing from 0V to 2.44V, as shown by the equation with the figure. Since the signal ground is around 1.22V, REFLO is offset above ground by using an LT1034CS8-1.2 as shown.



$$V_{OA/B} = (V_{IN} - V_{REFLO})\left[GAIN\left(\frac{D_{IN}}{4096} - 1\right) + 1\right] + V_{REFLO}$$

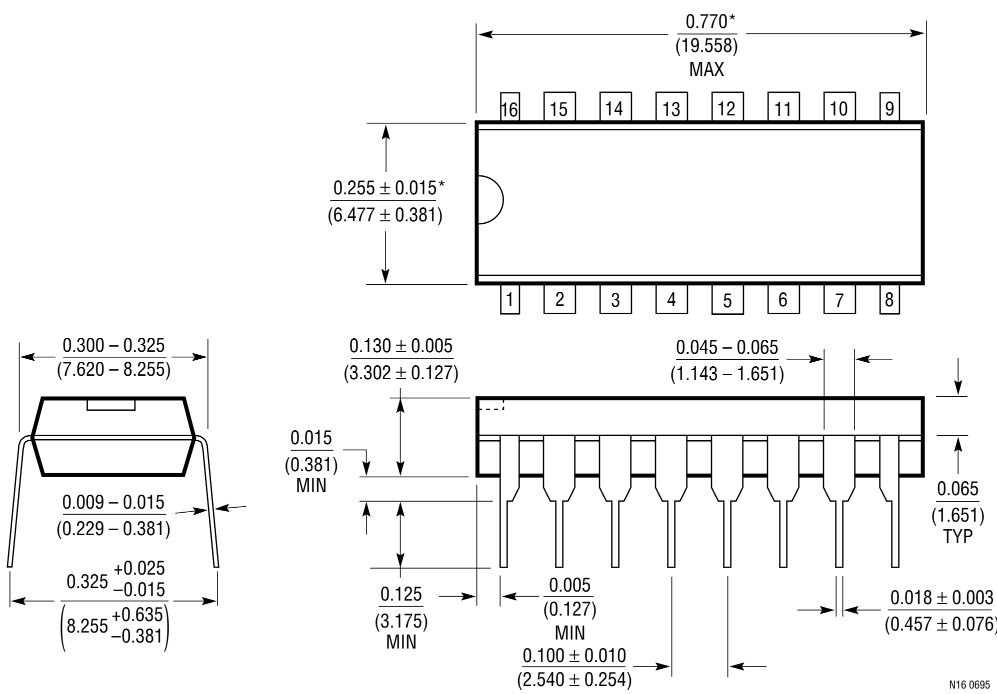
$$= (V_{IN} - 1.22)\left(2.0\,\frac{D_{IN}}{4096} - 1.0\right) + 1.22V$$

Figure 2

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

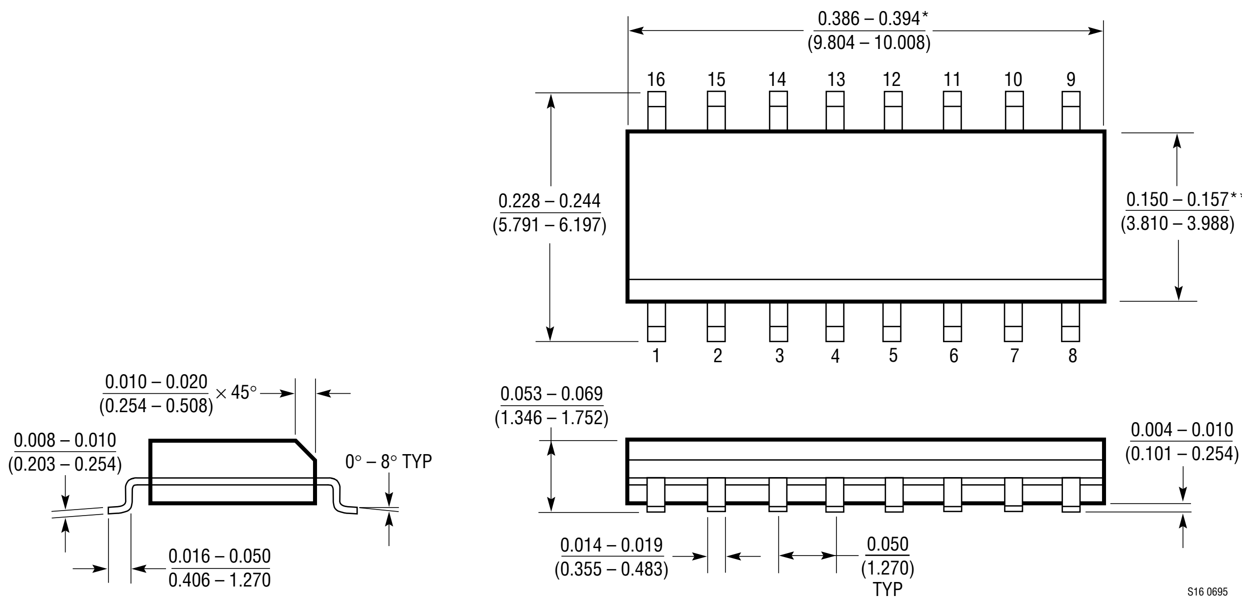


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

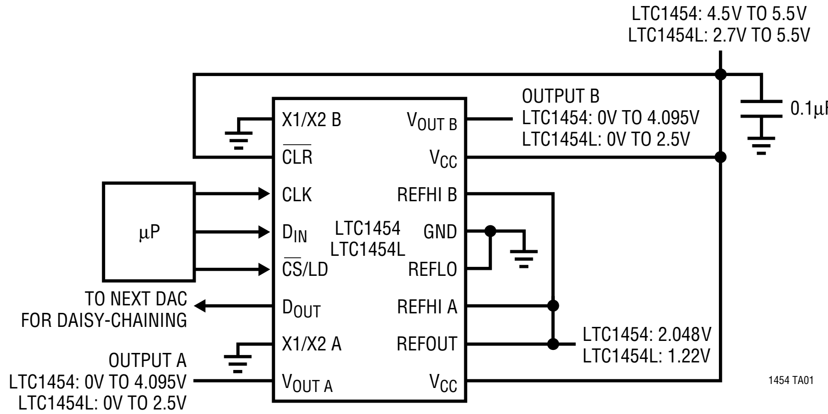
S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V, Reference Can Be Overdriven up to 12V, i.e., FS_{MAX} = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit Rail-to-Rail Output DACs in an SO-8 Package	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1450/LTC1450L	Single 12-Bit Rail-to-Rail Output DACs with Parallel Interface	LTC1450: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1450L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1451	Single 12-Bit DAC, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single 12-Bit Rail-to-Rail Output V_{OUT} Multiplying DAC, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single 12-Bit V_{OUT} DAC, Full Scale: 2.5V, V_{CC}: 2.7V to 5.5V	3V, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package, with Clear Pin
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417 • (408) 432-1900
FAX: (408) 434-0507 • TELEX: 499-3977 • www.linear-tech.com
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