

Dual and Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps

FEATURES

- **Offset Voltage: 50 μ V Maximum (LT1881A)**
- **Input Bias Current: 200pA Maximum (LT1881A)**
- **Offset Voltage Drift: 0.8 μ V/ $^{\circ}$ C Maximum**
- **Rail-to-Rail Output Swing**
- **Supply Range: 2.7V to 36V**
- Operates with Single or Split Supplies
- Open-Loop Voltage Gain: 1 Million Minimum
- 1mA Maximum Supply Current Per Amplifier
- Stable at $A_V = 1$, $C_L = 1000$ pF
- Standard Pinouts

APPLICATIONS

- Thermocouple Amplifiers
- Bridge Transducer Conditioners
- Instrumentation Amplifiers
- Battery-Powered Systems
- Photo Current Amplifiers

DESCRIPTION

The LT[®]1881 and LT1882 op amps bring high accuracy input performance to amplifiers with rail-to-rail output swing. Input bias currents and capacitive load driving capabilities are superior to the similar LT1884 and LT1885 amplifiers, at the cost of a slight loss in speed. Input offset voltage is trimmed to less than 50 μ V and the low drift maintains this accuracy over the operating temperature range. Input bias currents are an ultralow 200pA maximum.

The amplifiers work on any total power supply voltage between 2.7V and 36V (fully specified from 5V to ± 15 V). Output voltage swings to within 40mV of the negative supply and 220mV of the positive supply make these amplifiers good choices for low voltage single supply operation.

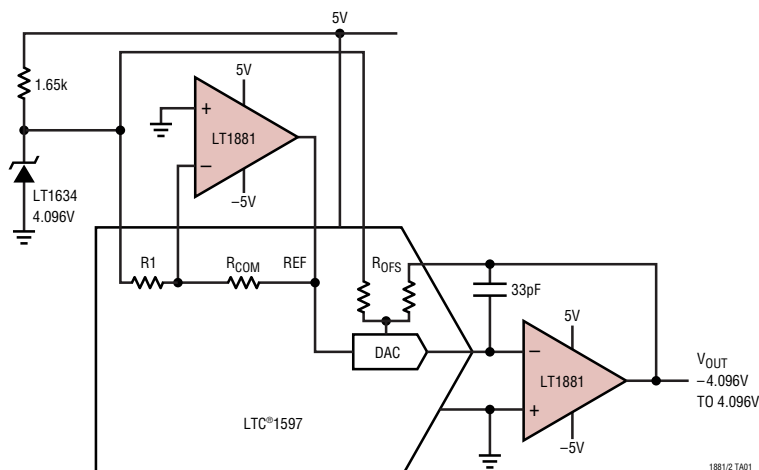
Capacitive loads up to 1000pF can be driven directly in unity-gain follower applications.

The dual LT1881 and LT1881A are available with standard pinouts in S8 and PDIP packages. The quad LT1882 is in a 14-pin SO package. For a higher speed device with similar DC specifications, see the LT1884/LT1885.

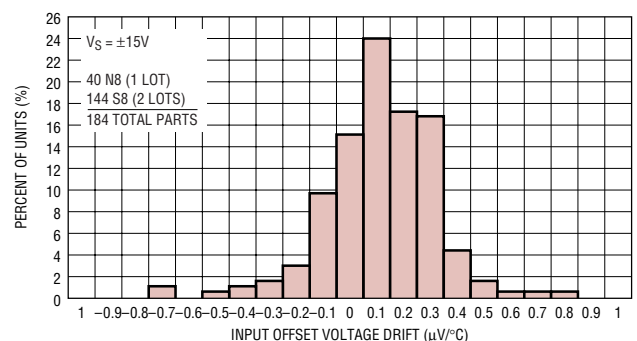
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TYPICAL APPLICATION

16-Bit Voltage Output DAC on ± 5 V Supply



TC V_{OS} Distribution, Industrial Grade



LT1881/LT1882

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-)	40V	Operating Temperature Range (Note 4) ..	-40°C to 85°C
Differential Input Voltage (Note 2)	$\pm 10\text{V}$	Specified Temperature Range (Note 5) ...	-40°C to 85°C
Input Voltage	V^+ to V^-	Maximum Junction Temperature	150°C
Input Current (Note 2)	$\pm 10\text{mA}$	Storage Temperature Range	-65°C to 150°C
Output Short-Circuit Duration (Note 3)	Indefinite	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>N8 PACKAGE 8-LEAD PDIP</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$ (N8) $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$ (S8)</p>	ORDER PART NUMBER	<p>S PACKAGE 14-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$</p>	ORDER PART NUMBER
	LT1881CN8 LT1881IN8 LT1881CS8 LT1881IS8 LT1881ACN8 LT1881AIN8 LT1881ACS8 LT1881AIS8		LT1882CS LT1882IS
	S8 PART MARKING		
	1881 1881I 1881A 1881AI	Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/	

Consult LTC marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$.
 Single supply operation $V_S = 5\text{V}$, 0V ; $V_{CM} = V_S/2$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1881A)	$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$		25	50	μV
		$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$	●		85	μV
			●		110	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$		0.3	0.8	$\mu\text{V}/^{\circ}\text{C}$
		$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$	●	0.3	0.8	$\mu\text{V}/^{\circ}\text{C}$
			●			
$\Delta V_{OS}/\Delta \text{TIME}$	Long-Term Input Offset Voltage Stability			0.3		$\mu\text{V}/\text{month}$
I_{OS}	Input Offset Current (LT1881A)	$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$		100	200	pA
		$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$	●		250	pA
			●		300	pA
I_{OS}	Input Offset Current (LT1881/LT1882)	$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$		150	500	pA
		$-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$	●		600	pA
			●		700	pA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.
 Single supply operation $V_S = 5\text{V}$, 0V ; $V_{CM} = V_S/2$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
I_B	Input Bias Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	100	200	μA	
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		250	μA	
	Input Bias Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	150	500	μA	
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		600	μA	
	Input Noise Voltage	0.1Hz to 10Hz		0.5		$\mu\text{V}_{\text{P-P}}$	
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		14		$\text{nV}/\sqrt{\text{Hz}}$	
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.03		$\text{pA}/\sqrt{\text{Hz}}$	
R_{IN}	Input Resistance	Differential Mode	●	20		$\text{M}\Omega$	
		Common Mode	●	100		$\text{G}\Omega$	
C_{IN}	Input Capacitance		●	2		pF	
V_{CM}	Input Voltage Range		●	$V^- + 1.0$	$V^+ - 1.0$	V	
			●	$V^- + 1.2$	$V^+ - 1.2$	V	
CMRR	Common Mode Rejection Ratio	$1\text{V} < V_{CM} < 4\text{V}$	●	106	128	dB	
		$1.2\text{V} < V_{CM} < 3.8\text{V}$	●	104		dB	
PSRR	Power Supply Rejection Ratio	$V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$	●	106	132	dB	
		$0^\circ\text{C} < T_A < 85^\circ\text{C}$, $2.7\text{V} < V^+ < 32\text{V}$ $T_A = -40^\circ\text{C}$, $3\text{V} < V^+ < 32\text{V}$	●	106	132	dB	
	Minimum Operating Supply Voltage		●	2.4	2.7	V	
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}$; $1\text{V} < V_{OUT} < 4\text{V}$	●	500	1600	V/mV	
			●	350		V/mV	
		$R_L = 2\text{k}$; $1\text{V} < V_{OUT} < 4\text{V}$	●	300	800	V/mV	
		$R_L = 1\text{k}$; $1\text{V} < V_{OUT} < 4\text{V}$	●	250		V/mV	
			●	200	400	V/mV	
V_{OL}	Output Voltage Swing Low	No Load	●	20	40	mV	
		$I_{SINK} = 100\mu\text{A}$	●	25	50	mV	
		$I_{SINK} = 1\text{mA}$	●	70	150	mV	
		$I_{SINK} = 5\text{mA}$	●	270	600	mV	
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load	●	120	220	mV	
		$I_{SOURCE} = 100\mu\text{A}$	●	130	230	mV	
		$I_{SOURCE} = 1\text{mA}$	●	180	300	mV	
		$I_{SOURCE} = 5\text{mA}$	●	360	600	mV	
I_S	Supply Current Per Amplifier	$V_S = 3\text{V}$, 0V	●	0.45	0.65	0.85	mA
			●			1.2	mA
		$V_S = 5\text{V}$, 0V	●	0.5	0.65	0.9	mA
			●			1.4	mA
		$V_S = 12\text{V}$, 0V	●	0.5	0.70	1.0	mA
			●			1.5	mA
I_{SC}	Short-Circuit Current	V_{OUT} Short to GND	●	15	30	mA	
		V_{OUT} Short to V^+	●	15	30	mA	
GBW	Gain Bandwidth Product	$f = 20\text{kHz}$		0.35	1.0	MHz	
	Channel Separation	$f = 1\text{kHz}$		120		dB	
t_S	Settling Time	0.01%, $V_{OUT} = 1.5\text{V}$ to 3.5V , $A_V = -1$, $R_L = 2\text{k}$		30		μs	

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Single supply operation $V_S = 5\text{V}$, 0V ; $V_{CM} = V_S/2$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SR ⁺	Slew Rate Positive	$A_V = -1$	0.15 0.12	0.35		V/ μs V/ μs
SR ⁻	Slew Rate Negative	$A_V = -1$	0.11 0.08	0.18		V/ μs V/ μs
FPBW	Full-Power Bandwidth	$V_{OUT} = 4V_{P-P}$ (Note 10)	8.75 6.35	14		kHz kHz
ΔV_{OS}	Offset Voltage Match (LT1881A)	(Note 7) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		30	70 125 160	μV μV μV
	Offset Voltage Match (LT1881/LT1882)	(Note 7) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		35	125 175 235	μV μV μV
	Offset Voltage Match Drift	(Notes 6, 7)		0.4	1.2	$\mu\text{V}/^\circ\text{C}$
ΔI_B^+	Noninverting Bias Current Match (LT1881A)	(Notes 7, 8) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		200	300 400 500	pA pA pA
	Noninverting Bias Current Match (LT1881/LT1882)	(Notes 7, 8) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		250	700 900 1000	pA pA pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	102	125		dB
ΔPSRR	Power Supply Rejection Match (Notes 7, 9)	$V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$ $0^\circ\text{C} < T_A < 85^\circ\text{C}$, $2.7\text{V} < V^+ < 32\text{V}$	104	126		dB
		$T_A = -40^\circ\text{C}$, $3\text{V} < V^+ < 32\text{V}$	104	126		dB

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Split supply operation $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$		25	50	μV
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$			85 110	μV μV
	Input Offset Voltage (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$		30	80	μV
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$			125 150	μV μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$		0.3	0.8	$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$		0.3	0.8	$\mu\text{V}/^\circ\text{C}$
$\Delta V_{OS}/\Delta\text{TIME}$	Long-Term Input Offset Voltage Stability			0.3		$\mu\text{V}/\text{month}$
I_{OS}	Input Offset Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$		150	200	pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$			250 300	pA pA
	Input Offset Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$		150	500	pA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$			600 700	pA pA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Split supply operation $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_B	Input Bias Current (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	150	200	μA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		250 300	μA μA
	Input Bias Current (LT1881/LT1882)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$	●	150	500	μA
		$-40^\circ\text{C} < T_A < 85^\circ\text{C}$	●		600 700	μA μA
	Input Noise Voltage	0.1Hz to 10Hz		0.5		$\mu\text{V}_{\text{P-P}}$
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		14		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.03		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential Mode	●	20		$\text{M}\Omega$
		Common Mode	●	100		$\text{G}\Omega$
C_{IN}	Input Capacitance		●	2		pF
V_{CM}	Input Voltage Range		●	$V^- + 1.0$	$V^+ - 1.0$	V
			●	$V^- + 1.2$	$V^+ - 1.2$	V
CMRR	Common Mode Rejection Ratio	$-13.5\text{V} < V_{CM} < 13.5\text{V}$	●	114	130	dB
+PSRR	Positive Power Supply Rejection Ratio	$V^- = -15\text{V}$, $V_{CM} = 0\text{V}$; $1.5\text{V} < V^+ < 18\text{V}$	●	110	132	dB
-PSRR	Negative Power Supply Rejection Ratio	$V^+ = 15\text{V}$, $V_{CM} = 0\text{V}$; $-1.5\text{V} < V^- < -18\text{V}$	●	106	132	dB
	Minimum Operating Supply Voltage		●	± 1.2	± 1.35	V
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10\text{k}$; $-13.5\text{V} < V_{OUT} < 13.5\text{V}$	●	1000 700	1600	V/mV V/mV
		$R_L = 2\text{k}$; $-13.5\text{V} < V_{OUT} < 13.5\text{V}$	●	175 125	420	V/mV V/mV
		$R_L = 1\text{k}$; $-12\text{V} < V_{OUT} < 12\text{V}$	●	90 65	230	V/mV V/mV
V_{OL}	Output Voltage Swing Low (Referred to V_{EE})	No Load	●	20	40	mV
		$I_{SINK} = 100\mu\text{A}$	●	25	50	mV
		$I_{SINK} = 1\text{mA}$	●	70	150	mV
		$I_{SINK} = 5\text{mA}$	●	270	600	mV
V_{OH}	Output Voltage Swing High (Referred to V_{CC})	No Load	●	160	220	mV
		$I_{SOURCE} = 100\mu\text{A}$	●	160	230	mV
		$I_{SOURCE} = 1\text{mA}$	●	180	300	mV
		$I_{SOURCE} = 5\text{mA}$	●	360	600	mV
I_S	Supply Current Per Amplifier	$V_S = \pm 15\text{V}$	●	0.5	0.85	mA
					1.1	1.6
I_{SC}	Short-Circuit Current	V_{OUT} Short to V^-	●	20 15	40	mA mA
		V_{OUT} Short to V^+	●	20 15	30	mA mA
GBW	Gain Bandwidth Product	$f = 20\text{kHz}$		0.4	0.85	MHz
	Channel Separation	$f = 1\text{kHz}$		120		dB
t_S	Settling Time	0.01%, $V_{OUT} = -5\text{V}$ to 5V , $A_V = -1$, $R_L = 2\text{k}$		35		μs
SR^+	Slew Rate Positive	$A_V = -1$	●	0.21	0.4	$\text{V}/\mu\text{s}$
				0.18		$\text{V}/\mu\text{s}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Split supply operation $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SR^-	Slew Rate Negative	$A_V = -1$	0.13 0.1	0.20		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_{OUT} = 28\text{V}_{P-P}$ (Note 10)	1.47 1.13	2.25		kHz kHz
ΔV_{OS}	Offset Voltage Match (LT1881/LT1882)	(Note 5) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		42	125	μV μV μV
	Offset Voltage Match (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		35	70	μV μV μV
	Offset Voltage Match Drift	(Notes 6, 7)		0.4	1.1	$\mu\text{V}/^\circ\text{C}$
ΔI_{B+}	Noninverting Bias Current Match (LT1881/LT1882)	(Notes 7, 8) $0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		240	700	pA pA pA
	Noninverting Bias Current Match (LT1881A)	$0^\circ\text{C} < T_A < 70^\circ\text{C}$ $-40^\circ\text{C} < T_A < 85^\circ\text{C}$		200	300	pA pA pA
ΔCMRR	Common Mode Rejection Match	(Notes 7, 9)	110	125		dB
$\Delta+\text{PSRR}$	Positive Power Supply Rejection Match	$V^- = -15\text{V}$, $V_{CM} = 0\text{V}$, $1.5\text{V} < V^+ < 18\text{V}$, (Notes 7, 9)	108	130		dB
$\Delta-\text{PSRR}$	Negative Power Supply Rejection Match	$V^+ = 15\text{V}$, $V_{CM} = 0\text{V}$, $-1.5\text{V} < V^- < -18\text{V}$, (Notes 7, 9)	104	130		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by internal resistors and back-to-back diodes. If the differential input voltage exceeds $\pm 0.7\text{V}$, the input current should be limited externally to less than 10mA .

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1881C, LT1882C, LT1881I and LT1882I are guaranteed functional over the operating temperature range of -40°C to 85°C .

Note 5: The LT1881C and LT1882C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not

tested or QA sampled at these temperatures. The LT1881I and LT1882I are guaranteed to meet specified performance from -40°C to 85°C .

Note 6: This parameter is not 100% tested.

Note 7: Matching parameters are the difference between amplifiers A and B in the LT1881; and between amplifiers A and D and B and C in the LT1882.

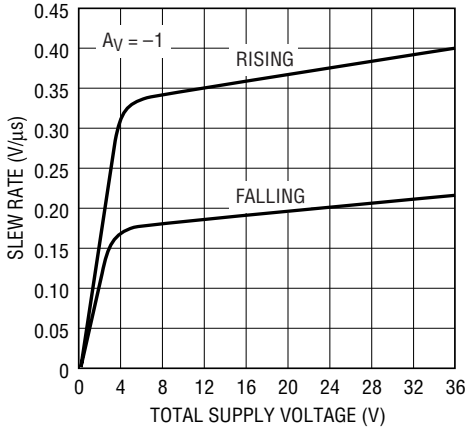
Note 8: This parameter is the difference between the two noninverting input bias currents.

Note 9: ΔCMRR and ΔPSRR are defined as follows: CMRR and PSRR are measured in $\mu\text{V}/\text{V}$ on each amplifier. The difference is calculated in $\mu\text{V}/\text{V}$ and then converted to dB .

Note 10: Full power bandwidth is calculated from the slew rate: $\text{FPBW} = \text{SR}/2\pi V_P$.

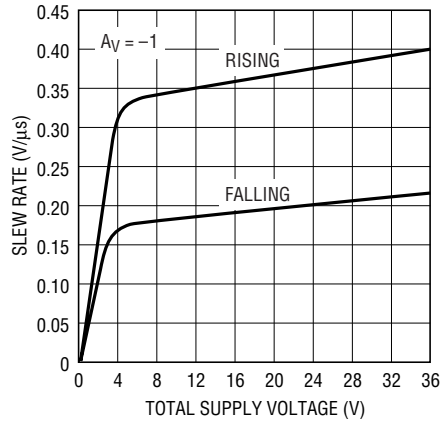
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current per Amplifier vs Supply Voltage



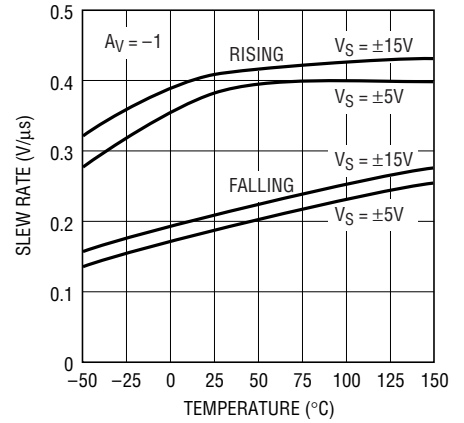
1881/2 G02

Slew Rate vs Supply Voltage



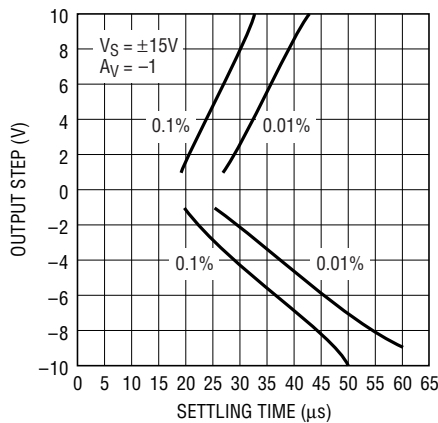
1881/2 G02

Slew Rate vs Temperature



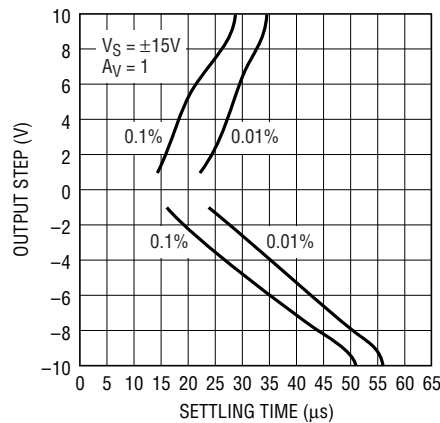
1881/2 G03

Settling Time vs Output Step



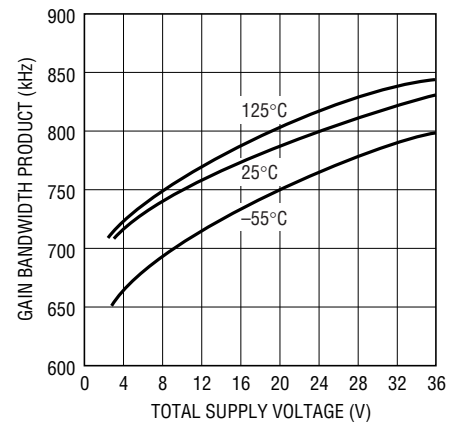
1881/2 G04

Settling Time vs Output Step



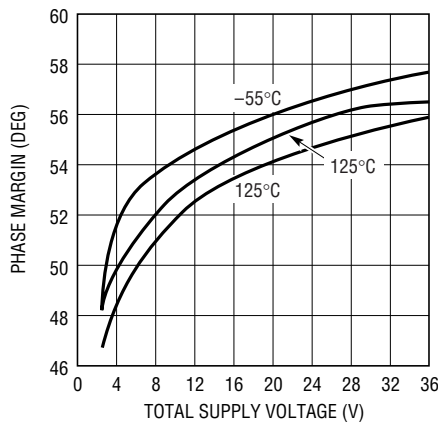
1881/2 G05

Gain Bandwidth Product vs Supply Voltage



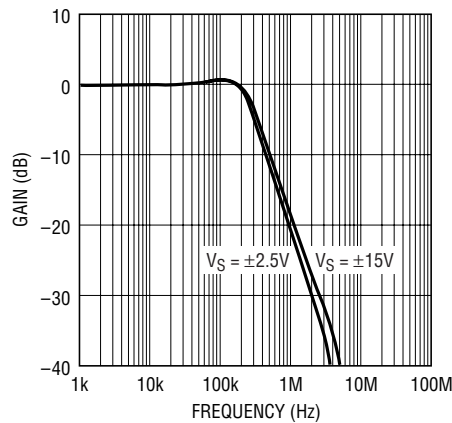
1881/2 G06

Phase Margin vs Supply Voltage



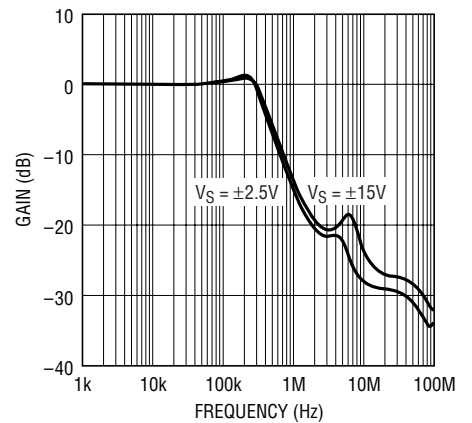
1881/2 G07

Gain vs Frequency, Av = -1



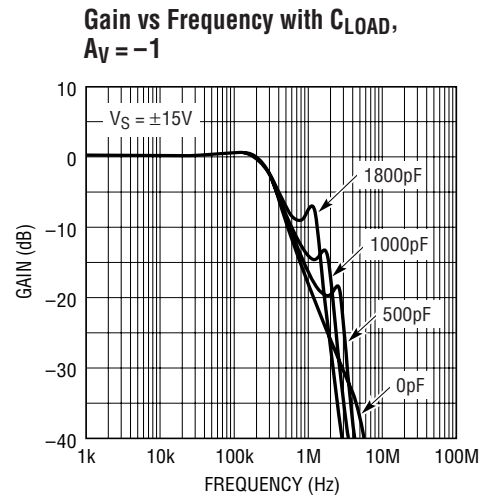
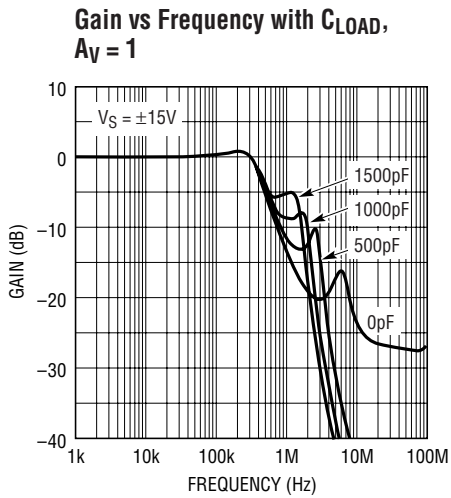
1881/2 G08

Gain vs Frequency, Av = 1

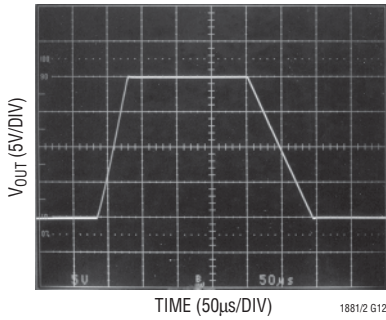


1881/2 G09

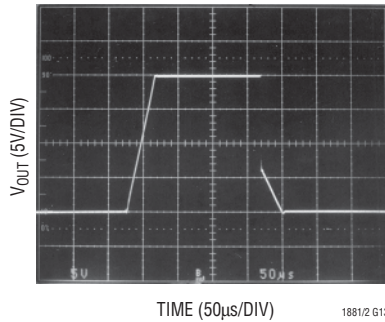
TYPICAL PERFORMANCE CHARACTERISTICS



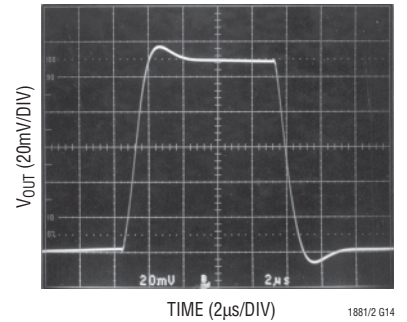
Large Signal Response, $A_V = -1$



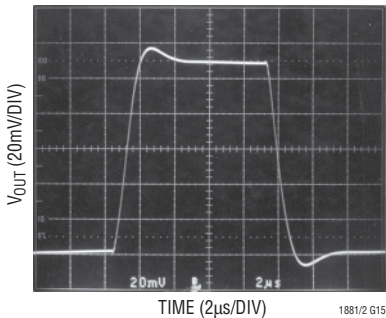
Large Signal Response, $A_V = 1$



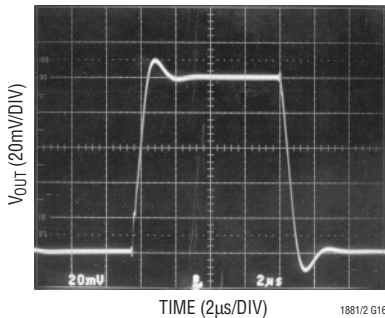
Small Signal Response, $A_V = -1$, No Load



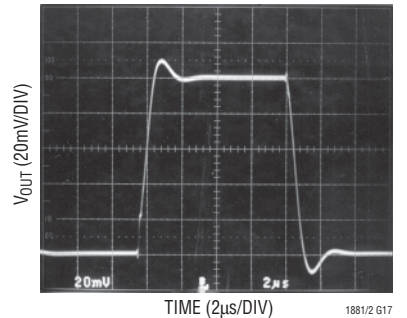
Small Signal Response, $A_V = -1$, $C_L = 1000pF$



Small Signal Response, $A_V = 1$, $R_L = 2k$

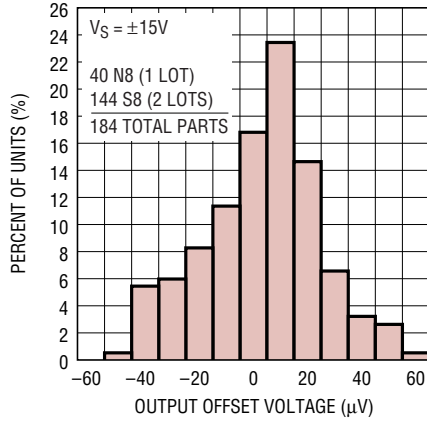


Small Signal Response, $A_V = 1$, $C_L = 500pF$



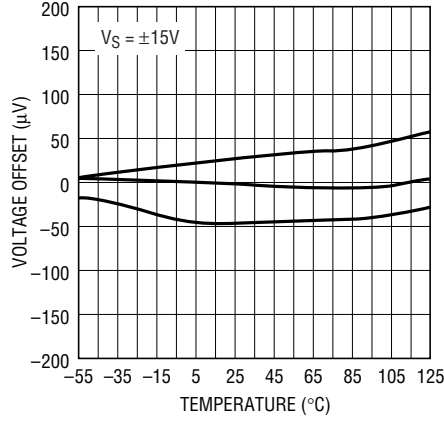
TYPICAL PERFORMANCE CHARACTERISTICS

LT1881 V_{OS} Distribution, $T_A = 25^\circ\text{C}$



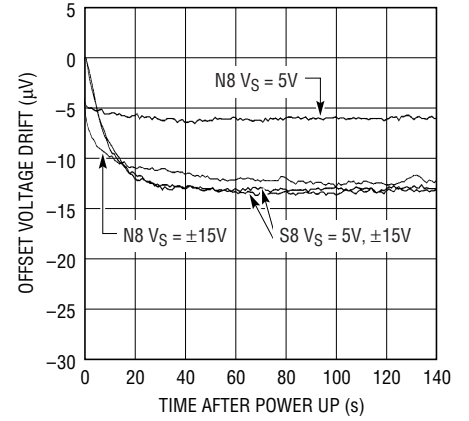
1881/2 G18

LT1881S8 Voltage Offset vs Temperature



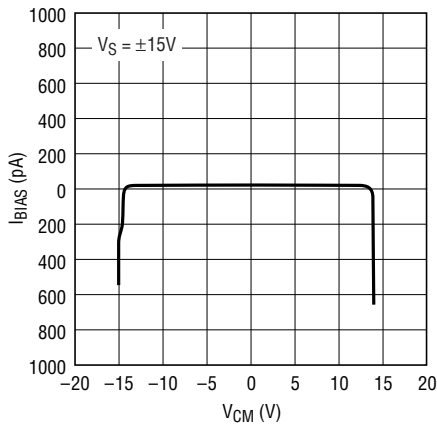
1881/2 G19

Warm-Up Drift vs Time



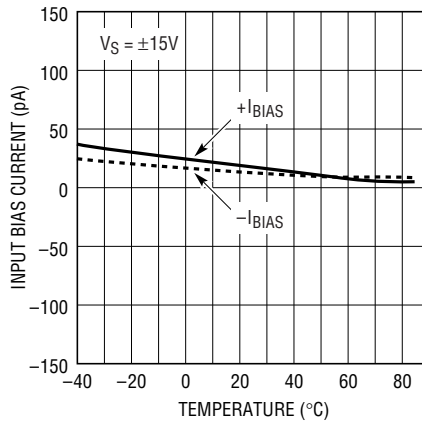
1881/2 G20

LT1881 Input Bias Current vs Common Mode Voltage



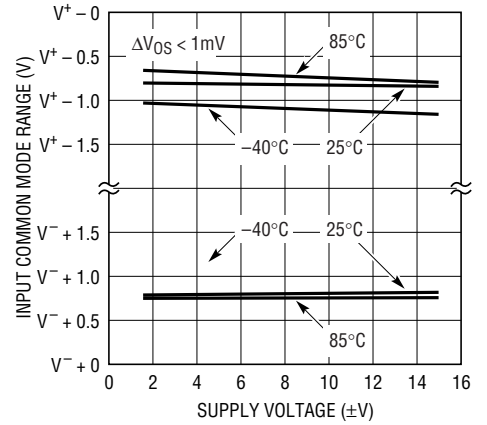
1881/2 G21

LT1881 Input Bias Current vs Temperature



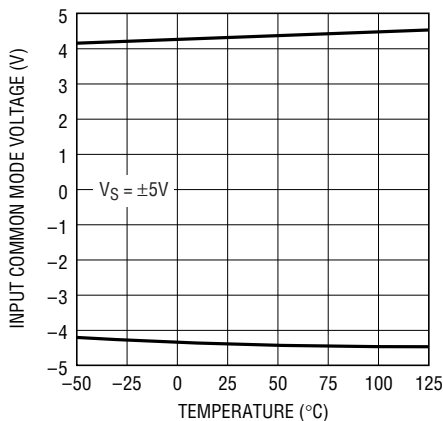
1881/2 G22

LT1881 Input Common Mode Range vs Supply Voltage



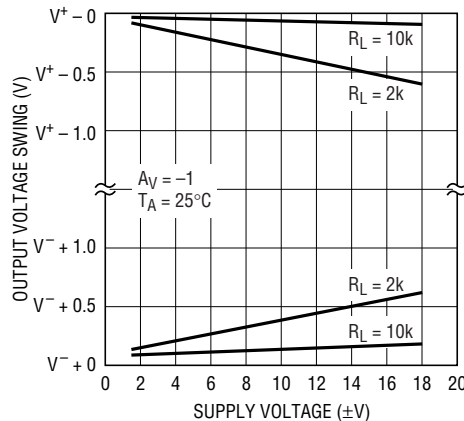
1881/2 G23

LT1881 Input Common Mode Voltage vs Temperature



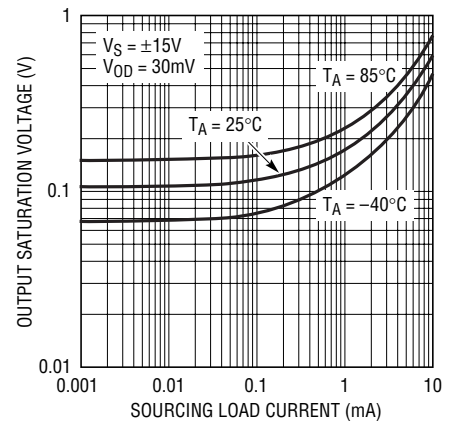
1881/2 G24

LT1881 Output Voltage Swing vs Supply Voltage



1881/2 G25

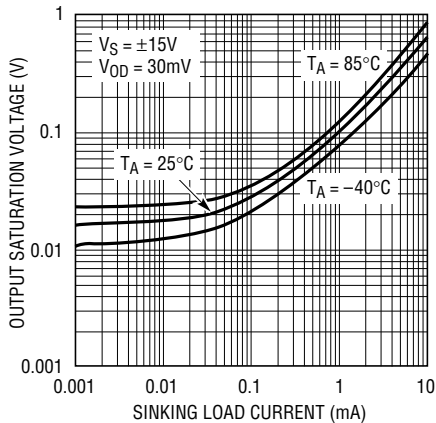
LT1881 Output Saturation Voltage vs Load Current (Output High)



1881/2 G26

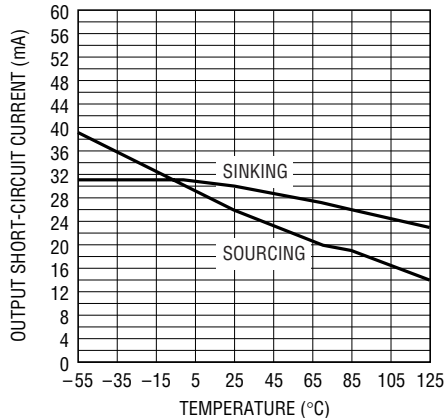
TYPICAL PERFORMANCE CHARACTERISTICS

LT1881 Output Saturation Voltage vs Load Current (Output Low)



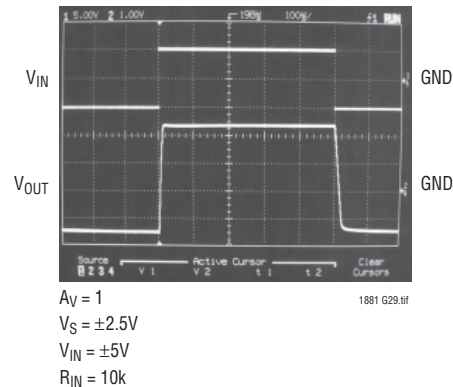
1881/2 G27

LT1881 Output Short-Circuit Current vs Temperature



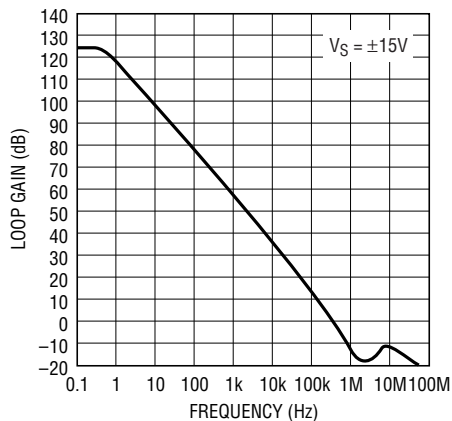
1881/2 G28

LT1881 Output Voltage vs Large Input Voltage



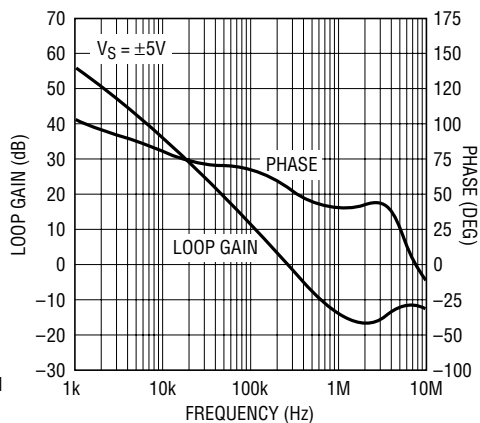
1881 G29.tif

LT1881 Open-Loop Gain vs Frequency



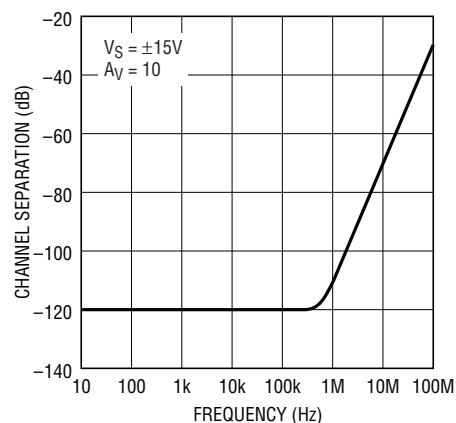
1881/2 G30

LT1881 Open-Loop Gain and Phase vs Frequency



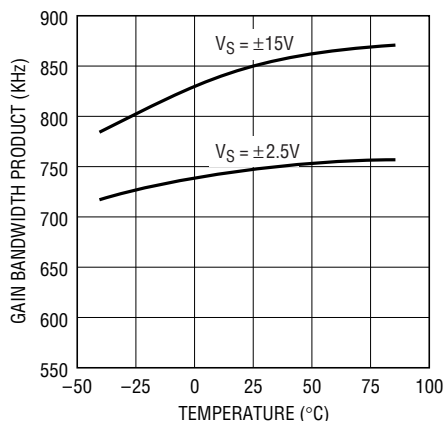
1881/2 G31

LT1881 Channel Separation vs Frequency



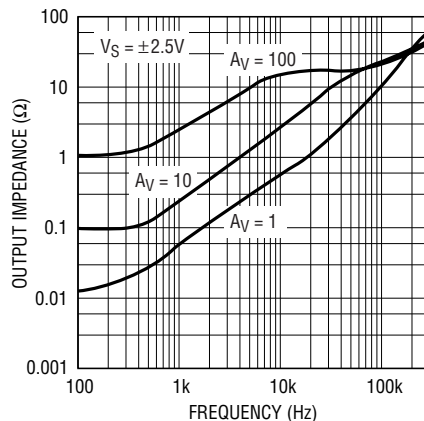
1881/2 G32

Gain Bandwidth Product vs Temperature



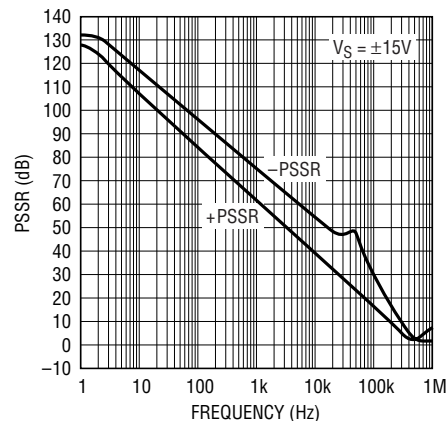
1881/2 G33

Output Impedance vs Frequency



1881/2 G34

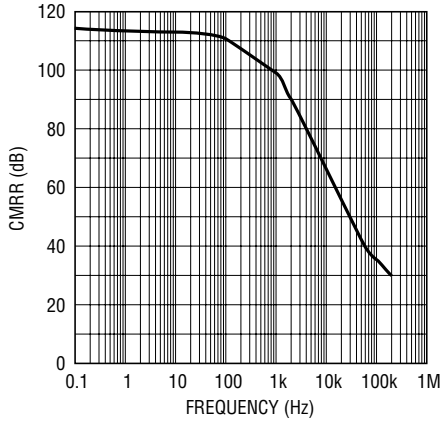
LT1881 PSRR vs Frequency



1881/2 G35

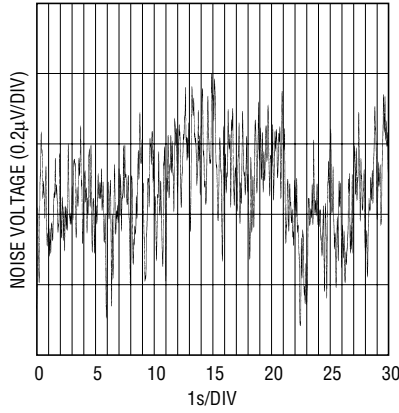
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection Ratio vs Frequency



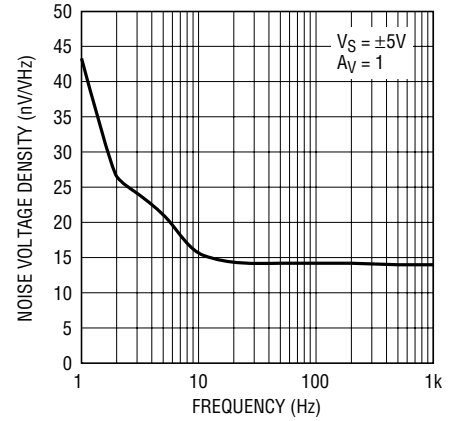
1881/2 G36

LT1881 0.1Hz to 10Hz Noise



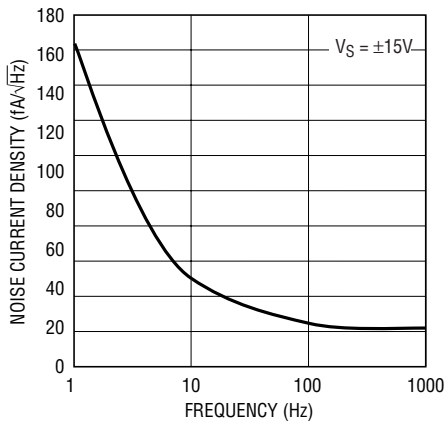
1881/2 G37

LT1881 Noise Voltage vs Frequency



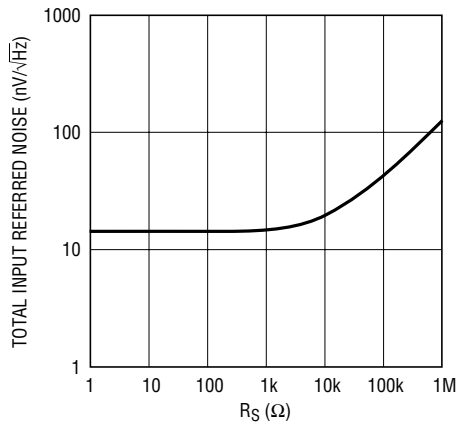
1881/2 G38

LT1881 Noise Current Density vs Frequency



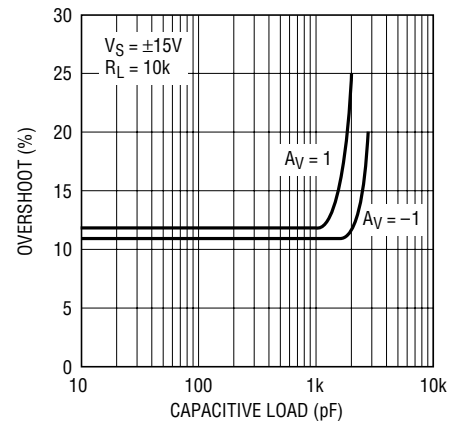
1881/2 G39

LT1881A Total Noise vs Source Resistance



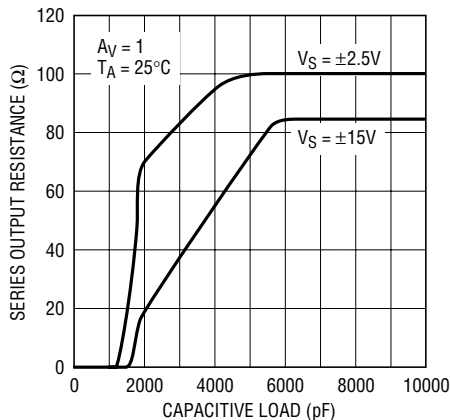
1881/2 G36

LT1881 Overshoot vs Capacitive Load



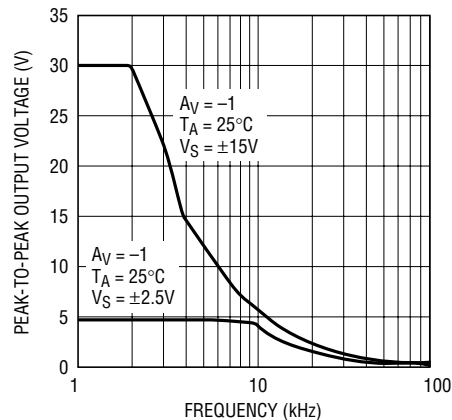
1881/2 G41

LT1881 Series Output Resistance vs Capacitive Load



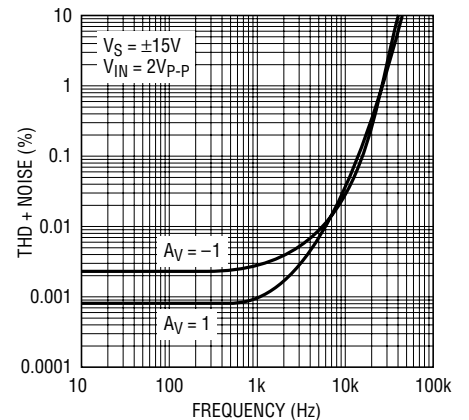
1881/2 G42

LT1881 Undistorted Output Swing vs Frequency



1881/2 G43

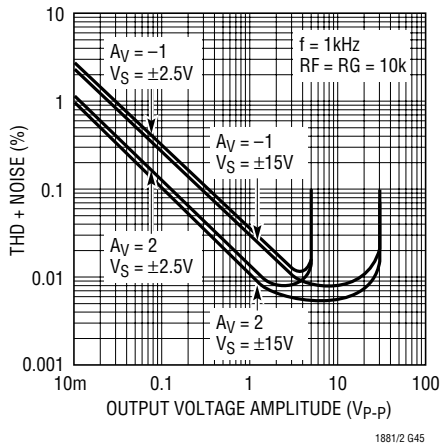
LT1881 THD + Noise vs Frequency



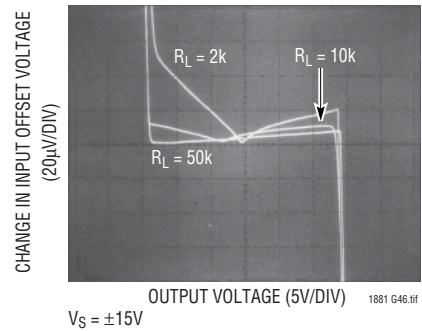
1881/2 G44

TYPICAL PERFORMANCE CHARACTERISTICS

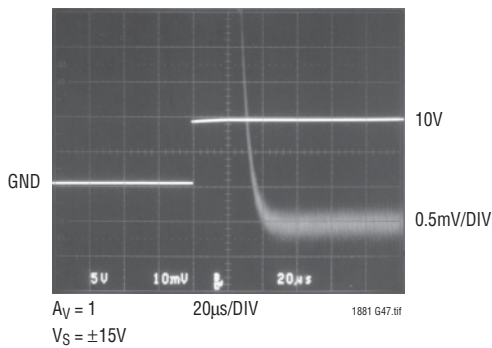
LT1881 Total Harmonic Distortion + Noise vs Output Voltage Amplitude



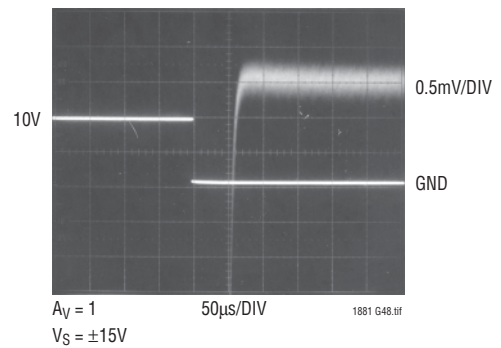
LT1881 Open-Loop Gain



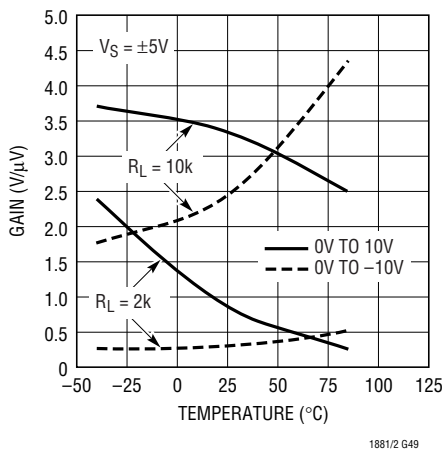
LT1881 Settling Time/ Output Step 0.01%



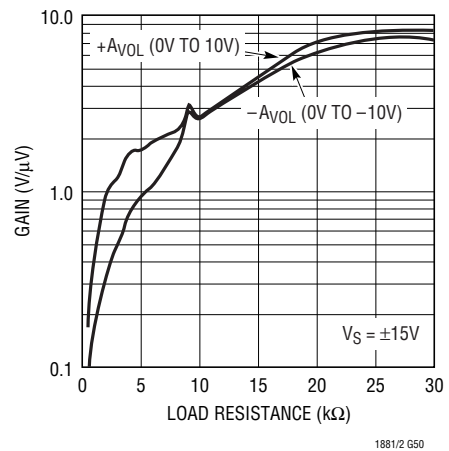
LT1881 Settling Time/ Output Step 0.01%



LT1881 Gain vs Temperature



LT1881 Gain vs Load Resistance



APPLICATIONS INFORMATION

The LT1881 dual and LT1882 quad op amps feature exceptional input precision with rail-to-rail output swing. The amplifiers are similar to the LT1884 and LT1885 devices. The LT1881 and LT1882 offer superior capacitive load driving capabilities over the LT1884 and LT1885 in low voltage gain configurations. Offset voltages are trimmed to less than $50\mu\text{V}$ and input bias currents are less than 200pA on the “A” grade devices. Obtaining beneficial advantage of these precision input characteristics depends upon proper applications circuit design and board layout.

Preserving Input Precision

Preserving the input voltage accuracy of the LT1881/LT1882 requires that the applications circuit and PC board layout do not introduce errors comparable to or greater than the $30\mu\text{V}$ offset. Temperature differentials across the input connections can generate thermocouple voltages of 10’s of microvolts. PC board layouts should keep connections to the amplifier’s input pins close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

The extremely low input bias currents, 150pA , allow high accuracy to be maintained with high impedance sources and feedback networks. The LT1881/LT1882’s low input bias currents are obtained by using a cancellation circuit on-chip. This causes the resulting $I_{\text{BIAS}+}$ and $I_{\text{BIAS}-}$ to be uncorrelated, as implied by the I_{OS} specification being greater than the I_{BIAS} . The user should not try to balance the input resistances in each input lead, as is commonly recommended with most amplifiers. The impedance at either input should be kept as small as possible to minimize total circuit error.

PC board layout is important to insure that leakage currents do not corrupt the low I_{BIAS} of the amplifier. In high precision, high impedance circuits, the input pins should be surrounded by a guard ring of PC board interconnect, with the guard driven to the same common mode voltage as the amplifier inputs.

Input Common Mode Range

The LT1881 and LT1882 outputs are able to swing nearly to each power supply rail, but the input stage is limited to operating between $V^- +1\text{V}$ and $V^+ -1\text{V}$. Exceeding this common mode range will cause the gain to drop to zero; however, no phase reversal will occur.

Input Protection

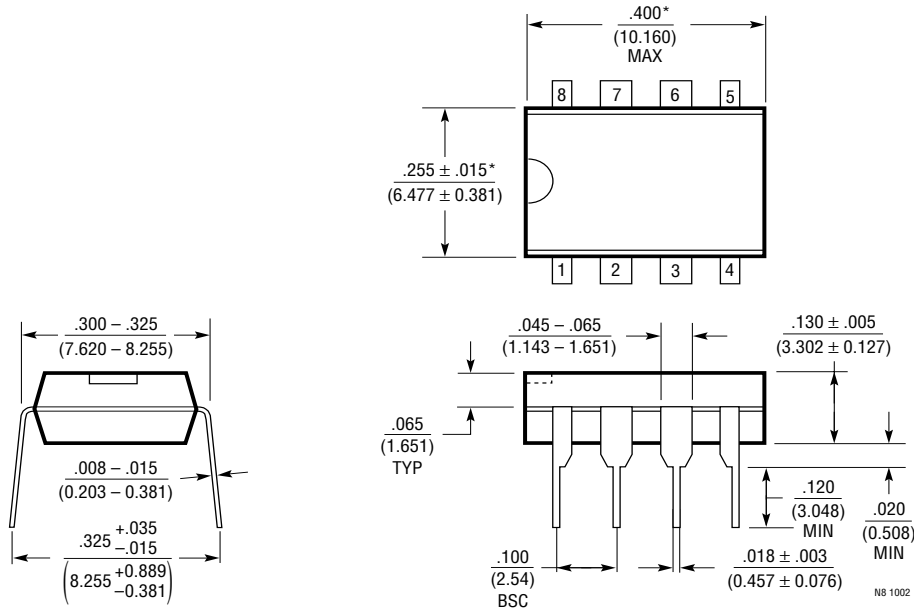
The inverting and noninverting input pins of the LT1881 and LT1882 have limited on-chip protection. ESD protection is provided to prevent damage during handling. The input transistors have voltage clamping and limiting resistors to protect against input differentials up to 10V . Short transients above this level will also be tolerated. If the input pins can see a sustained differential voltage above 10V , external limiting resistors should be used to prevent damage to the amplifier. A 1k resistor in each input lead will provide protection against a 30V differential voltage.

Capacitive Loads

The LT1881 and LT1882 can drive capacitive loads up to 1000pF in unity-gain. The capacitive load driving increases as the amplifier is used in higher gain configurations. Capacitive load driving may be increased by decoupling the capacitance from the output with a small resistance.

PACKAGE DESCRIPTION

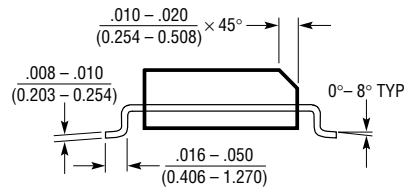
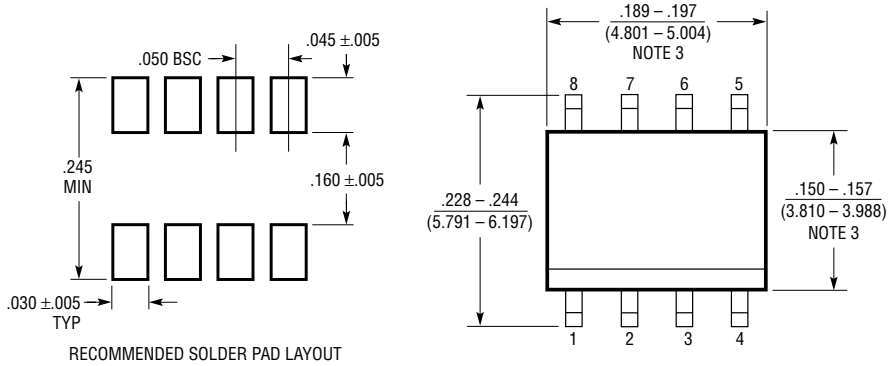
N8 Package
8-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)



NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 *THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

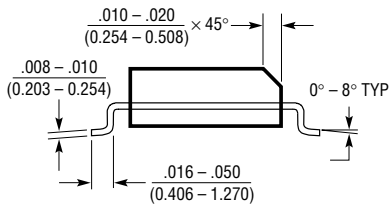
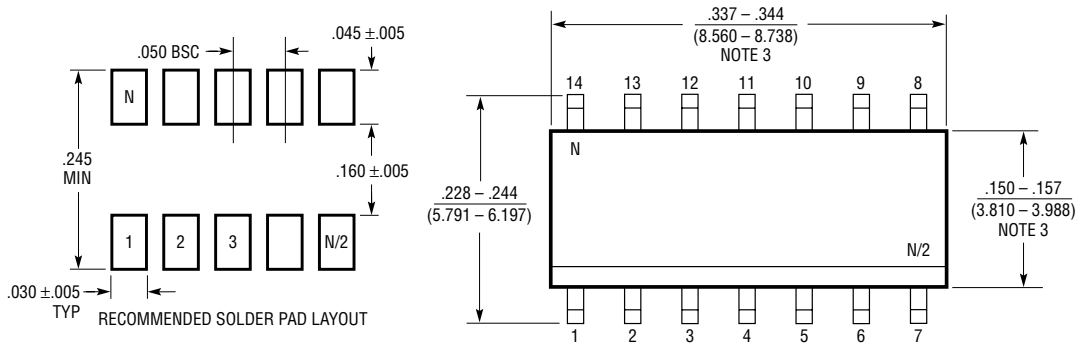
S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

S Package 14-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)

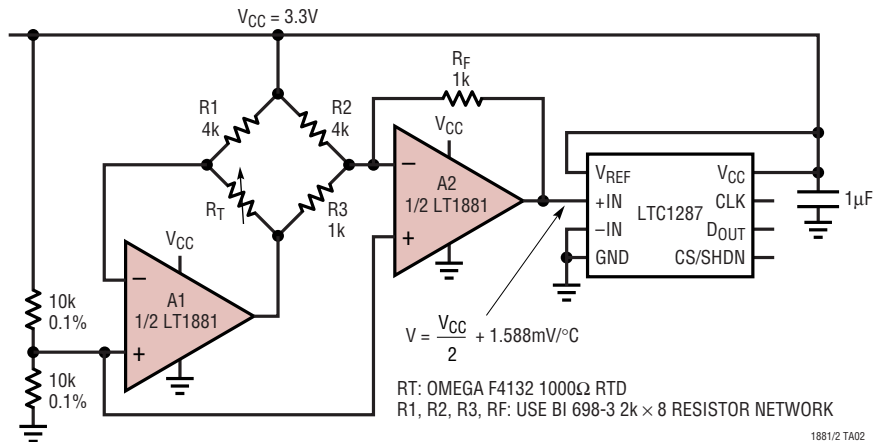


- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S14 0502

TYPICAL APPLICATION

-50°C to 600°C Digital Thermometer Operates on 3.3V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1112/LT1114	Dual/Quad Picoamp Input Op Amp	$V_{OS} = 60\mu\text{V}$ Max
LT1167	Gain Programmable Instrumentation Amp	Gain Error = 0.08% Max
LT1677	Low Noise, Rail-to-Rail Precision Op Amp	$e_n = 3.2\text{nV}/\sqrt{\text{Hz}}$
LT1793	Low Noise JFET Op Amp	$I_B = 10\text{pA}$ Max
LT1880	SOT-23 Picoamp Input Precision Op Amp	150μV Max V_{OS} , -40°C to 85°C Operation Guaranteed, SOT-23 Package
LT1884/LT1885	Dual/Quad Picoamp Input Op Amp	3 Times Faster than LT1881/LT1882
LTC2050	Zero Drift Op Amp in SOT-23	$V_{OS} = 3\mu\text{V}$ Max, Rail-to-Rail Output