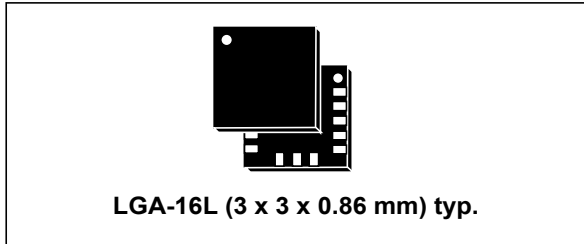


## iNEMO inertial module: always-on 3D accelerometer and 3D gyroscope

Datasheet - production data



### Features

- Power consumption: 0.9 mA in combo normal mode and 1.25 mA in combo high-performance mode up to 1.6 kHz.
- “Always-on” experience with low power consumption for both accelerometer and gyroscope
- Smart FIFO up to 8 kbyte based on features set
- Compliant with Android K and L
- $\pm 2/\pm 4/\pm 8/\pm 16$  g full scale
- $\pm 125/\pm 245/\pm 500/\pm 1000/\pm 2000$  dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- Independent IOs supply (1.62 V)
- Compact footprint, 3 mm x 3 mm x 0.86 mm
- SPI/I<sup>2</sup>C serial interface with main processor data synchronization feature
- Embedded temperature sensor
- ECOPACK<sup>®</sup>, RoHS and “Green” compliant

### Applications

- Pedometer, step detector and step counter
- Significant motion and tilt functions
- Indoor navigation
- Tap and double-tap detection
- IoT and connected devices
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

### Description

The LSM6DS33 is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope performing at 1.25 mA (up to 1.6 kHz ODR) in high-performance mode and enabling always-on low-power features for an optimal motion experience for the consumer.

The LSM6DS33 supports main OS requirements, offering real, virtual and batch sensors with 8 kbyte for dynamic data batching.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DS33 has a full-scale acceleration range of  $\pm 2/\pm 4/\pm 8/\pm 16$  g and an angular rate range of  $\pm 125/\pm 245/\pm 500/\pm 1000/\pm 2000$  dps.

High robustness to mechanical shock makes the LSM6DS33 the preferred choice of system designers for the creation and manufacturing of reliable products.

The LSM6DS33 is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packing
LSM6DS33	-40 to +85	LGA-16L (3 x 3 x 0.86 mm)	Tray
LSM6DS33TR	-40 to +85		Tape & Reel

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# 1 Overview

The LSM6DS33 is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The integrated power-efficient modes are able to reduce the power consumption down to 1.25 mA in high-performance mode, combining always-on low-power features with superior sensing precision for an optimal motion experience for the consumer thanks to ultra-low noise performance for both the gyroscope and accelerometer.

The LSM6DS33 delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers and consumers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, tap and double-tap sensing, activity or inactivity, and wakeup events.

The LSM6DS33 supports main OS requirements, offering real, virtual and batch mode sensors. In addition, the LSM6DS33 can efficiently run the sensor-related features specified in Android, saving power and enabling faster reaction time. In particular, the LSM6DS33 has been designed to implement hardware features such as significant motion, tilt, pedometer functions, and time stamping.

Up to 8 kbyte of FIFO with dynamic allocation of significant data (i.e. sensors, temperature, step counter and time stamp) allows overall power saving of the system.

Like the entire portfolio of MEMS sensor modules, the LSM6DS33 leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DS33 is available in a small plastic land grid array (LGA) package of 3 x 3 x 0.86 mm to address ultra-compact solutions.

## 2 Embedded low-power features

The LSM6DS33 has been designed to be fully compliant with Android, featuring the following on-chip functions:

- 8 kbyte data buffering
  - 100% efficiency with flexible configurations and partitioning
  - possibility to store time stamp
- Event-detection interrupts (fully configurable):
  - free-fall
  - wakeup
  - 6D orientation
  - tap and double-tap sensing
  - activity / inactivity recognition
- Specific IP blocks with negligible power consumption and high-performance:
  - pedometer functions: step detector and step counters
  - tilt (Android compliant, refer to [Section 2.1: Tilt detection](#) for additional info)
  - significant motion (Android compliant)

### 2.1 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve both the targets of ultra-low power consumption and robustness during the short duration of dynamic accelerations.

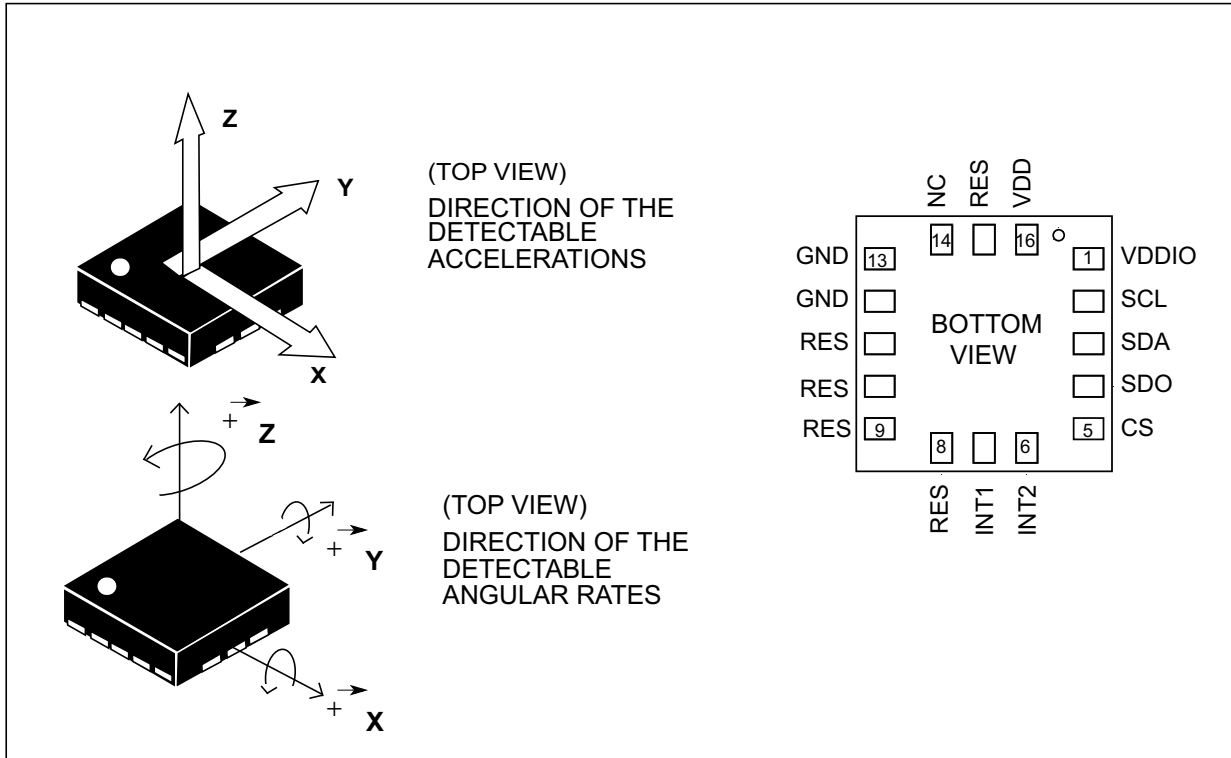
It is based on a trigger of an event each time the device's tilt changes by an angle greater than 35 degrees from the start position.

The tilt function can be used with different scenarios, for example:

- a) Trigger when phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting;
- b) Doesn't trigger when phone is in a front pants pocket and the user is walking, running or going upstairs.

### 3 Pin description

Figure 1. Pin connections



In the LSM6DS33 an I<sup>2</sup>C slave interface or SPI (3- and 4-wire) serial interface is available.

Table 2. Pin description

Pin#	Name	Function
1	VDDIO <sup>(1)</sup>	Power supply for I/O pins
2	SCL	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
3	SDA	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO/SA0	SPI 4-wire interface serial data output (SDO) I <sup>2</sup> C least significant bit of the device address (SA0)
5	CS	I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
6	INT2	Programmable interrupt
7	INT1	Programmable interrupt
8	RES	Reserved, connect to GND
9	RES	Reserved, connect to GND
10	RES	Reserved, connect to GND
11	RES	Reserved, connect to GND
12	GND	0 V supply
13	GND	0 V supply
14	NC	Leave unconnected
15	RES	Reserved, connect to GND
16	VDD <sup>(2)</sup>	Power supply

1. Recommended 100 nF filter capacitor.

2. Recommended 100 nF capacitor.

## 4 Module specifications

### 4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 3. Mechanical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		g
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±245		
				±500		
				±1000		
				±2000		
LA_So	Linear acceleration sensitivity	FS = ±2		0.061		mg/LSB
		FS = ±4		0.122		
		FS = ±8		0.244		
		FS = ±16		0.488		
G_So	Angular rate sensitivity	FS = ±125		4.375		mdps/LSB
		FS = ±245		8.75		
		FS = ±500		17.50		
		FS = ±1000		35		
		FS = ±2000		70		
LA_SoDr	Linear acceleration sensitivity change vs. temperature <sup>(2)</sup>	from -40° to +85° delta from T=25°		±1		%
G_SoDr	Angular rate sensitivity change vs. temperature <sup>(2)</sup>	from -40° to +85° delta from T=25°		±1.5		%
LA_TyOff	Linear acceleration typical zero-g level offset accuracy <sup>(3)</sup>			±40		mg
G_TyOff	Angular rate typical zero-rate level <sup>(3)</sup>			±10		dps
LA_OffDr	Linear acceleration zero-g level change vs. temperature <sup>(2)</sup>			±0.5		mg/°C
G_OffDr	Angular rate typical zero-rate level change vs. temperature <sup>(2)</sup>			±0.05		dps/°C
Rn	Rate noise density			7		mdps/√Hz
An	Acceleration noise density	FS= ±2 g ODR = 104 Hz		90		μg/√Hz

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_ODR	Linear acceleration output data rate			13		Hz
				26		
				52		
				104		
				208		
				416		
				833		
				1666		
				3332		
				6664		
G_ODR	Angular rate output data rate			13		Hz
				26		
				52		
				104		
				208		
				416		
				833		
				1666		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Measurements are performed in a uniform temperature setup.
3. Values after soldering.



## 4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vdd	Supply voltage		1.71	1.8	3.6	V
Vdd_IO	Power supply for I/O		1.62		Vdd+0.1	V
IddHP	Gyroscope and accelerometer in high-performance mode	up to ODR = 1.6 kHz		1.25		mA
IddNM	Gyroscope and accelerometer in normal mode	ODR = 208 Hz		0.9		mA
IddLP	Gyroscope and accelerometer in low-power mode	ODR = 13 Hz		0.42		mA
LA_IddHP	Accelerometer current consumption in high-performance mode	up to ODR = 1.6 kHz		240		μA
LA_IddNM	Accelerometer current consumption in normal mode	ODR = 104 Hz		70		μA
LA_IddLM	Accelerometer current consumption in low-power mode	ODR = 13 Hz		24		μA
IddPD	Gyroscope and accelerometer in power down			6		μA
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

For details related to the LSM6DS33 operating modes, refer to [5.2: Gyroscope power modes](#) and [5.3: Accelerometer power modes](#).

## 4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

**Table 5. Temperature sensor characteristics**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
TODR	Temperature refresh rate			52		Hz
Toff	Temperature offset <sup>(2)</sup>		-15		+15	°C
TSen	Temperature sensitivity			16		LSB/°C
TST	Temperature stabilization time <sup>(3)</sup>				500	µs
T_ADC_res	Temperature ADC resolution			12		bit
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. Time from power ON bit to valid data based on characterization data.

## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

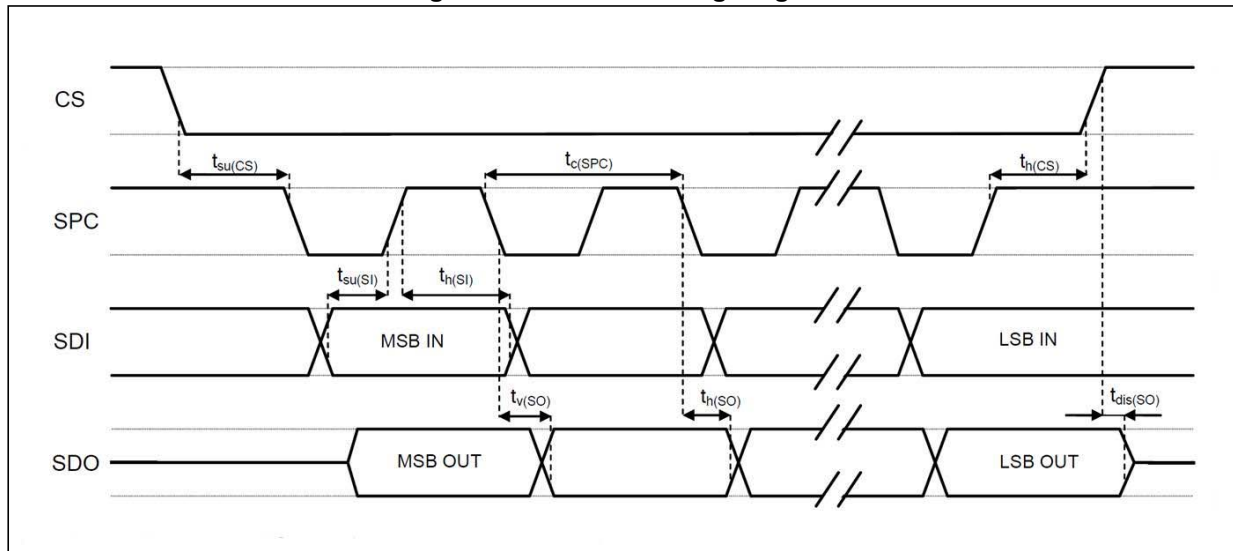
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 2. SPI slave timing diagram



Note: Measurement points are done at  $0.2 \cdot V_{dd\_IO}$  and  $0.8 \cdot V_{dd\_IO}$ , for both input and output ports.

### 4.4.2 I<sup>2</sup>C - inter-IC control interface

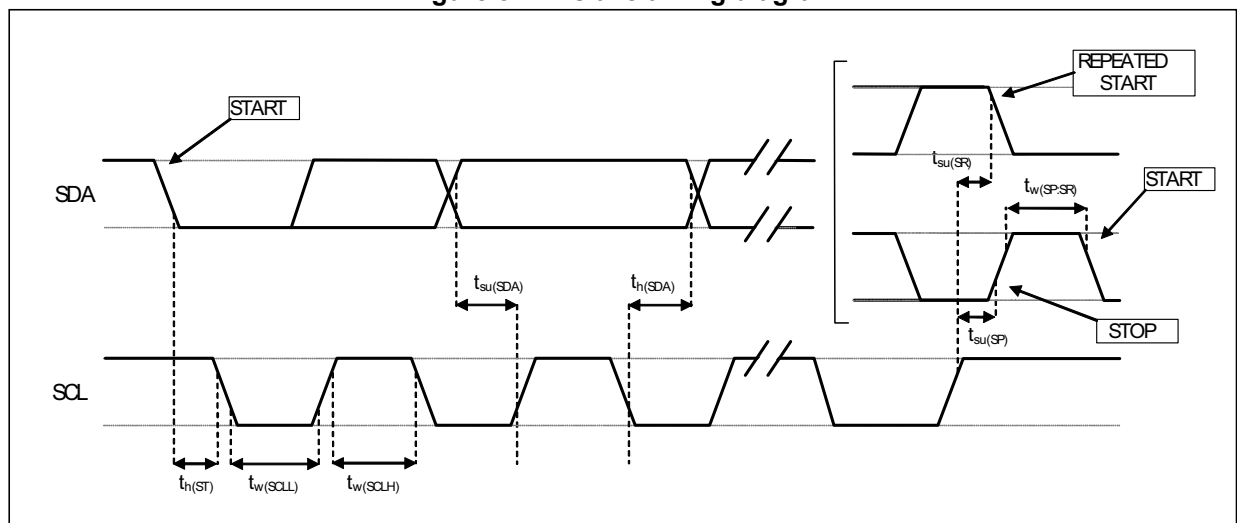
Subject to general operating conditions for Vdd and Top.

Table 7. I<sup>2</sup>C slave timing values

Symbol	Parameter	I <sup>2</sup> C Standard mode <sup>(1)</sup>		I <sup>2</sup> C Fast mode <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
f <sub>(SCL)</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>w(SCLL)</sub>	SCL clock low time	4.7		1.3		
t <sub>w(SCLH)</sub>	SCL clock high time	4.0		0.6		μs
t <sub>su(SDA)</sub>	SDA setup time	250		100		ns
t <sub>h(SDA)</sub>	SDA data hold time	0	3.45	0	0.9	μs
t <sub>h(ST)</sub>	START condition hold time	4		0.6		μs
t <sub>su(SR)</sub>	Repeated START condition setup time	4.7		0.6		
t <sub>su(SP)</sub>	STOP condition setup time	4		0.6		
t <sub>w(SP:SR)</sub>	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

Figure 3. I<sup>2</sup>C slave timing diagram



Note: Measurement points are done at 0.2·Vdd<sub>IO</sub> and 0.8·Vdd<sub>IO</sub>, for both ports.

## 4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	g
ESD	Electrostatic discharge protection (HBM)	2	kV
V <sub>in</sub>	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	0.3 to Vdd_IO +0.3	V

*Note:* Supply Voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so,  $\pm 1$  *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

### 4.6.2 Zero-g and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in [Table 3](#). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

## 5 Functionality

### 5.1 Operating modes

The LSM6DS33 has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power down by writing ODR\_XL[3:0] in [CTRL1\\_XL \(10h\)](#) while the gyroscope is activated from power-down by writing ODR\_G[3:0] in [CTRL2\\_G \(11h\)](#). For combo mode the ODRs are totally independent.

### 5.2 Gyroscope power modes

In the LSM6DS33, the gyroscope can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the G\_HM\_MODE bit in [CTRL7\\_G \(16h\)](#). If G\_HM\_MODE is set to '0', high-performance mode is valid for all ODRs (from 13 Hz up to 1.6 kHz).

To enable the low-power and normal mode, the G\_HM\_MODE bit has to be set to '1'. Low-power mode is available for lower ODR (13, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

### 5.3 Accelerometer power modes

In the LSM6DS33, the accelerometer can be configured in four different operating modes: power-down, low-power, normal mode and high-performance mode. The operating mode selected depends on the value of the XL\_HM\_MODE bit in [CTRL6\\_C \(15h\)](#). If XL\_HM\_MODE is set to '0', high-performance mode is valid for all ODRs (from 13 Hz up to 6.66 kHz).

To enable the low-power and normal mode, the XL\_HM\_MODE bit has to be set to '1'. Low-power mode is available for lower ODRs (13, 26, 52 Hz) while normal mode is available for ODRs equal to 104 and 208 Hz.

### 5.4 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

LSM6DS33 embeds 8 kbytes data FIFO to store the following data:

- gyroscope
- accelerometer
- step counter and time stamp
- temperature

Writing data in the FIFO can be configured to be triggered by the:

- accelerometer/gyroscope data-ready signal; in which case the ODR must be lower than or equal to both the accelerometer and gyroscope ODRs;
- step detection signal.

In addition, each data can be stored at a decimated data rate compared to FIFO ODR and it is configurable by the user, setting the registers *FIFO\_CTRL3 (08h)* and *FIFO\_CTRL4 (09h)*. The available decimation factors are 2, 3, 4, 8, 16, 32.

Programmable FIFO threshold can be set in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)* using the FTH [11:0] bits.

To monitor the FIFO status, dedicated registers (*FIFO\_STATUS1 (3Ah)*, *FIFO\_STATUS2 (3Bh)*, *FIFO\_STATUS3 (3Ch)*, *FIFO\_STATUS4 (3Dh)*) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO threshold status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pads of these status events, the configuration can be set in *INT1\_CTRL (0Dh)* and *INT2\_CTRL (0Eh)*.

FIFO buffer can be configured according to five different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode

Each mode is selected by the FIFO\_MODE\_[2:0] in *FIFO\_CTRL5 (0Ah)* register. To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

#### 5.4.1 Bypass mode

In Bypass mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

#### 5.4.2 FIFO mode

In FIFO mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 001) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, Bypass mode should be selected by writing *FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0]) to '001'.

FIFO buffer memorizes up to 4096 samples of 16 bits each but the depth of the FIFO can be resized by setting the FTH [11:0] bits in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*. If the STOP\_ON\_FTH bit in *CTRL4\_C (13h)* is set to '1', FIFO depth is limited up to FTH [11:0] bits in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*.

#### 5.4.3 Continuous mode

Continuous mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 110) provides a continuous FIFO update: as new data arrives, the older data is discarded.



A FIFO threshold flag *FIFO\_STATUS2 (3Bh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*(FTH [11:0]).

It is possible to route *FIFO\_STATUS2 (3Bh)* (FTH) to the INT1 pin by writing in register *INT1\_CTRL (0Dh)* (INT1\_FTH) = '1' or to the INT2 pin by writing in register *INT2\_CTRL (0Eh)* (INT2\_FTH) = '1'.

A full-flag interrupt can be enabled, *INT1\_CTRL (0Dh)* (INT\_FULL\_FLAG) = '1', in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the OVER\_RUN flag in *FIFO\_STATUS2 (3Bh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO\_STATUS1 (3Ah)* and *FIFO\_STATUS2 (3Bh)* (DIFF\_FIFO[11:0]).

#### 5.4.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = 011), FIFO behavior changes according to the trigger event detected in one of the following interrupt registers *FUNC\_SRC (53h)*, *TAP\_SRC (1Ch)*, *WAKE\_UP\_SRC (1Bh)* and *D6D\_SRC (1Dh)*.

When the selected trigger bit is equal to '1', FIFO operates in FIFO mode.

When the selected trigger bit is equal to '0', FIFO operates in Continuous mode.

#### 5.4.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO\_CTRL5 (0Ah)* (FIFO\_MODE\_[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when selected triggers in one of the following interrupt registers *FUNC\_SRC (53h)*, *TAP\_SRC (1Ch)*, *WAKE\_UP\_SRC (1Bh)* and *D6D\_SRC (1Dh)* are equal to '1', otherwise FIFO content is reset (Bypass mode).

#### 5.4.6 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers (*FIFO\_DATA\_OUT\_L (3Eh)* and *FIFO\_DATA\_OUT\_H (3Fh)*) and each FIFO sample is composed of 16 bits.

All FIFO status registers (*FIFO\_STATUS1 (3Ah)*, *FIFO\_STATUS2 (3Bh)*, *FIFO\_STATUS3 (3Ch)*, *FIFO\_STATUS4 (3Dh)*) can be read at the start of a reading operation, minimizing the intervention of the application processor.

Saving data in the FIFO buffer is organized in four FIFO data sets consisting of 6 bytes each:

The 1<sup>st</sup> FIFO data set is reserved for gyroscope data;

The 2<sup>nd</sup> FIFO data set is reserved for accelerometer data;

5.4.7 Filter block diagrams

Figure 4. Accelerometer chain

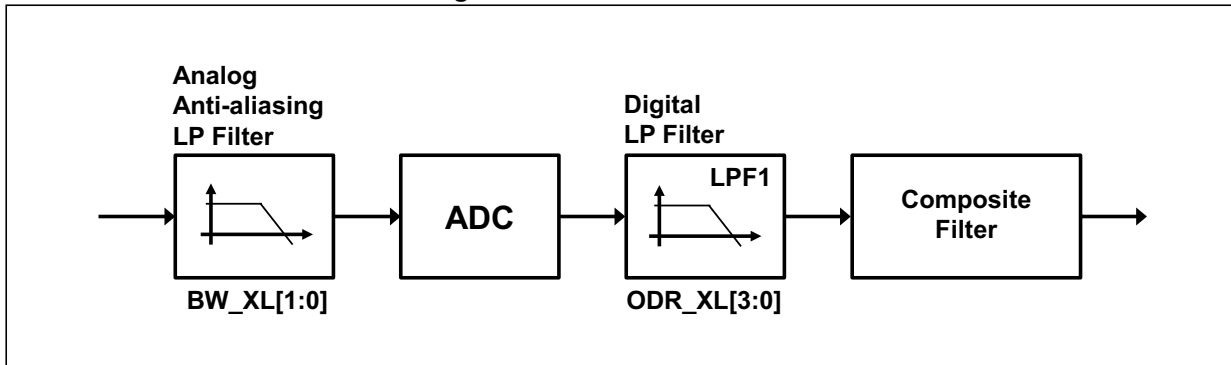


Figure 5. Accelerometer composite filter

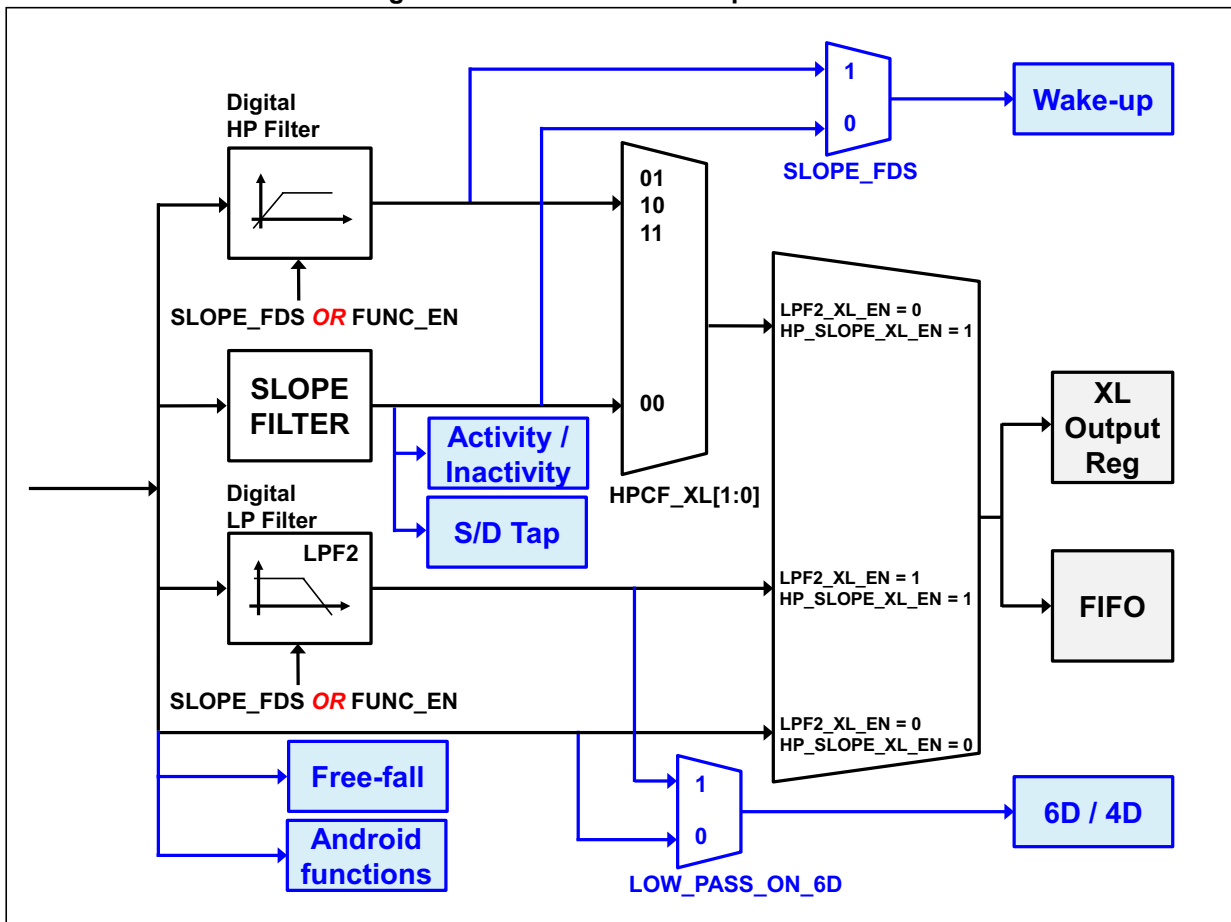
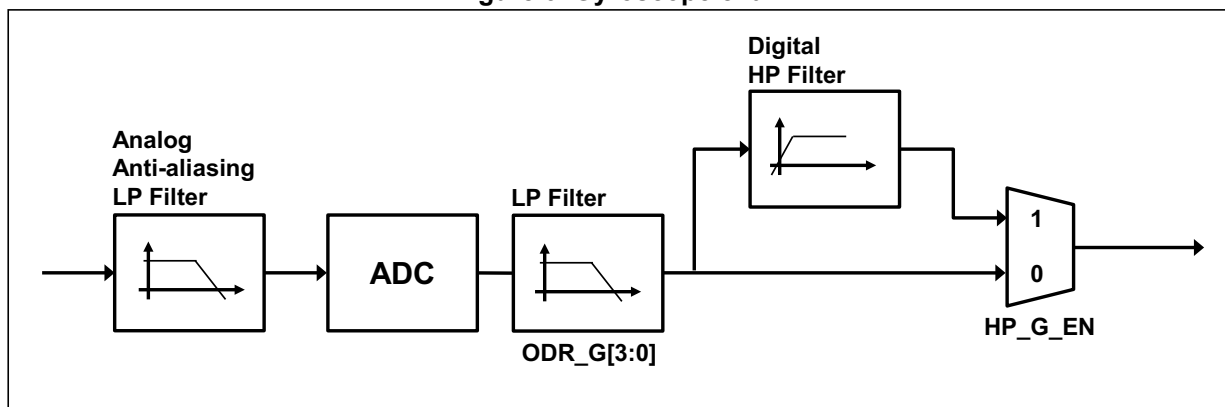


Figure 6. Gyroscope chain



## 6 Digital interfaces

The registers embedded inside the LSM6DS33 may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e connected to Vdd\_IO).

**Table 9. Serial interface pin description**

Pin name	Pin description
CS	SPI enable I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
SCL/SPC	I <sup>2</sup> C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I <sup>2</sup> C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I <sup>2</sup> C less significant bit of the device address

### 6.1 I<sup>2</sup>C serial interface

The LSM6DS33 I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data to the registers, whose content can also be read back.

The relevant I<sup>2</sup>C terminology is provided in the table below.

**Table 10. I<sup>2</sup>C terminology**

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the Serial DATA line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is implemented with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the standard mode.

In order to disable the I<sup>2</sup>C block, (I2C\_disable) = 1 must be written in [CTRL4\\_C \(13h\)](#).

### 6.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LSM6DS33 is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is '1' (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101010b). This solution permits to connect and address two different inertial modules to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LSM6DS33 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The increment of the address is configured by the *CTRL3\_C (12h)* (IF\_INC).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 11. SAD+Read/Write patterns**

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

**Table 12. Transfer when master is writing one byte to slave**

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

**Table 13. Transfer when master is writing multiple bytes to slave**

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

**Table 14. Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

**Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

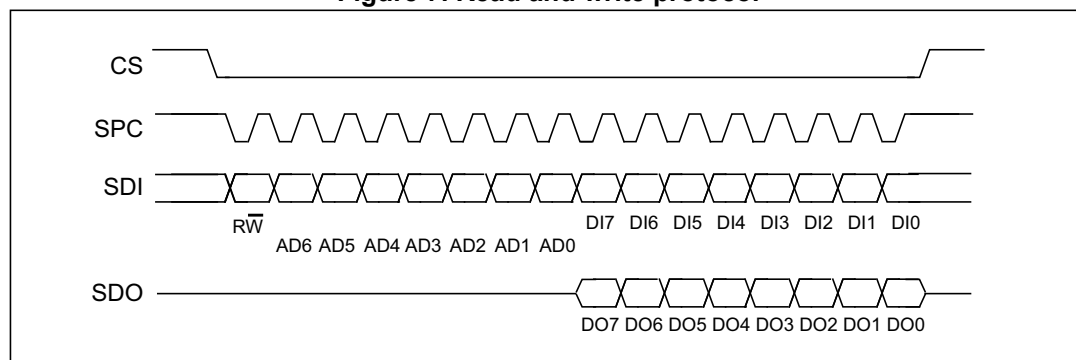
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

## 6.2 SPI bus interface

The LSM6DS33 SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface communicates to the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 7. Read and write protocol**



**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data  $DI(7:0)$  is written into the device. When 1, the data  $DO(7:0)$  from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

**bit 1-7:** address  $AD(6:0)$ . This is the address field of the indexed register.

**bit 8-15:** data  $DI(7:0)$  (write mode). This is the data that is written into the device (MSb first).

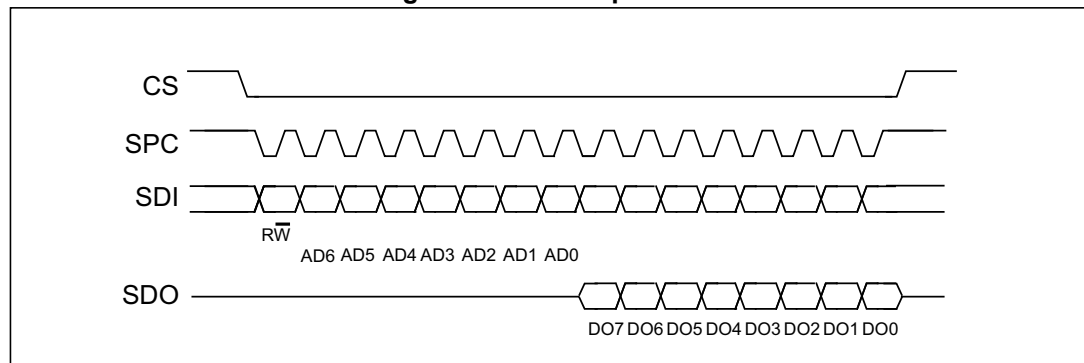
**bit 8-15:** data  $DO(7:0)$  (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the [CTRL3\\_C \(12h\)](#) (IF\_INC) bit is '0', the address used to read/write data remains the same for every block. When the [CTRL3\\_C \(12h\)](#) (IF\_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 6.2.1 SPI read

Figure 8. SPI read protocol



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

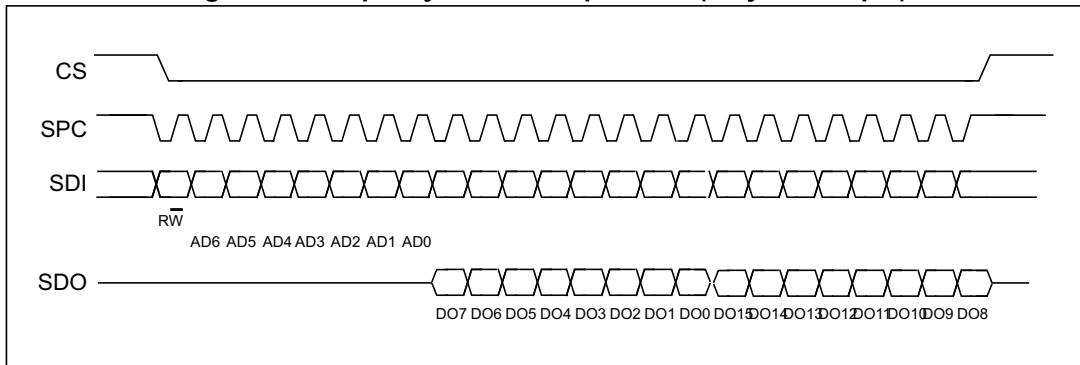
**bit 0:** READ bit. The value is 1.

**bit 1-7:** address  $AD(6:0)$ . This is the address field of the indexed register.

**bit 8-15:** data  $DO(7:0)$  (read mode). This is the data that will be read from the device (MSb first).

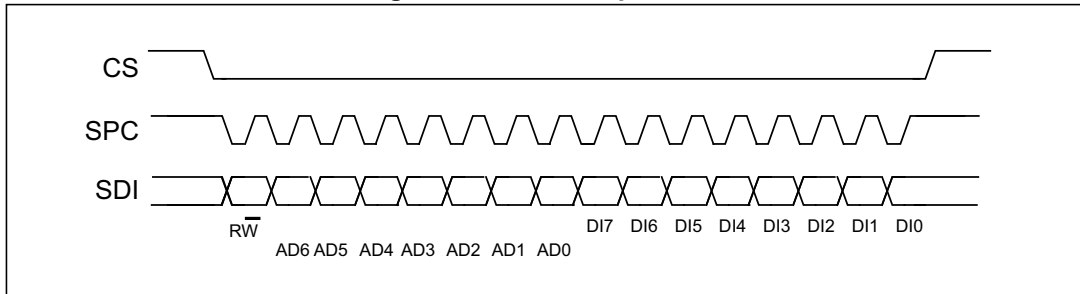
**bit 16-...:** data  $DO(...-8)$ . Further data in multiple byte reads.

Figure 9. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 10. SPI write protocol



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

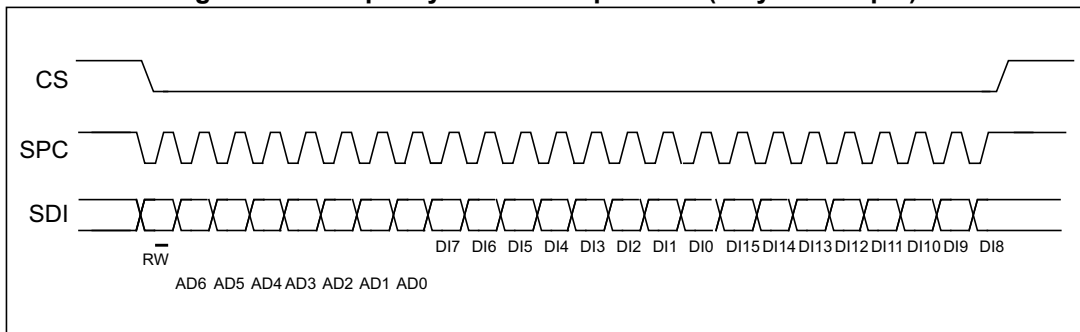
**bit 0:** WRITE bit. The value is 0.

**bit 1 -7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

Figure 11. Multiple byte SPI write protocol (2-byte example)

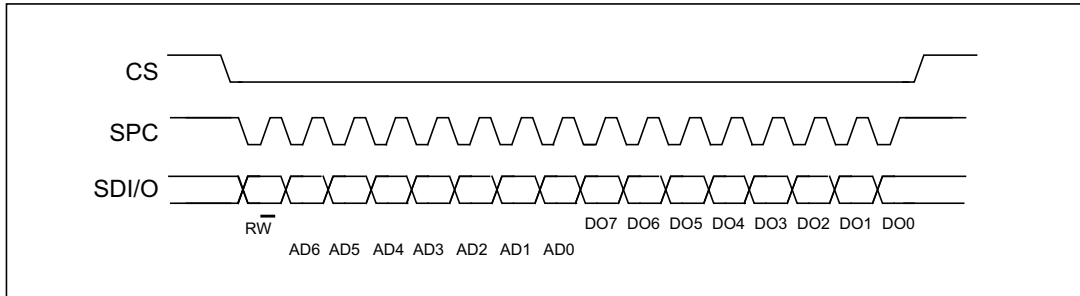




### 6.2.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting the *CTRL3\_C (12h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 12. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

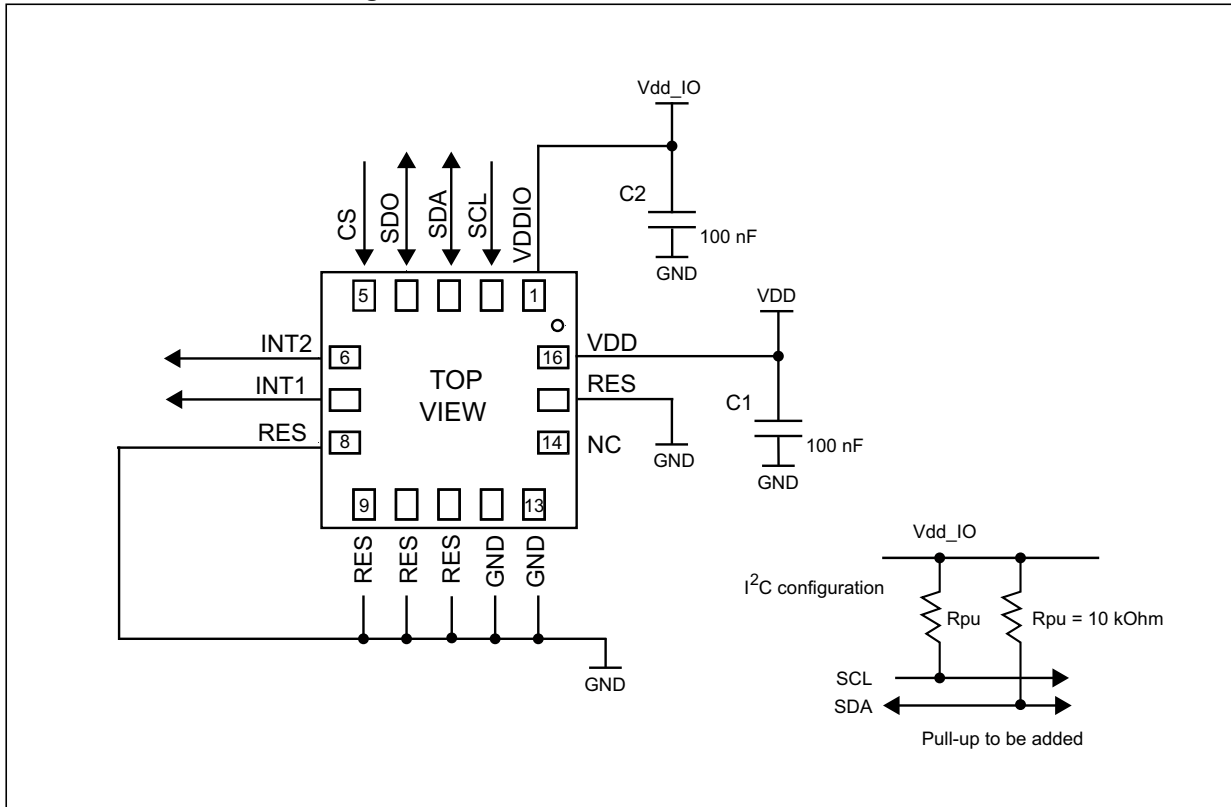
**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 7 Application hints

### 7.1 LSM6DS33 electrical connections

Figure 13. LSM6DS33 electrical connections



The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C interface.

## 7.2 Pin compatibility with LSM6DS0

Figure 14. Schematic 1 (pin 15 connected to GND)

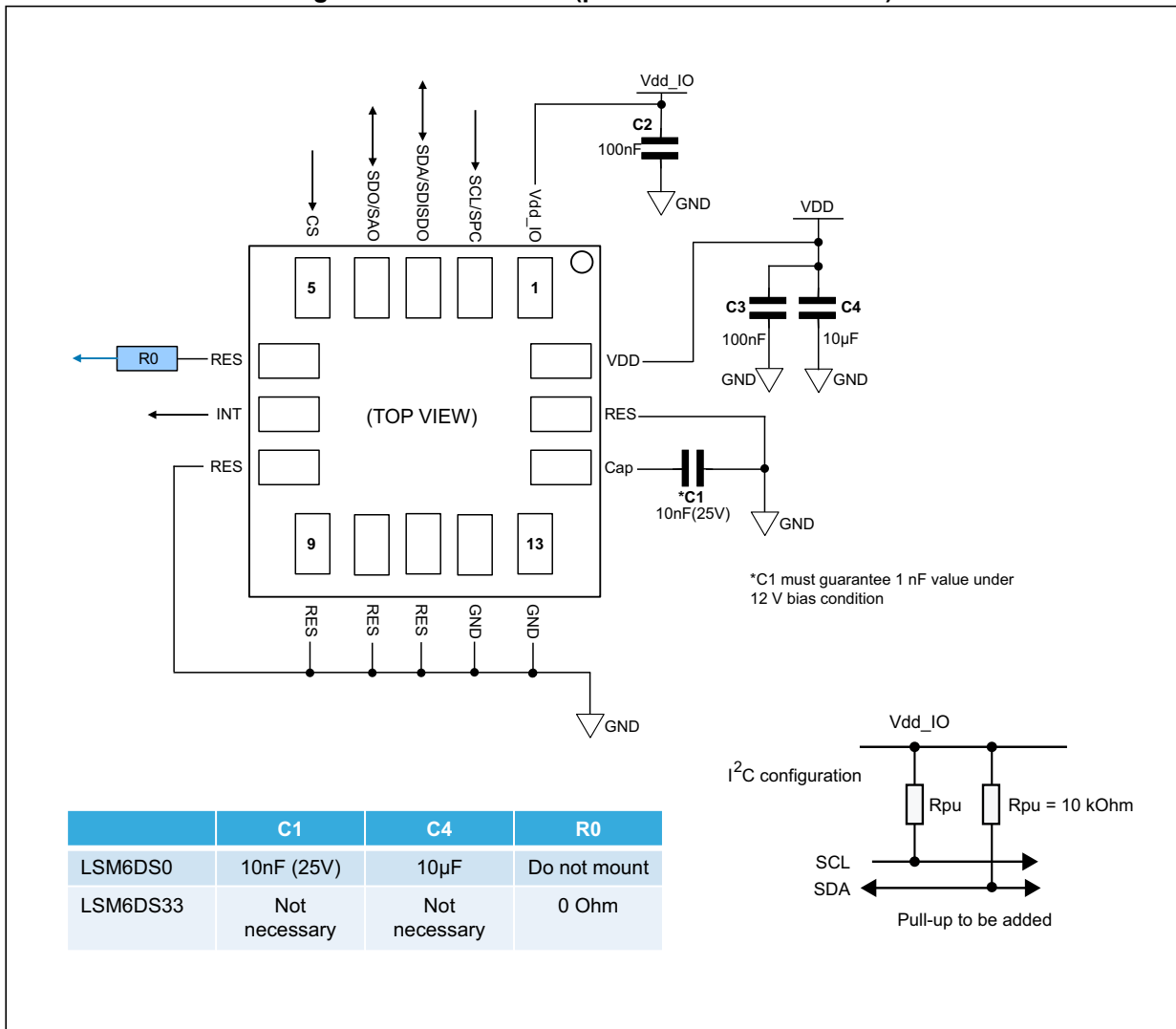
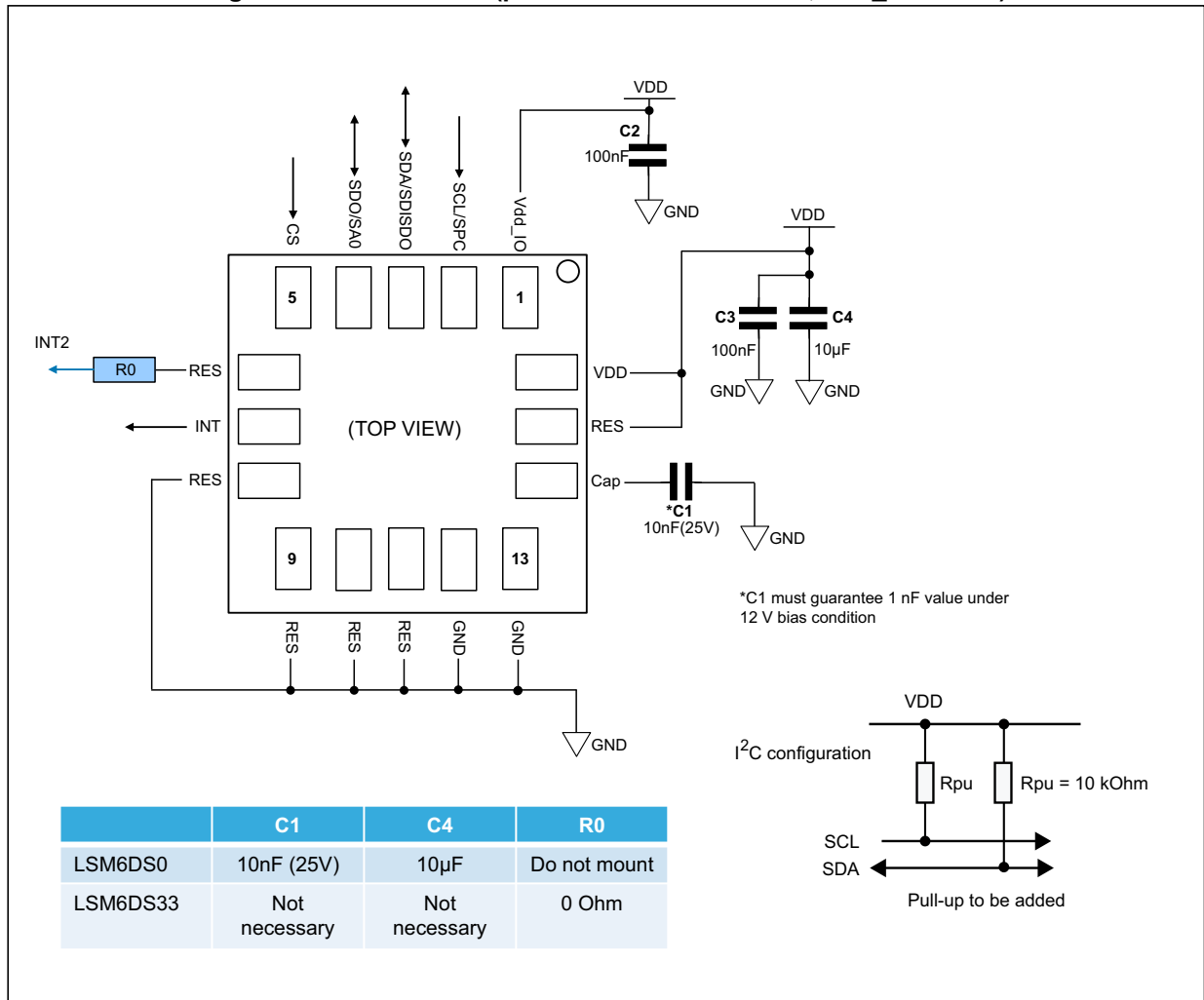


Figure 15. Schematic 2 (pin 15 connected to VDD, Vdd\_IO = VDD)



## 8 Register mapping

The table given below provides a list of the 8/16 bit registers embedded in the device and the corresponding addresses.

**Table 16. Registers address map**

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	r/w	00	00000000	00000000	Reserved
FUNC_CFG_ACCESS	r/w	01	00000001	00000000	Embedded functions configuration register
RESERVED	r/w	02-05		-	Reserved
FIFO_CTRL1	r/w	06	00000110	00000000	FIFO configuration registers
FIFO_CTRL2	r/w	07	00000111	00000000	
FIFO_CTRL3	r/w	08	00001000	00000000	
FIFO_CTRL4	r/w	09	00001001	00000000	
FIFO_CTRL5	r/w	0A	00001010	00000000	
ORIENT_CFG_G	r/w	0B	00001011	00000000	
RESERVED	r/w	0C	00001100	-	Reserved
INT1_CTRL	r/w	0D	00001101	00000000	INT1 pin control
INT2_CTRL	r/w	0E	00001110	00000000	INT2 pin control
WHO_AM_I	r	0F	00001111	01101001	Who I am ID
CTRL1_XL	r/w	10	00010000	00000000	Accelerometer and gyroscope control registers
CTRL2_G	r/w	11	00010001	00000000	
CTRL3_C	r/w	12	00010010	00000100	
CTRL4_C	r/w	13	00010011	00000000	
CTRL5_C	r/w	14	00010100	00000000	
CTRL6_C	r/w	15	00010101	00000000	
CTRL7_G	r/w	16	00010110	00000000	
CTRL8_XL	r/w	17	0001 0111	00000000	
CTRL9_XL	r/w	18	00011000	00111000	
CTRL10_C	r/w	19	00011001	00111000	
RESERVED		1A	00011010	-	Reserved
WAKE_UP_SRC	r	1B	00011011	output	Interrupts registers
TAP_SRC	r	1C	00011100	output	
D6D_SRC	r	1D	00011101	output	

Table 16. Registers address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
STATUS_REG	r	1E	00011110	output	Status data register
RESERVED	r	1F	00011111	-	Reserved
OUT_TEMP_L	r	20	00100000	output	Temperature output data register
OUT_TEMP_H	r	21	00100001	output	
OUTX_L_G	r	22	00100010	output	Gyroscope output register
OUTX_H_G	r	23	00100011	output	
OUTY_L_G	r	24	00100100	output	
OUTY_H_G	r	25	00100101	output	
OUTZ_L_G	r	26	00100110	output	
OUTZ_H_G	r	27	00100111	output	
OUTX_L_XL	r	28	00101000	output	Accelerometer output register
OUTX_H_XL	r	29	00101001	output	
OUTY_L_XL	r	2A	00101010	output	
OUTY_H_XL	r	2B	00101011	output	
OUTZ_L_XL	r	2C	00101100	output	
OUTZ_H_XL	r	2D	00101101	output	
RESERVED		2E-39		-	Reserved
FIFO_STATUS1	r	3A	00111010	output	FIFO status registers
FIFO_STATUS2	r	3B	00111011	output	
FIFO_STATUS3	r	3C	00111100	output	
FIFO_STATUS4	r	3D	00111101	output	
FIFO_DATA_OUT_L	r	3E	00111110	output	FIFO data output registers
FIFO_DATA_OUT_H	r	3F	00111111	output	
TIMESTAMP0_REG	r	40	01000000	output	Timestamp output registers
TIMESTAMP1_REG	r	41	01000001	output	
TIMESTAMP2_REG	r/w	42	01000010	output	
RESERVED		43-48		-	Reserved
STEP_TIMESTAMP_L	r	49	0100 1001	output	Step counter timestamp registers
STEP_TIMESTAMP_H	r	4A	0100 1010	output	
STEP_COUNTER_L	r	4B	01001011	output	Step counter output registers
STEP_COUNTER_H	r	4C	01001100	output	
RESERVED		4D-52		-	Reserved

Table 16. Registers address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
FUNC_SRC	r	53	01010011	output	Interrupt register
RESERVED		54-57		-	Reserved
TAP_CFG	r/w	58	01011000	00000000	Interrupt registers
TAP_THS_6D	r/w	59	01011001	00000000	
INT_DUR2	r/w	5A	01011010	00000000	
WAKE_UP_THS	r/w	5B	01011011	00000000	
WAKE_UP_DUR	r/w	5C	01011100	00000000	
FREE_FALL	r/w	5D	01011101	00000000	
MD1_CFG	r/w	5E	01011110	00000000	
MD2_CFG	r/w	5F	01011111	00000000	
RESERVED		60-6B		-	Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

### 9.1 FUNC\_CFG\_ACCESS (01h)

Enable embedded functions register (r/w).

**Table 17. FUNC\_CFG\_ACCESS register**

FUNC_CFG_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 18. FUNC\_CFG\_ACCESS register description**

FUNC_CFG_EN	Enable access to the embedded functions configuration registers <sup>(1)</sup> from address 02h to 32h. Default value: 0. (0: disable access to embedded functions configuration registers; 1: enable access to embedded functions configuration registers)
-------------	---

1. The embedded functions configuration registers details are available in [10: Embedded functions register mapping](#) and [11: Embedded functions registers description](#).

### 9.2 FIFO\_CTRL1 (06h)

FIFO control register (r/w).

**Table 19. FIFO\_CTRL1 register**

FTH_7	FTH_6	FTH_5	FTH_4	FTH_3	FTH_2	FTH_1	FTH_0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 20. FIFO\_CTRL1 register description**

FTH_[7:0]	FIFO threshold level setting <sup>(1)</sup> . Default value: 0000 0000. Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level. Minimum resolution for the FIFO is 1 LSB = 2 bytes (1 word) in FIFO
-----------	---

1. For a complete watermark threshold configuration, consider FTH\_[11:8] in [FIFO\\_CTRL2 \(07h\)](#).

### 9.3 FIFO\_CTRL2 (07h)

FIFO control register (r/w).

**Table 21. FIFO\_CTRL2 register**

TIMER_PEDO_FIF0_EN	TIMER_PEDO_FIF0_DRDY	0 <sup>(1)</sup>	0 <sup>(1)</sup>	FTH_11	FTH10	FTH_9	FTH_8
--------------------	----------------------	------------------	------------------	--------	-------	-------	-------

1. This bit must be set to '0' for the correct operation of the device.



**Table 22. FIFO\_CTRL2 register description**

TIMER_PEDO_FIF0_EN	Enable pedometer step counter and time stamp. Default: 0 (0: disable step counter and time stamp data; 1: enable step counter and time stamp data.)
TIMER_PEDO_FIF0_DRDY	FIFO write mode. Default: 0 (0: enable write in FIFO based on XL/Gyro data-ready; 1: enable write in FIFO at every step detected by step counter.)
FTH_[11:8]	FIFO threshold level setting <sup>(1)</sup> . Default value: 0000 Watermark flag rises when the number of bytes written to FIFO after the next write is greater than or equal to the threshold level. Minimum resolution for the FIFO is 1LSB = 2 bytes (1 word) in FIFO

1. For a complete watermark threshold configuration, consider FTH\_[11:8] in [FIFO\\_CTRL1 \(06h\)](#)

## 9.4 FIFO\_CTRL3 (08h)

FIFO control register (r/w).

**Table 23. FIFO\_CTRL3 register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	DEC_FIF0_GYRO2	DEC_FIF0_GYRO1	DEC_FIF0_GYRO0	DEC_FIF0_XL2	DEC_FIF0_XL1	DEC_FIF0_XL0
------------------	------------------	----------------	----------------	----------------	--------------	--------------	--------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 24. FIFO\_CTRL3 register description**

DEC_FIF0_GYRO [2:0]	Gyro FIFO (first data set) decimation setting. Default: 000 For the configuration setting, refer to <a href="#">Table 25</a> .
DEC_FIF0_XL [2:0]	Accelerometer FIFO (second data set) decimation setting. Default: 000 For the configuration setting, refer to <a href="#">Table 26</a> .

**Table 25. Gyro FIFO decimation setting**

DEC_FIF0_GYRO [2:0]	Configuration
000	Gyro sensor not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

**Table 26. Accelerometer FIFO decimation setting**

DEC_FIFO_XL [2:0]	Configuration
000	Accelerometer sensor not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

## 9.5 FIFO\_CTRL4 (09h)

FIFO control register (r/w).

**Table 27. FIFO\_CTRL4 register**

0 <sup>(1)</sup>	ONLY_HIGH_DATA	TIMER_PEDO_DEC_FIFO2	TIMER_PEDO_DEC_FIFO1	TIMER_PEDO_DEC_FIFO1	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
------------------	----------------	----------------------	----------------------	----------------------	------------------	------------------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 28. FIFO\_CTRL4 register description**

ONLY_HIGH_DATA	8-bit data storage in FIFO. Default: 0 (0: disable MSByte only memorization in FIFO for XL and Gyro; 1: enable MSByte only memorization in FIFO for XL and Gyro in FIFO)
TIMER_PEDO_DEC_FIFO[2:0]	Third FIFO data set decimation setting. Default: 000 For the configuration setting, refer to <a href="#">Table 29</a> . These bits are used when the bit TIMER_PEDO_FIFO_EN is set to '1' in <a href="#">FIFO_CTRL2 (07h)</a>

**Table 29. Third FIFO data set decimation setting**

TIMER_PEDO_DEC_FIFO[2:0]	Configuration
000	Third FIFO data set not in FIFO
001	No decimation
010	Decimation with factor 2
011	Decimation with factor 3
100	Decimation with factor 4
101	Decimation with factor 8
110	Decimation with factor 16
111	Decimation with factor 32

## 9.6 FIFO\_CTRL5 (0Ah)

FIFO control register (r/w).

**Table 30. FIFO\_CTRL5 register**

0 <sup>(1)</sup>	ODR_FIFO_3	ODR_FIFO_2	ODR_FIFO_1	ODR_FIFO_0	FIFO_MODE_2	FIFO_MODE_1	FIFO_MODE_0
------------------	------------	------------	------------	------------	-------------	-------------	-------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 31. FIFO\_CTRL5 register description**

ODR_FIFO_[3:0]	FIFO ODR selection, setting FIFO_MODE also. Default: 0000 For the configuration setting, refer to <a href="#">Table 32</a>
FIFO_MODE_[2:0]	FIFO mode selection bits, setting ODR_FIFO also. Default value: 000 For the configuration setting refer to <a href="#">Table 33</a>

**Table 32. FIFO ODR selection**

ODR_FIFO_[3:0]	Configuration <sup>(1)</sup>
0000	FIFO disabled
0001	FIFO ODR is set to 13 Hz
0010	FIFO ODR is set to 26 Hz
0011	FIFO ODR is set to 52 Hz
0100	FIFO ODR is set to 104 Hz
0101	FIFO ODR is set to 208 Hz
0110	FIFO ODR is set to 416 Hz
0111	FIFO ODR is set to 833 Hz
1000	FIFO ODR is set to 1.66 kHz
1001	FIFO ODR is set to 3.33 kHz
1010	FIFO ODR is set to 6.66 kHz

1. If the device is working at an ODR slower than the one selected, FIFO ODR is limited to that ODR value. Moreover, these bits are effective if the TIMER\_PEDO\_FIFO\_DRDY bit of [FIFO\\_CTRL2 \(07h\)](#) is set to 0.

**Table 33. FIFO mode selection**

FIFO_MODE_[2:0]	Configuration mode
000	Bypass mode. FIFO disabled.
001	FIFO mode. Stops collecting data when FIFO is full.
010	Reserved
011	Continuous mode until trigger is deasserted, then FIFO mode.
100	Bypass mode until trigger is deasserted, then Continuous mode.
101	Reserved
110	Continuous mode. If the FIFO is full, the new sample overwrites the older one.
111	Reserved

## 9.7 ORIENT\_CFG\_G (0Bh)

Angular rate sensor sign and orientation register (r/w).

**Table 34. ORIENT\_CFG\_G register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	SignX_G	SignY_G	SignZ_G	Orient_2	Orient_1	Orient_0
------------------	------------------	---------	---------	---------	----------	----------	----------

1. This bit must be set to '0' for the correct operation of the device.

**Table 35. ORIENT\_CFG\_G register description**

SignX_G	Pitch axis (X) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignY_G	Roll axis (Y) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
SignZ_G	Yaw axis (Z) angular rate sign. Default value: 0 (0: positive sign; 1: negative sign)
Orient [2:0]	Directional user-orientation selection. Default value: 000 For the configuration setting, refer to <a href="#">Table 36</a> .

**Table 36. Settings for orientation of axes**

Orient [2:0]	000	001	010	011	100	101
Pitch	X	X	Y	Y	Z	Z
Roll	Y	Z	X	Z	X	Y
Yaw	Z	Y	Z	X	Y	X

## 9.8 INT1\_CTRL (0Dh)

INT1 pad control register (r/w).

Each bit in this register enables a signal to be carried through INT1. The pad's output will supply the OR combination of the selected signals.

**Table 37. INT1\_CTRL register**

INT1_ STEP_ DETECTOR	INT1_SIGN _MOT	INT1_FULL _FLAG	INT1_ FIFO_OVR	INT1_ FTH	INT1_ BOOT	INT1_ DRDY_G	INT1_ DRDY_XL
----------------------------	-------------------	--------------------	-------------------	--------------	---------------	-----------------	------------------

**Table 38. INT1\_CTRL register description**

INT1_STEP_DETECTOR	Pedometer step recognition interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_SIGN_MOT	Significant motion interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FULL_FLAG	FIFO full flag interrupt enable on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FIFO_OVR	FIFO overrun interrupt on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FTH	FIFO threshold interrupt on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_BOOT	Boot status available on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_G	Gyroscope Data Ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_XL	Accelerometer Data Ready on INT1 pad. Default value: 0 (0: disabled; 1: enabled)

## 9.9 INT2\_CTRL (0Eh)

INT2 pad control register (r/w).

Each bit in this register enables a signal to be carried through INT2. The pad's output will supply the OR combination of the selected signals.

**Table 39. INT2\_CTRL register**

INT2_STEP_DELTA	INT2_STEP_COUNT_OV	INT2_FULL_FLAG	INT2_FIFO_OVR	INT2_FTH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL
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**Table 40. INT2\_CTRL register description**

INT2_STEP_DELTA	Pedometer step recognition interrupt on delta time <sup>(1)</sup> enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_STEP_COUNT_OV	Step counter overflow interrupt enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_FULL_FLAG	FIFO full flag interrupt enable on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_FIFO_OVR	FIFO overrun interrupt on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_TEMP	Temperature Data Ready in INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_G	Gyroscope Data Ready on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_XL	Accelerometer Data Ready on INT2 pad. Default value: 0 (0: disabled; 1: enabled)

1. Delta time value is defined in register STEP\_COUNT\_DELTA (15h).

## 9.10 WHO\_AM\_I (0Fh)

Who\_AM\_I register (r). This register is a read-only register. Its value is fixed at 69h.

**Table 41. WHO\_AM\_I register**

0	1	1	0	1	0	0	1
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## 9.11 CTRL1\_XL (10h)

Linear acceleration sensor control register 1 (r/w).

**Table 42. CTRL1\_XL register**

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS_XL1	FS_XL0	BW_XL1	BW_XL0
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**Table 43. CTRL1\_XL register description**

ODR_XL [3:0]	Output data rate and power mode selection. Default value: 0000 (see <a href="#">Table 44</a> ).
FS_XL [1:0]	Accelerometer full-scale selection. Default value: 00. (00: $\pm 2$ g; 01: $\pm 16$ g; 10: $\pm 4$ g; 11: $\pm 8$ g)
BW_XL [1:0]	Anti-aliasing filter bandwidth selection. Default value: 00 (00: 400 Hz; 01: 200 Hz; 10: 100 Hz; 11: 50 Hz)

**Table 44. Accelerometer ODR register setting**

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz] when XL_HM_MODE = 1	ODR selection [Hz] when XL_HM_MODE = 0
0	0	0	0	Power-down	Power-down
0	0	0	1	13 Hz (low power)	13 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (normal mode)	104 Hz (high performance)
0	1	0	1	208 Hz (normal mode)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1.66 kHz (high performance)	1.66 kHz (high performance)
1	0	0	1	3.33 kHz (high performance)	3.33 kHz (high performance)
1	0	1	0	6.66 kHz (high performance)	6.66 kHz (high performance)

Table 45. BW and ODR (high-performance mode)

ODR <sup>(1)</sup>	Analog filter BW (XL_HM_MODE = 0)	
	XL_BW_SCAL_ODR = 0	XL_BW_SCAL_ODR = 1
6.66 - 3.33 kHz	Filter not used	Bandwidth is determined by setting BW_XL[1:0] in <a href="#">CTRL1_XL (10h)</a>
1.66 kHz	400 Hz	
833 Hz	400 Hz	
416 Hz	200 Hz	
208 Hz	100 Hz	
104 - 13 Hz	50 Hz	

1. Filter not used when accelerometer is in normal and low-power modes.

## 9.12 CTRL2\_G (11h)

Angular rate sensor control register 2 (r/w).

**Table 46. CTRL2\_G register**

ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS_G1	FS_G0	FS_125	0 <sup>(1)</sup>
--------	--------	--------	--------	-------	-------	--------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 47. CTRL2\_G register description**

ODR_G [3:0]	Gyroscope output data rate selection. Default value: 0000 (Refer to <a href="#">Table 46</a> )
FS_G [1:0]	Gyroscope full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 10: 1000 dps; 11: 2000 dps)
FS_125	Gyroscope full-scale at 125 dps. Default value: 0 (0: disabled; 1: enabled)

**Table 48. Gyroscope ODR configuration setting**

ODR_G3	ODR_G2	ODR_G1	ODR_G0	ODR [Hz] when G_HM_MODE = 1	ODR [Hz] when G_HM_MODE = 0
0	0	0	0	Power down	Power down
0	0	0	1	13 Hz (low power)	13 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (normal mode)	104 Hz (high performance)
0	1	0	1	208 Hz (normal mode)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1.66 kHz (high performance)	1.66 kHz (high performance)



## 9.13 CTRL3\_C (12h)

Control register 3 (r/w).

**Table 49. CTRL3\_C register**

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	BLE	SW_RESET
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**Table 50. CTRL3\_C register description**

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content <sup>(1)</sup> )
BDU	Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pads active high; 1: interrupt output pads active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pads. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I <sup>2</sup> C or SPI). Default value: 1 (0: disabled; 1: enabled)
BLE	Big/Little Endian Data selection. Default value 0 (0: data LSB @ lower address; 1: data MSB @ lower address)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is cleared by hardware after next flash boot.

1. Boot request is executed as soon as internal oscillator is turned on. It is possible to set bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

## 9.14 CTRL4\_C (13h)

Control register 4 (r/w).

**Table 51. CTRL4\_C register**

XL_BW_ SCAL_ODR	SLEEP_G	INT2_on_ INT1	FIFO_ TEMP_EN	DRDY_ MASK	I2C_disable	0	STOP_ON_ _FTH
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**Table 52. CTRL4\_C register description**

XL_BW_ SCAL_ODR	Accelerometer bandwidth selection. Default value: 0 (0 <sup>(1)</sup> : bandwidth determined by ODR selection, refer to <a href="#">Table 45</a> ; 1 <sup>(2)</sup> : bandwidth determined by setting BW_XL[1:0] in <a href="#">CTRL1_XL (10h)</a> register.)
SLEEP_G	Gyroscope sleep mode enable. Default value: 0 (0: disabled; 1: enabled)
INT2_on_INT1	All interrupt signals available on INT1 pad enable. Default value: 0 (0: interrupt signals divided between INT1 and INT2 pads; 1: all interrupt signals in logic or on INT1 pad)
FIFO_TEMP_EN	Enable temperature data as 4 <sup>th</sup> FIFO data set <sup>(3)</sup> . Default: 0 (0: disable temperature data as 4 <sup>th</sup> FIFO data set; 1: enable temperature data as 4 <sup>th</sup> FIFO data set)
DRDY_MASK	Configuration 1 <sup>(4)</sup> data available enable bit. Default value: 0 (0: DA timer disabled; 1: DA timer enabled)
I2C_disable	Disable I <sup>2</sup> C interface. Default value: 0 (0: both I <sup>2</sup> C and SPI enabled; 1: I <sup>2</sup> C disabled, SPI only)
STOP_ON_FTH	Enable FIFO threshold level use. Default value: 0. (0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)

1. Filter used in high-performance mode only with ODR less than 3.33 kHz.
2. Filter used in high-performance mode only.
3. This bit is effective if the TIMER\_PEDO\_FIFO\_EN bit of FIFO\_CTRL2 register is set to 0.
4. In configuration 1, switching to combo mode, data are collected in FIFO only when both accelerometer and gyroscope are set. Switching to accelerometer only, data are collected in FIFO after filter setting.

## 9.15 CTRL5\_C (14h)

Control register 5 (r/w).

**Table 53. CTRL5\_C register**

ROUNDING2	ROUNDING1	ROUNDING0	0 <sup>(1)</sup>	ST1_G	ST0_G	ST1_XL	ST0_XL
-----------	-----------	-----------	------------------	-------	-------	--------	--------

1. This bit must be set to '0' for the correct operation of the device

**Table 54. CTRL5\_C register description**

ROUNDING[2:0]	Circular burst-mode (rounding) read from output registers. Default: 000 (000: no rounding; Others: refer to <a href="#">Table 55</a> )
ST_G [1:0]	Angular rate sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to <a href="#">Table 56</a> )
ST_XL [1:0]	Linear acceleration sensor self-test enable. Default value: 00 (00: Self-test disabled; Other: refer to <a href="#">Table 57</a> )

**Table 55. Output registers rounding pattern**

ROUNDING[2:0]	Rounding pattern
000	No rounding
001	Accelerometer only
010	Gyroscope only
011	Gyroscope + accelerometer

**Table 56. Angular rate sensor self-test mode selection**

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

**Table 57. Linear acceleration sensor self-test mode selection**

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

## 9.16 CTRL6\_C (15h)

Angular rate sensor control register 6 (r/w).

**Table 58. CTRL6\_C register**

TRIG_EN	LVLen	LVL2_EN	XL_HM_MODE	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
---------	-------	---------	------------	------------------	------------------	------------------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 59. CTRL6\_C register description**

TRIG_EN	Gyroscope data edge-sensitive trigger enable. Default value: 0 (0: external trigger disabled; 1: external trigger enabled)
LVLen	Gyroscope data level-sensitive trigger enable. Default value: 0 (0: level-sensitive trigger disabled; 1: level sensitive trigger enabled)
LVL2_EN	Gyroscope level-sensitive latched enable. Default value: 0 (0: level-sensitive latched disabled; 1: level sensitive latched enabled)
XL_HM_MODE	High-performance operating mode disable for accelerometer <sup>(1)</sup> . Default value: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)

1. Normal and low-power mode depends on the ODR setting, for details refer to [Table 44](#).

## 9.17 CTRL7\_G (16h)

Angular rate sensor control register 7 (r/w).

**Table 60. CTRL7\_G register**

G_HM_MODE	HP_G_EN	HPCF_G1	HPCF_G0	HP_G_RST	ROUNDING_STATUS	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-----------	---------	---------	---------	----------	-----------------	------------------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 61. CTRL7\_G register description**

G_HM_MODE	High-performance operating mode disable for gyroscope <sup>(1)</sup> . Default: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
HP_G_EN	Gyroscope high-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled)
HP_G_RST	Gyro digital HP filter reset. Default: 0 (0: gyro digital HP filter reset OFF; 1: gyro digital HP filter reset ON)
ROUNDING_STATUS	Source register rounding function enable on <i>STATUS_REG (1Eh)</i> , <i>FUNC_SRC (53h)</i> and <i>WAKE_UP_SRC (1Bh)</i> registers. Default value: 0 (0: disabled; 1: enabled)
HPCF_G[1:0]	Gyroscope high-pass filter cutoff frequency selection. Default value: 00. Refer to <a href="#">Table 62</a> .

1. Normal and low-power mode depends on the ODR setting, for details refer to [Table 48](#).

**Table 62. Gyroscope high-pass filter mode configuration**

HPCF_G1	HPCF_G0	High-pass filter cutoff frequency
0	0	0.0081 Hz
0	1	0.0324 Hz
1	0	2.07 Hz
1	1	16.32 Hz

## 9.18 CTRL8\_XL (17h)

Linear acceleration sensor control register 8 (r/w).

**Table 63. CTRL8\_XL register**

LPF2_XL_EN	HPCF_XL1	HPCF_XL0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	HP_SLOPE_XL_EN	0 <sup>(1)</sup>	LOW_PASS_ON_6D
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1. This bit must be set to '0' for the correct operation of the device.

**Table 64. CTRL8\_XL register description**

LPF2_XL_EN	Accelerometer low-pass filter LPF2 selection. Refer to <i>Figure 5</i> .
HPCF_XL[1:0]	Accelerometer slope filter and high-pass filter configuration and cutoff setting. Refer to <i>Table 65</i> .
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to <i>Figure 5</i> .
LOW_PASS_ON_6D	Low-pass filter on 6D function selection. Refer to <i>Figure 5</i> .

**Table 65. Accelerometer slope and high-pass filter selection and cutoff frequency**

HPCF_XL[1:0]	Applied filter	HP filter cutoff frequency [Hz]
00	Slope	ODR_XL/50
01	High-pass	ODR_XL/100
10	High-pass	ODR_XL/9
11	High-pass	ODR_XL/400

## 9.19 CTRL9\_XL (18h)

Linear acceleration sensor control register 9 (r/w).

**Table 66. CTRL9\_XL register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	Zen_XL	Yen_XL	Xen_XL	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
------------------	------------------	--------	--------	--------	------------------	------------------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 67. CTRL9\_XL register description**

Zen_XL	Accelerometer Z-axis output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_XL	Accelerometer Y-axis output enable. Default value: 1 (0: Y-axis output disabled; 1: Y-axis output enabled)
Xen_XL	Accelerometer X-axis output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)

## 9.20 CTRL10\_C (19h)

Control register 10 (r/w).

**Table 68. CTRL10\_C register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	Zen_G	Yen_G	Xen_G	FUNC_EN	PEDO_RST_STEP	SIGN_MOTION_EN
------------------	------------------	-------	-------	-------	---------	---------------	----------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 69. CTRL10\_C register description**

Zen_G	Gyroscope yaw axis (Z) output enable. Default value: 1 (0: Z-axis output disabled; 1: Z-axis output enabled)
Yen_G	Gyroscope roll axis (Y) output enable. Default value: 1 (0: Y-axis output disabled; 1: Y axis output enabled)
Xen_G	Gyroscope pitch axis (X) output enable. Default value: 1 (0: X-axis output disabled; 1: X-axis output enabled)
FUNC_EN	Enable embedded functionalities (pedometer, tilt, significant motion) and accelerometer HP and LPF2 filters (refer to <a href="#">Figure 5</a> ). Default value: 0 (0: disable functionalities of embedded functions and accelerometer filters; 1: enable functionalities of embedded functions and accelerometer filters)
PEDO_RST_STEP	Reset pedometer step counter. Default value: 0 (0: disabled; 1: enabled)
SIGN_MOTION_EN	Enable significant motion function. Default value: 0 (0: disabled; 1: enabled)

## 9.21 WAKE\_UP\_SRC (1Bh)

Wake up interrupt source register (r).

**Table 70. WAKE\_UP\_SRC register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	FF_IA	SLEEP_STATE_IA	WU_IA	X_WU	Y_WU	Z_WU
------------------	------------------	-------	----------------	-------	------	------	------

1. This bit must be set to '0' for the correct operation of the device.

**Table 71. WAKE\_UP\_SRC register description**

FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE_IA	Sleep event status. Default value: 0 (0: sleep event not detected; 1: sleep event detected)
WU_IA	Wakeup event detection status. Default value: 0 (0: wakeup event not detected; 1: wakeup event detected.)
X_WU	Wakeup event detection status on X-axis. Default value: 0 (0: wakeup event on X-axis not detected; 1: wakeup event on X-axis detected)
Y_WU	Wakeup event detection status on Y-axis. Default value: 0 (0: wakeup event on Y-axis not detected; 1: wakeup event on Y-axis detected)
Z_WU	Wakeup event detection status on Z-axis. Default value: 0 (0: wakeup event on Z-axis not detected; 1: wakeup event on Z-axis detected)

## 9.22 TAP\_SRC (1Ch)

Tap source register (r).

**Table 72. TAP\_SRC register**

0 <sup>(1)</sup>	TAP_IA	SINGLE_TAP	DOUBLE_TAP	TAP_SIGN	X_TAP	Y_TAP	Z_TAP
------------------	--------	------------	------------	----------	-------	-------	-------

1. This bit must be set to '0' for the correct operation of the device.

**Table 73. TAP\_SRC register description**

TAP_IA	Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected)
SINGLE_TAP	Single-tap event status. Default value: 0 (0: single tap event not detected; 1: single tap event detected)
DOUBLE_TAP	Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected.)
TAP_SIGN	Sign of acceleration detected by tap event. Default: 0 (0: positive sign of acceleration detected by tap event; 1: negative sign of acceleration detected by tap event)
X_TAP	Tap event detection status on X-axis. Default value: 0 (0: tap event on X-axis not detected; 1: tap event on X-axis detected)
Y_TAP	Tap event detection status on Y-axis. Default value: 0 (0: tap event on Y-axis not detected; 1: tap event on Y-axis detected)
Z_TAP	Tap event detection status on Z-axis. Default value: 0 (0: tap event on Z-axis not detected; 1: tap event on Z-axis detected)

## 9.23 D6D\_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (r)

**Table 74. D6D\_SRC register**

0 <sup>(1)</sup>	D6D_IA	ZH	ZL	YH	YL	XH	XL
------------------	--------	----	----	----	----	----	----

1. This bit must be set to '0' for the correct operation of the device.

**Table 75. D6D\_SRC register description**

D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
X_H	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
X_L	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

## 9.24 STATUS\_REG (1Eh)

**Table 76. STATUS\_REG register**

-	-	-	-	EV_BOOT	TDA	GDA	XLDA
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**Table 77. STATUS\_REG register description**

EV_BOOT	Boot running flag signal. Default value: 0 (0: no boot running; 1: boot running)
TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

## 9.25 OUT\_TEMP\_L (20h), OUT\_TEMP(21h)

Temperature data output register (r). L and H registers together express a 16-bit word in two's complement (r).

**Table 78. OUT\_TEMP\_L register**

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 79. OUT\_TEMP\_H register**

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8
--------	--------	--------	--------	--------	--------	-------	-------

**Table 80. OUT\_TEMP register description**

Temp[15:0]	Temperature sensor output data The value is expressed as two's complement sign extended on the MSB.
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## 9.26 OUTX\_L\_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement. (r)

**Table 81. OUTX\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 82. OUTX\_L\_G register description**

D[7:0]	Pitch axis (X) angular rate value (LSbyte)
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### 9.27 OUTX\_H\_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (r). The value is expressed as a 16-bit word in two's complement. (r)

**Table 83. OUTX\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 84. OUTX\_H\_G register description**

D[15:8]	Pitch axis (X) angular rate value (MSbyte)
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### 9.28 OUTY\_L\_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement. (r).

**Table 85. OUTY\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 86. OUTY\_L\_G register description**

D[7:0]	Roll axis (Y) angular rate value (LSbyte)
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### 9.29 OUTY\_H\_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (r). The value is expressed as a 16-bit word in two's complement. (r).

**Table 87. OUTY\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 88. OUTY\_H\_G register description**

D[15:8]	Roll axis (Y) angular rate value (MSbyte)
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### 9.30 OUTZ\_L\_G (26h)

Angular rate sensor yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement. (r).

**Table 89. OUTZ\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 90. OUTZ\_L\_G register description**

D[7:0]	Yaw axis (Z) angular rate value (LSbyte)
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### 9.31 OUTZ\_H\_G (27h)

Angular rate sensor Yaw axis (Z) angular rate output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 91. OUTZ\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 92. OUTZ\_H\_G register description**

D[15:8]	Yaw axis (Z) angular rate value (MSbyte)
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### 9.32 OUTX\_L\_XL (28h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 93. OUTX\_L\_XL register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 94. OUTX\_L\_XL register description**

D[7:0]	X-axis linear acceleration value (LSbyte)
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### 9.33 OUTX\_H\_XL (29h)

Linear acceleration sensor X-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 95. OUTX\_H\_XL register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 96. OUTX\_H\_XL register description**

D[15:8]	X-axis linear acceleration value (MSbyte)
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### 9.34 OUTY\_L\_XL (2Ah)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 97. OUTY\_L\_XL register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 98. OUTY\_L\_XL register description**

D[7:0]	Y-axis linear acceleration value (LSbyte)
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### 9.35 OUTY\_H\_XL (2Bh)

Linear acceleration sensor Y-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 99. OUTY\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 100. OUTY\_H\_G register description**

D[15:8]	Y-axis linear acceleration value (MSbyte)
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### 9.36 OUTZ\_L\_XL (2Ch)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 101. OUTZ\_L\_XL register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 102. OUTZ\_L\_XL register description**

D[7:0]	Z-axis linear acceleration value (LSbyte)
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### 9.37 OUTZ\_H\_XL (2Dh)

Linear acceleration sensor Z-axis output register (r). The value is expressed as a 16-bit word in two's complement.

**Table 103. OUTZ\_H\_XL register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 104. OUTZ\_H\_XL register description**

D[15:8]	Z-axis linear acceleration value (MSbyte)
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### 9.38 FIFO\_STATUS1 (3Ah)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in *CTRL3\_C (12h)* to 1.

**Table 105. FIFO\_STATUS1 register**

DIFF_FIFO_7	DIFF_FIFO_6	DIFF_FIFO_5	DIFF_FIFO_4	DIFF_FIFO_3	DIFF_FIFO_2	DIFF_FIFO_1	DIFF_FIFO_0
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**Table 106. FIFO\_STATUS1 register description**

DIFF_FIFO_[7:0]	Number of unread words (16-bit axes) stored in FIFO <sup>(1)</sup> .
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1. For a complete number of unread samples, consider DIFF\_FIFO [11:8] in *FIFO\_STATUS2 (3Bh)*

### 9.39 FIFO\_STATUS2 (3Bh)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in *CTRL3\_C (12h)* to 1.

**Table 107. FIFO\_STATUS2 register**

FTH	FIFO_OVER_RUN	FIFO_FULL	FIFO_EMPTY	DIFF_FIFO_11	DIFF_FIFO_10	DIFF_FIFO_9	DIFF_FIFO_8
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**Table 108. FIFO\_STATUS2 register description**

FTH	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than watermark level <sup>(1)</sup> ; 1: FIFO filling is equal to or higher than the watermark level)
FIFO_OVER_RUN	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL	FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
FIFO_EMPTY	FIFO empty bit. Default value: 0 (0: FIFO contains data; 1: FIFO is empty)
DIFF_FIFO_[7:0]	Number of unread words (16-bit axes) stored in FIFO <sup>(2)</sup> .

1. FIFO watermark level is set in FTH\_[11:0] in *FIFO\_CTRL1 (06h)* and *FIFO\_CTRL2 (07h)*
2. For a complete number of unread samples, consider DIFF\_FIFO [11:8] in *FIFO\_STATUS1 (3Ah)*

### 9.40 FIFO\_STATUS3 (3Ch)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in *CTRL3\_C (12h)* to 1.

**Table 109. FIFO\_STATUS3 register**

FIFO_PATTERN_7	FIFO_PATTERN_6	FIFO_PATTERN_5	FIFO_PATTERN_4	FIFO_PATTERN_3	FIFO_PATTERN_2	FIFO_PATTERN_1	FIFO_PATTERN_0
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**Table 110. FIFO\_STATUS3 register description**

FIFO_PATTERN_[7:0]	Word of recursive pattern read at the next reading.
--------------------	---

### 9.41 FIFO\_STATUS4 (3Dh)

FIFO status control register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3\\_C \(12h\)](#) to 1.

**Table 111. FIFO\_STATUS4 register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	FIFO_PATTERN_9	FIFO_PATTERN_8
------------------	------------------	------------------	------------------	------------------	------------------	----------------	----------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 112. FIFO\_STATUS4 register description**

FIFO_PATTERN_[9:8]	Word of recursive pattern read at the next reading.
--------------------	---

### 9.42 FIFO\_DATA\_OUT\_L (3Eh)

FIFO data output register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3\\_C \(12h\)](#) to 1.

**Table 113. FIFO\_DATA\_OUT\_L register**

DATA_OUT_FIFO_L_7	DATA_OUT_FIFO_L_6	DATA_OUT_FIFO_L_5	DATA_OUT_FIFO_L_4	DATA_OUT_FIFO_L_3	DATA_OUT_FIFO_L_2	DATA_OUT_FIFO_L_1	DATA_OUT_FIFO_L_0
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**Table 114. FIFO\_DATA\_OUT\_L register description**

DATA_OUT_FIFO_L_[7:0]	FIFO data output (first byte)
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### 9.43 FIFO\_DATA\_OUT\_H (3Fh)

FIFO data output register (r). For a proper reading of the register, it is recommended to set the BDU bit in [CTRL3\\_C \(12h\)](#) to 1.

**Table 115. FIFO\_DATA\_OUT\_H register**

DATA_OUT_FIFO_H_7	DATA_OUT_FIFO_H_6	DATA_OUT_FIFO_H_5	DATA_OUT_FIFO_H_4	DATA_OUT_FIFO_H_3	DATA_OUT_FIFO_H_2	DATA_OUT_FIFO_H_1	DATA_OUT_FIFO_H_0
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**Table 116. FIFO\_DATA\_OUT\_H register description**

DATA_OUT_FIFO_H_[7:0]	FIFO data output (second byte)
-----------------------	--------------------------------

## 9.44 TIMESTAMP0\_REG (40h)

Time stamp first byte data output register (r). The value is expressed as a 24-bit word and the bit resolution is defined by setting the value in [WAKE\\_UP\\_DUR \(5Ch\)](#).

**Table 117. TIMESTAMP0\_REG register**

TIMESTA MP0_7	TIMESTA MP0_6	TIMESTA MP0_5	TIMESTA MP0_4	TIMESTA MP0_3	TIMESTA MP0_2	TIMESTA MP0_1	TIMESTA MP0_0
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

**Table 118. TIMESTAMP0\_REG register description**

TIMESTAMP0_[7:0]	TIMESTAMP first byte data output
------------------	----------------------------------

## 9.45 TIMESTAMP1\_REG (41h)

Time stamp second byte data output register (r). The value is expressed as a 24-bit word and the bit resolution is defined by setting value in [WAKE\\_UP\\_DUR \(5Ch\)](#).

**Table 119. TIMESTAMP1\_REG register**

TIMESTA MP1_7	TIMESTA MP1_6	TIMESTA MP1_5	TIMESTA MP1_4	TIMESTA MP1_3	TIMESTA MP1_2	TIMESTA MP1_1	TIMESTA MP1_0
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

**Table 120. TIMESTAMP1\_REG register description**

TIMESTAMP1_[7:0]	TIMESTAMP second byte data output
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## 9.46 TIMESTAMP2\_REG (42h)

Time stamp third byte data output register (r/w). The value is expressed as a 24-bit word and the bit resolution is defined by setting the value in [WAKE\\_UP\\_DUR \(5Ch\)](#). To reset the timer, the AAh value has to be stored in this register.

**Table 121. TIMESTAMP2\_REG register**

TIMESTA MP2_7	TIMESTA MP2_6	TIMESTA MP2_5	TIMESTA MP2_4	TIMESTA MP2_3	TIMESTA MP2_2	TIMESTA MP2_1	TIMESTA MP2_0
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

**Table 122. TIMESTAMP2\_REG register description**

TIMESTAMP2_[7:0]	TIMESTAMP third byte data output
------------------	----------------------------------

## 9.47 STEP\_TIMESTAMP\_L (49h)

Step counter timestamp information register (r). When a step is detected, the value of TIMESTAMP\_REG1 register is copied in STEP\_TIMESTAMP\_L.

**Table 123. STEP\_TIMESTAMP\_L register**

STEP_ TIMESTA MP_L_7	STEP_ TIMESTA MP_L_6	STEP_ TIMESTA MP_L_5	STEP_ TIMESTA MP_L_4	STEP_ TIMESTA MP_L_3	STEP_ TIMESTA MP_L_2	STEP_ TIMESTA MP_L_1	STEP_ TIMESTA MP_L_0
----------------------------	----------------------------	----------------------------	----------------------------	----------------------------	----------------------------	----------------------------	----------------------------

**Table 124. STEP\_TIMESTAMP\_L register description**

STEP_TIMESTAMP_L[7:0]	Timestamp of last step detected.
-----------------------	----------------------------------

### 9.48 STEP\_TIMESTAMP\_H (4Ah)

Step counter timestamp information register (r). When a step is detected, the value of TIMESTAMP\_REG2 register is copied in STEP\_TIMESTAMP\_H.

**Table 125. STEP\_TIMESTAMP\_H register**

STEP_TIMESTAMP_H_7	STEP_TIMESTAMP_H_6	STEP_TIMESTAMP_H_5	STEP_TIMESTAMP_H_4	STEP_TIMESTAMP_H_3	STEP_TIMESTAMP_H_2	STEP_TIMESTAMP_H_1	STEP_TIMESTAMP_H_0
--------------------	--------------------	--------------------	--------------------	--------------------	--------------------	--------------------	--------------------

**Table 126. STEP\_TIMESTAMP\_H register description**

STEP_TIMESTAMP_H[7:0]	Timestamp of last step detected.
-----------------------	----------------------------------

### 9.49 STEP\_COUNTER\_L (4Bh)

Step counter output register (r).

**Table 127. STEP\_COUNTER\_L register**

STEP_COUNTER_L_7	STEP_COUNTER_L_6	STEP_COUNTER_L_5	STEP_COUNTER_L_4	STEP_COUNTER_L_3	STEP_COUNTER_L_2	STEP_COUNTER_L_1	STEP_COUNTER_L_0
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

**Table 128. STEP\_COUNTER\_L register description**

STEP_COUNTER_L[7:0]	Step counter output (LSbyte)
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### 9.50 STEP\_COUNTER\_H (4Ch)

Step counter output register (r).

**Table 129. STEP\_COUNTER\_H register**

STEP_COUNTER_H_7	STEP_COUNTER_H_6	STEP_COUNTER_H_5	STEP_COUNTER_H_4	STEP_COUNTER_H_3	STEP_COUNTER_H_2	STEP_COUNTER_H_1	STEP_COUNTER_H_0
------------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

**Table 130. STEP\_COUNTER\_H register description**

STEP_COUNTER_H[7:0]	Step counter output (MSbyte)
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### 9.51 FUNC\_SRC (53h)

Significant motion, tilt, step detector interrupt source register (r).

**Table 131. FUNC\_SRC register**

STEP_COUNT_DELTA_IA	SIGN_MOTION_IA	TILT_IA	STEP_DETECTED	STEP_OVERFLOW	0	0	0
---------------------	----------------	---------	---------------	---------------	---	---	---

**Table 132. FUNC\_SRC register description**

STEP_COUNT_DELTA_IA	Pedometer step recognition on delta time status. Default value: 0 (0: no step recognized during delta time; 1: at least one step recognized during delta time)
SIGN_MOTION_IA	Significant motion event detection status. Default value: 0 (0: significant motion event not detected; 1: significant motion event detected)
TILT_IA	Tilt event detection status. Default value: 0 (0: tilt event not detected; 1: tilt event detected)
STEP_DETECTED	Step detector event detection status. Default value: 0 (0: step detector event not detected; 1: step detector event detected)
STEP_OVERFLOW	Step counter overflow status. Default value: 0 (0: step counter value < 2 <sup>16</sup> ; 1: step counter value reached 2 <sup>16</sup> )

## 9.52 TAP\_CFG (58h)

Time stamp, pedometer, tilt, filtering, and tap recognition functions configuration register (r/w).

**Table 133. TAP\_CFG register**

TIMER_EN	PEDO_EN	TILT_EN	SLOPE_FDS	TAP_X_EN	TAP_Y_EN	TAP_Z_EN	LIR
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**Table 134. TAP\_CFG register description**

TIMER_EN	Time stamp count enable, output data are collected in <i>TIMESTAMP0_REG (40h)</i> , <i>TIMESTAMP1_REG (41h)</i> , <i>TIMESTAMP2_REG (42h)</i> register. Default: 0 (0: time stamp count disabled; 1: time stamp count enabled)
PEDO_EN	Pedometer algorithm enable. Default value: 0 (0: pedometer algorithm disabled; 1: pedometer algorithm enabled)
TILT_EN	Tilt calculation enable. Default value: 0 (0: tilt calculation disabled; 1: tilt calculation enabled.)
SLOPE_FDS	Enable accelerometer HP and LPF2 filters (refer to <i>Figure 5</i> ). Default value: 0 (0: disable; 1: enable)
TAP_X_EN	Enable X direction in tap recognition. Default value: 0 (0: X direction disabled; 1:X direction enabled)
TAP_Y_EN	Enable Y direction in tap recognition. Default value: 0 (0: Y direction disabled; 1:Y direction enabled)
TAP_Z_EN	Enable Z direction in tap recognition. Default value: 0 (0: Z direction disabled; 1:Z direction enabled)
LIR	Latched Interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)



### 9.53 TAP\_THS\_6D (59h)

Portrait/landscape position and tap function threshold register (r/w).

**Table 135. TAP\_THS\_6D register**

D4D_EN	SIXD_THS 1	SIXD_THS 0	TAP_THS 4	TAP_THS 3	TAP_THS 2	TAP_THS 1	TAP_THS 0
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**Table 136. TAP\_THS\_6D register description**

D4D_EN	4D orientation detection enable (Z-axis position detection is disabled). Default value: 0 (0: disabled; 1: enabled)
SIXD_THS[1:0]	Threshold for D6D function. Default value: 00 For details, refer to <a href="#">Table 137</a> .
TAP_THS[4:0]	Threshold for tap recognition. Default value: 00000

**Table 137. Threshold for D4D/D6D function**

SIXD_THS[1:0]	Threshold value
00	80 degrees
01	70 degrees
10	60 degrees
11	50 degrees

### 9.54 INT\_DUR2 (5Ah)

Tap recognition function setting register (r/w).

**Table 138. INT\_DUR2 register**

DUR3	DUR2	DUR1	DUR0	QUIET1	QUIET0	SHOCK1	SHOCK0
------	------	------	------	--------	--------	--------	--------

**Table 139. INT\_DUR2 register description**

DUR[3:0]	Duration of maximum time gap for double tap recognition. Default: 0000 When double tap recognition is enabled, this register expresses the maximum time between two consecutive detected taps to determine a double tap event. The default value of these bits is 0000b which corresponds to 16*ODR_XL time. If DUR[3:0] bits are set to a different value, 1LSB corresponds to 32*ODR_XL time.
QUIET[1:0]	Expected quiet time after a tap detection. Default value: 00 Quiet time is the time after the first detected tap in which there must not be any overthreshold event. The default value of these bits is 00b which corresponds to 2*ODR_time. If QUIET[1:0] bits are set to a different value, 1LSB corresponds to 4*ODR_time.
SHOCK[1:0]	Maximum duration of overthreshold event. Default value: 00 Maximum duration is the maximum time of an overthreshold signal detection to be recognized as a tap event. The default value of these bits is 00b which corresponds to 4*ODR_time. If SHOCK[1:0] bits are set to a different value, 1LSB corresponds to 8*ODR_time.

## 9.55 WAKE\_UP\_THS (5Bh)

Single and double-tap function threshold register (r/w).

**Table 140. WAKE\_UP\_THS register**

SINGLE_ DOUBLE_ _TAP	INACTIVITY	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0
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**Table 141. WAKE\_UP\_THS register description**

SINGLE_DOUBLE_TAP	Single/double-tap event enable. Default: 0 (0: only single-tap event enabled; 1: both single and double-tap events enabled)
INACTIVITY	Inactivity event enable. Default value: 0 (0: sleep disabled; 1: sleep enabled)
WK_THS[5:0]	Threshold for wakeup. Default value: 000000

## 9.56 WAKE\_UP\_DUR (5Ch)

Free-fall, wakeup, time stamp and sleep mode functions duration setting register (r/w).

**Table 142. WAKE\_UP\_DUR register**

FF_DUR5	WAKE_ DUR1	WAKE_ DUR0	TIMER_ HR	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0
---------	------------	------------	-----------	-------------	-------------	-------------	-------------

**Table 143. WAKE\_UP\_DUR register description**

FF_DUR5	Free fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in <a href="#">FREE_FALL (5Dh)</a> configuration.
WAKE_DUR[1:0]	Wake up duration event. Default: 00 1LSB = 1 ODR_time
TIMER_HR	Time stamp register resolution setting <sup>(1)</sup> . Default value: 0 (0: 1LSB = 6.4 ms; 1: 1LSB = 25 μs)
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 1 LSB = 512 ODR

1. Configuration of this bit affects [TIMESTAMP0\\_REG \(40h\)](#), [TIMESTAMP1\\_REG \(41h\)](#), [TIMESTAMP2\\_REG \(42h\)](#), [STEP\\_TIMESTAMP\\_L \(49h\)](#), [STEP\\_TIMESTAMP\\_H \(4Ah\)](#), and [STEP\\_COUNT\\_DELTA \(15h\)](#) registers.

### 9.57 FREE\_FALL (5Dh)

Free-fall function duration setting register (r/w).

**Table 144. FREE\_FALL register**

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0
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**Table 145. FREE\_FALL register description**

FF_DUR[4:0]	Free-fall duration event. Default: 0 For the complete configuration of the free fall duration, refer to FF_DUR5 in <a href="#">WAKE_UP_DUR (5Ch)</a> configuration
FF_THS[2:0]	Free fall threshold setting. Default: 000 For details refer to <a href="#">Table 146</a> .

**Table 146. Threshold for free-fall function**

FF_THS[2:0]	Threshold value
000	156 mg
001	219 mg
010	250 mg
011	312 mg
100	344 mg
101	406 mg
110	469 mg
111	500 mg

### 9.58 MD1\_CFG (5Eh)

Functions routing on INT1 register (r/w).

**Table 147. MD1\_CFG register**

INT1_INACT_STATE	INT1_SINGLE_TAP	INT1_WU	INT1_FF	INT1_DOUBLE_TAP	INT1_6D	INT1_TILT	INT1_TIMER
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**Table 148. MD1\_CFG register description**

INT1_INACT_STATE	Routing on INT1 of inactivity mode. Default: 0 (0: routing on INT1 of inactivity disabled; 1: routing on INT1 of inactivity enabled)
INT1_SINGLE_TAP	Single-tap recognition routing on INT1. Default: 0 (0: routing of single-tap event on INT1 disabled; 1: routing of single-tap event on INT1 enabled)
INT1_WU	Routing of wakeup event on INT1. Default value: 0 (0: routing of wakeup event on INT1 disabled; 1: routing of wakeup event on INT1 enabled)

**Table 148. MD1\_CFG register description (continued)**

INT1_FF	Routing of free-fall event on INT1. Default value: 0 (0: routing of free-fall event on INT1 disabled; 1: routing of free-fall event on INT1 enabled)
INT1_DOUBLE_TAP	Routing of tap event on INT1. Default value: 0 (0: routing of double-tap event on INT1 disabled; 1: routing of double-tap event on INT1 enabled)
INT1_6D	Routing of 6D event on INT1. Default value: 0 (0: routing of 6D event on INT1 disabled; 1: routing of 6D event on INT1 enabled)
INT1_TILT	Routing of tilt event on INT1. Default value: 0 (0: routing of tilt event on INT1 disabled; 1: routing of tilt event on INT1 enabled)
INT1_TIMER	Routing of end counter event of timer on INT1. Default value: 0 (0: routing of end counter event of timer on INT1 disabled; 1: routing of end counter event of timer event on INT1 enabled)

## 9.59 MD2\_CFG (5Fh)

Functions routing on INT2 register (r/w).

**Table 149. MD2\_CFG register**

INT2_INACT_STATE	INT2_SINGLE_TAP	INT2_WU	INT2_FF	INT2_DOUBLE_TAP	INT2_6D	INT2_TILT	0 <sup>(1)</sup>
------------------	-----------------	---------	---------	-----------------	---------	-----------	------------------

1. This bit must be set to '0' for the correct operation of the device.

**Table 150. MD2\_CFG register description**

INT2_INACT_STATE	Routing on INT2 of inactivity mode. Default: 0 (0: routing on INT2 of inactivity disabled; 1: routing on INT2 of inactivity enabled)
INT2_SINGLE_TAP	Single-tap recognition routing on INT2. Default: 0 (0: routing of single-tap event on INT2 disabled; 1: routing of single-tap event on INT2 enabled)
INT2_WU	Routing of wakeup event on INT2. Default value: 0 (0: routing of wakeup event on INT2 disabled; 1: routing of wake-up event on INT2 enabled)
INT2_FF	Routing of free-fall event on INT2. Default value: 0 (0: routing of free-fall event on INT2 disabled; 1: routing of free-fall event on INT2 enabled)
INT2_DOUBLE_TAP	Routing of tap event on INT2. Default value: 0 (0: routing of double-tap event on INT2 disabled; 1: routing of double-tap event on INT2 enabled)
INT2_6D	Routing of 6D event on INT2. Default value: 0 (0: routing of 6D event on INT2 disabled; 1: routing of 6D event on INT2 enabled)
INT2_TILT	Routing of tilt event on INT2. Default value: 0 (0: routing of tilt event on INT2 disabled; 1: routing of tilt event on INT2 enabled)

## 10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when FUNC\_CFG\_EN is set to '1' in *FUNC\_CFG\_ACCESS (01h)*.

**Table 151. Registers address map - embedded functions**

Name	Type	Register address		Default	Comment
		Hex	Binary		
RESERVED	-	02-0E			Reserved
PEDO_THS_REG	r/w	0F	00001111	00000000	
RESERVED	-	10-12			Reserved
SM_THS	r/w	13	00010011	00000110	
PEDO_DEB_REG	r/w	14	00010100	00000000	
STEP_COUNT_DELTA	r/w	15	0001 0101	00000000	
RESERVED	-	24-32			Reserved

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 11 Embedded functions registers description

## 11.1 PEDO\_THS\_REG (0Fh)

**Table 152. PEDO\_THS\_REG register default values**

PEDO_4G	-	-	THS_MIN4	THS_MIN3	THS_MIN2	THS_MIN1	THS_MIN0
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**Table 153. PEDO\_THS\_REG register description**

PEDO_4G	This bit sets the internal full scale used in pedometer functions. Using this bit, saturation is avoided (e.g. FAST walk). 0: internal full scale = 2 g. 1: internal full scale 4 g (device full_scale @CTRL1_XL must be ≥ 4 g, otherwise internal full scale is 2 g)
THS_MIN[4:0]	Configurable minimum threshold. 1LSB = 16 mg @PEDO_4G=0, 1LSB = 32 mg @PEDO_4G=1

Procedure to modify the pedometer minimum threshold:

- Write reg FUNC\_CFG\_ACCESS (01h) = 80h (Enables access to the embedded functions registers)
- Set min threshold in bits [4:0] of reg 0Fh (1LSB = 16 mg @ FS = 2 g)
- Write reg FUNC\_CFG\_ACCESS (01h) = 00h (Disables access to the embedded functions registers)

*Note:* All modifications of the content of the embedded functions registers have to be performed with the device in power-down mode.

## 11.2 SM\_THS (13h)

Significant motion configuration register (r/w).

**Table 154. SM\_THS register**

SM_THS_7	SM_THS_6	SM_THS_5	SM_THS_4	SM_THS_3	SM_THS_2	SM_THS_1	SM_THS_0
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**Table 155. SM\_THS register description**

SM_THS[7:0]	Significant motion threshold. Default value: 00000110
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### 11.3 PEDO\_DEB\_REG (14h)

**Table 156. PEDO\_DEB\_REG register default values**

DEB_TIME4	DEB_TIME3	DEB_TIME2	DEB_TIME1	DEB_TIME0	DEB_STEP2	DEB_STEP1	DEB_STEP0
0	0	0	0	0	1	1	0

**Table 157. PEDO\_DEB\_REG register description**

DEB_TIME[4:0]	If this time between steps is greater than DEB_TIME*80ms, the debouncer is reactivated
DEB_STEP[2:0]	Minimum number of steps to increment step counter (debouncer)

The procedure to modify the pedometer debounce time is the following:

- Write reg FUNC\_CFG\_ACCESS (01h) = 80h (Enables access to the embedded functions)
- Set debounce time in bits [3:7] of reg 14h (1LSB = 80 ms. This value must be > 0)
- Write reg FUNC\_CFG\_ACCESS (01h) = 00h (Disables access to the embedded functions registers)

*Note:* All modifications of the content of the embedded functions registers have to be performed with the device in power-down mode.

### 11.4 STEP\_COUNT\_DELTA (15h)

Time period register for step detection on delta time (r/w).

**Table 158. STEP\_COUNT\_DELTA register**

SC_DELTA_7	SC_DELTA_6	SC_DELTA_5	SC_DELTA_4	SC_DELTA_3	SC_DELTA_2	SC_DELTA_1	SC_DELTA_0
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**Table 159. STEP\_COUNT\_DELTA register description**

SC_DELTA[7:0]	Time period value <sup>(1)</sup> (1LSB = 1.6384 s)
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1. This value is effective if the TIMER\_EN bit of the TAP\_CFG register is set to 1 and the TIMER\_HR bit of the WAKE\_UP\_DUR register is set to 0.

## 12 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave "Pin 1 Indicator" unconnected during soldering.

Land pattern and soldering recommendations are available at [www.st.com/mems](http://www.st.com/mems).

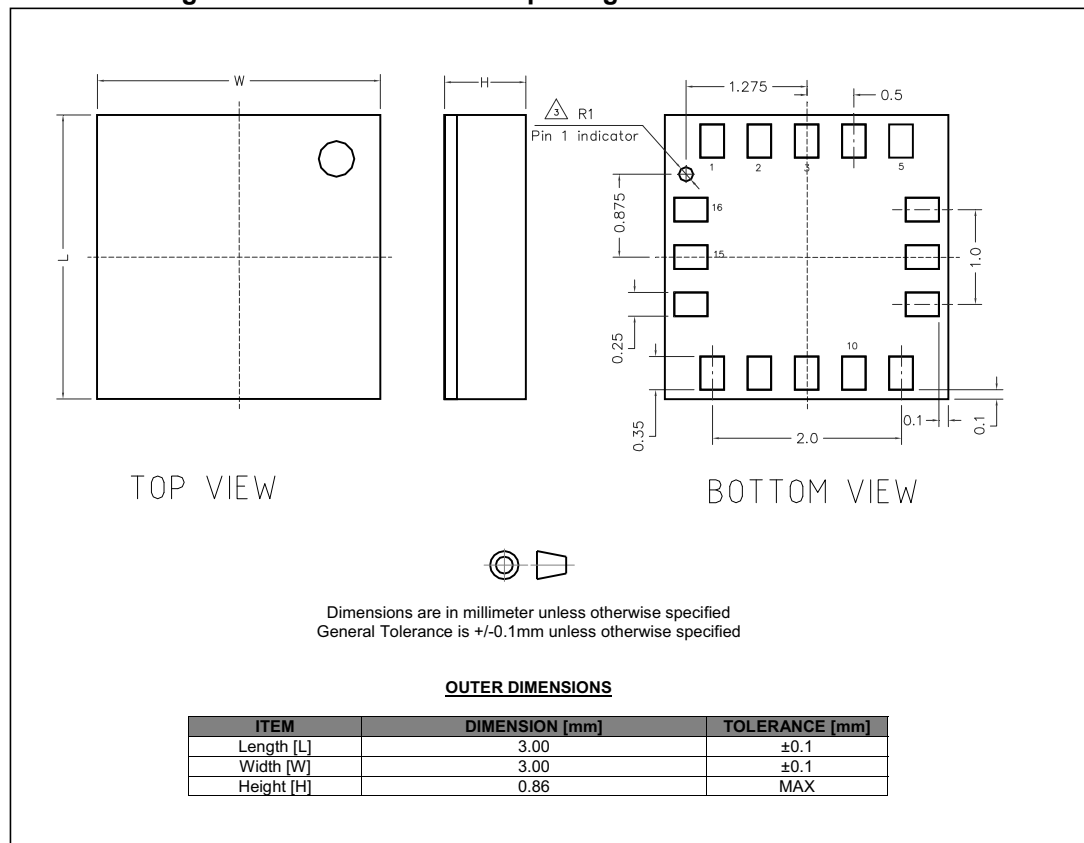


# 13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 13.1 LGA-16 package information

Figure 16. LGA 3x3x0.86 16L package outline and dimensions



### 13.2 LGA-16 packing information

Figure 17. Carrier tape information for LGA-16 package

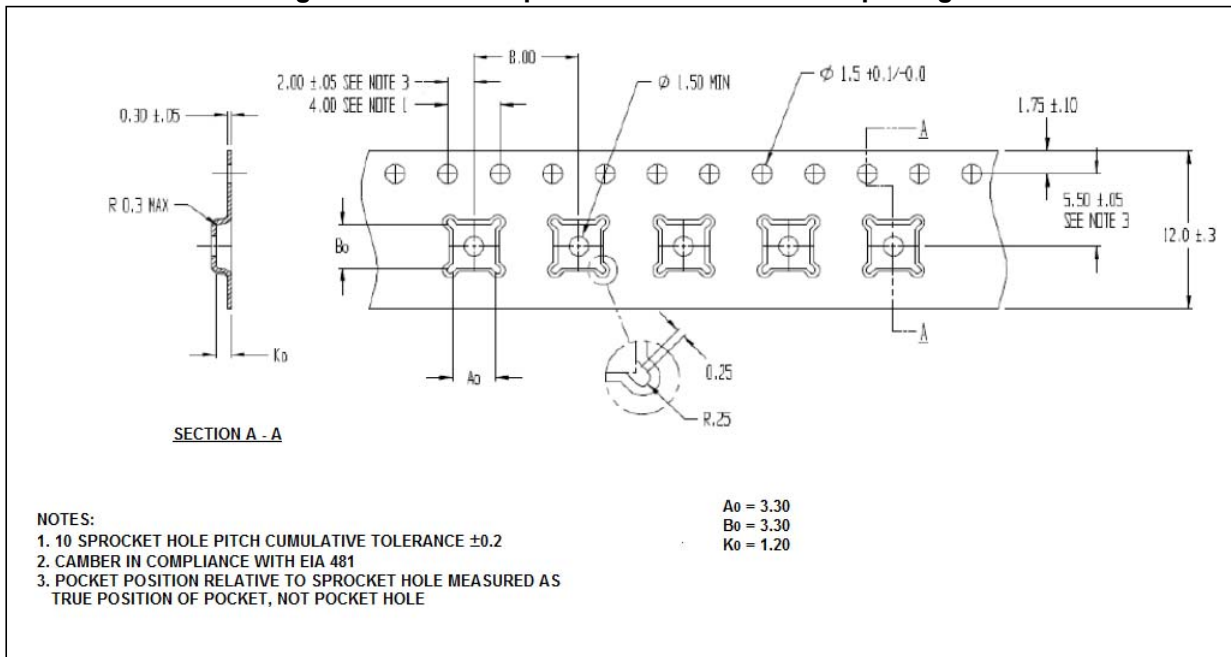


Figure 18. LGA-16 package orientation in carrier tape

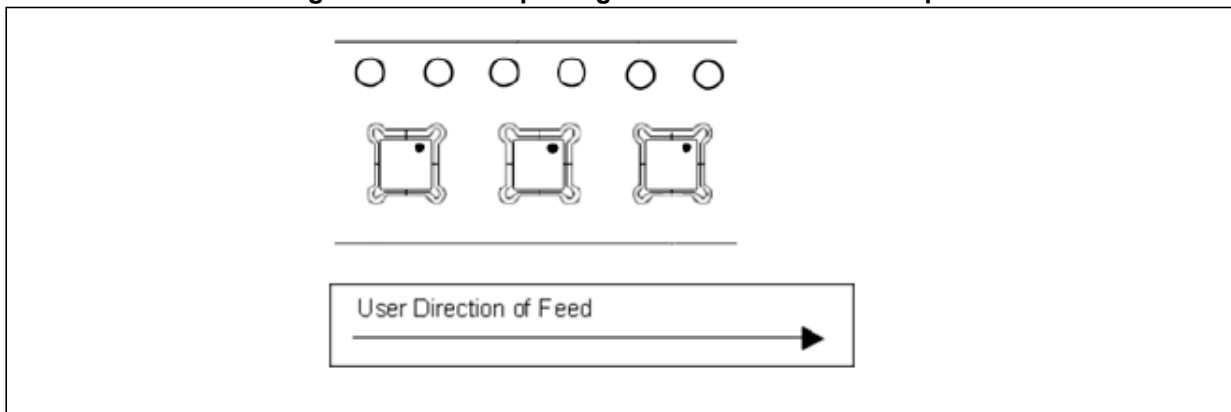


Figure 19. Reel information for carrier tape of LGA-16 package

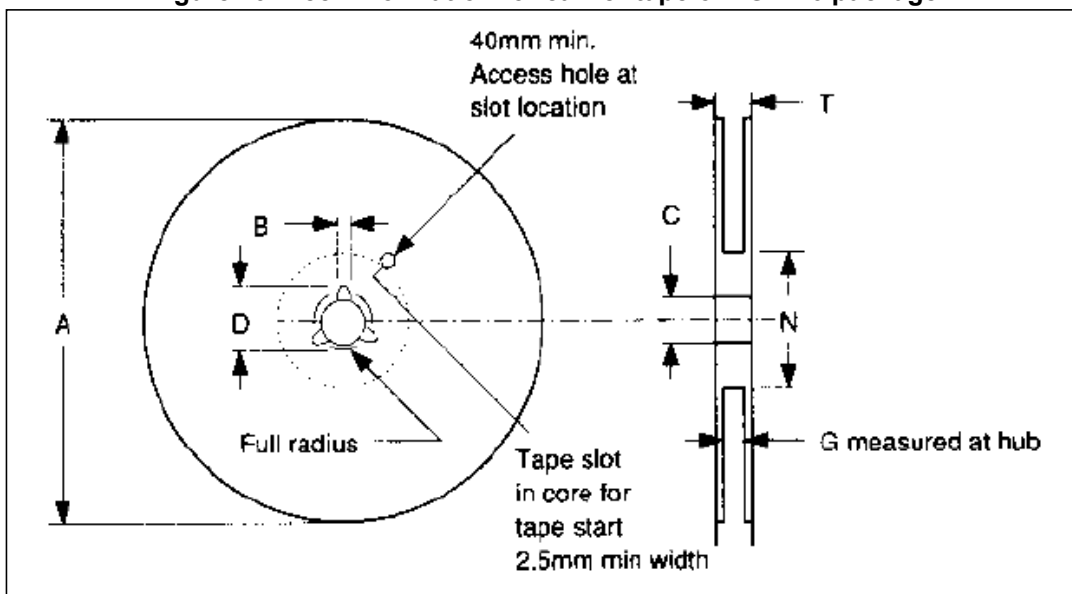


Table 160. Reel dimensions for carrier tape of LGA-16 package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

## 14 Revision history

Table 161. Document revision history

Date	Revision	Changes
18-Feb-2015	1	Initial release
17-Jul-2015	2	Updated registers in <i>Section 9: Register description</i>
27-Jul-2015	3	First public release
09-Oct-2015	4	Updated package representation on page 1 Added <i>PEDO_THS_REG (0Fh)</i> and <i>PEDO_DEB_REG (14h)</i> Added <i>Section 13.2: LGA-16 packing information</i>

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