February 11, 2009

National Semiconductor

LP8900

Ultra Low Noise, Dual 200mA Linear Regulator for RF/ Analog Circuits

General Description

The LP8900 is a dual linear regulator capable of supplying 200mA output current per regulator. Designed to meet the requirements of RF/Analog circuits, the LP8900 provides low device noise, High PSRR, low quiescent current and superior line transient response figures.

Using new innovative design techniques the LP8900 offers class-leading device noise performance without a noise by-pass capacitor.

The LP8900 is designed to be stable with space saving ceramic capacitors as small as 0402 case size, enabling a solution size <4mm ^{2}.

Performance is specified for a -40°C to 125°C junction temperature range.

Output voltage options are available between 1.2V and 3.6V, for availability please contact your local NSC sales office.

Features

- Operation from 1.8V to 5.5V Input
- 1% accuracy Over Temperature
- Output Voltage from 1.2V to 3.6V
- 6µV_{RMS} Output Voltage Noise
- PSRR 75dB at 1kHz
- 110mV Dropout at 200mA load
- 48µA Quiescent Current per regulator
- 80µs Start-Up time
- Stable with Ceramic Capacitors as small as 0402
- Thermal-Overload and Short-Circuit Protection

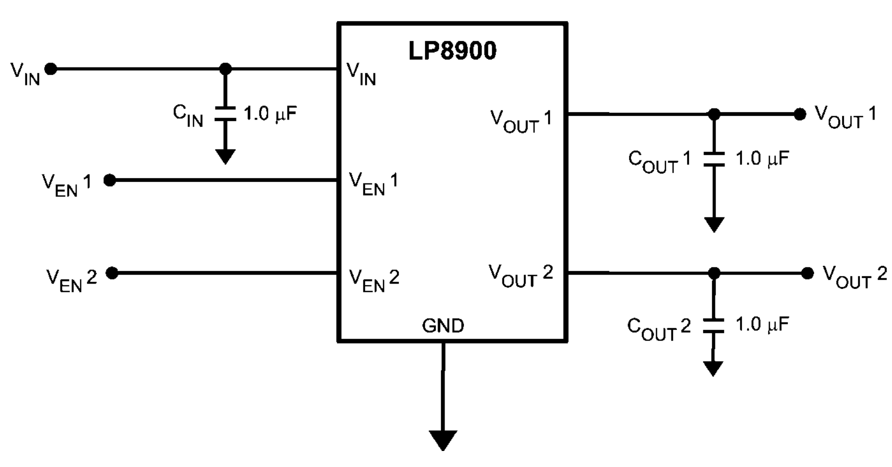
Package

- 6 pin micro SMD (1.5mm x 1.1mm)

Applications

- Battery Operated Devices
- Hand-Held Information Appliances
- Noise Sensitive RF Applications
- DC/DC Convertor Post Regulation/Filter

Typical Application Circuit



LP8900 Ultra Low Noise, Dual 200mA Linear Regulator for RF/Analog Circuits

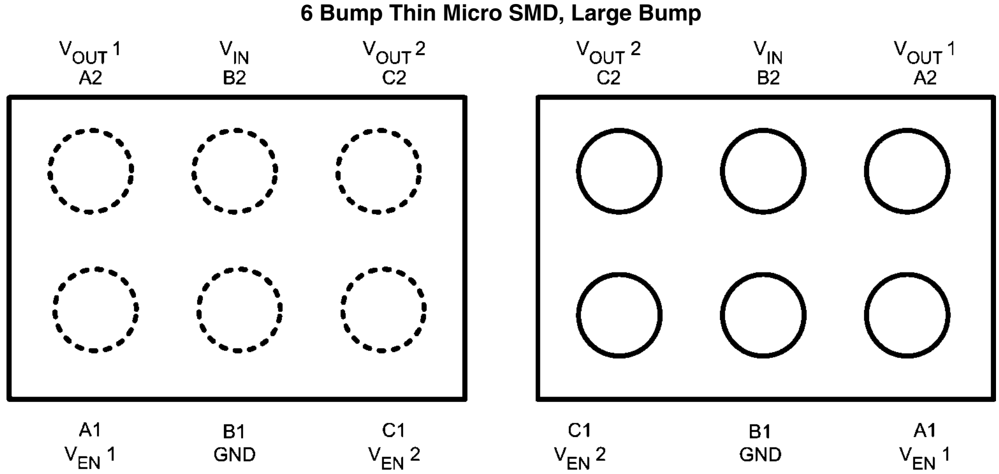
Pin Descriptions

Packages

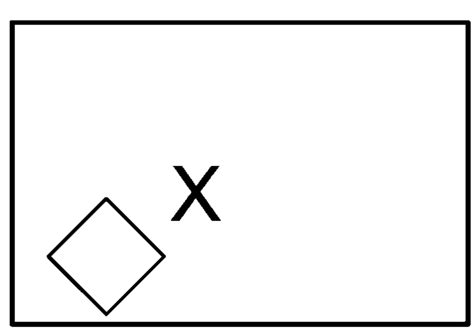
Pin No.	Symbol	Name and Function
A1	V_{EN} 1	Enable Input; Enables the Regulator when ≥ 1.2V. Disables the Regulator when ≤ 0.4V. Enable Input has an internal 3MΩ pull-down resistor to GND.
B1	GND	Common Ground.
C1	V_{EN} 2	Enable Input; Enables the Regulator when ≥ 1.2V. Disables the Regulator when ≤ 0.4V. Enable Input has an internal 3MΩ pull-down resistor to GND.
C2	V_{OUT} 2	Voltage output. A Low ESR Ceramic Capacitor should be connected from this pin to GND. (See Application Information) Connect this output to the load circuit.
B2	V_{IN}	Voltage Supply Input. A 1.0µF capacitor should be connected from this pin to GND.
A2	V_{OUT} 1	Voltage output. A Low ESR Ceramic Capacitor should be connected from this pin to GND. (See Application Information) Connect this output to the load circuit.

Connection Diagram

6 Bump Thin Micro SMD, Large Bump



Top View **Bottom View**



Top Marking

30039306

See NS package number TLA06

Ordering Information (6-Bump Micro SMD)

Only available as Lead Free.

Output Voltage (V) Grade		Order Number Supplied as 250 Units, Tape and Reel	Order Number Supplied as 3000 Units, Tape and Reel
Vout 1	Vout2		
2.8V	2.8V	LP8900TLE_3333	LP8900TLX_3333
2.8V	2.7V	LP8900TLE_AAEB	LP8900TLX_AAEB
2.8V	1.2V	LP8900TLE_AAEC	LP8900TLX_AAEC
*2.8V	1.8V	LP8900TLE_AACB	LP8900TLX_AACB
2.7V	2.7V	LP8900TLE_AAAH	LP8900TLX_AAAH

* Contact your local NSC Sales Office for availability

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}, V_{OUT} Pins: Voltage to GND	-0.3 to 6.5V
V_{EN} : Voltage to GND	-0.3 to (V_{IN} + 0.3V) to 6.5V (max)
Junction Temperature	150°C
Lead/Pad Temp. (Note 3)	
Micro SMD	260°C
Storage Temperature	-65 to 150°C
Continuous Power Dissipation (Note 4)	Internally Limited
ESD (Note 5)	
Human Body Model	2KV
Machine Model	200V

Operating Ratings (Note 1)

Input Voltage Range	1.8 to 5.5V
Recommended Load Current per channel	200mA
Junction Temperature	-40°C to 125°C
Ambient Temperature T_A Range (Note 6)	-40°C to 85°C

Thermal Properties (Note 1)

Junction To Ambient Thermal Resistance(Note 7)	
$θ_{JA}$ JEDEC Board (Note 8)	108°C/W
$θ_{JA}$ 4 Layer Board	172°C/W

Electrical Characteristics

Unless otherwise noted, V_{EN} =1.2V, V_{IN} = V_{OUT} + 0.5V, or 1.8V, whichever is higher , where V_{OUT} is the higher of V_{OUT1} and $V_{OUT2.}$ C_{IN} = C_{OUT} = 1µF, I_{OUT} = 1.0mA .

Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, –40 to +125°C. (Note 9)

Symbol	Parameter	Conditions	Typ	Limit Min	Limit Max	Units
V_{IN}	Input Voltage	(Note 10)		1.8	5.5	V
$ΔV_{OUT}$	Output Voltage Tolerance	V_{IN} = $V_{OUT(NOM)}$ + 0.5V to 5.5V I_{LOAD} = 1mA		**-1.0**	**1.0**	%
		V_{IN} = 1.8V to 5.5V I_{LOAD} = 1mA, V_{OUT} = 1.2V		**-2.25**	**2.25**	%
	Line Regulation Error	V_{IN} = $V_{OUT(NOM)}$ +0.5V to 5.5V, I_{OUT} = 1mA	0.05			%/V
	Load Regulation Error	I_{OUT} = 1mA to 200mA	4		**9**	mV
V_{DO}	Dropout Voltage(Note 11)	I_{OUT} = 200mA, V_{OUT} = 3.6V	55		**82**	mV
		I_{OUT} = 200mA, V_{OUT} = 2.8V	110		**164**	
		I_{OUT} = 200mA, V_{OUT} = 1.8V	185		**260**	
I_{LOAD}	Load Current	(Note 12)		0	**200**	mA
I_Q	Quiescent Current	V_{EN1} = 1.2V, V_{EN2} = 0V I_{OUT} = 0mA	48		**120**	µA
		V_{EN1} = 1.2V, V_{EN2} = 1.2V I_{OUT} = 0mA	85		**200**	
		V_{EN1} = 1.2V, V_{EN2} = 1.2V I_{OUT} = 200mA	210			
		V_{EN} ≲ 0.4V	0.003		**1.0**	
I_{SC}	Short Circuit Current Limit	V_{IN} = 3.6V (Note 13)	600		**900**	mA
PSRR	Power Supply Rejection Ratio (Note 14)	f = 1kHz, I_{OUT} = 200mA	75			dB
		f = 10kHz, I_{OUT} = 200mA	65			
		f = 100kHz, I_{OUT} = 200mA	45			
		f = 1MHz, I_{OUT} = 200mA	30			
e_n	Output noise Voltage (Note 14)	BW = 10Hz to 100kHz, V_{IN} = 4.2V, C_{OUT} = 1.0µF, I_{OUT} = 0mA	6			$µV_{RMS}$
		I_{OUT} = 1mA	10			
		I_{OUT} = 200mA	6			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature	155			°C
		Hysteresis	15			

Electrical Characteristics con't.

Unless otherwise noted, V_{EN} =1.2V, V_{IN} = V_{OUT} + 0.5V, or 1.8V, whichever is higher, where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN}= C_{OUT} = 1µF, I_{OUT} = 1mA.

Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125°C. (Note 9)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
Enable Control Characteristics							
I_{EN}	Maximum Input Current at V_{EN} Input(Note 15)	V_{EN} = 0V, V_{IN} = 5.5V		0.003			µA
		V_{EN} = V_{IN} = 5.5V				**4**	
V_{IL}	Low Input Threshold	V_{IN} = 1.8V to 5.5V				**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 1.8V to 5.5V			**1.2**		V
Timing\Transient Characteristics(Note 14)							
T_{ON}	Turn On Time	To 95% Level $V_{OUT(nom)}$		80		**200**	µs
T_{OFF}	Turn Off Time	5% of $V_{OUT(NOM)}$, I_{OUT}= 0mA		0.4		**1**	ms
	Line Transient Response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 30µs δV_{IN} = 600mV		1			mV (pk - pk)
Transient Response	Load Transient Response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 1µs	I_{OUT} = 1 mA to 200mA	80			mV
			I_{OUT} = 200mA to 1mA	70			
	Overshoot on Start-up			0		**1**	%

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: For further information on these packages please refer to the following application notes,AN-1112 Micro SMD Wafer Level Chip Scale Package.

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 5: The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 6: The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part / package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Note 7: Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Note 8: Full details can be found in JESD61-7

Note 9: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 10: The minimum input voltage = $V_{OUT(NOM)}$ + 0.5V or 1.8V, whichever is greater.

Note 11: Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter is only specified for output voltages above 1.8V.

Note 12: The device maintains the regulated output voltage without a load.

Note 13: Short circuit current is measured with V_{OUT} pulled to 0V.

Note 14: This electrical specification is guaranteed by design.

Note 15: Enable Pin has an internal 3MΩ typical, resistor connected to GND.

Note 16: The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R or X5R. (See capacitor section in Applications Hints)

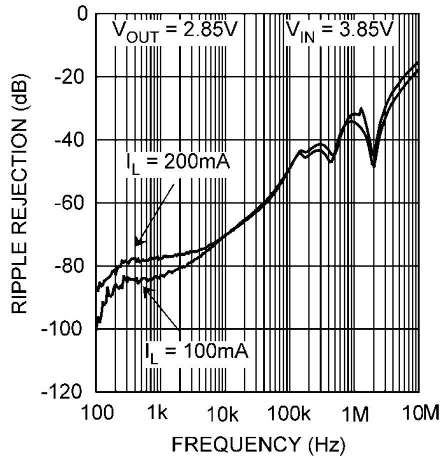
Recommended Capacitor Specifications

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_{IN}	Input Capacitor	Capacitance (Note 16)	1.0	**0.33**	**10**	µF
C_{OUT}	Output Capacitor		1.0	**0.33**	**4.7**	
		ESR		**5**	**500**	mΩ

Typical Performance Characteristics.

Unless otherwise specified, $C_{IN} = C_{OUT}$=1.0µF Ceramic, $V_{IN} = V_{OUT(NOM)}$ + 1.0V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 2.85V , Enable pin is tied to V_{IN}.

Power Supply Rejection Ratio



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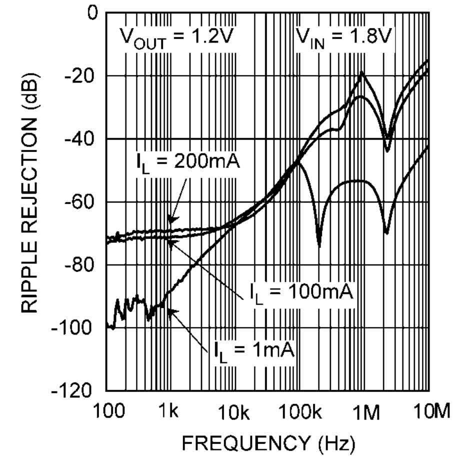
Power Supply Rejection Ratio



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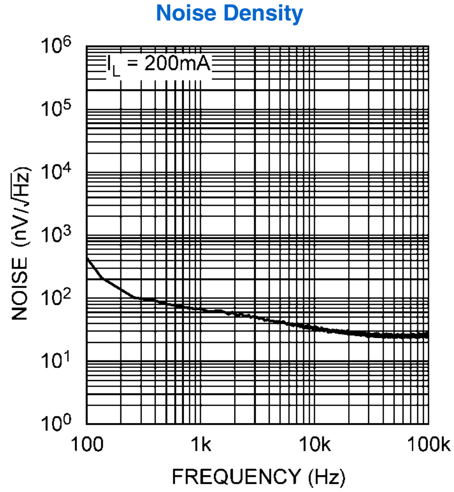
Noise Density



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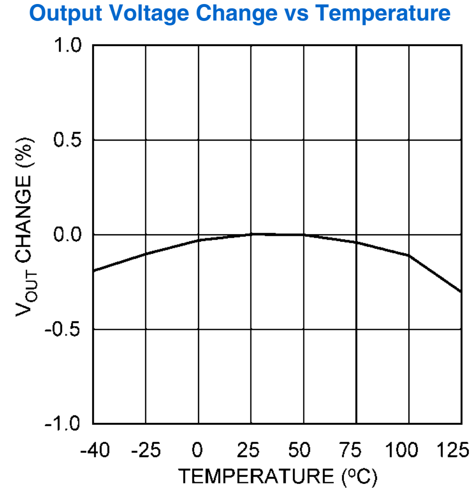
Output Voltage Change vs Temperature



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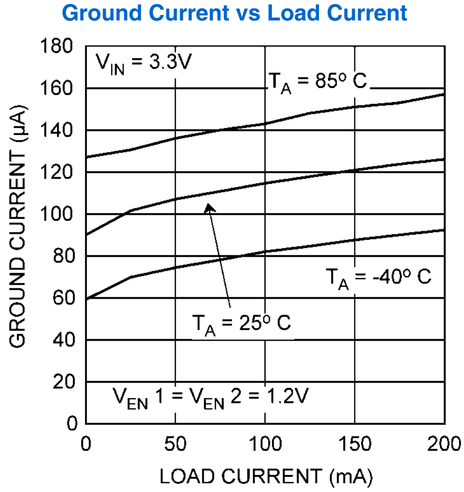
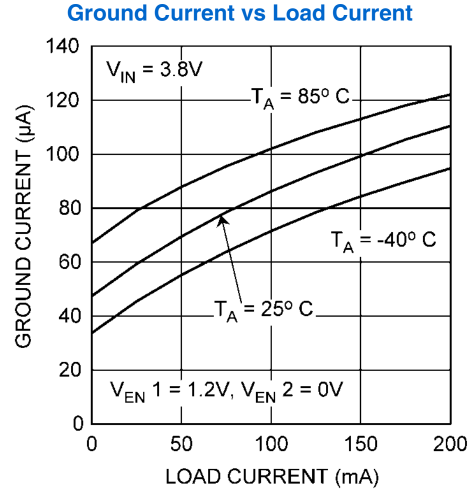
Ground Current vs Load Current



30039314

Ground Current vs Load Current



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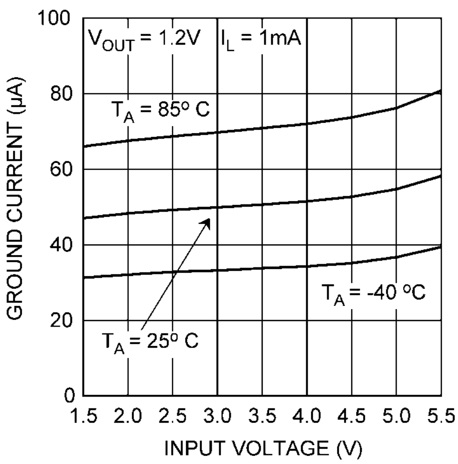
Typical Performance Characteristics con't.

Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\mu F$ Ceramic, $V_{IN} = V_{OUT(NOM)} + 1.0V$ or 1.8V whichever is greater, $T_A = 25°C$, $V_{OUT(NOM)} = 2.85V$, Enable pin is tied to V_{IN}.

Ground Current vs V_{IN}



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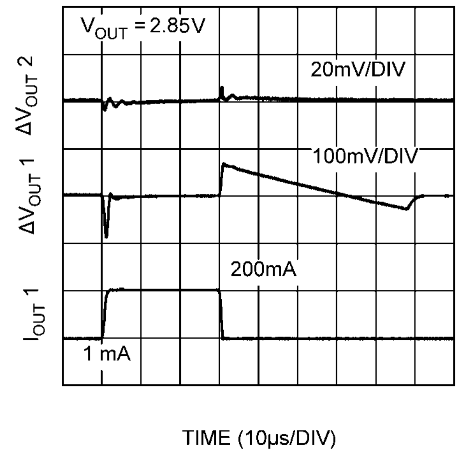
Vout 1 Load Transient 1 to 200mA



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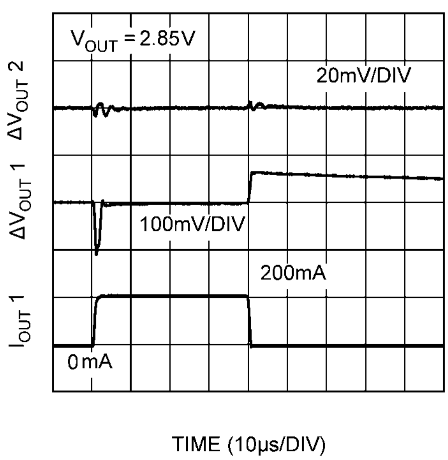
Vout 1 Load Transient 0 to 200mA



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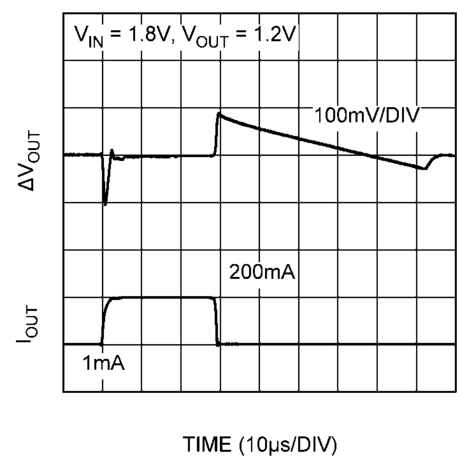
Load Transient. Vin = 1.8V, Vout = 1.2V



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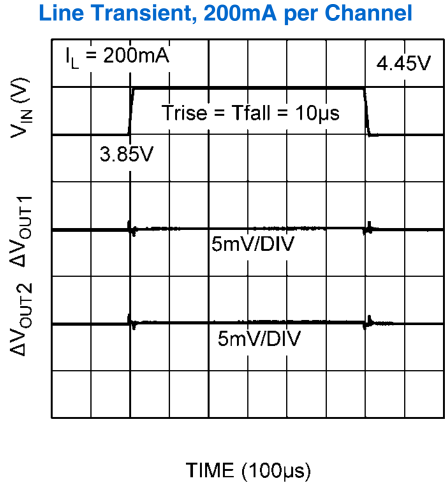
Line Transient, 200mA per Channel



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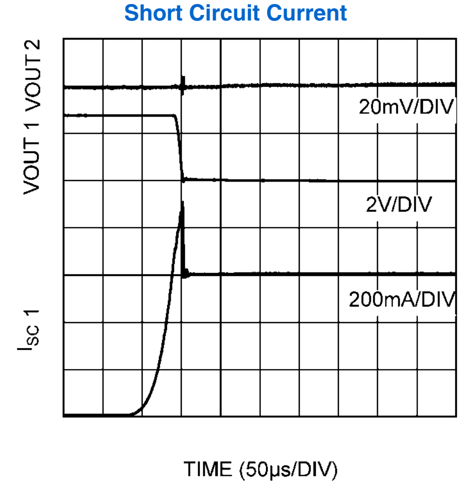
Short Circuit Current



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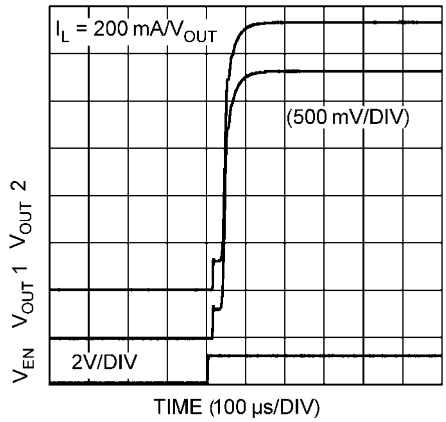
Typical Performance Characteristics con't.

Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0\mu F$ Ceramic, $V_{IN} = V_{OUT(NOM)} + 1.0V$ or 1.8V whichever is greater, $T_A = 25°C$, $V_{OUT(NOM)} = 2.85V$, Enable pin is tied to V_{IN}.

Enable Start-up Characteristics



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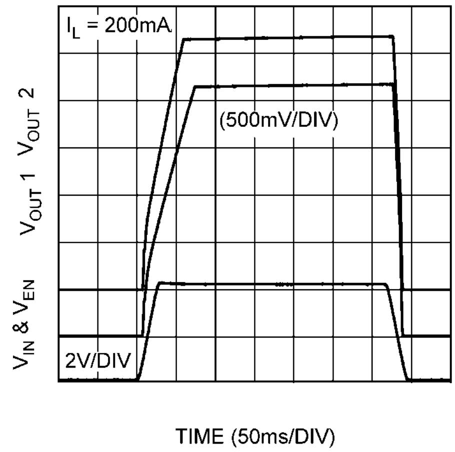
Vin and Enable Tied Together



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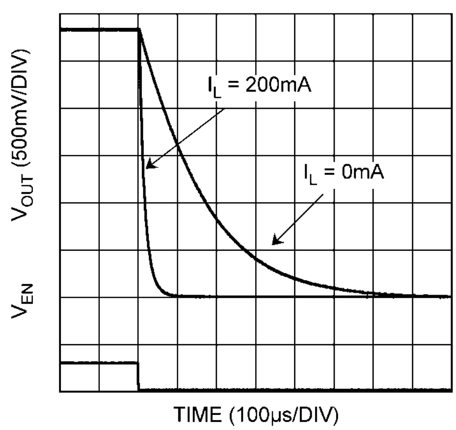
Shutdown Characteristics



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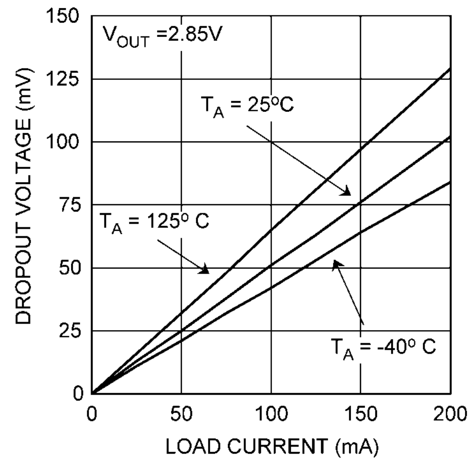
Dropout Voltage



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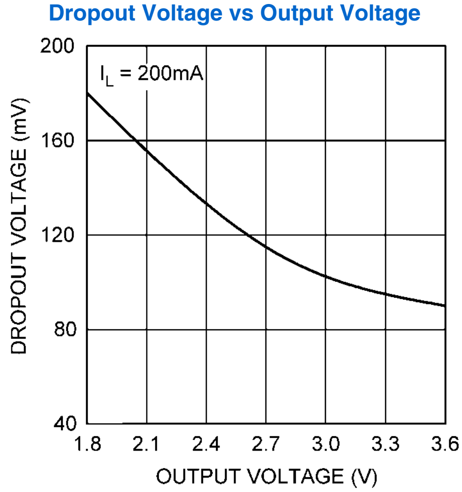
Dropout Voltage vs Output Voltage



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Application Information

EXTERNAL CAPACITORS

In common with most regulators, the LP8900 requires external capacitors for regulator stability. The LP8900 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP8900 input pin and ground (this capacitance value may be increased to 10µF).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance, temperature, and voltage coefficients must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value.

The LP8900 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (dielectric type X7R or X5R) with an ESR between 5mΩ to 500mΩ, is suitable in the LP8900 application circuit.

Other ceramic types such as Y5V and Z5U are less suitable owing to their inferior temperature characteristics. (See section on Capacitor Characteristics).

It is also recommended that the output capacitor is placed within 1cm of the output pin and returned to a clean, low impedance, ground connection.

It is possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

NO-LOAD STABILITY

The LP8900 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP8900 is designed to work with ceramic capacitors on the input and outputs to take advantage of the benefits they offer. For capacitance values around 1.0µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular, to ensure stability, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

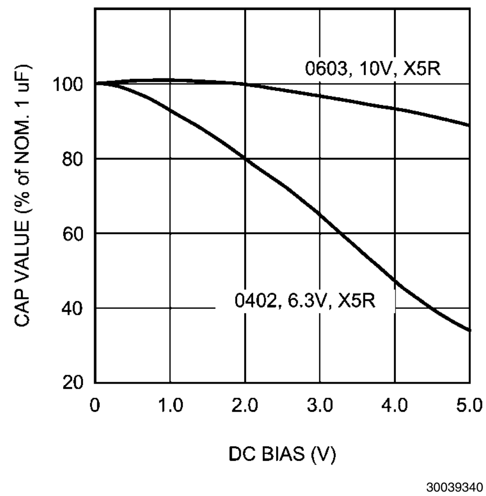


FIGURE 1. Effect of DC bias on Capacitance Value.

As an example *Figure 1* shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 4.7µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP8900. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range -55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of -55°C to +85°C. Some large value ceramic capacitors (4.7µF) are manufactured with Z5U or Y5V temperature characteristics, which can result in the capacitance dropping by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R or X5R types are recommended in applications where the temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

ENABLE CONTROL

The LP8900 may be switched ON or OFF by a logic input at the ENABLE pin.A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3nA. However if the application does not require the shutdown feature, the V_{EN} pin can be tied to V_{IN} to keep the regulator permanantly on. To ensure fast start-up is achieved, V_{EN} should be driven separately.

A 3MΩ pulldown resister ties the V_{EN} input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

micro SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in the National Semiconductor Application Note (AN-1112). Referring to the section *Surface Mount Technology (SMT) Assenbly Considerations*, it should be noted that the pad style which must be used with the 6 pin package is NSMD (non-solder mask defined) type.

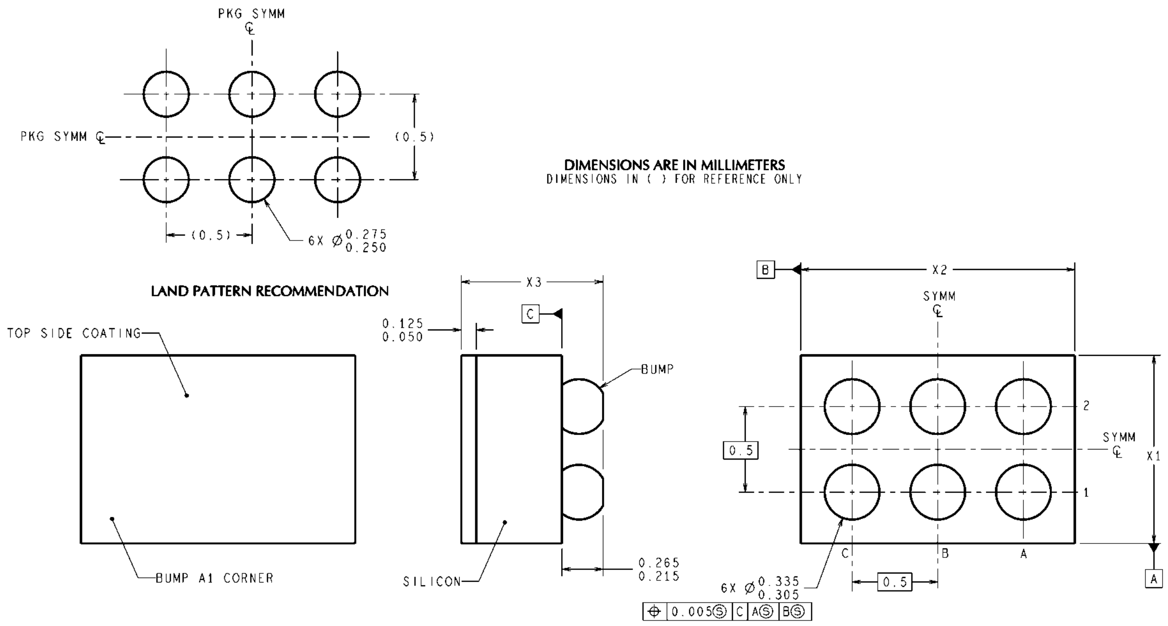
For best results during assembly, alignment ordinals on the PCB may be used to facilitate placement of the micro SMD device.

micro SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct sunlight may cause mis-operation of the device. Light sources such as halogen lamps can affect the electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that fluorescent lighting, used inside most buildings will have little effect on performance.

Physical Dimensions inches (millimeters) unless otherwise noted



TLA06XXX (Rev C)

6 Bump Thin micro SMD, Large Bump
NS Package Number TLA06CZA
The Dimensions for X1, X2 and X3 as given as:
X1 = 1.057mm ± 0.030mm
X2 = 1.463mm ± 0.03mm
X3 = 0.60mm ± 0.075mm

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
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