



# Single-Supply, High-Speed, Precision LOGARITHMIC AMPLIFIER

## FEATURES

- **ADVANTAGES:**
  - Tiny for High Density Systems
  - Precision on One Supply
  - Fast Over Eight Decades
  - Fully-Tested Function
- **TWO SCALING AMPLIFIERS**
- **WIDE INPUT DYNAMIC RANGE:**  
Eight Decades, 100pA to 10mA
- **2.5V REFERENCE**
- **STABLE OVER TEMPERATURE**
- **LOW QUIESCENT CURRENT: 10mA**
- **DUAL OR SINGLE SUPPLY: ±5V, +5V**
- **PACKAGE: Small QFN-16 (4mm x 4mm)**
- **SPECIFIED TEMPERATURE RANGE:**  
–5°C to +75°C

## APPLICATIONS

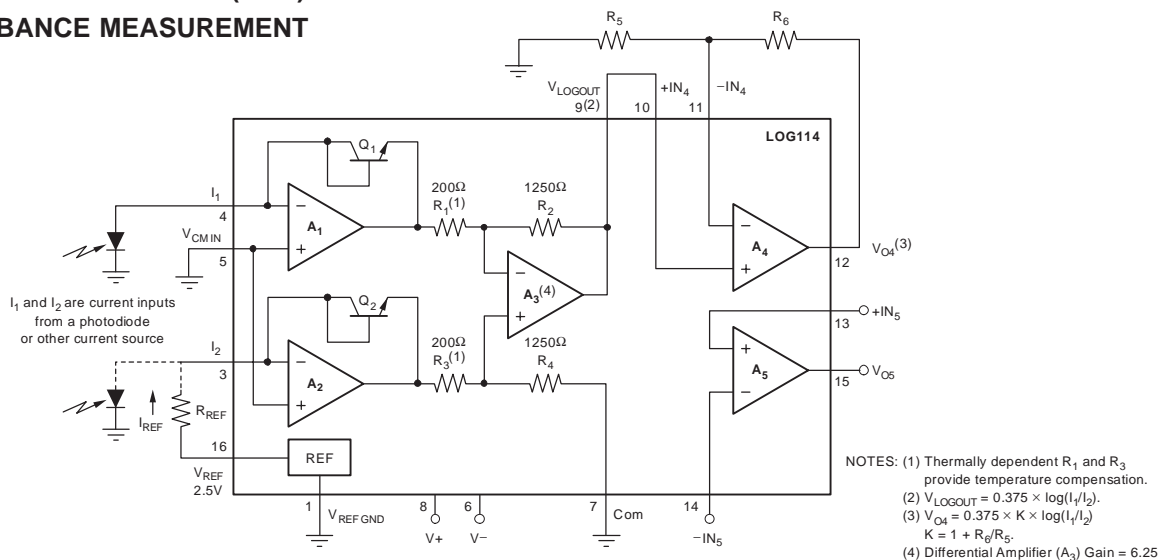
- **ONET ERBIUM-DOPED FIBER OPTIC AMPLIFIER (EDFA)**
- **LASER OPTICAL DENSITY MEASUREMENT**
- **PHOTODIODE SIGNAL COMPRESSION AMP**
- **LOG, LOG-RATIO FUNCTION**
- **ANALOG SIGNAL COMPRESSION IN FRONT OF ANALOG-TO-DIGITAL (ADC) CONVERTER**
- **ABSORBANCE MEASUREMENT**

## DESCRIPTION

The LOG114 is specifically designed for measuring low-level and wide dynamic range currents in communications, lasers, medical, and industrial systems. The device computes the logarithm or log-ratio of an input current or voltage relative to a reference current or voltage (logarithmic transimpedance amplifier).

High precision is ensured over a wide dynamic range of input signals on either bipolar (±5V) or single (+5V) supply. Special temperature drift compensation circuitry is included on-chip. In log-ratio applications, the signal current may be from a high impedance source such as a photodiode or resistor in series with a low impedance voltage source. The reference current is provided by a resistor in series with a precision internal voltage reference, photo diode, or active current source.

The output signal at  $V_{LOGOUT}$  has a scale factor of 0.375V out per decade of input current, which limits the output so that it fits within a 5V or 10V range. The output can be scaled and offset with one of the available additional amplifiers, so it matches a wide variety of ADC input ranges. Stable dc performance allows accurate measurement of low-level signals over a wide temperature range. The LOG114 is specified over a –5°C to +75°C temperature range and can operate from –40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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### ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V-	12V
Signal Input Terminals, Voltage(2)	(V-) -0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Junction Temperature	+150°C
ESD Rating (Human Body Model)	2000V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
- (3) Short-circuit to ground.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PRECISION CURRENT MEASUREMENT PRODUCTS

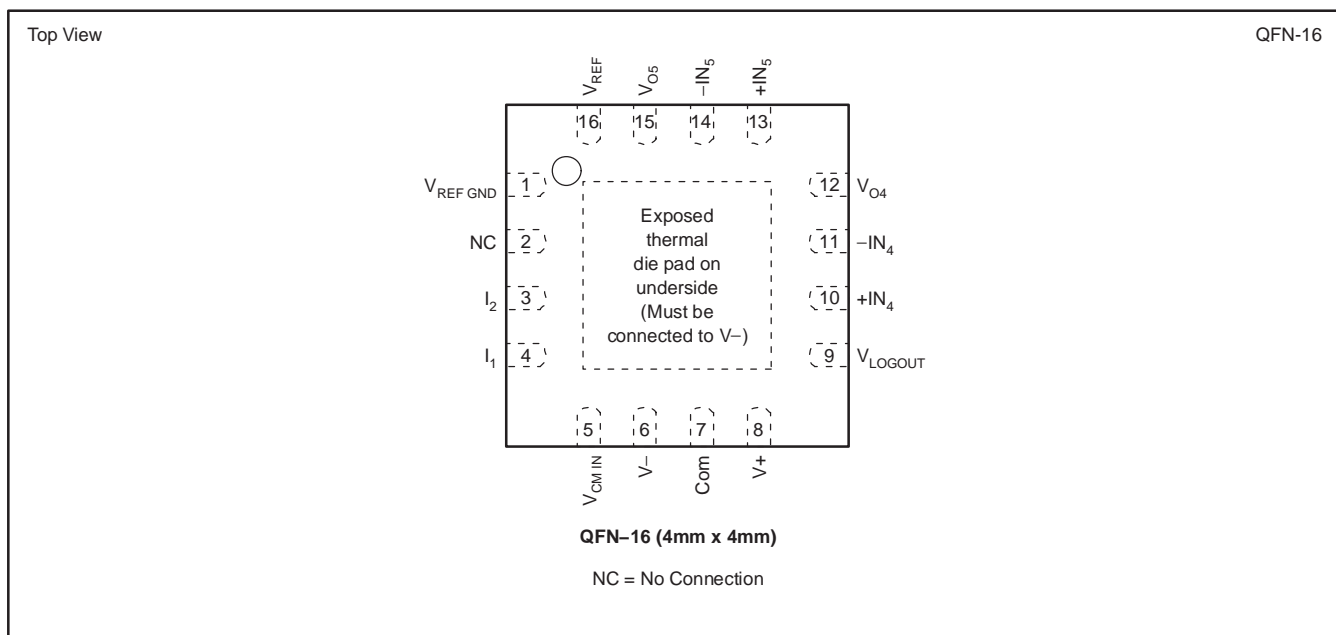
FEATURES	PRODUCT
Logarithmic Transimpedance Amplifier, 5V, Eight Decades	LOG114
Logarithmic Transimpedance, 36V, 7.5 Decades	LOG112
Resistor-Feedback Transimpedance, 5V, 5.5 Decades	OPA380, OPA381
Switched Integrator Transimpedance, Six Decades	IVC102
Direct Digital Converter, Six Decades	DDC112

### ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
LOG114	QFN-16	RGV	LOG114

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### PIN CONFIGURATION



**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 5V$** 
**Boldface** limits apply over the specified temperature range,  $T_A = -5^\circ\text{C}$  to  $+75^\circ\text{C}$ .

 All specifications at  $T_A = +25^\circ\text{C}$ ,  $R_{V\text{LOGOUT}} = 10\text{k}\Omega$ ,  $V_{\text{CM}} = \text{GND}$ , unless otherwise noted.

PARAMETER	CONDITIONS	LOG114			UNITS
		MIN	TYP	MAX	
<b>CORE LOG FUNCTION</b>	$I_{\text{IN}}/V_{\text{OUT}}$ Equation	$V_O = (0.375V) \text{Log}(I_1/I_2)$			V
<b>LOG CONFORMITY ERROR<sup>(1)</sup></b>					
Initial	1nA to 100 $\mu$ A (5 decades)		0.1	0.2	%
	100pA to 3.5mA (7.5 decades)		0.009	0.017	dB
			0.9		%
			0.08		dB
<b>Over Temperature</b>	1mA to 10mA	See Typical Characteristics			
	<b>1nA to 100<math>\mu</math>A (5 decades)</b>		<b>0.1</b>	<b>0.4</b>	%
	<b>100pA to 3.5mA (7.5 decades)</b>		<b>0.5</b>		%
	<b>1mA to 10mA</b>	See Typical Characteristics			%
<b>TRANSFER FUNCTION (GAIN)<sup>(2)</sup></b>					
Initial Scaling Factor	100pA to 10mA		0.375		V/decade
Scaling Factor Error	1nA to 100 $\mu$ A		0.4	$\pm 2.5$	%
			0.035	0.21	dB
<b>Over Temperature</b>	<b><math>T_{\text{MIN}}</math> to <math>T_{\text{MAX}}</math></b>		<b>1.5</b>	<b><math>\pm 3.5</math></b>	%
	<b><math>+15^\circ\text{C}</math> to <math>+50^\circ\text{C}</math></b>		0.7	$\pm 3$	%
<b>INPUT, <math>A_1</math> and <math>A_2</math></b>					
Offset Voltage	$V_{\text{OS}}$		$\pm 1$	$\pm 4$	mV
<b>vs Temperature</b>	$dV/dT$		<b><math>\pm 15</math></b>		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR	$V_S = \pm 2.25V$ to $\pm 5.5V$	75	400	$\mu\text{V}/V$
Input Bias Current	$I_B$		$\pm 5$		pA
<b>vs Temperature</b>			<b>Doubles every <math>10^\circ\text{C}</math></b>		
Input Common-Mode Voltage Range	$V_{\text{CM}}$		(V-) +1.5 to (V+) -1.5		V
Voltage Noise	$e_n$	$f = 0.1\text{Hz}$ to 10kHz	3		$\mu\text{Vrms}$
		$f = 1\text{kHz}$	30		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise	$i_n$	$f = 1\text{kHz}$	4		$\text{fA}/\sqrt{\text{Hz}}$
<b>OUTPUT, <math>A_3</math> (<math>V_{\text{LOGOUT}}</math>)</b>					
Output Offset, $V_{\text{OSO}}$ , Initial	$V_{\text{OSO}}$		$\pm 11$	$\pm 50$	mV
<b>Over Temperature</b>			<b><math>\pm 15</math></b>	<b><math>\pm 65</math></b>	mV
Full-Scale Output (FSO) <sup>(3)</sup>			(V-) + 0.6	(V+) - 0.6	V
Gain Bandwidth Product	GBW	$I_{\text{IN}} = 1\mu\text{A}$	50		MHz
Short-Circuit Current	$I_{\text{SC}}$		$\pm 18$		mA
Capacitive Load			100		pF
<b>OP AMP, <math>A_4</math> and <math>A_5</math></b>					
Input Offset Voltage	$V_{\text{OS}}$		$\pm 250$	$\pm 1000$	$\mu\text{V}$
<b>vs Temperature</b>	$dV/dT$		<b><math>\pm 2</math></b>		$\mu\text{V}/^\circ\text{C}$
vs Supply	PSRR	$V_S = \pm 4.5V$ to $\pm 5.5V$	30	250	$\mu\text{V}/V$
vs Common-Mode Voltage	CMRR		74		dB
Input Bias Current	$I_B$		-1		$\mu\text{A}$
Input Offset Current	$I_{\text{OS}}$		$\pm 0.05$		$\mu\text{A}$
Input Voltage Range			(V-)	(V+) - 2	V
Input Noise $f = 0.1\text{Hz}$ to 10Hz			2		$\mu\text{Vpp}$
$f = 1\text{kHz}$			13		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise	$i_n$		2		$\text{pA}/\sqrt{\text{Hz}}$
Open-Loop Voltage Gain	$A_{\text{OL}}$		100		dB
Gain Bandwidth Product	GBW		15		MHz
Slew Rate	SR		5		V/ $\mu\text{s}$
Settling Time 0.01%	$t_S$	$G = -1$ , 3V Step, $C_L = 100\text{pF}$	1.5		$\mu\text{s}$
Rated Output			(V-) + 0.5	(V+) - 0.5	V
Short-Circuit Current	$I_{\text{SC}}$		+4/-10		mA

**ELECTRICAL CHARACTERISTICS:  $V_S = \pm 5V$  (continued)****Boldface** limits apply over the specified temperature range,  $T_A = -5^\circ\text{C}$  to  $+75^\circ\text{C}$ .All specifications at  $T_A = +25^\circ\text{C}$ ,  $R_{V\text{LOGOUT}} = 10\text{k}\Omega$ ,  $V_{\text{CM}} = \text{GND}$ , unless otherwise noted.

PARAMETER	CONDITIONS	LOG114			UNITS
		MIN	TYP	MAX	
<b>TOTAL ERROR(4, 5)</b>		See Typical Characteristics			
<b>FREQUENCY RESPONSE, Core Log<sup>(6)</sup></b> BW, 3dB $I_1$ or $I_2 =$	$I_{\text{AC}} = 10\%$ of $I_{\text{DC}}$ value, $I_{\text{REF}} = 1\mu\text{A}$				
1nA			5		kHz
10nA			12		kHz
100nA			120		kHz
1 $\mu\text{A}$			2.3		MHz
10 $\mu\text{A}$ to 1mA (ratio 1:100)			> 5		MHz
1mA to 3.5mA (ratio 1:3.5)			> 5		MHz
3.5mA to 10mA (ratio 1:2.9)			> 5		MHz
<b>Step Response</b>	$I_{\text{REF}} = 1\mu\text{A}$				
Increasing ( $I_1$ or $I_2$ )					
8nA to 240nA (ratio 1:30)			0.7		$\mu\text{s}$
10nA to 100nA (ratio 1:10)			1.5		$\mu\text{s}$
10nA to 1 $\mu\text{A}$ (ratio 1:100)			0.15		$\mu\text{s}$
10nA to 10 $\mu\text{A}$ (ratio 1:1k)			0.07		$\mu\text{s}$
10nA to 1mA (ratio 1:100k)			0.06		$\mu\text{s}$
1mA to 10mA (ratio 1:10)			1		$\mu\text{s}$
Decreasing ( $I_1$ or $I_2$ )	$I_{\text{REF}} = 1\mu\text{A}$				
8nA to 240nA (ratio 1:30)			1		$\mu\text{s}$
10nA to 100nA (ratio 1:10)			2		$\mu\text{s}$
10nA to 1 $\mu\text{A}$ (ratio 1:100)			0.25		$\mu\text{s}$
10nA to 10 $\mu\text{A}$ (ratio 1:1k)			0.05		$\mu\text{s}$
10nA to 1mA (ratio 1:100k)			0.03		$\mu\text{s}$
1mA to 10mA (ratio 1:10)			1		$\mu\text{s}$
<b>VOLTAGE REFERENCE</b>					
Bandgap Voltage			2.5		V
Error, Initial			$\pm 0.15$	$\pm 1$	%
<b>vs Temperature</b>			<b><math>\pm 25</math></b>		<b>ppm/<math>^\circ\text{C}</math></b>
vs Supply	$V_S = \pm 4.5\text{V}$ to $\pm 5.5\text{V}$		$\pm 30$		ppm/V
vs Load	$I_O = \pm 2\text{mA}$		$\pm 200$		ppm/mA
Short-Circuit Current			$\pm 10$		mA
<b>POWER SUPPLY</b>					
Dual Supply Operating Range	$V_S$		$\pm 2.4$	$\pm 5.5$	V
Quiescent Current	$I_Q$	$I_O = 0$	$\pm 10$	$\pm 15$	mA
<b>TEMPERATURE RANGE</b>					
Specification, $T_{\text{MIN}}$ to $T_{\text{MAX}}$			-5	+75	$^\circ\text{C}$
Operating			-40	+85	$^\circ\text{C}$
Storage			-55	+125	$^\circ\text{C}$
Thermal Resistance, $\theta_{\text{JA}}$			62		$^\circ\text{C}/\text{W}$

(1) Log conformity error is peak deviation from the best-fit straight line of  $V_O$  vs  $\text{Log}(I_1/I_2)$  curve expressed as a percent of peak-to-peak full-scale output. Scale factor,  $K$ , equals 0.375V output per decade of input current.

(2) Scale factor of core log function is trimmed to 0.375V output per decade change of input current.

(3) Specified by design.

(4) Worst-case total error for any ratio of  $I_1/I_2$ , as the largest of the two errors, when  $I_1$  and  $I_2$  are considered separately.

(5) Total error includes offset voltage, bias current, gain, and log conformity.

(6) Small signal bandwidth (3dB) and transient response are a function of the level of input current. Smaller input current amplitude results in lower bandwidth.

**ELECTRICAL CHARACTERISTICS:  $V_S = +5V$** 
**Boldface** limits apply over the specified temperature range,  $T_A = -5^\circ\text{C}$  to  $+75^\circ\text{C}$ .

 All specifications at  $T_A = +25^\circ\text{C}$ ,  $R_{V\text{LOGOUT}} = 10\text{k}\Omega$ ,  $V_{\text{CM}} = +2.5\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	LOG114			UNITS
		MIN	TYP	MAX	
<b>CORE LOG FUNCTION</b>	$I_{\text{IN}}/V_{\text{OUT}}$ Equation	$V_O = (0.375V) \text{Log} (I_1/I_2) + V_{\text{CM}}$			V
<b>LOG CONFORMITY ERROR<sup>(1)</sup></b>					
Initial	1nA to 100 $\mu$ A (5 decades)		0.1	0.25	%
	100pA to 3.5mA (7.5 decades)		0.009	0.022	dB
			0.9		%
			0.08		dB
<b>Over Temperature</b>	1mA to 10mA <b>1nA to 100<math>\mu</math>A (5 decades)</b> <b>100pA to 3.5mA (7.5 decades)</b> <b>1mA to 10mA</b>	See Typical Characteristics			
			<b>0.1</b>	<b>0.4</b>	%
			<b>0.5</b>		%
		See Typical Characteristics			
<b>TRANSFER FUNCTION (GAIN)<sup>(2)</sup></b>					
Initial Scaling Factor	10nA to 100 $\mu$ A		0.375		V/decade
Scaling Factor Error	1nA to 100 $\mu$ A		0.4	$\pm 2.5$	%
			0.035	0.21	dB
<b>Over Temperature</b>	<b><math>T_{\text{MIN}}</math> to <math>T_{\text{MAX}}</math></b> <b><math>+15^\circ\text{C}</math> to <math>+50^\circ\text{C}</math></b>		<b>0.035</b>	<b><math>\pm 3.5</math></b>	%
			0.7	$\pm 3$	%
<b>INPUT, <math>A_1</math> and <math>A_2</math></b>					
Offset Voltage	$V_{\text{OS}}$		$\pm 1$	$\pm 7$	mV
<b>vs Temperature</b>	$dV/dT$	<b><math>T_{\text{MIN}}</math> to <math>T_{\text{MAX}}</math></b>	<b><math>\pm 30</math></b>		$\mu\text{V}/^\circ\text{C}$
<b>vs Power Supply</b>	PSRR	$V_S = +4.5\text{V}$ to $+5.5\text{V}$	300		$\mu\text{V}/\text{V}$
Input Bias Current	$I_B$		$\pm 5$		pA
<b>vs Temperature</b>		<b><math>T_{\text{MIN}}</math> to <math>T_{\text{MAX}}</math></b>	<b>Doubles every <math>10^\circ\text{C}</math></b>		
Input Common-Mode Voltage Range	$V_{\text{CM}}$		(V-) +1.5 to (V+) -1.5		V
Voltage Noise	$e_n$	$f = 0.1\text{Hz}$ to $10\text{kHz}$	3		$\mu\text{V}_{\text{rms}}$
		$f = 1\text{kHz}$	30		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise	$i_n$	$f = 1\text{kHz}$	4		$\text{fA}/\sqrt{\text{Hz}}$
<b>OUTPUT, <math>A_3</math> (<math>V_{\text{LOGOUT}}</math>)</b>					
Output Offset, $V_{\text{OSO}}$ , Initial	$V_{\text{OSO}}$		$\pm 14$	$\pm 65$	mV
<b>Over Temperature</b>		<b><math>T_{\text{MIN}}</math> to <math>T_{\text{MAX}}</math></b>	<b><math>\pm 18</math></b>	<b><math>\pm 80</math></b>	<b>mV</b>
Full Scale Output (FSO) <sup>(3)</sup>		$V_S = +5\text{V}$	(V-) + 0.6	(V+) - 0.6	V
Gain Bandwidth Product	GBW	$I_{\text{IN}} = 1\mu\text{A}$	50		MHz
Short-Circuit Current	$I_{\text{SC}}$		$\pm 18$		mA
Capacitive Load			100		pF
<b>OP AMP, <math>A_4</math> and <math>A_5</math></b>					
Input Offset Voltage	$V_{\text{OS}}$		$\pm 250$	$\pm 4000$	$\mu\text{V}$
<b>vs Temperature</b>	$dV/dT$	<b><math>T_{\text{MIN}}</math> to <math>T_{\text{MAX}}</math></b>	<b><math>\pm 2</math></b>		$\mu\text{V}/^\circ\text{C}$
<b>vs Supply</b>	PSRR	$V_S = +4.8\text{V}$ to $+5.5\text{V}$	30		$\mu\text{V}/\text{V}$
<b>vs Common-Mode Voltage</b>	CMRR		70		dB
Input Bias Current	$I_B$		-1		$\mu\text{A}$
Input Offset Current	$I_{\text{OS}}$		$\pm 0.05$		$\mu\text{A}$
Input Voltage Range			(V-)	(V+) - 1.5	V
Input Noise $f = 0.1\text{Hz}$ to $10\text{Hz}$			1		$\mu\text{V}_{\text{PP}}$
			28		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise	$i_n$		2		$\text{pA}/\sqrt{\text{Hz}}$
Open-Loop Voltage Gain	$A_{\text{OL}}$		100		dB
Gain Bandwidth Product	GBW		15		MHz
Slew Rate	SR		5		V/ $\mu\text{s}$
Settling Time 0.01%	$t_S$	$G = -1$ , 3V Step, $C_L = 100\text{pF}$	1.5		$\mu\text{s}$
Rated Output			(V-) + 0.5	(V+) - 0.5	V
Short-Circuit Current	$I_{\text{SC}}$		+4/-10		mA

**ELECTRICAL CHARACTERISTICS:  $V_S = +5V$  (continued)****Boldface** limits apply over the specified temperature range,  $T_A = -5^\circ\text{C}$  to  $+75^\circ\text{C}$ .All specifications at  $T_A = +25^\circ\text{C}$ ,  $R_{V\text{LOGOUT}} = 10\text{k}\Omega$ ,  $V_{\text{CM}} = +2.5\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	LOG114			UNITS
		MIN	TYP	MAX	
<b>TOTAL ERROR</b> (4, 5)		See Typical Characteristics			
<b>FREQUENCY RESPONSE, Core Log</b> (6) BW, 3dB $I_1$ or $I_2 =$	$I_{\text{AC}} = 10\%$ of $I_{\text{DC}}$ value, $I_{\text{REF}} = 1\mu\text{A}$				
1nA			5		kHz
10nA			12		kHz
100nA			120		kHz
1 $\mu\text{A}$			2.3		MHz
10 $\mu\text{A}$ to 1mA (ratio 1:100)			> 5		MHz
1mA to 3.5mA (ratio 1:3.5)			> 5		MHz
3.5mA to 10mA (ratio 1:2.9)			> 5		MHz
Step Response	$I_{\text{REF}} = 1\mu\text{A}$				
Increasing ( $I_1$ or $I_2$ )					
8nA to 240nA (ratio 1:30)			0.7		$\mu\text{s}$
10nA to 100nA (ratio 1:10)			1.5		$\mu\text{s}$
10nA to 1 $\mu\text{A}$ (ratio 1:100)			0.15		$\mu\text{s}$
10nA to 10 $\mu\text{A}$ (ratio 1:1k)			0.07		$\mu\text{s}$
10nA to 1mA (ratio 1:100k)			0.06		$\mu\text{s}$
1mA to 10mA (ratio 1:10)			1		$\mu\text{s}$
Decreasing ( $I_1$ or $I_2$ )	$I_{\text{REF}} = 1\mu\text{A}$				
8nA to 240nA (ratio 1:30)			1		$\mu\text{s}$
10nA to 100nA (ratio 1:10)			2		$\mu\text{s}$
10nA to 1 $\mu\text{A}$ (ratio 1:100)			0.25		$\mu\text{s}$
10nA to 10 $\mu\text{A}$ (ratio 1:1k)			0.05		$\mu\text{s}$
10nA to 1mA (ratio 1:100k)			0.03		$\mu\text{s}$
1mA to 10mA (ratio 1:10)			1		$\mu\text{s}$
<b>VOLTAGE REFERENCE</b>					
Bandgap Voltage			2.5		V
Error, Initial			$\pm 0.15$	$\pm 1$	%
<b>vs Temperature</b>			<b><math>\pm 25</math></b>		<b>ppm/<math>^\circ\text{C}</math></b>
vs Supply	$V_S = +4.8\text{V}$ to $+11\text{V}$		$\pm 30$		ppm/V
vs Load	$I_O = \pm 2\text{mA}$		$\pm 200$		ppm/mA
Short-Circuit Current			$\pm 10$		mA
<b>POWER SUPPLY</b>					
Single Supply Operating Range	$V_S$	4.8		11	V
Quiescent Current	$I_Q$		$\pm 10$	$\pm 15$	mA
<b>TEMPERATURE RANGE</b>					
Specification, $T_{\text{MIN}}$ to $T_{\text{MAX}}$		-5		+75	$^\circ\text{C}$
Operating		-40		+85	$^\circ\text{C}$
Storage		-55		+125	$^\circ\text{C}$
Thermal Resistance, $\theta_{\text{JA}}$			62		$^\circ\text{C/W}$

(1) Log conformity error is peak deviation from the best-fit straight line of  $V_O$  vs  $\text{Log}(I_1/I_2)$  curve expressed as a percent of peak-to-peak full-scale output. Scale factor,  $K$ , equals 0.375V output per decade of input current.

(2) Scale factor of core log function is trimmed to 0.375V output per decade change of input current.

(3) Specified by design.

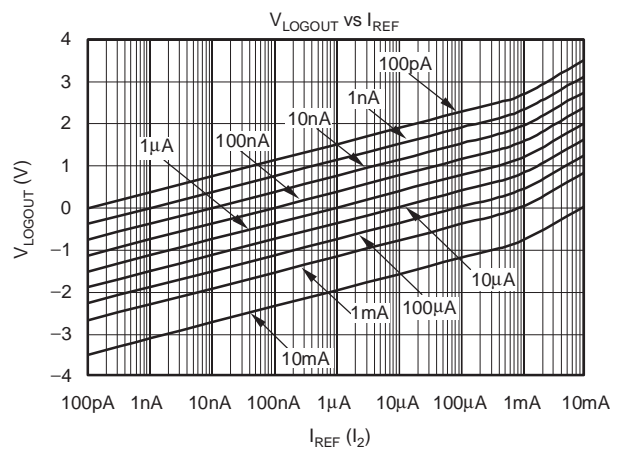
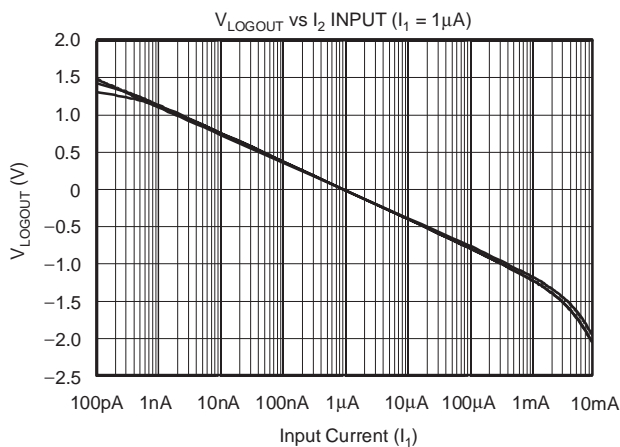
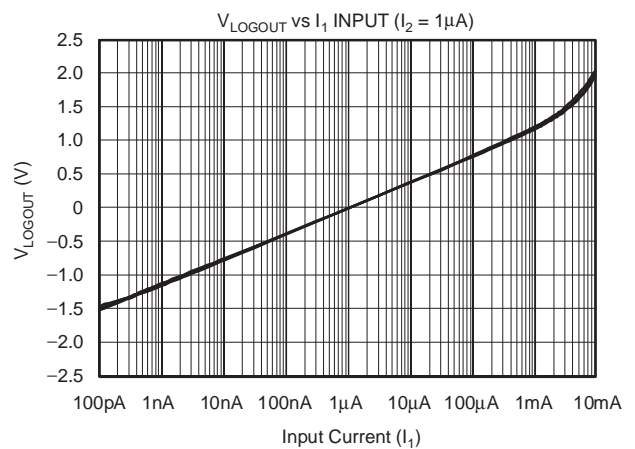
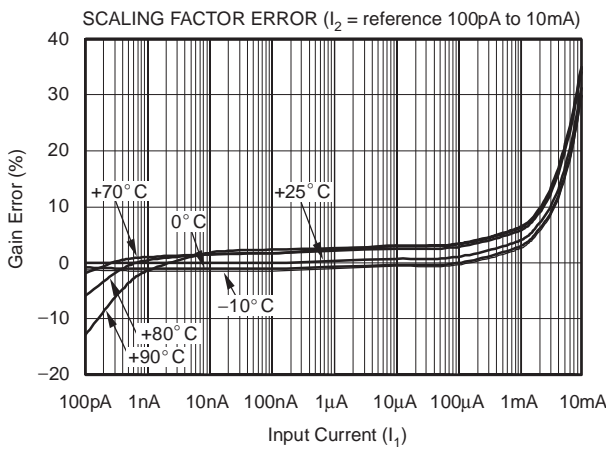
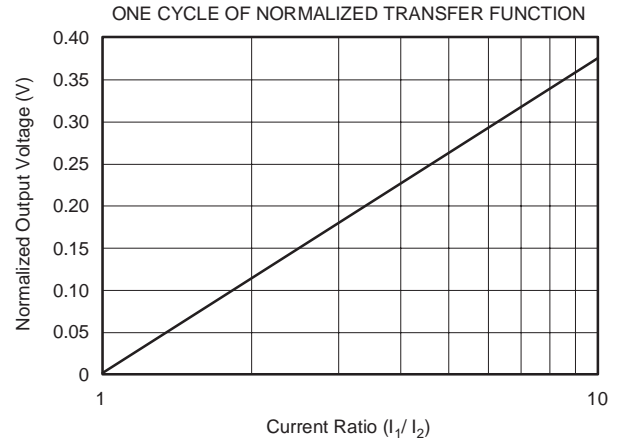
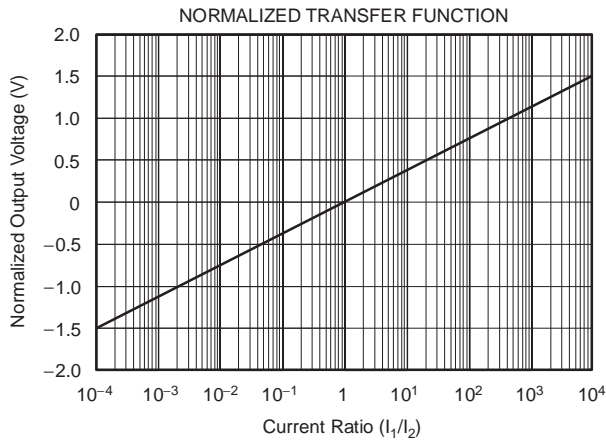
(4) Worst-case total error for any ratio of  $I_1/I_2$ , as the largest of the two errors, when  $I_1$  and  $I_2$  are considered separately.

(5) Total error includes offset voltage, bias current, gain, and log conformity.

(6) Small signal bandwidth (3dB) and transient response are a function of the level of input current. Smaller input current amplitude results in lower bandwidth.

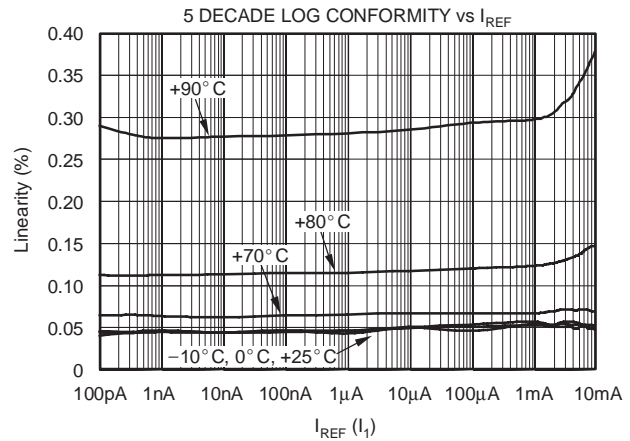
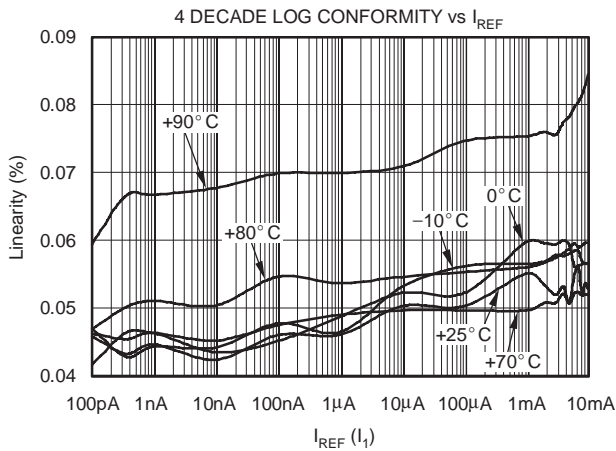
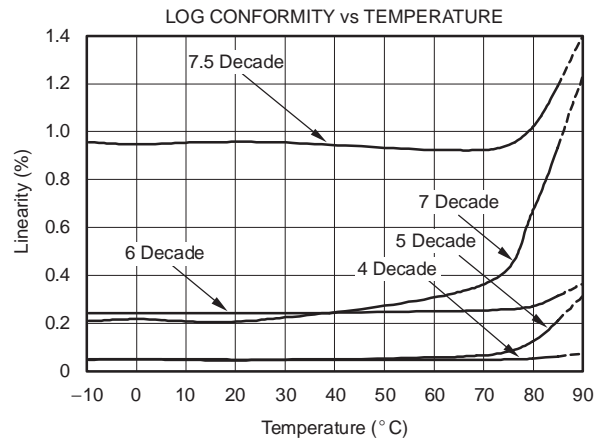
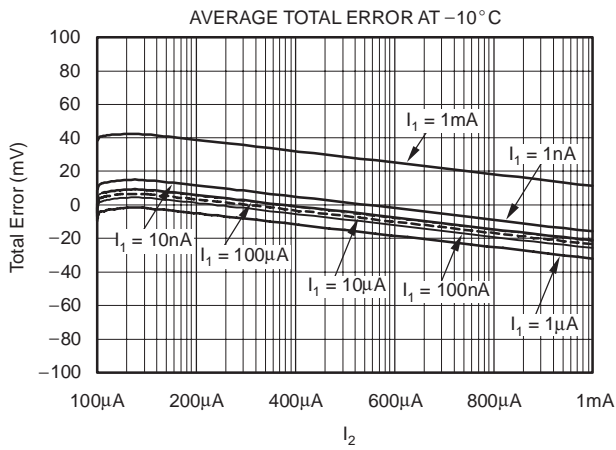
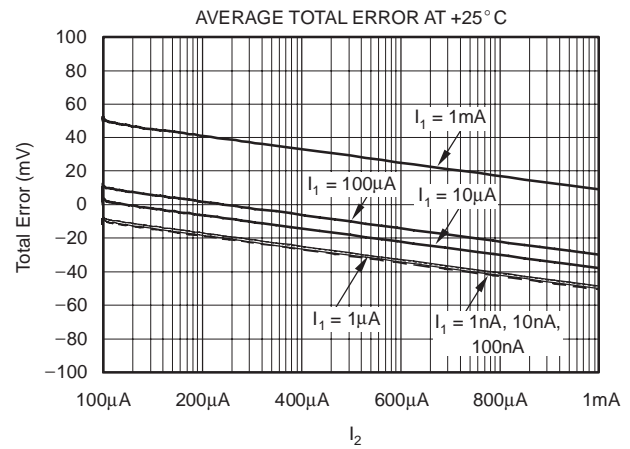
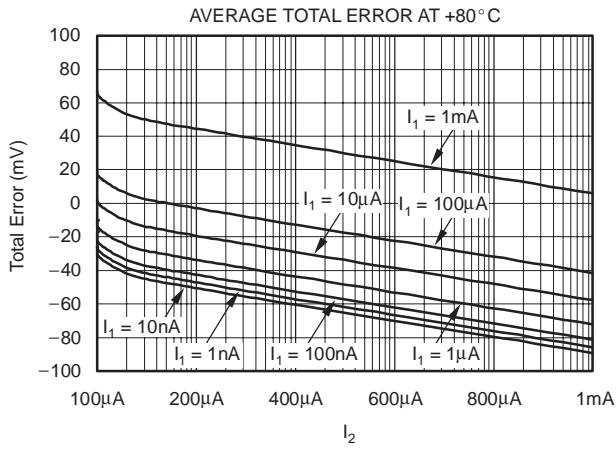
## TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

All specifications at  $T_A = +25^\circ\text{C}$ ,  $R_{V\text{LOGOUT}} = 10\text{k}\Omega$ ,  $V_{\text{CM}} = \text{GND}$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

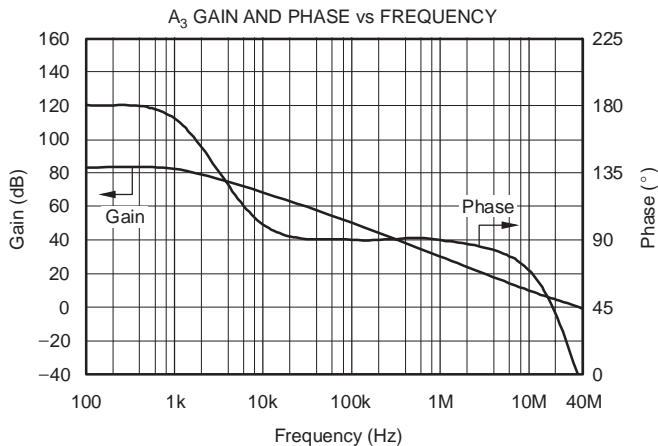
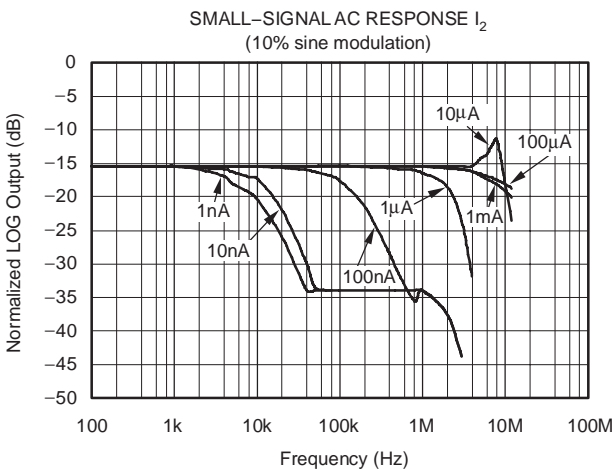
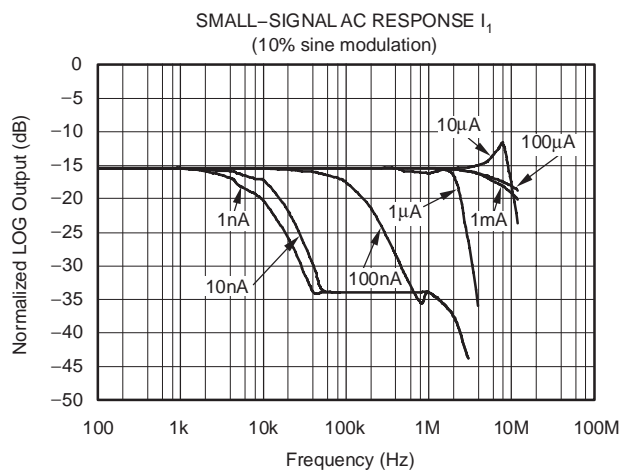
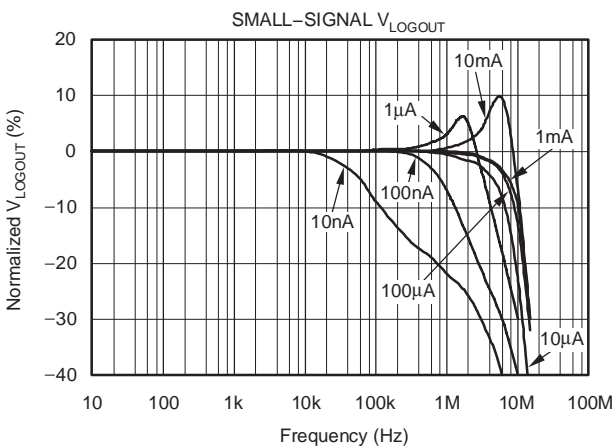
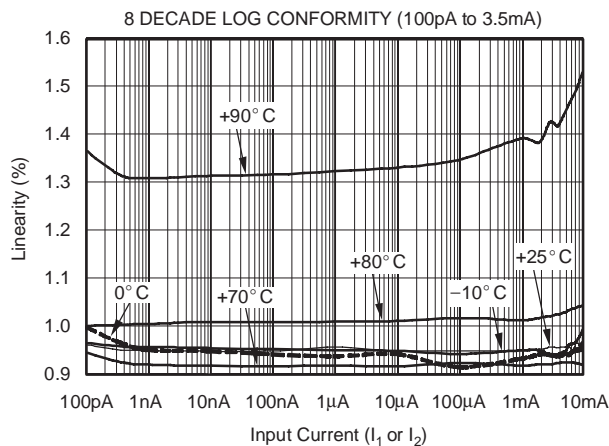
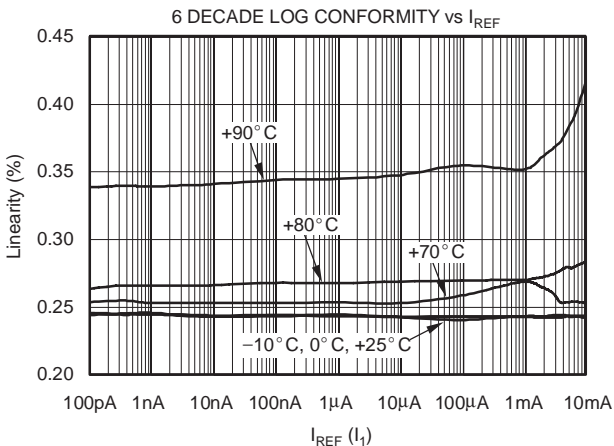
All specifications at  $T_A = +25^\circ C$ ,  $R_{VLOGOUT} = 10k\Omega$ ,  $V_{CM} = GND$ , unless otherwise noted.





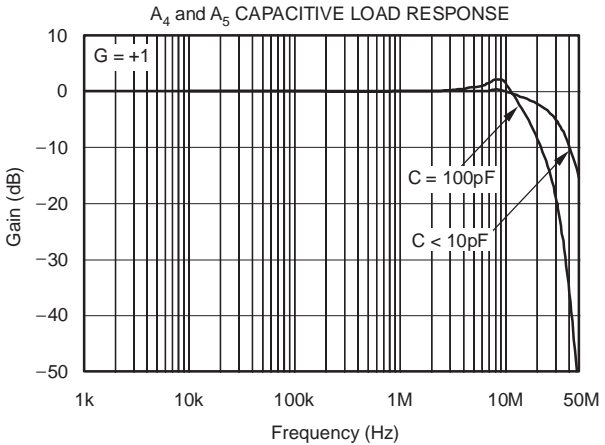
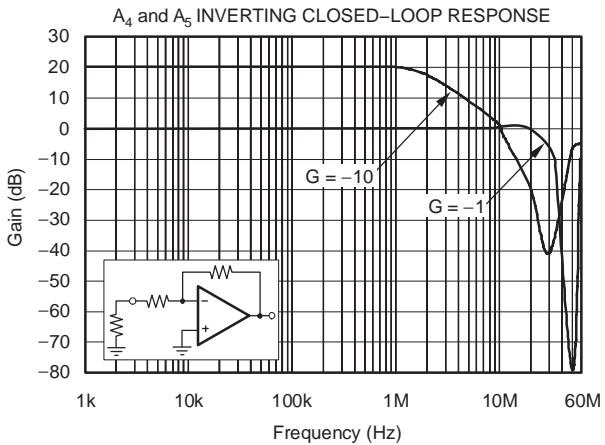
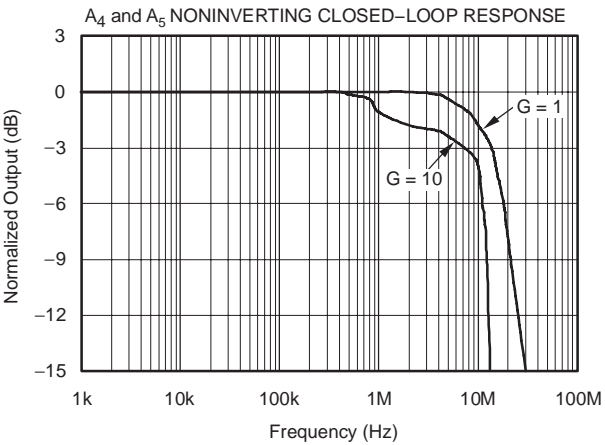
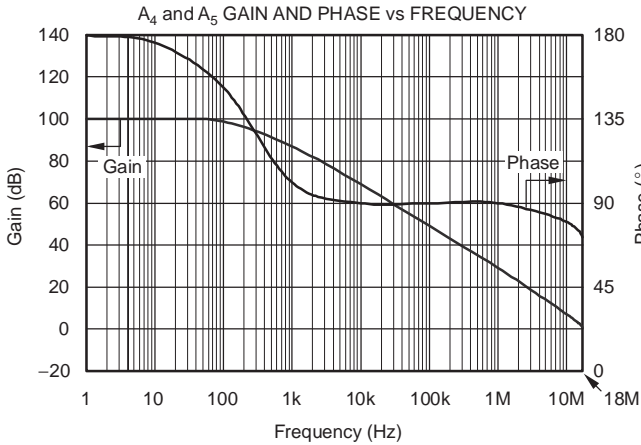
## TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

All specifications at  $T_A = +25^\circ C$ ,  $R_{V_{LOGOUT}} = 10k\Omega$ ,  $V_{CM} = GND$ , unless otherwise noted. For ac measurements, small signal means up to approximately 10% of dc level.



# TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

All specifications at  $T_A = +25^\circ C$ ,  $R_{VLOGOUT} = 10k\Omega$ ,  $V_{CM} = GND$ , unless otherwise noted.



## APPLICATIONS INFORMATION

### OVERVIEW

The LOG114 is a precision logarithmic amplifier that is capable of measuring currents over a dynamic range of eight decades. It computes the logarithm, or log ratio, of an input current relative to a reference current according to equation (1).

$$V_{\text{LOGOUT}} = 0.375 \times \log_{10} \left( \frac{I_1}{I_2} \right) \quad (1)$$

The output at  $V_{\text{LOGOUT}}$  can be digitized directly, or scaled for an ADC input using an uncommitted or external op amp.

An offsetting voltage ( $V_{\text{Com}}$ ) can be connected to the Com pin to raise the voltage at  $V_{\text{LOGOUT}}$ . When an offsetting voltage is used, the transfer function becomes:

$$V_{\text{LOGOUT}} = 0.375 \times \log_{10} \left( \frac{I_1}{I_2} \right) + V_{\text{Com}} \quad (2)$$

Either  $I_1$  or  $I_2$  can be held constant to serve as the reference current, with the other input being used for the input signal. The value of the reference current is selected such that the output at  $V_{\text{LOGOUT}}$  (pin 9) is zero when the reference current and input current are equal. An on-chip 2.5V reference is provided for use in generating the reference current.

Two additional amplifiers,  $A_4$  and  $A_5$ , are included in the LOG114 for use in scaling, offsetting, filtering, threshold detection, or other functions.

### BASIC CONNECTIONS

Figure 1 and Figure 2 show the LOG114 in typical dual and single-supply configurations, respectively. To reduce the influence of lead inductance of power-supply lines, it is recommended that each supply be bypassed with a 10 $\mu$ F tantalum capacitor in parallel with a 1000pF ceramic capacitor as shown in Figure 1 and Figure 2. Connecting these capacitors as close to the LOG114  $V+$  supply pin to ground as possible improves supply-related noise rejection.

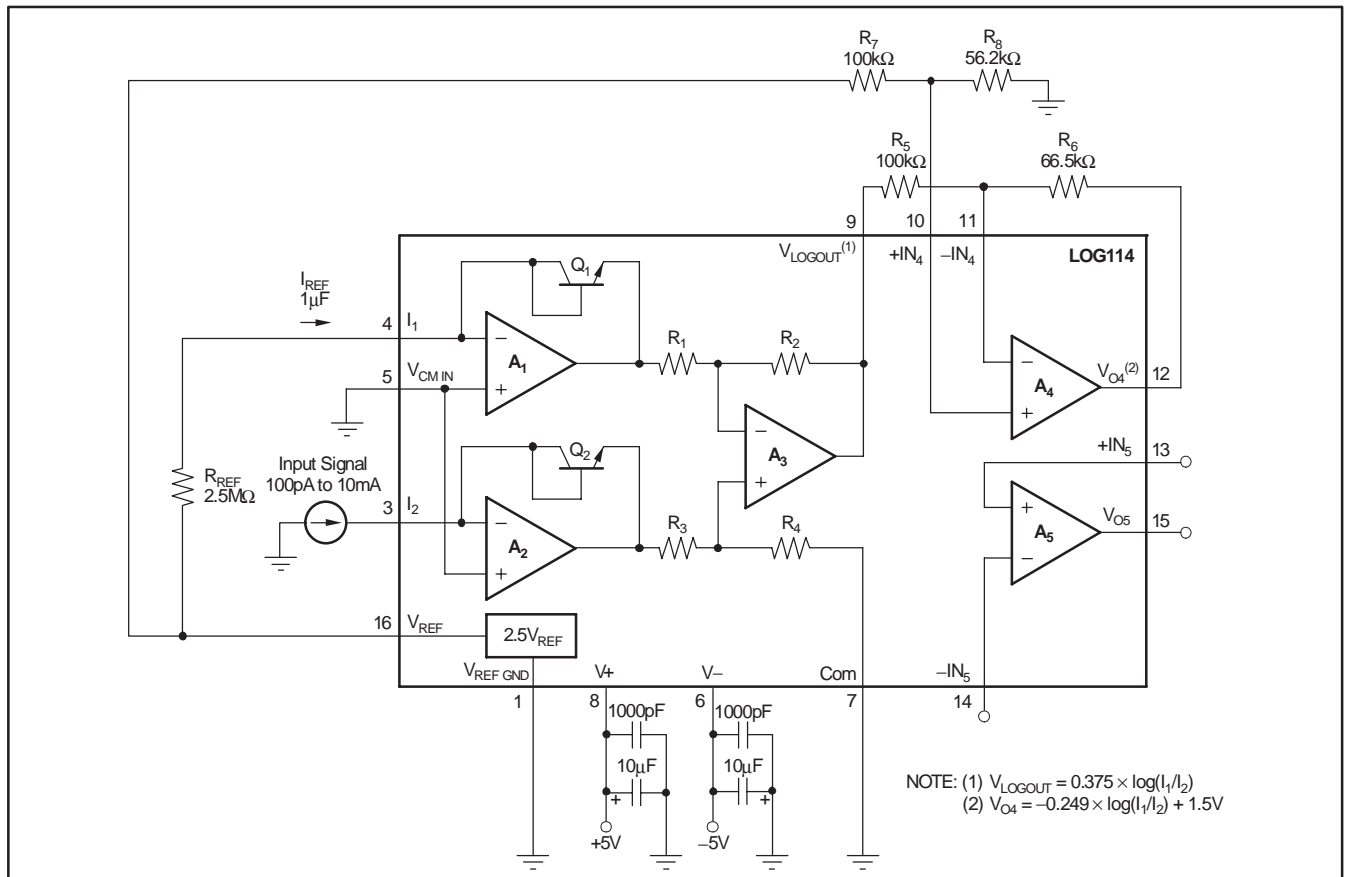


Figure 1. Dual Supply Configuration Example for Best Accuracy Over Eight Decades.

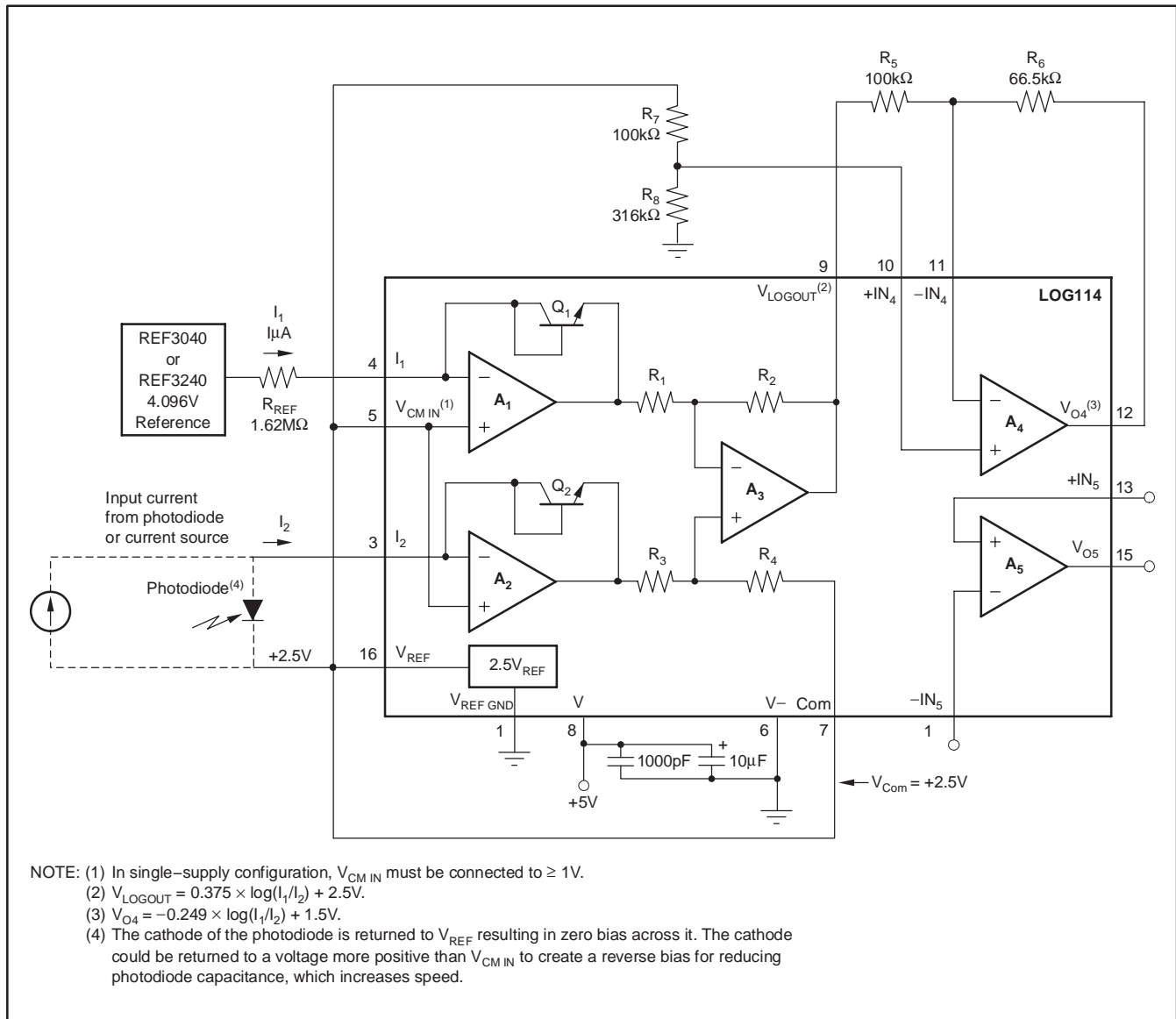


Figure 2. Single-Supply Configuration Example for Measurement Over Eight Decades.

**DESIGN EXAMPLE FOR DUAL-SUPPLY CONFIGURATION**

Given these conditions:

- $V_+ = 5V$  and  $V_- = -5V$
  - $100pA \leq$  Input signal
  - The stage following the LOG114 is an analog-to-digital converter (ADC) with +5V supply and +2.5V reference voltage, so  $V_{O4}$  swings from +0.5V to +2.5V.
1. Due to LOG114 symmetry, you can choose either  $I_1$  or  $I_2$  as the signal input pin. Choosing  $I_1$  as the reference makes the resistor network around  $A_4$  simpler. (Note: Current must flow into pins 3 ( $I_1$ ) and pin 4 ( $I_2$ ).)
  2. Select the magnitude of the reference current. Since the signal ( $I_2$ ) spans eight decades, set  $I_1$  to  $1\mu A$  – four decades above the minimum  $I_2$  value. (Note that it does not have to be placed in the middle. If  $I_2$  spanned seven decades,  $I_1$  could be set three decades above the minimum and four decades below the maximum  $I_2$  value.) This configuration results in more swing amplitude in the negative direction, which provides more sensitivity ( $\Delta V_{O4}$  per  $\Delta I_2$ ) when the current signal decreases.
  3. Using Equation (1) calculate the expected range of log outputs at  $V_{LOGOUT}$ :

For  $I_2 = 10mA$  :

$$\begin{aligned}
 V_{LOGOUT} &= 0.375 \times \log\left(\frac{I_1}{I_2}\right) \\
 &= 0.375 \times \log\left(\frac{1\mu A}{10mA}\right) = -1.5V
 \end{aligned}$$

For  $I_2 = 100pA$  :

$$\begin{aligned}
 V_{LOGOUT} &= 0.375 \times \log\left(\frac{I_1}{I_2}\right) \\
 &= 0.375 \times \log\left(\frac{1\mu A}{100pA}\right) = +1.5V
 \end{aligned}
 \tag{3}$$

Therefore, the expected voltage range at the output of amplifier  $A_3$  is:

$$-1.5V \leq V_{LOGOUT} \leq +1.5V \tag{4}$$

4. The  $A_4$  amplifier scales and offsets the  $V_{LOGOUT}$  signal for use by the ADC using the equation:

$$V_{O4} = -S_{FACTOR} \times (V_{LOGOUT}) + V_{OFFSET} \tag{5}$$

The  $A_4$  amplifier is specified with a rated output swing capability from  $(V_-) +0.5V$  to  $(V_+) - 0.5V$ .

Therefore, choose the final  $A_4$  output:

$$0V \leq V_{O4} \leq +2.5V$$

This output results in a 2.5V range for the 3V  $V_{LOGOUT}$  range, or 2.5V/3V scaling factor.

5. When  $I_2 = 10mA$ ,  $V_{LOGOUT} = -1.5V$ . Using the equation in step 5:

$$\begin{aligned}
 V_{O4} &= -S_{FACTOR} \times (V_{LOGOUT}) + V_{OFFSET} \\
 0V &= -2.5V/3V(-1.5V) + V_{OFFSET}
 \end{aligned}
 \tag{6}$$

Therefore,  $V_{OFFSET} = 0V$

The  $A_4$  amplifier configuration for  $V_{O4} = -2.5/3(V_{LOGOUT}) + 0V$  is seen in Figure 3.

The overall transfer function is:

$$V_{O4} = -0.249 \times \log\left(\frac{I_1}{I_2}\right) + 1.5V \tag{7}$$

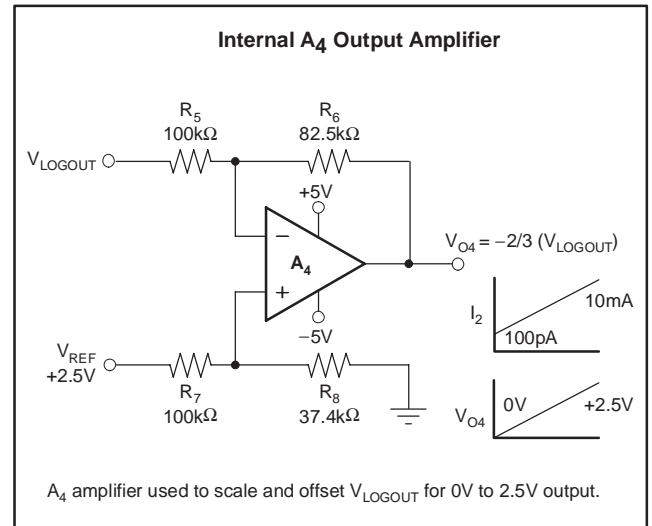


Figure 3. Operational Amplifier Configuration for Scaling the Output Going to ADC Stage.

## DESIGN EXAMPLE FOR SINGLE-SUPPLY CONFIGURATION

Given these conditions:

- $V_+ = 5V$
  - $V_- = GND$
  - $100pA \leq \text{Input signal} \leq 10mA$
  - The stage following the LOG114 is an analog to digital converter (ADC) with +5V supply and +2.5V reference voltage
1. Choose either  $I_1$  or  $I_2$  as the signal input pin. For this example,  $I_2$  is used. Choosing  $I_1$  as the reference current makes the resistor network around  $A_4$  simpler. (Note: Current only flows into the  $I_1$  and  $I_2$  pins.)
  2. Select the magnitude of the reference current. Since the signal ( $I_2$ ) spans eight decades, set  $I_1$  to  $1\mu A$  – four decades above the minimum  $I_2$  value, and four decades below the maximum  $I_2$  value. (Note that it does not have to be placed in the middle. If  $I_2$  spanned seven decades,  $I_1$  could be set three decades above the minimum and four decades below the maximum  $I_2$  value.) This configuration results in more swing amplitude in the negative direction, which provides more sensitivity ( $\Delta V_{O4}$  per  $\Delta I_2$ ) when the current signal decreases.
  3. Using Equation (1) calculate the expected range of log outputs at  $V_{LOGOUT}$ :

For  $I_2 = 10mA$  :

$$\begin{aligned} V_{LOGOUT} &= 0.375 \times \log\left(\frac{I_1}{I_2}\right) \\ &= 0.375 \times \log\left(\frac{1\mu A}{10mA}\right) = -1.5V \end{aligned}$$

For  $I_2 = 100pA$  :

$$\begin{aligned} V_{LOGOUT} &= 0.375 \times \log\left(\frac{I_1}{I_2}\right) \\ &= 0.375 \times \log\left(\frac{1\mu A}{100pA}\right) = +1.5V \end{aligned} \quad (8)$$

Therefore, the expected voltage range at the output of amplifier  $A_3$  is:

$$-1.5V \leq V_{LOGOUT} \leq +1.5V \quad (9)$$

This result would be fine in a dual-supply system ( $V_+ = +5V$ ,  $V_- = -5V$ ) where the output can swing below ground, but does not work in a single supply +5V system. Therefore, an offset voltage must be added to the system.

4. Select an offset voltage,  $V_{Com}$  to use for centering the output between  $(V_-) + 0.6V$  and  $(V_+) - 0.6V$ , which is the full-scale output capability of the  $A_3$  amplifier. Choosing  $V_{Com} = 2.5V$ , and recalculating the expected voltage output range for  $V_{LOGOUT}$  using Equation (2), results in:

$$+1V \leq V_{LOGOUT} \leq +4V \quad (10)$$

5. The  $A_4$  amplifier scales and offsets the  $V_{LOGOUT}$  signal for use by the ADC using the equation:

$$V_{O4} = -S_{FACTOR} \times (V_{LOGOUT}) + V_{OFFSET} \quad (11)$$

The  $A_4$  amplifier is specified with a rated output swing capability from  $(V_-) + 0.5V$  to  $(V_+) - 0.5V$ .

Therefore, choose the final  $A_4$  output:

$$+0.5V \leq V_{O4} \leq +2.5V$$

This output results in a 2V range for the 3V  $V_{LOGOUT}$  range, or 2V/3V scaling factor.

6. When  $I_2 = 10mA$ ,  $V_{LOGOUT} = +1V$ , and  $V_{O4} = 2.5V$ . Using the equation in step 5:

$$\begin{aligned} V_{O4} &= -S_{FACTOR} \times (V_{LOGOUT}) + V_{OFFSET} \\ 2.5V &= -2V/3V(1V) + V_{OFFSET} \end{aligned} \quad (12)$$

Therefore,  $V_{OFFSET} = 3.16V$

The  $A_4$  amplifier configuration for  $V_{O4} = -2/3(V_{LOGOUT}) + 3.16$  is seen in Figure 4a.

The overall transfer function is:

$$V_{O4} = -0.249 \times \log\left(\frac{I_1}{I_2}\right) + 1.5V \quad (13)$$

A similar process can be used for configuring an external rail-to-rail output op amp, such as the OPA335. Because the OPA335 op amp can swing down to 0V using a pulldown resistor,  $R_P$ , connected to  $-5V$  (for details, refer to the OPA335 data sheet, available for download at [www.ti.com](http://www.ti.com)), the scaling factor is 2.5V/3V and the corresponding  $V_{OFFSET}$  is 3.3V. This circuit configuration is shown in Figure 4b.

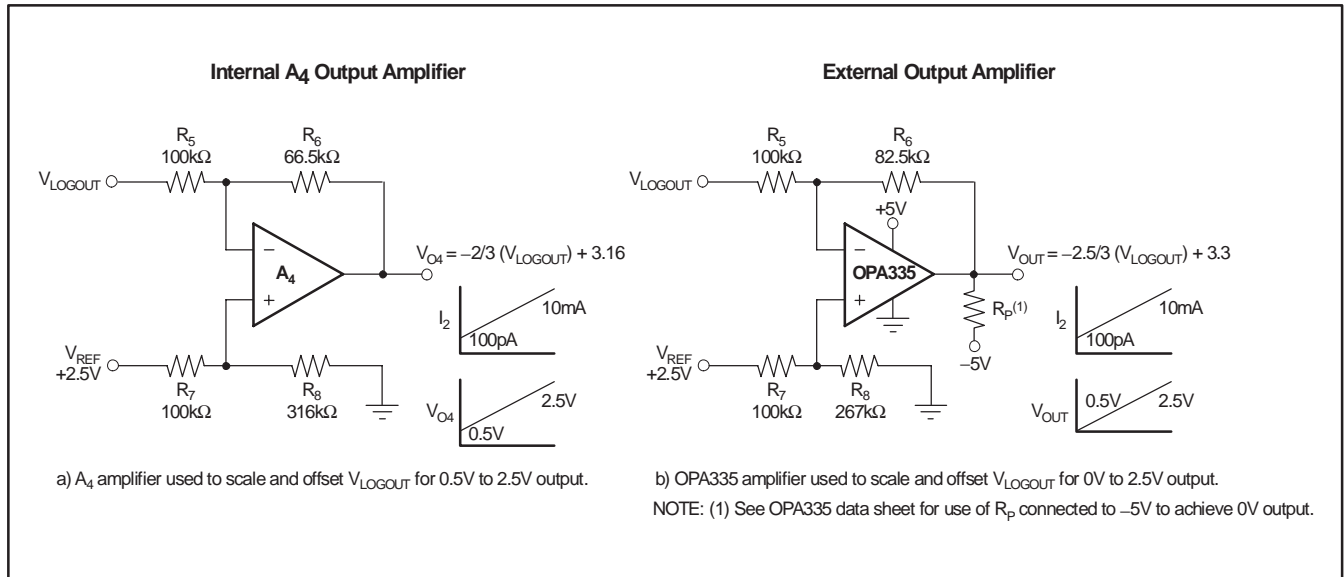


Figure 4. Operational Amplifier Configuration for Scaling and Offsetting the Output Going to ADC Stage.

### ADVANTAGES OF DUAL-SUPPLY OPERATION

The LOG114 performs very well on a single +5V supply by level-shifting pin 7 (Com) to half-supply and raising the common-mode voltage (pin 5,  $V_{CM IN}$ ) of the input amplifiers. This level-shift places the input amplifiers in the linear operating range. However, there are also some advantages to operating the LOG114 on dual  $\pm 5V$  supplies. These advantages include:

- 1) eliminating the need for the +4.096V precision reference;
- 2) eliminating a small additional source of error arising from the noise and temperature drift of the level-shifting voltage; and
- 3) allowing increased magnitude of a reverse bias voltage on the photodiode.

### COM (PIN 7) VOLTAGE RANGE

The voltage on the Com pin is used to bias the differential amplifier,  $A_3$ , within its linear range. This voltage can provide an asymmetrical offset of the  $V_{LOGOUT}$  voltage.

### $V_{CM IN}$ (Pin 5)

The  $V_{CM IN}$  pin is used to bias the  $A_1$  and  $A_2$  amplifier into its common-mode input voltage range,  $(V-) + 1.5V$  to  $(V+) - 1.5V$ .

### INPUT CURRENT RANGE

To maintain specified accuracy, the input current range of the LOG114 should be limited from 100pA to 3.5mA. Input currents outside of this range may compromise the LOG114 performance. Input currents larger than 3.5mA result in increased nonlinearity. An absolute maximum input current rating of 10mA is included to prevent excessive power dissipation that may damage the input transistor.

**SETTING THE REFERENCE CURRENT**

When the LOG114 is used to compute logarithms, either  $I_1$  or  $I_2$  can be held constant to become the reference current to which the other is compared.

If  $I_{REF}$  is set to the lowest current in the span of the signal current (as shown in the front page figure),  $V_{LOGOUT}$  will range from:

$$V_{LOGOUT} = 0.375 \times \log_{10} \left( \frac{I_1 \text{ min}}{I_1 \text{ max signal}} \right) \cong 0V \tag{14}$$

to some maximum value:

$$V_{LOGOUT} = 0.375 \times \log_{10} \left( \frac{I_1 \text{ min}}{I_1 \text{ max signal}} \right) \tag{15}$$

While convenient, this approach does not usually result in best performance, because  $I_1$  min accuracy is difficult to achieve, particularly if it is  $< 20nA$ .

A better way to achieve higher accuracy is to choose  $I_{REF}$  to be in the center of the full signal range. For example, for a signal range of 1nA to 1mA, it is better to use this approach:

$$I_{REF} = I_{SIGNAL \text{ min}} \times \sqrt{1mA/1nA} = 1\mu A \text{ dc} \tag{16}$$

than it is to set  $I_{REF} = 1nA$ . It is much easier and more precise (that is, dc accuracy, temperature stability, and lower noise) to establish a 1mA dc current level than a 1nA level for the reference current.

The reference current may be derived from a voltage source with one or more resistors. When a single resistor is used, the value may be large depending on  $I_{REF}$ . If  $I_{REF}$  is 10nA and +2.5V is used:

$$R_{REF} = 2.5V/10nA = 250M\Omega$$

A voltage divider may be used to reduce the value of the resistor, as shown in Figure 5. When using this method, one must consider the possible errors caused by the amplifier input offset voltage. The input offset voltage of amplifier  $A_1$  has a maximum value of 4mV in a  $\pm 5V$  supply system, and a maximum value of 7mV in a +5V supply system. Resistor temperature stability and noise contributions should also be considered.

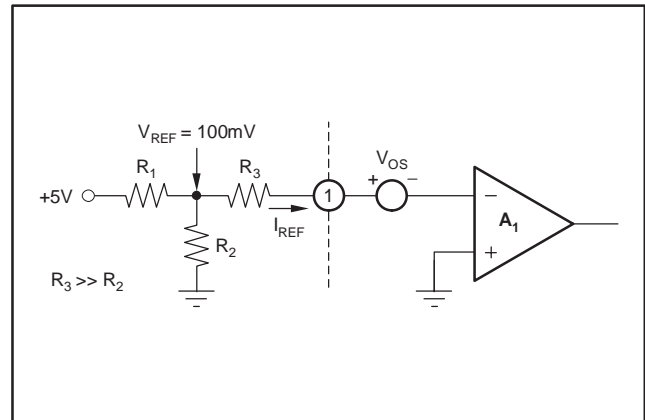


Figure 5. T-Network for Reference Current.

$V_{REF}$  may be an external precision voltage reference, or the on-chip 2.5V voltage reference of the LOG114.

$I_{REF}$  can be derived from an external current source, such as that shown in Figure 6.

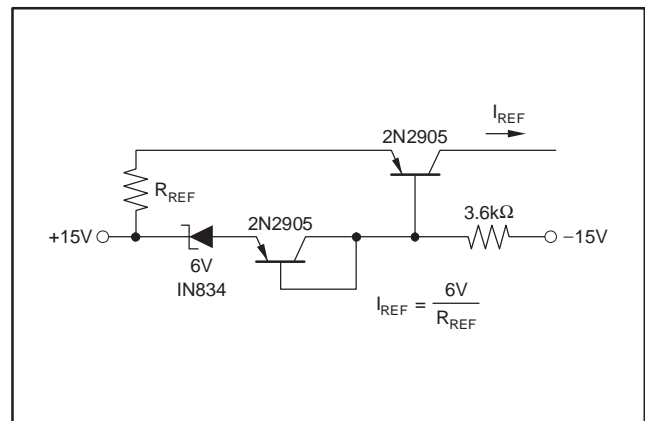


Figure 6. Temperature-Compensated Current Source.



**NEGATIVE INPUT CURRENTS**

The LOG114 functions only with positive input currents (conventional current flows into input current pins). In

situations where negative input currents are needed, the example circuits in Figure 7, Figure 8, and Figure 9 may be used.

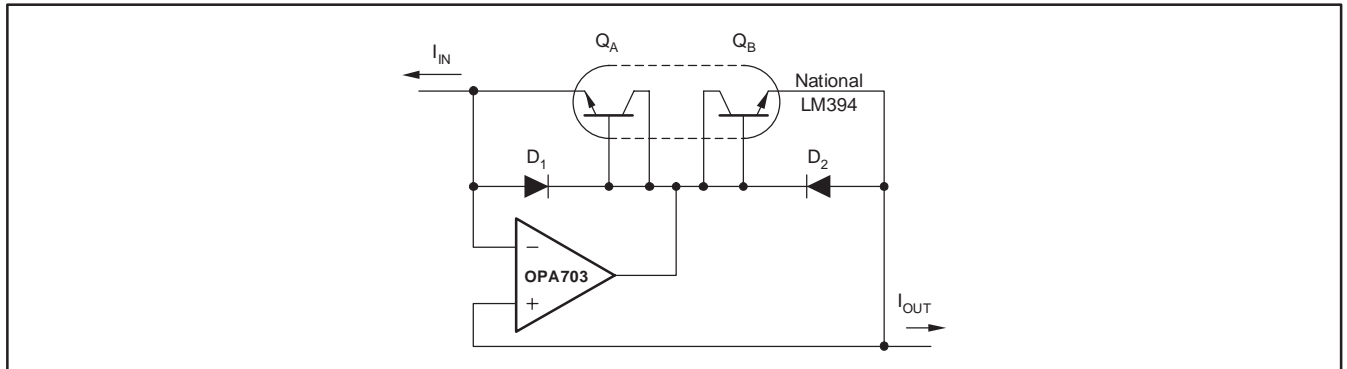


Figure 7. Current Inverter/Current Source.

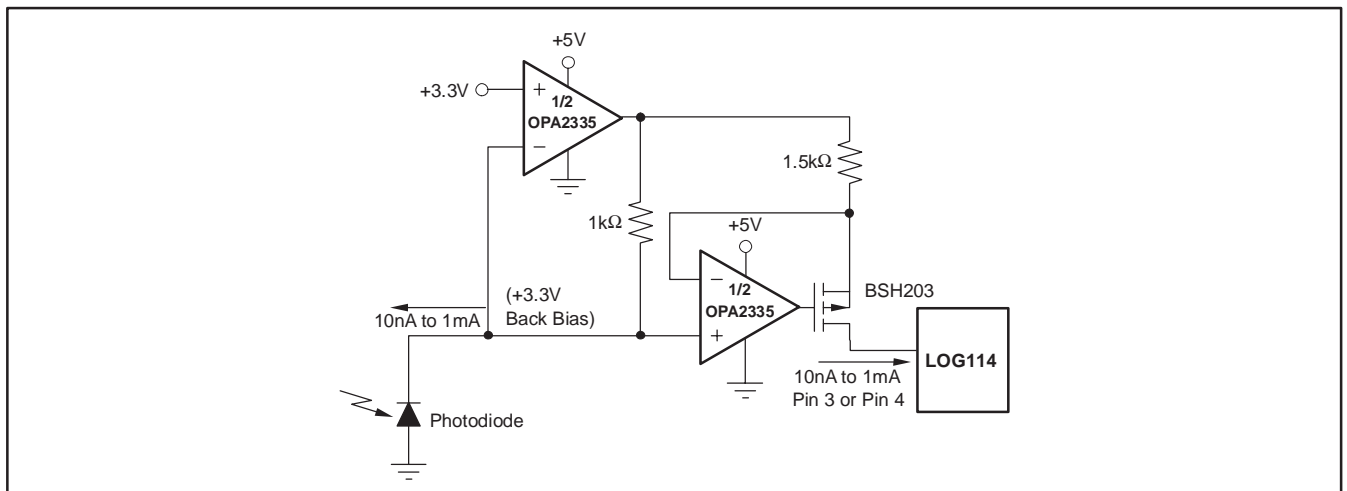


Figure 8. Precision Current Inverter/Current Source.

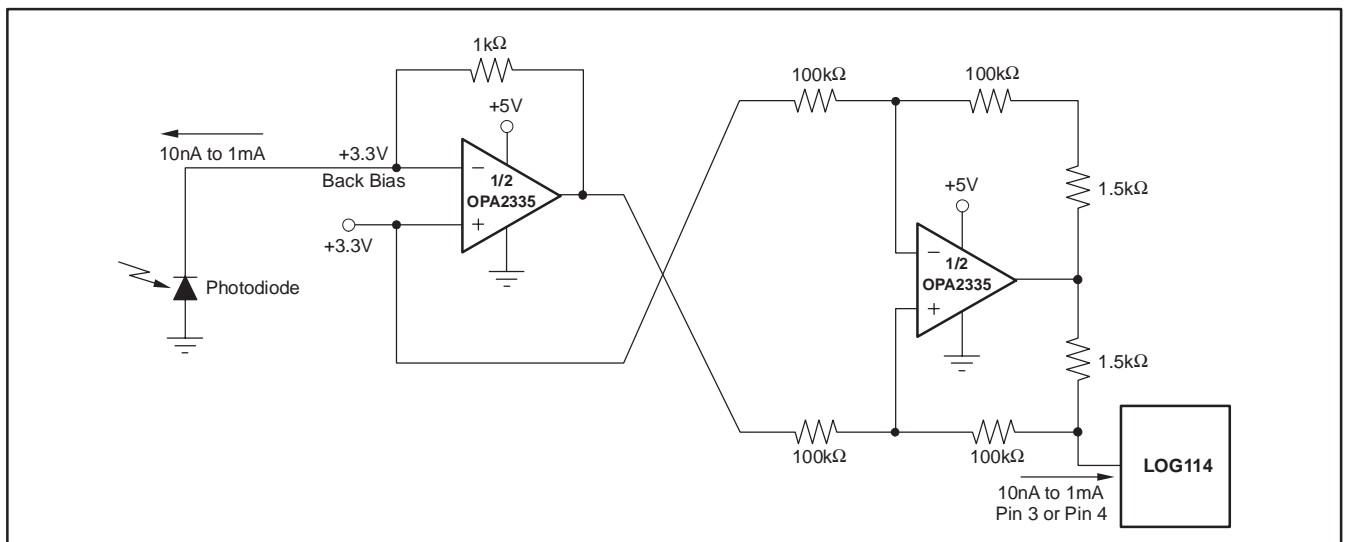


Figure 9. Precision Current Inverter/Current Source.

**VOLTAGE INPUTS**

The LOG114 provides the best performance with current inputs. Voltage inputs may be handled directly by using a low-impedance voltage source with series resistors, but the dynamic input range is limited to approximately three decades of input voltage. This limitation exists because of the magnitude of the required input voltage and size of the corresponding series resistor. For 10nA of input current, a 10V voltage source and a 1GΩ resistor would be required. Voltage and current

noise from these sources must be considered and can limit the usefulness of this technique.

**APPLICATION CIRCUITS**

**LOG RATIO**

One of the more common uses of log ratio amplifiers is to measure absorbance. See Figure 10 for a typical application. Absorbance of the sample is  $A = \log \lambda_1'/\lambda_1$ . If  $D_1$  and  $D_2$  are matched,  $A \propto (0.375V) \log(I_1/I_2)$ .

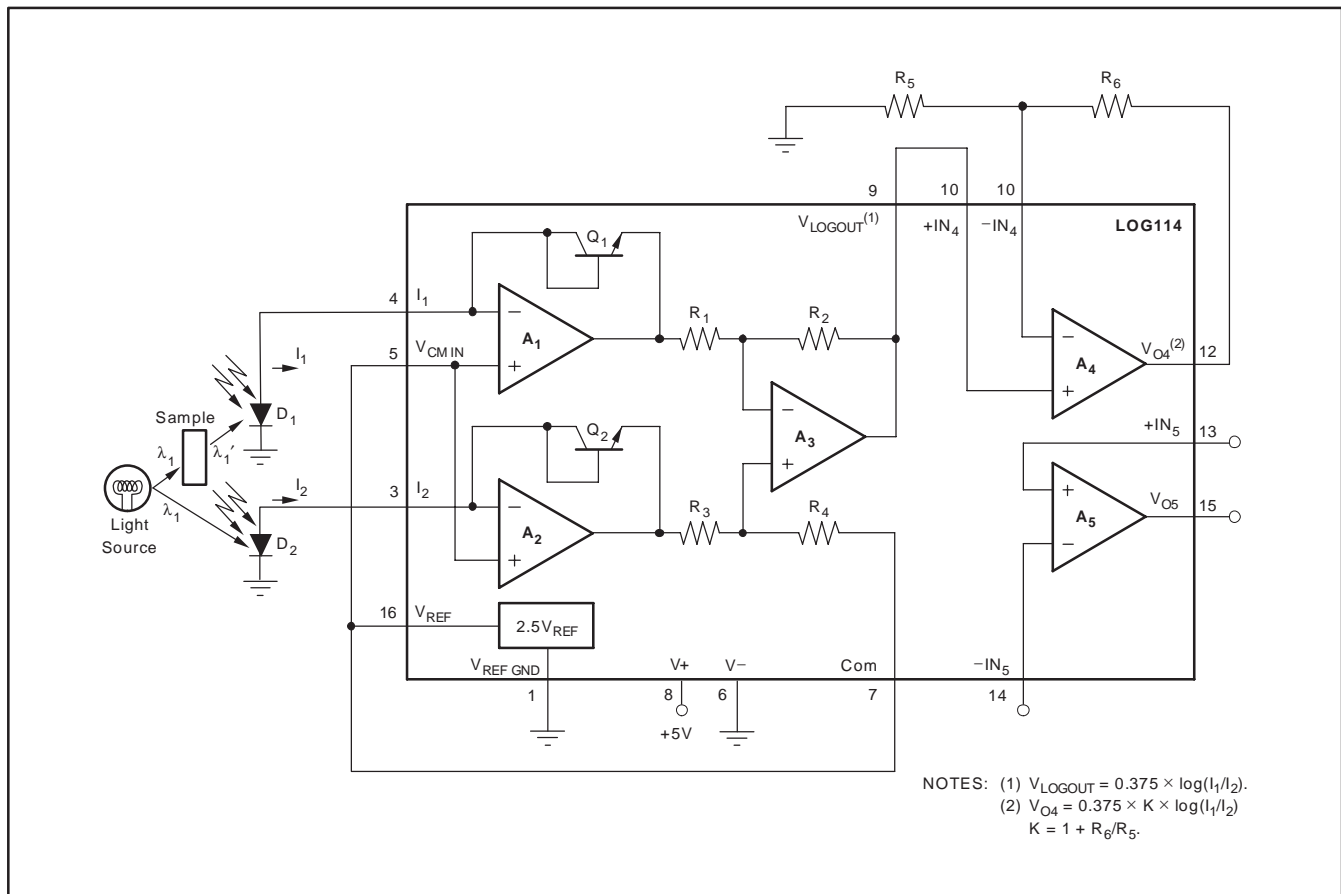


Figure 10. Using the LOG114 to Measure Absorbance.

**DATA COMPRESSION**

In many applications, the compressive effects of the logarithmic transfer function are useful. For example, a LOG114 preceding a 12-bit ADC can produce the dynamic range equivalent to a 20-bit converter. (Suggested products: ADS7818, ADS7834).

**+3.3V OPERATION**

For systems with only a +3.3V power supply, the TPS60241 zero-ripple switched cap buck-boost 2.7V to 5.5V input to 5V output converter may be used to generate a +5V supply for the LOG114, as shown in Figure 11.

Likewise, the TPS6040 negative charge pump may be connected to the +5V output of the TPS60241 to generate a -5V supply to create a ±5V supply for the LOG114, as Figure 12 illustrates.

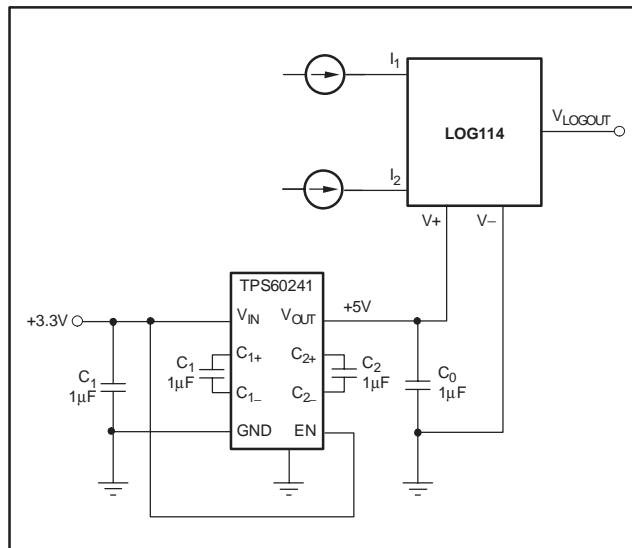


Figure 11. Creating a +5V Supply from a +3.3V Supply.

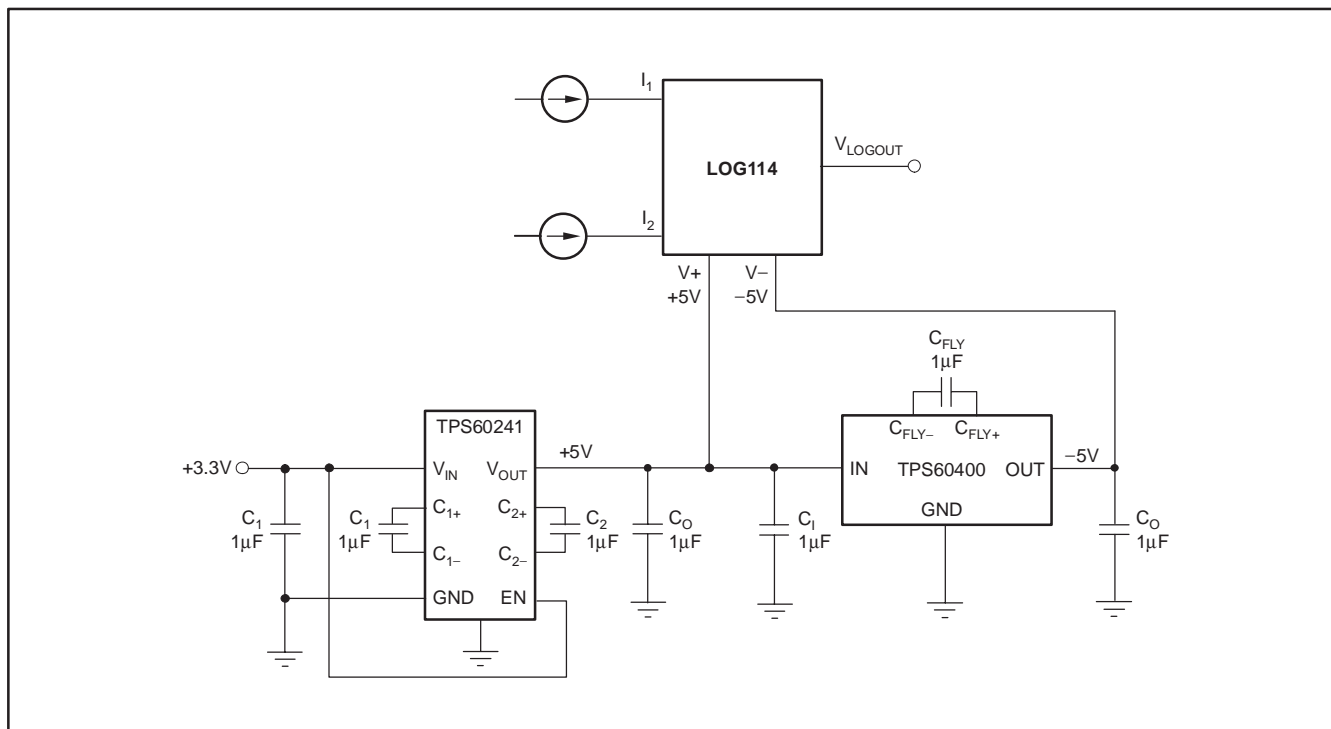


Figure 12. Creating a ±5V Supply from a +3.3V Supply.

## ERBIUM-DOPED FIBER OPTIC AMPLIFIER (EDFA)

The LOG114 was designed for optical networking systems. Figure 13 shows a block diagram of the LOG114 in a typical EDFA application. This application uses two log amps to measure the optical input and output power of the amplifier. A difference amplifier subtracts the log output signals of both log amps and applies an error voltage to the proportional-integral-derivative (PID) controller. The controller output adjusts a voltage-controlled current source ( $V_{CCS}$ ), which then drives the power op amp and pump laser. The desired optical gain is achieved when the error voltage at the PID is zero.

The log ratio function is the optical power gain of the EDFA. This circuitry forms an automatic power level control loop.

An alternate design of the system shown in Figure 13 is possible because the LOG114 inherently takes the log ratio. Therefore, one log amp can be eliminated by connecting one of the photodiodes to the LOG114  $I_1$  input, and the other to the  $I_2$  input. The differential amplifier would then be eliminated.

The LOG114 is uniquely suited for most EDFA applications because of its fast rise and fall times (typically less than  $1\mu\text{s}$  for a 100:1 current input step). It also measures a very wide dynamic range of up to eight decades.

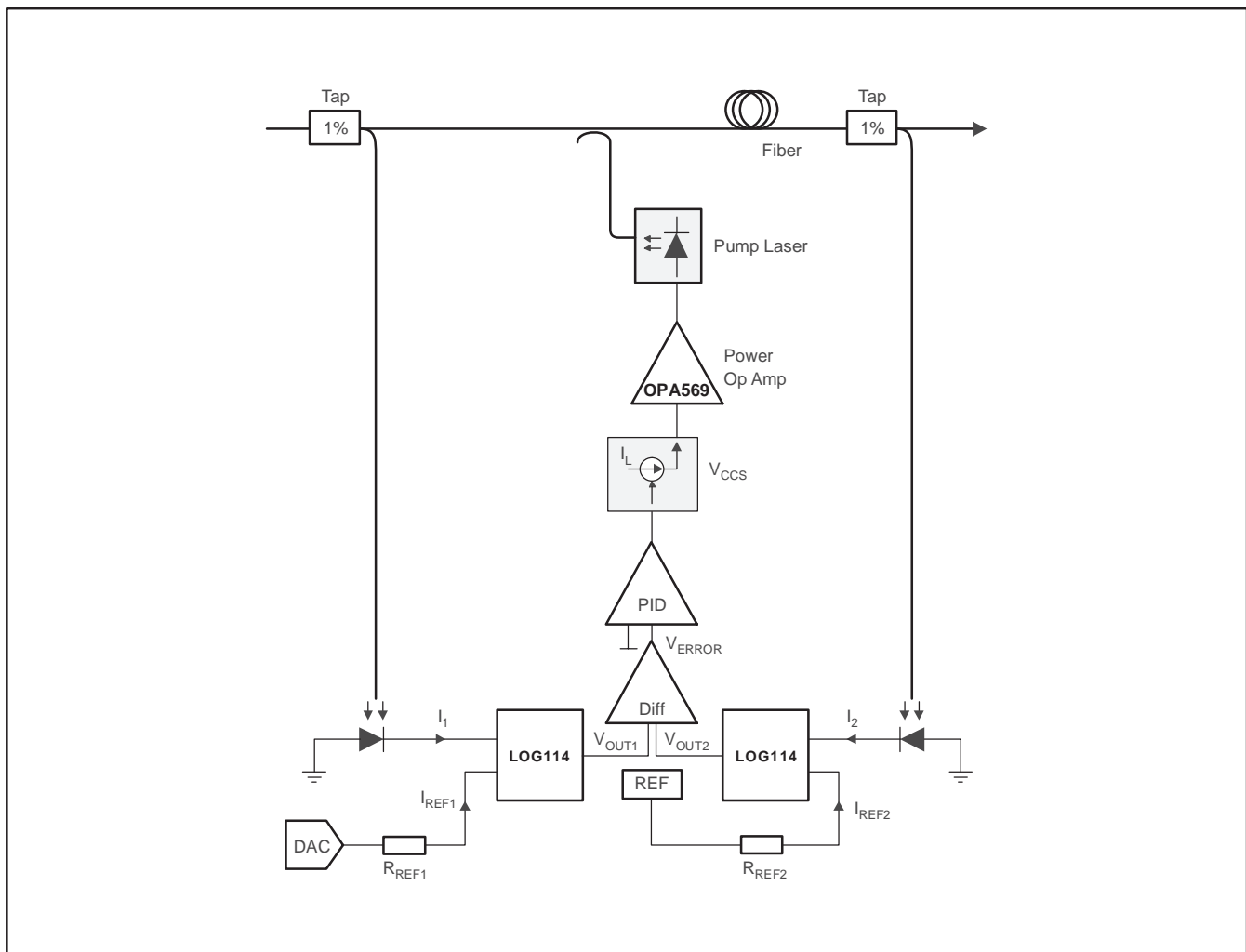


Figure 13. Erbium-Doped Fiber Optic Amplifier (EDFA) block diagram.

## INSIDE THE LOG114

The LOG114 uses two matched logarithmic amplifiers ( $A_1$  and  $A_2$  with logging diodes in the feedback loops) to generate the outputs  $\log(I_1)$  and  $\log(I_2)$ , respectively. The gain of 6.25 differential amplifier ( $A_3$ ) subtracts the output of  $A_2$  from the output of  $A_1$ , resulting in  $[\log(I_1) - \log(I_2)]$ , or  $\log(I_1/I_2)$ . The symmetrical design of the  $A_1$  and  $A_2$  logarithmic amps allows  $I_1$  and  $I_2$  to be used interchangeably, and provides good bandwidth and phase characteristics with frequency.

## DEFINITION OF TERMS

### Transfer Function

The ideal transfer function of the LOG114 is:

$$V_{\text{LOGOUT}} = 0.375 \times \log\left(\frac{I_1}{I_2}\right) \quad (17)$$

This transfer function can be seen graphically in the typical characteristic curve,  $V_{\text{LOGOUT}}$  vs  $I_{\text{REF}}$ .

When a pedestal, or offset, voltage ( $V_{\text{Com}}$ ) is connected to the Com pin, an additional offset term is introduced into the equation:

$$V_{\text{LOGOUT}} = 0.375 \times \log\left(\frac{I_1}{I_2}\right) + V_{\text{Com}} \quad (18)$$

### Accuracy

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. This complexity exists because the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

### Total Error

The total error is the deviation of the actual output from the ideal output. Thus,

$$V_{\text{LOGOUT(ACTUAL)}} = V_{\text{LOGOUT(IDEAL)}} \pm \text{Total Error}$$

It represents the sum of all the individual components of error normally associated with the log amp when operating in the current input mode. The worst-case error for any given ratio of  $I_1/I_2$  is the largest of the two errors when  $I_1$  and  $I_2$  are considered separately. Temperature can also affect total error.

### Errors RTO and RTI

As with any transfer function, errors generated by the function may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect, log amps have a unique property: given some error voltage at the log amp output, that error corresponds to a constant percent of the input, regardless of the actual input level.

## Log Conformity

For the LOG114, log conformity is calculated in the same way as linearity and is plotted as  $I_1/I_2$  on a semi-log scale. In many applications, log conformity is the most important specification. This condition is true because bias current errors are negligible (5pA for the LOG114), and the scale factor and offset errors may be trimmed to zero or removed by system calibration. These factors leave log conformity as the major source of error.

Log conformity is defined as the peak deviation from the best fit straight line of the  $V_{\text{LOGOUT}}$  versus  $\log(I_1/I_2)$  curve. Log conformity is then expressed as a percent of ideal full-scale output. Thus, the nonlinearity error expressed in volts over  $m$  decades is:

$$V_{\text{LOGOUT(NONLIN)}} = 0.375\text{V/decade} \cdot 2Nm$$

where  $N$  is the log conformity error, in percent.

## INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is:

$$V_{\text{LOGOUT IDEAL}} = 0.375 \times \log\left(\frac{I_1}{I_2}\right) \quad (19)$$

The actual transfer function with the major components of error is:

$$0.375(1 \pm \Delta K) \times \log\left(\frac{I_1}{I_2}\right) \pm 2Nm \pm V_{\text{OSO}} \quad (20)$$

where:

$\Delta K$  = gain error (0.4%, typ, as specified in the *Electrical Characteristics* table)

$I_{B1}$  = bias current of  $A_1$  (5pA, typ)

$I_{B2}$  = bias current of  $A_2$  (5pA, typ)

$m$  = number of decades over which the log conformity error is specified

$N$  = log conformity error (0.1%, typ for  $m = 5$  decades; 0.9% typ for  $m = 7.5$  decades)

$V_{\text{OSO}}$  = output offset voltage (11mV, typ for  $\pm 5\text{V}$  supplies; 14mV, typ for +5V supplies)

To determine the typical error resulting from these error components, first compute the ideal output. Then calculate the output again, this time including the individual error components. Then determine the error in percent using Equation (21):

$$\% \text{error} = \frac{|V_{\text{LOGOUT IDEAL}} - V_{\text{LOGOUT TYP}}|}{V_{\text{LOGOUT IDEAL}}} \times 100\% \quad (21)$$

For example, in a system configured for measurement of five decades, with  $I_1 = 1\text{mA}$ , and  $I_2 = 10\mu\text{A}$ :

$$V_{\text{LOGOUT IDEAL}} = 0.375 \times \log\left(\frac{10^{-3}}{10^{-5}}\right) = 0.75\text{V} \quad (22)$$

$$V_{\text{LOGOUT TYP}} = 0.375(1 \pm 0.004) \times \log\left(\frac{10^{-3-5} \times 10^{-12}}{10^{-5-5} \times 10^{-12}}\right) \pm 2(0.001)(5) \pm 0.011 \quad (23)$$

Using the positive error components (+ $\Delta K$ , +2Nm, and + $V_{\text{OSO}}$ ) to calculate the maximum typical output:

$$V_{\text{LOGOUT TYP}} = 0.774\text{V} \quad (24)$$

Therefore, the error in percent is:

$$\% \text{error} = \frac{|0.75 - 0.774|}{0.75} \times 100\% = 3.2\% \quad (25)$$

### QFN PACKAGE

The LOG114 comes in a QFN-16 package. This leadless package has lead contacts on all four sides of the bottom of the package, thereby maximizing board space. An exposed leadframe die pad on the bottom of the package enhances thermal and electrical characteristics.

QFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The QFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note *QFN/SON PCB Attachment* (SLUA271) and Application Report *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at [www.ti.com](http://www.ti.com).

**The exposed leadframe die pad on the bottom of the package should be connected to V–.**

### QFN LAYOUT GUIDELINES

The exposed leadframe die pad on the QFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
LOG114AIRGVR	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
LOG114AIRGVRG4	ACTIVE	VQFN	RGV	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
LOG114AIRGVT	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
LOG114AIRGVTG4	ACTIVE	VQFN	RGV	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

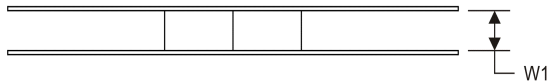
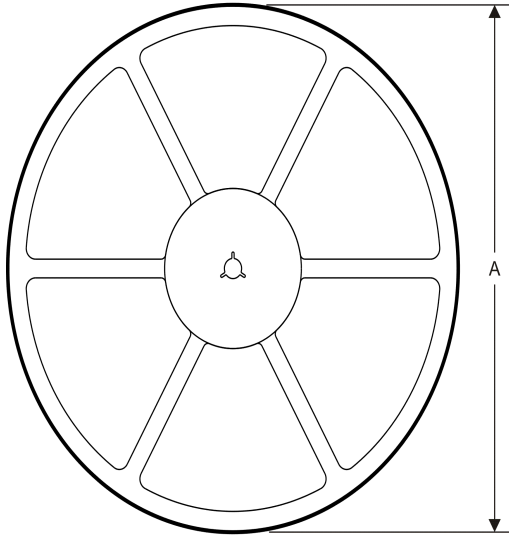
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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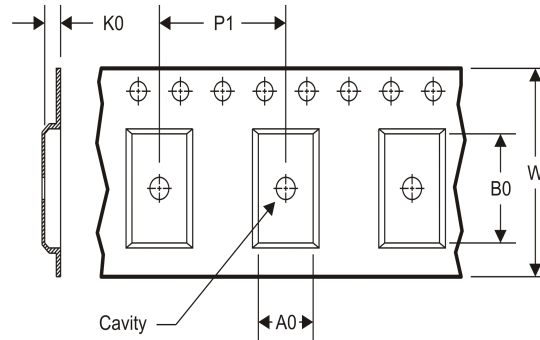
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LOG114AIRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
LOG114AIRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



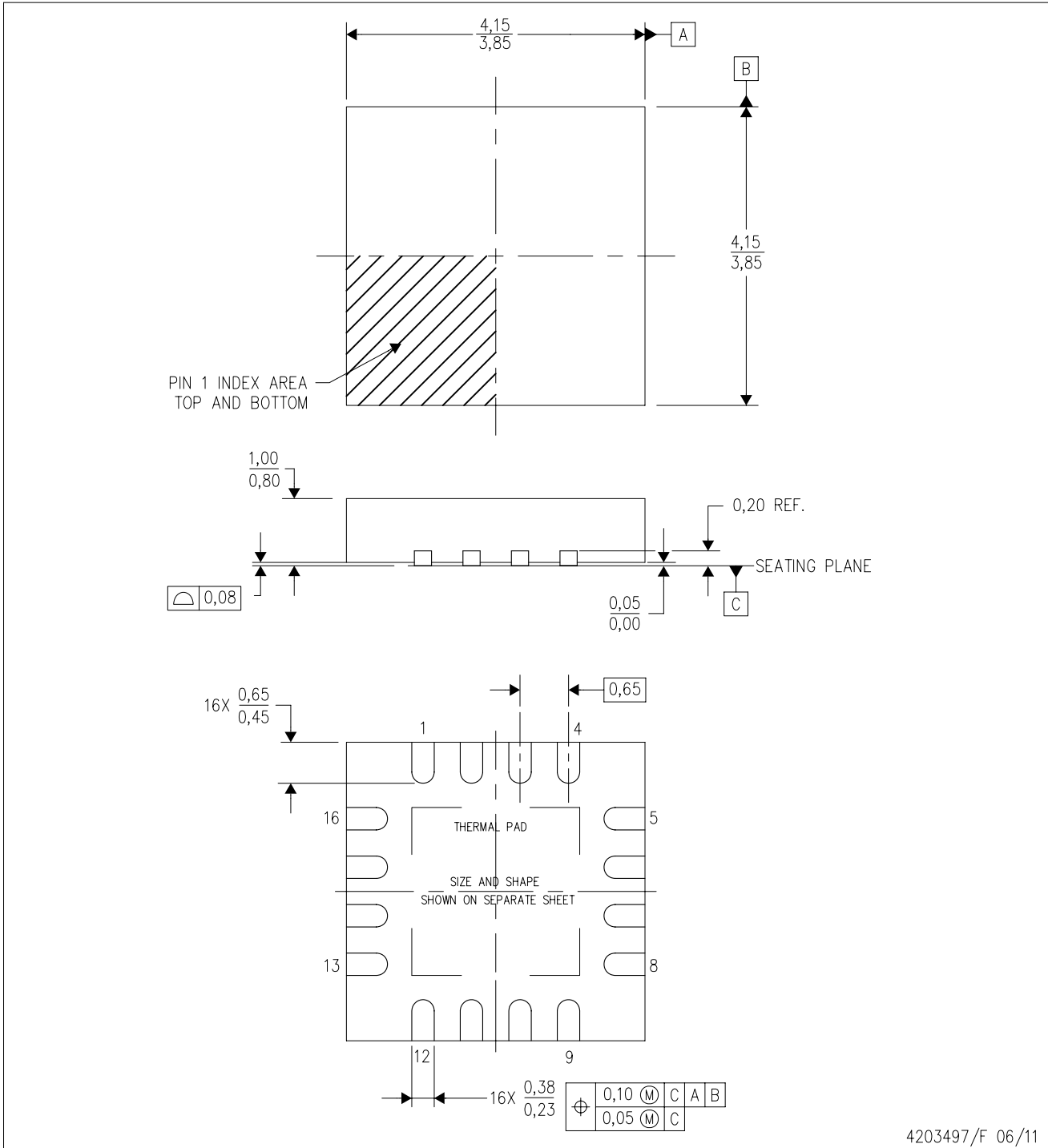
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LOG114AIRGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
LOG114AIRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203497/F 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

# THERMAL PAD MECHANICAL DATA

RGV (S-PVQFN-N16)

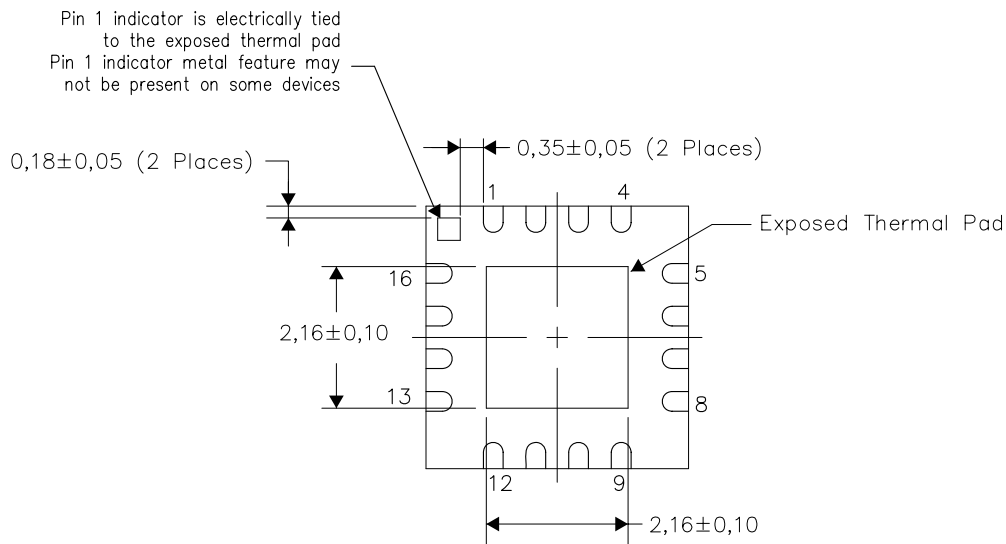
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



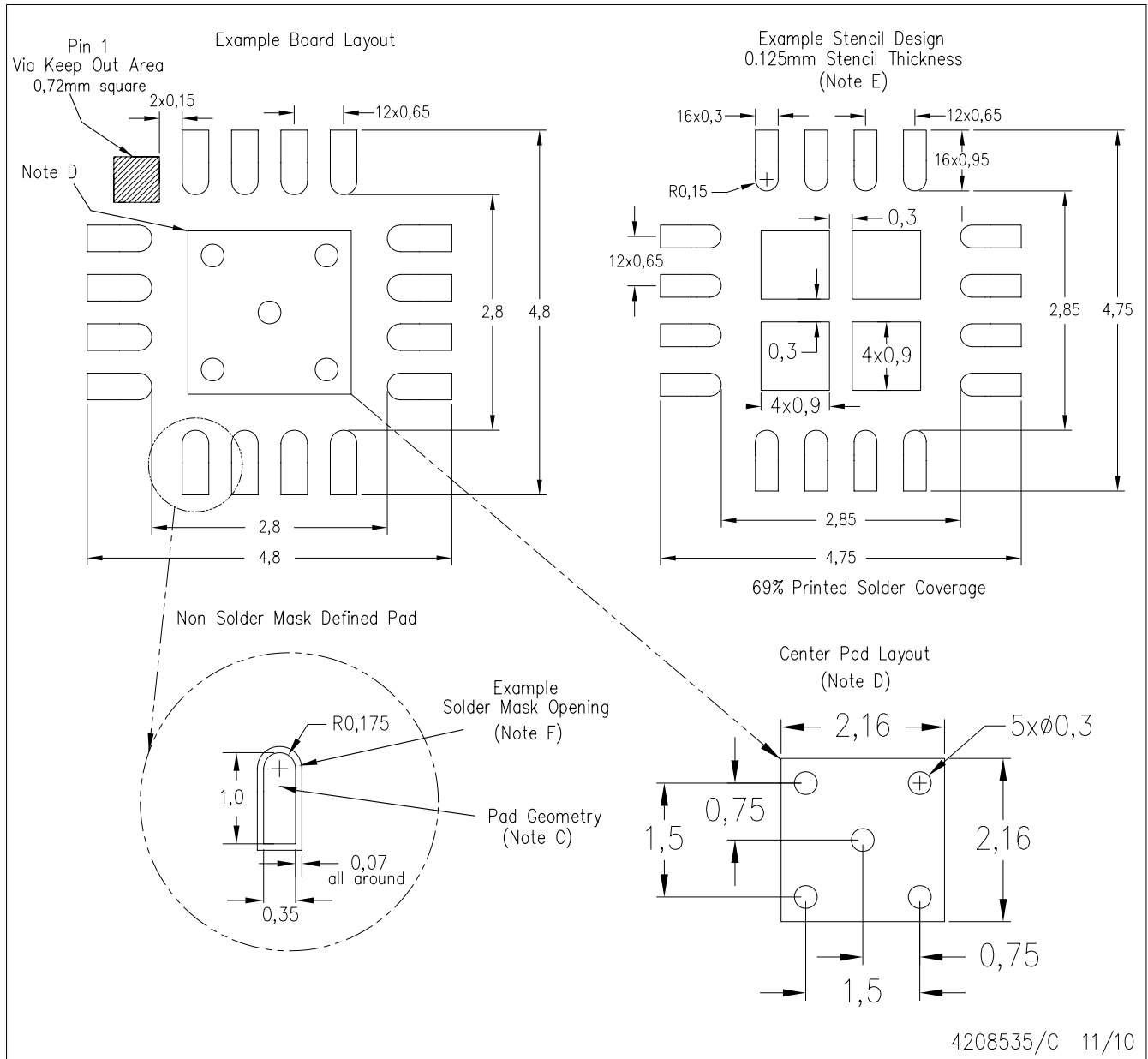
Exposed Thermal Pad Dimensions

4206351-2/J 06/11

NOTE: All linear dimensions are in millimeters

RGV (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Publication IPC-7351 is recommended for alternate designs.  
 D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.  
 E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
 F. Customers should contact their board fabrication site for solder mask tolerances.

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