

LMX2306/LMX2316/LMX2326 PLLatinum™ Low Power Frequency Synthesizer for RF Personal Communications

LMX2306	550 MHz
LMX2316	1.2 GHz
LMX2326	2.8 GHz

General Description

The LMX2306/16/26 are monolithic, integrated frequency synthesizers with prescalers that are designed to be used to generate a very stable low noise signal for controlling the local oscillator of an RF transceiver. They are fabricated using National's ABiC V silicon BiCMOS 0.5 μ process.

The LMX2306 contains a 8/9 dual modulus prescaler while the LMX2316 and the LMX2326 have a 32/33 dual modulus prescaler. The LMX2306/16/26 employ a digital phase locked loop technique. When combined with a high quality reference oscillator and loop filter, the LMX2306/16/26 provide the feedback tuning voltage for a voltage controlled oscillator to generate a low phase noise local oscillator signal. Serial data is transferred into the LMX2306/16/26 via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.3V to 5.5V. The LMX2306/16/26 feature ultra low current consumption; LMX2306 - 1.7 mA at 3V, LMX2316 - 2.5 mA at 3V, and LMX2326 - 4.0 mA at 3V.

The LMX2306/16/26 synthesizers are available in a 16-pin TSSOP surface mount plastic package.

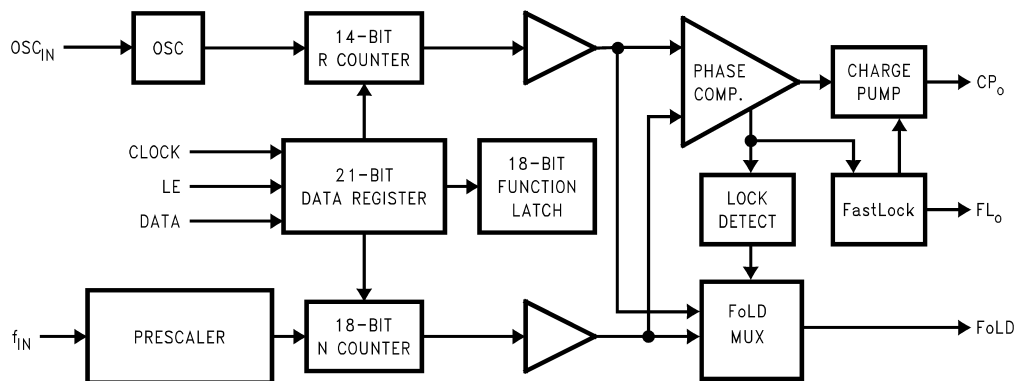
Features

- 2.3V to 5.5V operation
- Ultra low current consumption
- 2.5V V_{CC} JEDEC standard compatible
- Programmable or logical power down mode:
 - $I_{CC} = 1 \mu A$ typical at 3V
- Dual modulus prescaler:
 - LMX2306 8/9
 - LMX2316/26 32/33
- Selectable charge pump TRI-STATE® mode
- Selectable FastLock™ mode with timeout counter
- MICROWIRE™ Interface
- Digital Lock Detect

Applications

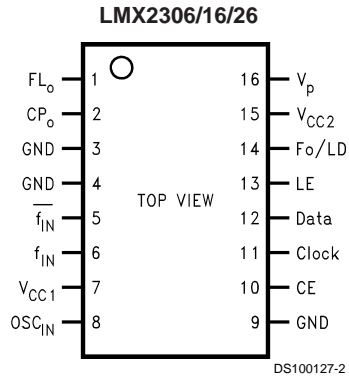
- Portable wireless communications (PCS/PCN, cordless)
- Wireless Local Area Networks (WLANs)
- Cable TV tuners (CATV)
- Pagers
- Other wireless communication systems

Functional Block Diagram



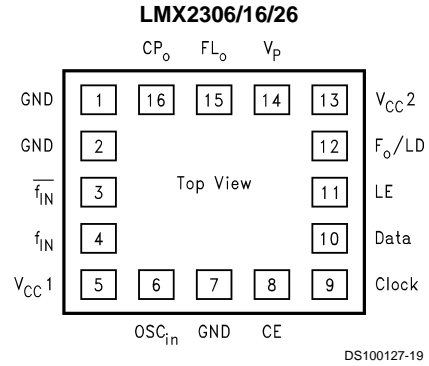
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Connection Diagrams



16-Lead (0.173" Wide) Thin Shrink Small Outline Package(TM)

Order Number **LMX2306TM, LMX2306TMX, LMX2316TM, LMX2316TMX, LMX2326TM or LMX2326TMX**
See NS Package Number **MTC16**



16-pin Chip Scale Package

Order Number **LMX2306SLBX, LMX2316SLBX or LM2326SLBX**
See NS Package Number **SLB16A**

Pin Descriptions

16-Pin TSSOP	16-Pin CSP	Pin Name	I/O	Description
1	15	FL _o	O	FastLock Output. For connection of parallel resistor to the loop filter. (See Section 1.3.4 FASTLOCK MODES description.)
2	16	CP _o	O	Charge Pump Output. For connection to a loop filter for driving the input of an external VCO.
3	1	GND		Charge Pump Ground.
4	2	GND		Analog Ground.
5	3	f _{IN} ⁻	I	RF Prescaler Complementary Input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The complementary input can be left unbypassed, with some degradation in RF sensitivity.
6	4	f _{IN}	I	RF Prescaler Input. Small signal input from the VCO.
7	5	V _{CC1}		Analog Power Supply Voltage Input. Input may range from 2.3V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. V _{CC1} must equal V _{CC2} .
8	6	OSC _{IN}	I	Oscillator Input. This input is a CMOS input with a threshold of approximately V _{CC} /2 and an equivalent 100k input resistance. The oscillator input is driven from a reference oscillator.
9	7	GND		Digital Ground.
10	8	CE	I	Chip Enable. A LOW on CE powers down the device and will TRI-STATE the charge pump output. Taking CE HIGH will power up the device depending on the status of the power down bit F2. (See Section 1.3.1 POWERDOWN OPERATION and Section 1.7.1 DEVICE PROGRAMMING AFTER FIRST APPLYING V _{CC} .)
11	9	Clock	I	High Impedance CMOS Clock Input. Data for the various counters is clocked in on the rising edge into the 21-bit shift register.
12	10	Data	I	Binary Serial Data Input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	11	LE	I	Load Enable CMOS Input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 3 appropriate latches (control bit dependent).
14	12	Fo/LD	O	Multiplexed Output of the RF Programmable or Reference Dividers and Lock Detect. CMOS output. (See Table 4.)
15	13	V _{CC2}		Digital Power Supply Voltage Input. Input may range from 2.3V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. V _{CC1} must equal V _{CC2} .
16	14	V _P		Power Supply for Charge Pump. Must be ≥ V _{CC} .

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage		
V_{CC1}	-0.3V to +6.5V	
V_{CC2}	-0.3V to +6.5V	
V_p	-0.3V to +6.5V	
Voltage on Any Pin		
with GND = 0V (V_I)	-0.3V to $V_{CC} + 0.3V$	
Storage Temperature Range (T_S)	-65°C to +150°C	
Lead Temperature (T_L)		+260°C
(solder, 4 sec.)		

Recommended Operating Conditions

	Min	Max	Units
Power Supply Voltage			
V_{CC1}	2.3	5.5	V
V_{CC2}	V_{CC1}	V_{CC1}	V
V_p	V_{CC}	5.5	V
Operating Temperature (T_A)	-40	+85	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating < 2 keV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

Electrical Characteristics

$V_{CC} = 3.0V$, $V_p = 3.0V$; $-40^\circ C < T_A < 85^\circ C$ except as specified

Symbol	Parameter	Conditions	Values			Units
			Min	Typ	Max	
I_{CC}	Power Supply Current	LMX2306	$V_{CC} = 2.3V$ to $5.5V$	1.7		mA
		LMX2316	$V_{CC} = 2.3V$ to $5.5V$	2.5		mA
		LMX2326	$V_{CC} = 2.3V$ to $5.5V$	4.0		mA
$I_{CC-PWDN}$	Powerdown Current	$V_{CC} = 3.0V$		1		μA
f_{IN}	RF Input Operating Frequency	LMX2306	$V_{CC} = 2.3V$ to $5.5V$	25	550	MHz
		LMX2316	$V_{CC} = 2.3V$ to $5.5V$	0.1	1.2	GHz
		LMX2326	$V_{CC} = 2.3V$ to $5.5V$	0.1	2.1	GHz
			$V_{CC} = 2.6V$ to $5.5V$	0.1	2.8	GHz
f_{OSC}	Maximum Oscillator Frequency		5	40	MHz	
$f\phi$	Maximum Phase Detector Frequency			10	MHz	
Pf_{IN}	RF Input Sensitivity	$V_{CC} = 3.0V$	-15	+0	dBm	
		$V_{CC} = 5.0V$	-10	+0	dBm	
		$V_{CC} = 2.3V$ to $5.5V$	-10	+0	dBm	
P_{OSC}	Oscillator Sensitivity	OSC_{IN}	-5		dBm	
V_{IH}	High-Level Input Voltage	(Note 4)	$0.8 \times V_{CC}$		V	
V_{IL}	Low-Level Input Voltage	(Note 4)		$0.2 \times V_{CC}$	V	
I_{IH}	High-Level Input Current	$V_{IH} = V_{CC} = 5.5V$ (Note 4)	-1.0	1.0	μA	
I_{IL}	Low-Level Input Current	$V_{IL} = 0V$, $V_{CC} = 5.5V$ (Note 4)	-1.0	1.0	μA	
I_{IH}	Oscillator Input Current	$V_{IH} = V_{CC} = 5.5V$		100	μA	
I_{IL}	Oscillator Input Current	$V_{IL} = 0V$, $V_{CC} = 5.5V$	-100		μA	
$ICP_{O-source}$	Charge Pump Output Current	$V_{DO} = V_p/2$, $ICP_o = LOW$ (Note 3)		-250	μA	
ICP_{O-sink}		$V_{DO} = V_p/2$, $ICP_o = LOW$ (Note 3)		250	μA	
$ICP_{O-source}$		$V_{DO} = V_p/2$, $ICP_o = HIGH$ (Note 3)		-1.0	mA	
ICP_{O-sink}		$V_{CPo} = V_p/2$, $ICP_o = HIGH$ (Note 3)		1.0	mA	
ICP_{O-Tri}	Charge Pump TRI-STATE Current	$0.5 \leq V_{CPo} \leq V_p - 0.5$ $-40^\circ C < T_A < 85^\circ C$	-1.0	1.0	nA	
ICP_{O-sink} vs $ICP_{O-source}$	CP Sink vs Source Mismatch	$V_{CPo} = V_p/2$ $T_A = 25^\circ C$		5	%	

Electrical Characteristics (Continued)

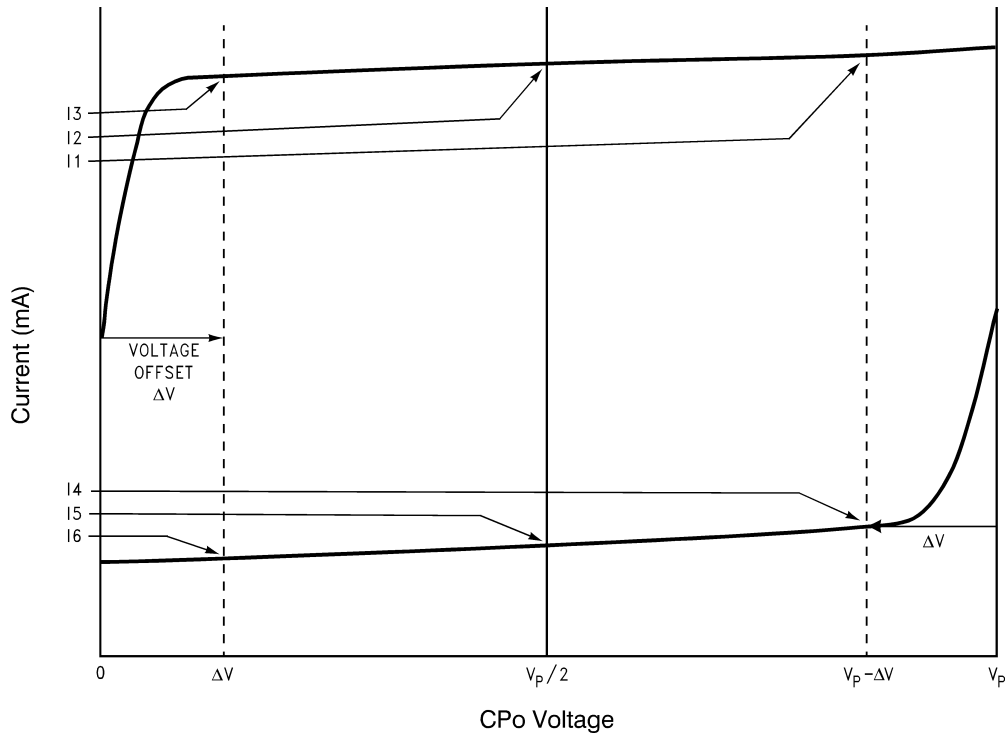
$V_{CC} = 3.0V$, $V_p = 3.0V$; $-40^{\circ}C < T_A < 85^{\circ}C$ except as specified

Symbol	Parameter	Conditions	Values			Units
			Min	Typ	Max	
ICP_o vs V_{D0}	CP Current vs Voltage	$0.5 \leq V_{CP0} \leq V_p - 0.5$ $T_A = 25^{\circ}C$		5		%
ICP_o vs T	CP Current vs Temperature	$V_{CP0} = V_p/2$ $-40^{\circ}C < T_A < 85^{\circ}C$		5		%
V_{OH}	High-Level Output Voltage	$I_{OH} = -500 \mu A$	$V_{CC} - 0.4$			V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 500 \mu A$			0.4	V
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns

Note 3: See PROGRAMMABLE MODES for ICP_o description

Note 4: Except f_{IN} and OSC_{IN} .

Charge Pump Current Specification Definitions



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I1 = CP sink current at $V_{CPo} = V_p - \Delta V$

I4 = CP source current at $V_{CPo} = V_p - \Delta V$

I2 = CP sink current at $V_{CPo} = V_p/2$

I5 = CP source current at $V_{CPo} = V_p/2$

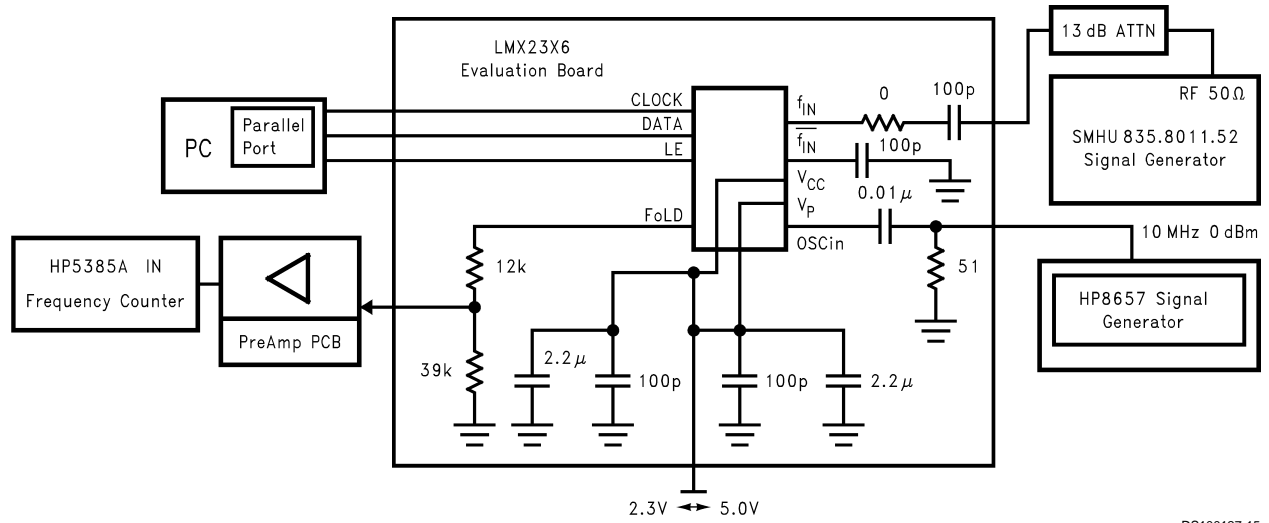
I3 = CP sink current at $V_{CPo} = \Delta V$

I6 = CP source current at $V_{CPo} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V

1. ICP_o vs V_{CPo} = Charge Pump Output Current magnitude variation vs Voltage = $[\frac{1}{2} * \{|I1| - |I3|\} / [\frac{1}{2} * \{|I1| + |I3|\}]] * 100\%$ and $[\frac{1}{2} * \{|I4| - |I6|\} / [\frac{1}{2} * \{|I4| + |I6|\}]] * 100\%$
2. ICP_{o-sink} vs $ICP_{o-source}$ = Charge Pump Output Current Sink vs Source Mismatch = $[|I2| - |I5|] / [\frac{1}{2} * \{|I2| + |I5|\}] * 100\%$
3. ICP_o vs T = Charge Pump Output Current magnitude variation vs Temperature = $[|I2 @ temp| - |I2 @ 25^\circ C|] / |I2 @ 25^\circ C| * 100\%$ and $[|I5 @ temp| - |I5 @ 25^\circ C|] / |I5 @ 25^\circ C| * 100\%$

RF Sensitivity Test Block Diagram



Note 5: N=10,000 R=50 P=32

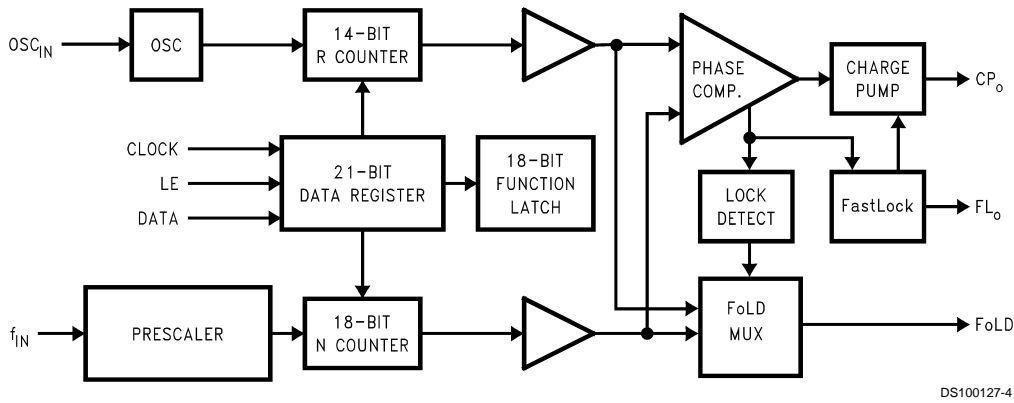
Note 6: Sensitivity limit is reached when the error of the divided RF output, FoLD, is greater than or equal to 1 Hz.

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1.0 Functional Description

The simplified block diagram below shows the 21-bit data register, a 14-bit R Counter, an 18-bit N Counter, and a 18-bit Function Latch (intermediate latches are not shown). The data stream is shifted (on the rising edge of LE) into the DATA input, MSB first. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:

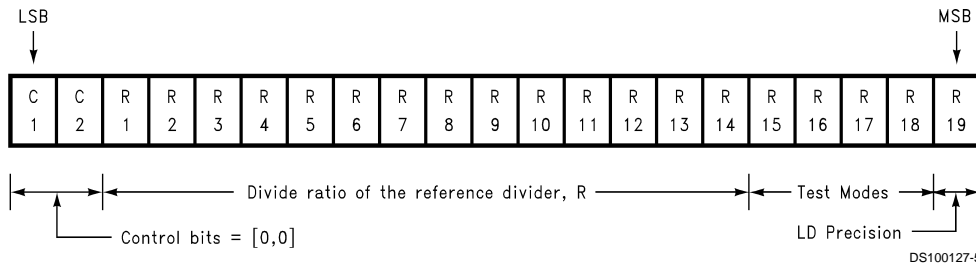
Control		DATA Location
C1	C2	
0	0	R Counter
1	0	N Counter
0	1	Function Latch
1	1	Initialization



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1.1 PROGRAMMABLE REFERENCE DIVIDER

If the Control Bits are $[C_1, C_2] = [0,0]$, data is transferred from the 21-bit shift register into a latch that sets the 14-bit R Counter. The 4 bits R15–R18 are for test modes, and should be set to 0 for normal use. The LD precision bit, R19, is described in the LOCK DETECT OUTPUT CHARACTERISTICS section. Serial data format is shown below.



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Note: R15 to R18 are test modes and should be zero for normal operation. Data is shifted in MSB first.

1.1.1 14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

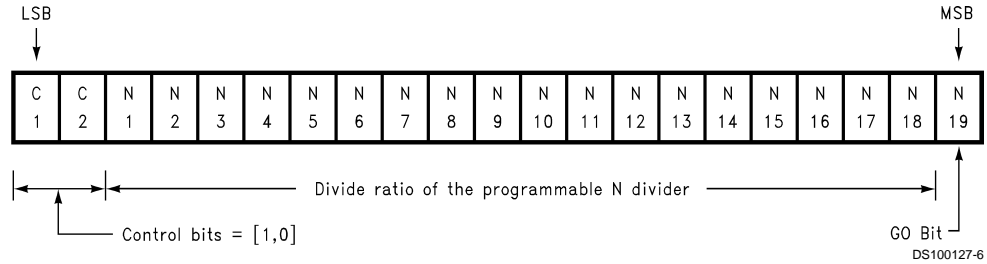
Divide Ratio	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratios less than 3 are prohibited.
Divide ratio: 3 to 16383
R1 to R14: These bits select the divide ratio of the programmable reference divider.

1.0 Functional Description (Continued)

1.2 PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 5-bit swallow counter (A counter) and the 13-bit programmable counter (B counter). If the Control Bits are $[C_1, C_2] = [1,0]$, data is transferred from the 21-bit shift register into a 5-bit latch (which sets the Swallow (A) Counter), a 13-bit latch (which sets the 13-bit programmable (B) Counter), and the GO bit (See Section 1.3.4 FastLock MODES section) MSB first. For the LMX2306 the maximum N value is 65535 and the minimum N value is 56. For the LMX2316/26, the maximum N value is 262143 and the minimum N value is 992. Serial data format is shown below.



Note: Data is shifted in MSB first.

1.2.1 5-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

LMX2316/26

Divide Ratio	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

Note: Divide ratio: 0 to 31
 $B \geq A$

LMX2306

Divide Ratio	N 5	N 4	N 3	N 2	N 1
0	X	X	0	0	0
1	X	X	0	0	1
•	•	•	•	•	•
7	X	X	1	1	1

Note: Divide ratio: 0 to 7
 $B \geq A$
 X denotes a Don't Care condition

1.2.2 13-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	N 7	N 6
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

Divide ratio: 3 to 8191 (Divide ratios less than 3 are prohibited) $B \geq A$

1.2.3 PULSE SWALLOW FUNCTION

$$f_{vco} = [(P \times B) + A] \times f_{osc}/R$$

f_{vco} : Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 13-bit programmable counter (3 to 8191)

A: Preset divide ratio of binary 5-bit swallow counter ($0 \leq A \leq 31$; $A \leq B$ for LMX2316/26) or ($0 \leq A \leq 7$, $A \leq B$ for LMX2306)

f_{osc} : Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)

P: Preset modulus of dual modulus prescaler
 for the LMX2306; $P = 8$ for the LMX2316/26; $P = 32$

1.0 Functional Description (Continued)

1.3 FUNCTION AND INITIALIZATION LATCHES

Both the function and initialization latches write to the same registers. (See Section 1.7.1 DEVICE PROGRAMMING AFTER FIRST APPLYING V_{CC} section for initialization latch description.)

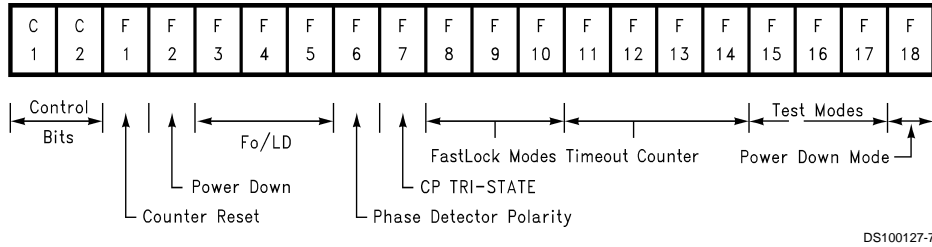


TABLE 1. Programmable Modes

C1	C2	F1	F2	F3–5	F6	F7	F8
0	1	COUNTER RESET	POWER DOWN	FoLD CONTROL	PD POLARITY	CP TRI-STATE	FASTLOCK ENABLE
F9		F10	F11–14		F15–F17	F18	
FAST-LOCK CONTROL		TIMEOUT COUNTER ENABLE	TIMEOUT COUNTER VALUE		TEST MODES	POWER DOWN MODE	

TABLE 2. Mode Select Truth Table

REGISTER LEVEL	COUNTER RESET	POWER DOWN	PHASE DETECTOR POLARITY	CP TRI-STATE
0	RESET DISABLED	POWERED UP	NEGATIVE	NORMAL OPERATION
1	RESET ENABLED	POWERED DOWN	POSITIVE	TRI-STATE

FUNCTION DESCRIPTION

F1. The Counter Reset enable mode bit F1, when activated, allows the reset of both N and R counters. Upon powering up, the F1 bit needs to be disabled, then the N counter resumes counting in “close” alignment with the R counter. (The maximum error is one prescalar cycle).

F2. Refer to Section 1.3.1 POWERDOWN OPERATION section.

F3–5. Controls output of FoLD pin. See FoLD truth table. See *Table 4*.

F6. Phase Detector Polarity. Depending upon VCO characteristics, F6 bit should be set accordingly. When VCO characteristics are positive F6 should be set HIGH; When VCO characteristics are negative F6 should be set LOW

F7. Charge Pump TRI-STATE is set using bit F7. For normal operation this bit is set to zero.

F8. When the **FastLock Enable** bit is set the part is forced into one of the four FastLock modes. See description in *Table 5*, Fast-Lock Decoding.

F9. The **FastLock Control** bit determines the mode of operation when in FastLock (F8 = 1). When not in FastLock mode, FL_o can be used as a general purpose output controlled by this bit. For F9 = 1, FL_o is HIGH and for F9 = 0, FL_o is LOW. See *Table 5* for truth table.

F10. Timeout Counter Enable bit is set to 1 to enable the timeout counter. See *Table 5* for truth table.

F11–14. FastLock Timeout Counter is set using bits F11-14. *Table 6* for counter values.

F15–17. Function bits F15–F17 are for **Test Modes**, and should be set to 0 for normal use.

F18. Refer to Section 1.3.1 POWERDOWN OPERATION section.

1.0 Functional Description (Continued)

1.3.1 POWERDOWN OPERATION

Bits F[2] and F[18] provide programmable powerdown modes when the CE pin is HIGH. When CE is LOW, the part is always immediately disabled regardless of powerdown bit status. Refer to *Table 3*.

Synchronous and asynchronous powerdown modes are both available by MICROWIRE selection. Synchronous powerdown occurs if the F[18] bit (Powerdown Mode) is HIGH when F[2] bit (Powerdown) becomes HIGH. Asynchronous powerdown occurs if the F[18] bit is LOW when its F[2] bit becomes HIGH.

In the synchronous powerdown mode (F[18] = HIGH), the powerdown function is gated by the charge pump to prevent unwanted frequency jumps. Once the powerdown program bit F[2] is loaded, the part will go into powerdown mode after the first successive charge pump event.

In the asynchronous powerdown mode (F[18] = LOW), the device powers down immediately after latching LOW data into bit F[2].

The device returns to an actively powered up condition in either synchronous or asynchronous mode immediately upon LE latching LOW data into bit F[2].

Activation of a powerdown condition in either synchronous or asynchronous mode including CE pin activated powerdown has the following effects:

- Removes all active DC current paths.
- Forces the R, N, and timeout counters to their load state conditions.
- Will TRI-STATE the charge pump.
- Resets the digital lock detect circuitry.
- Debiases the f_{IN} input to a high impedance state.
- Disables the oscillator input buffer circuitry.
- The MICROWIRE control register remains active and capable of loading the data.

TABLE 3. Power Down Truth Table

CE(Pin 10)	F[2]	F[18]	Mode
LOW	X	X	Asynchronous Power Down
HIGH	0	X	Normal Operation
HIGH	1	0	Asynchronous Power Down
HIGH	1	1	Synchronous Power Down

TABLE 4. The Fo/LD (pin 14) Output Truth Table

F[3]	F[4]	F[5]	Fo/LD Output State
0	0	0	TRI-STATE
0	0	1	R Divider Output (fr)
0	1	0	N Divider Output (fp)
0	1	1	Serial Data Output
1	0	0	Digital Lock Detect (See 1.3.2 LOCK DETECT OUTPUT Section)
1	0	1	n Channel Open Drain Lock Detect (See 1.3.2 LOCK DETECT OUTPUT Section)
1	1	0	Active HIGH
1	1	1	Active LOW

1.0 Functional Description (Continued)

1.3.2 LOCK DETECT OUTPUT CHARACTERISTICS

Output provided to indicate when the VCO frequency is in “lock.” When the loop is locked and the open drain lock detect mode is selected, the pin’s output is HIGH, with narrow pulses LOW. When digital lock detect is selected, the output will be HIGH when the absolute phase error is < 15 ns for three or five consecutive phase frequency detector reference cycles, depending on the value of R[19]. Once lock is detected the output stays HIGH unless the absolute phase error exceeds 30 ns for a single reference cycle. Setting the charge pump to TRI-STATE or power down (bits F2, F18) will reset the digital lock detect to the unlocked state. The LD precision bit, R[19], will select five consecutive reference cycles, instead of three, for entering the locked state when R[19] = HIGH.

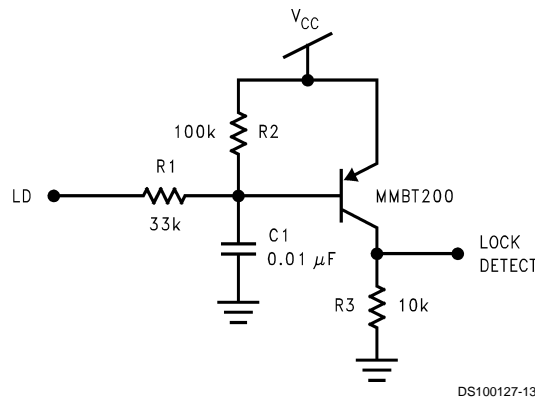


FIGURE 1. Typical Lock Detect Circuit

1.3.3 LOCK DETECT FILTER CALCULATION

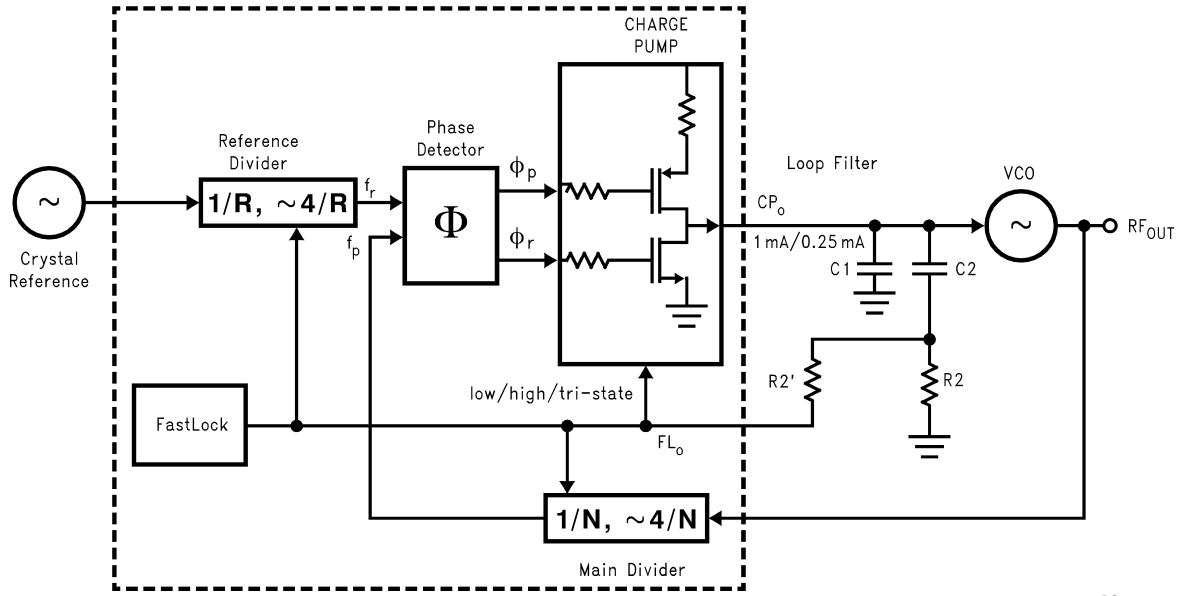
The component values for the open drain lock detect filter can be determined after assessing the qualifications for an in-lock condition. The in-lock condition can be specified as being a particular number (N) of consecutive reference cycles or duration (D) wherein the phase detector phase error is some factor less than the reference period. In an example where the phase detector reference period is 10 kHz, one might select the threshold for in-lock as occurring when 5 consecutive phase comparisons have elapsed where the phase errors are a 1000 times shorter than the reference period (100 ns). Here, $N = 5$ and $F = 1000$.

For the lock detect filter shown in *Figure 1*, when used in conjunction with an open drain (active sink only) lock detect output, the resistor value for R2 would be chosen to be a factor of $F * R1$. Thus, if resistor R1 were pulled low for only 1/1000th of the reference cycle period, its “effective” resistance would be on par with R2. The two resistors for that duty cycle condition on average appear to be two 1000x R1 resistors connected across the supply voltage with their common node voltage (V_c) at $V_{CC}/2$. Phase errors larger than 1/1000th of the reference cycle period would drag the average voltage of node V_c below $V_{CC}/2$ indicating an out-of-lock status. If the time constant of $R2 * C1$ is now calculated to be $N * \text{the reference period}$ (500 μs), then the voltage of node V_c would fall below $V_{CC}/2$ only after 5 consecutive phase errors whose average pulse width was greater than 100 ns.

1.3.4 FastLock MODES

FastLock enables the designer to achieve both fast frequency transitions and good phase noise performance by dynamically changing the PLL loop bandwidth. The FastLock modes allow wide band PLL fast locking with seamless transition to a low phase noise narrow band PLL. Consistent gain and phase margins are maintained by simultaneously changing charge pump current magnitude, counter values, and loop filter damping resistor. The four FastLock modes in *Table 5* are similar to the technique used in National Semiconductor’s LMX 233X series Dual Phase Locked Loops and are selected by F9, F10, and N19 when F8 is HIGH. Modes 1 and 2 change loop bandwidth by a factor of two while modes 3 and 4 change the loop bandwidth by a factor of 4. Modes 1 and 2 increase charge pump magnitude by a factor of 4 and should use $R2' = R2$ for consistent gain and phase margin. Modes 3 and 4 increase charge pump magnitude and decrease the counter values by a factor of 4. $R2' = 1/3 R2$ should be used for consistent stability margin in modes 3 and 4. When F8 is LOW, the FastLock modes are disabled, F9 controls only the FL_o output level ($FL_o = F9$), and N19 determines the charge pump current magnitude ($N19 = \text{LOW} \rightarrow ICP_o = 250 \mu\text{A}$, $N19 = \text{HIGH} \rightarrow ICP_o = 1 \text{ mA}$).

1.0 Functional Description (Continued)



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TABLE 5. FastLock Decoding

FastLock Status	F[8]	F[9]	F[10]	N[19] (Note 7)	FastLock State
FastLock Mode #1	1	0	0	1 (Note 7)	No Timeout Counter - 1X Divider
FastLock Mode #2	1	0	1	1	Timeout Counter - 1X Divider
FastLock Mode #3	1	1	0	1 (Note 7)	No Timeout Counter - 1/4X Divider
FastLock Mode #4	1	1	1	1	Timeout Counter - 1/4X Divider

Note 7: When the GO bit N[19] is set to one, the part is forced into the high gain mode. When the timeout counter is activated, termination of the counter cycle resets the GO bit to 0. If the timeout counter is not activated, N[19] must be reprogrammed to zero in order to remove the high gain state. See below for descriptions of each individual FastLock mode.

There are two techniques of switching in and out of FastLock. To program the device into any of the FastLock modes, the GO bit N[19] must be set to one to begin FastLock operation. In the first approach, the timeout counter can be used (FastLock 2 and 4) to stay in FastLock mode for a programmable number of phase detector reference cycles (up to 63) and then reset the GO bit automatically. In the second approach (FastLock 1 and 3) without the timeout counter, the PLL will remain in FastLock mode until the user resets the GO bit via the MICROWIRE serial bus. Once the GO bit is set to zero by the timeout counter or by MICROWIRE, the PLL will then return to normal operation. This transition does not effect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless transition between FastLock and standard mode.

FastLock Mode 1 In this mode, the output level of the FL_o is programmed in a low state while the ICP_o is in the 4x state. The device remains in this state until a command is received, resetting the N[19] bit to zero. Programming N[19] to zero will return the device to normal operation*, i.e., ICP_o = 1x and FL_o returned to TRI-STATE.

FastLock Mode 2 Identical to mode 1, except the switching of the device out of FastLock is controlled by the Timeout counter. The device will remain in FastLock until the timeout counter has counted down the appropriate number of phase detector cycles, at which time the PLL returns to normal operation*.

FastLock Mode 3 This mode is similar to mode 1 in that the output level of the FL_o is low and the ICP_o is switched to the 4x state. Additionally, the R and N divide ratios are reduced by one fourth during the transient, resulting in a 16x improved gain. As in mode 1, the device remains in this state until a MICROWIRE command is received, resetting the N[19] bit to zero and returning the device to normal operation*.

FastLock Mode 4 Identical to mode 3, except the switching of the device out of FastLock is controlled by the Timeout counter. The device will remain in FastLock until the timeout counter has counted down the appropriate number of phase detector cycles, at which time the PLL returns to normal operation*.

***Normal Operation** FastLock Normal Operation is defined as the device being in low current mode and standard divider values.

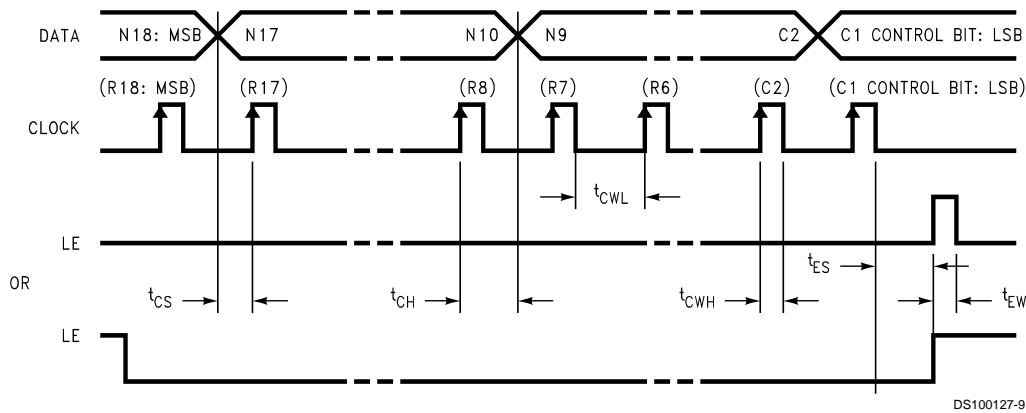
1.0 Functional Description (Continued)

TABLE 6. FastLock Timeout Counter Value Programming

Timeout (# PD Cycles) (Note 8)	3	7	11	15	19	23	27	31	35	•	59	63
F11 (4)	0	1	0	1	0	1	0	1	0	•	0	1
F12 (8)	0	0	1	1	0	0	1	1	0	•	1	1
F13 (16)	0	0	0	0	1	1	1	1	0	•	1	1
F14 (32)	0	0	0	0	0	0	0	0	1	•	1	1

Note 8: The timeout counter decrements after each phase detector comparison cycle.

1.4 SERIAL DATA INPUT TIMING



DS100127-9

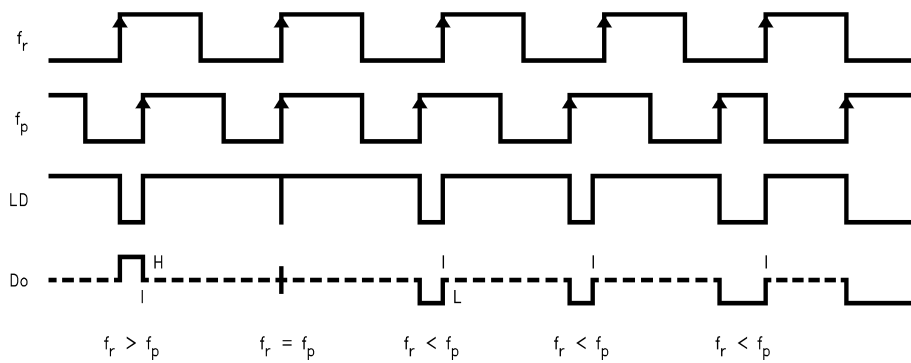
Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 1.84V @ $V_{CC} = 2.3V$ and 4.4V @ $V_{CC} = 5.5V$.

1.5 PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



DS100127-10

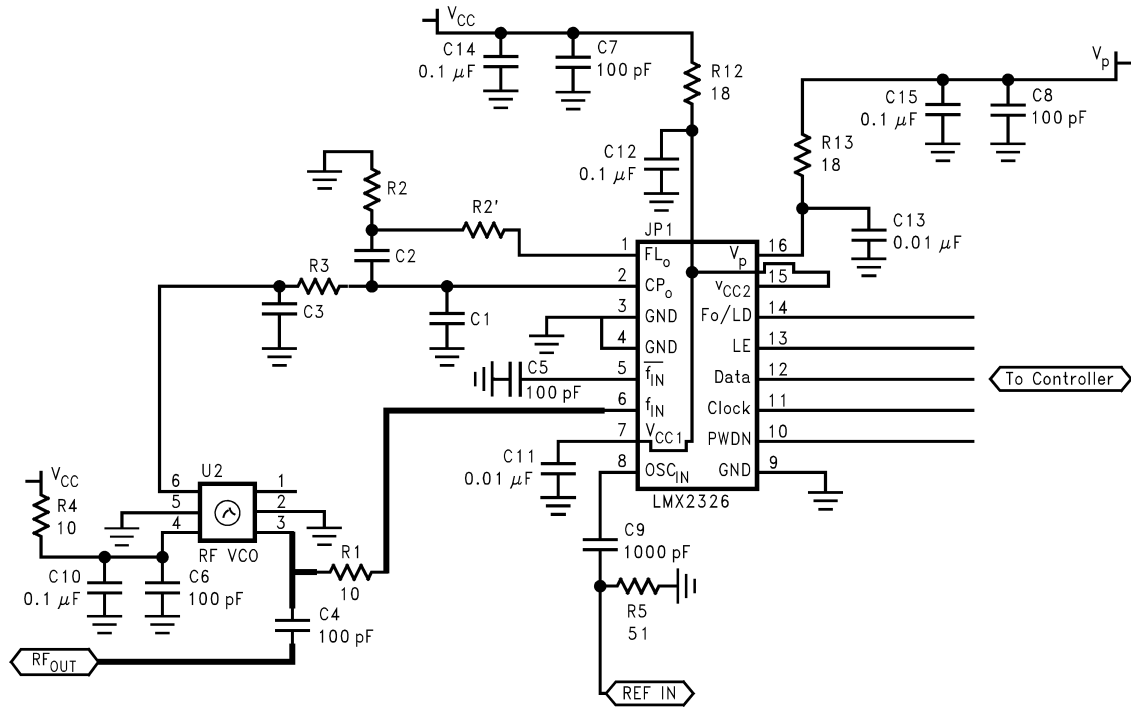
Notes: Phase difference detection range: -2π to $+2\pi$

The Phase Detector Polarity F[6] = HIGH

The minimum width pump up and pump down current pulses occur at the ICP_o pin when the loop is locked.

1.0 Functional Description (Continued)

1.6 Typical Application Example



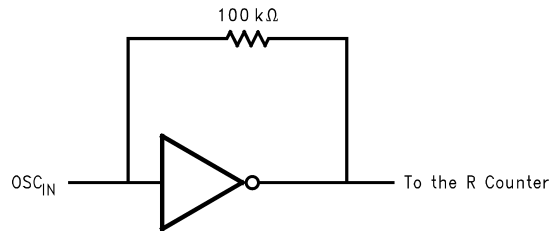
DS100127-11

OPERATIONAL NOTES:

*VCO is assumed AC coupled.

**R1 increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

**50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See Figure below.)



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1.7 Application Information

1.7.1 DEVICE PROGRAMMING AFTER FIRST APPLYING V_{CC}

Three MICROWIRE programming methods can be used to change the function latch, R counter latch, and N counter latch contents with close phase alignment of R and N counters to minimize lock up time after the cold power up.

1.7.2 INITIALIZATION SEQUENCE METHOD

Loading the function latch with $[C1, C2] = [1, 1]$ immediately followed by an R counter load, then an N counter load, efficiently programs the MICROWIRE. Loading the function latch with $[C1, C2] = [1, 1]$ programs the same function latch as a load with $[C1, C2] = [0, 1]$ and additionally provides an internal reset pulse described below. This program sequence insures that the counters are at load point when the N counter data is latched in and the part will begin counting in close phase alignment.

The following results from latching the MICROWIRE with an F latch word, $[C1, C2] = [1, 1]$:

- The function latch contents are loaded.
- An internal pulse resets the R, N, and timeout counters to load state conditions and will TRI-STATE the charge pump. If the function latch is programmed for the synchronous powerdown case; $CE = HIGH$, $F[2] = HIGH$, $F[18] = HIGH$, this internal pulse triggers powerdown. Refer to Section 1.3.1 POWERDOWN OPERATION section for a synchronous powerdown description. Note that the prescaler bandgap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N counter data after the initialization word will activate the same internal reset pulse. Successive N counter data loads without an initialization load will not trigger the internal reset pulse.

1.7.3 CE METHOD

Programming the function latch, R counter latch and N counter latch while the part is being held in a powerdown state by CE allows lowest possible power dissipation. After the MICROWIRE contents have been programmed and the part is enabled, the R and N counter contents will resume counting in close phase alignment. Note that after CE transitions from LOW to HIGH, a duration of 1 μs may be required for the prescaler bandgap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the part up and down by pin control in order to check for channel activity. The MICROWIRE does not need to be reprogrammed each time the part is enabled and disabled as long as it has been programmed at least once after V_{CC} was applied.

1.7.4 COUNTER RESET METHOD

This MICROWIRE programming method consists of a function latch load, $[C1, C2] = [0, 1]$, enabling the counter reset bit, F[1]. The R and N counter latches are then loaded followed by a final function latch load that disables the counter reset. This provides the same close phase alignment as the initialization sequence method with direct control over the internal reset. Note that counter reset holds the counters at load point and will TRI-STATE the charge pump, but does not trigger synchronous powerdown. The counter reset method requires an extra function latch load compared to the initialization sequence method.

1.7.5 DEVICE PROGRAMMING

When programming the LMX2306, LMX2316, and LMX2326, first determine the frequencies and mode of operation desired. Data register is programmed with a 21-bit data stream shifted into the R counter, N counter, or the F latch. The Functional Description section shows the bits for the R counter, and the corresponding information for the N counter. The FL_o programming information is given in the FUNCTION AND INITIALIZATION LATCHES section. Typical numbers for a GSM application example are given. In the example, the RF output is locking at 950 MHz (f_{vco}) with a 200 kHz channel spacing ($f_{comparison}$). The crystal oscillator reference input is 10 MHz (f_{osc}) and the prescaler value (P) is 32. An example of both methods of FastLock will be shown.

The last two bits (control bits C1 and C2) of each bit stream identify which counter or FL_o mode will be programmed. For example, to program the R counter, C1 and C2 will be 0,0. Immediately preceding these two bits is the N, R, or F bits providing the divide ratios and FastLock mode information.

Control Bits		DATA Location
C1	C2	
0	0	R Counter
1	0	N Counter
0	1	Function Latch
1	1	Initialization

For example, to load the N counter, the last two bits C1 and C2 must be 10.

Once the control bits have been determined, the frequency information must be determined. To begin, determine the N and R counter values as follows:

$$N = f_{vco}/f_{comparison}$$

and

$$R = f_{osc}/f_{comparison}$$

For this example R and N are determined as follows:

$$R = 10 \text{ MHz}/200 \text{ kHz} = 50$$

and

$$N = 950 \text{ MHz}/200 \text{ kHz} = 4750$$

1.7 Application Information (Continued)

1.7.6 N COUNTER

The calculated value of N, and the value of P are now used to determine the values of A and B where A and B are both integer values:

$$N = P * B + A$$

where B is the divisor and A is the remainder. Therefore:

$$B = \text{div} (N/P)$$

and

$$A = N - (B * P)$$

For this example, B and A are calculated as follows:

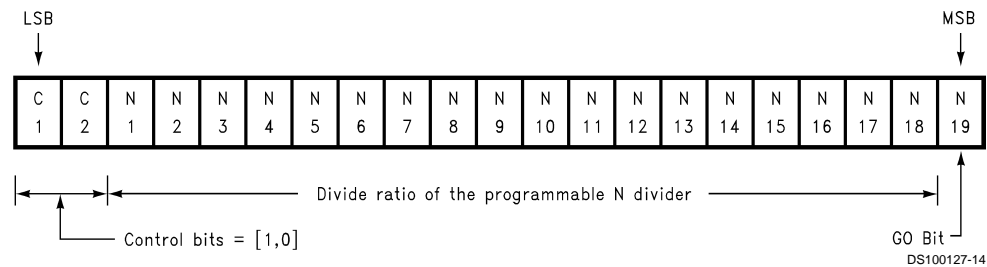
$$B = \text{div} (4750/32) = 148 = 0000010010100$$

and

$$A = 4750 - (148 * 32) = 14 = 01110$$

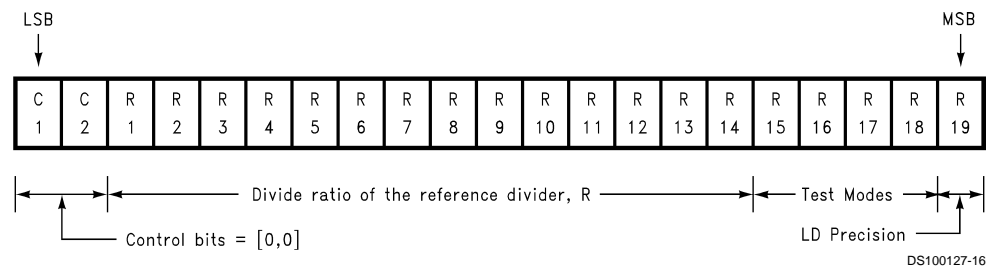
To load the N counter with these values, the programming bit stream would be as follows. The first bit, the GO bit, (MSB) N[19] is used for FastLock operation and will be discussed in the F Latch section. The next 13 bits, (N[18]–N[6]) shifted in, are the B counter value, 0000010010100_b *. Bits N[5]–N[1] are the A counter and are 01110_b in this example. The final two bits (the control bits) are 1,0 identifying the N counter. In programming the N counter, the value of B must be greater than or equal to A, and the value of B must be greater than or equal to 3.

Note: *In programming the counter, data is shifted in MSB first.



1.7.7 R COUNTER

Programming the R counter is done by shifting in the binary value of R calculated previously (50_d = 110010_b). The first bit shifted in is R[19] the LD precision bit. The next 4 bits (R[18]–R[15]) shifted in, are used for testing and should always be loaded with zeros. The R[14]–R[1] bits are used to program the reference divider ratio and should be 00000000110010_b for this example. The final two bits, C[1] and C[2] denote the R counter and should be 0, 0. The resulting bit stream looks as follows:



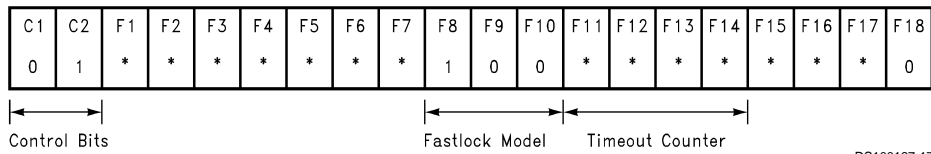
1.7.8 F LATCH

To program the device for any of the FastLock modes, C[1] = 0 and C[2] = 1 which direct data to the F latch. The Section 1.3 FUNCTION AND INITIALIZATION LATCH section discusses the 4 modes of FastLock operation. The user must first determine which FastLock mode will be used. When using any of the FastLock modes, the programmer needs to experimentally determine the length of time to stay in high gain mode. This is done by looking at the transient response and determining the time at which the device has settled to within the appropriate frequency tolerance. FastLock mode should be terminated just prior to “lock” to place the switching phase glitch within the transient settling time. The counter reset mode (F[1] bit) holds both the N and R counters at load point when F[1] = HIGH. Upon setting F[1] = LOW, the N and R counters will resume counting in close phase alignment. Other functions of the F latch such as FoLD output control, Phase detector polarity, and charge pump TRI-STATE are defined in the 1.3 FUNCTION AND INITIALIZATION LATCH section also.

1.7 Application Information (Continued)

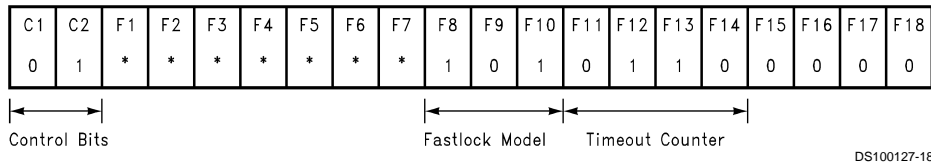
1.7.9 FastLock MODE 1 PROGRAMMING

The F[1]–F[7] bits will be denoted as (*) and are dependent on the desired modes of the applicable functions. To program the device for mode 1 FastLock, the F[8]–F[10] bits are programmed 100, while the N[19] bit is set to 1. The device will stay in the 4X current mode until another N bit stream is sent with the N[19] bit reset to 0. This gives a bit stream as follows:



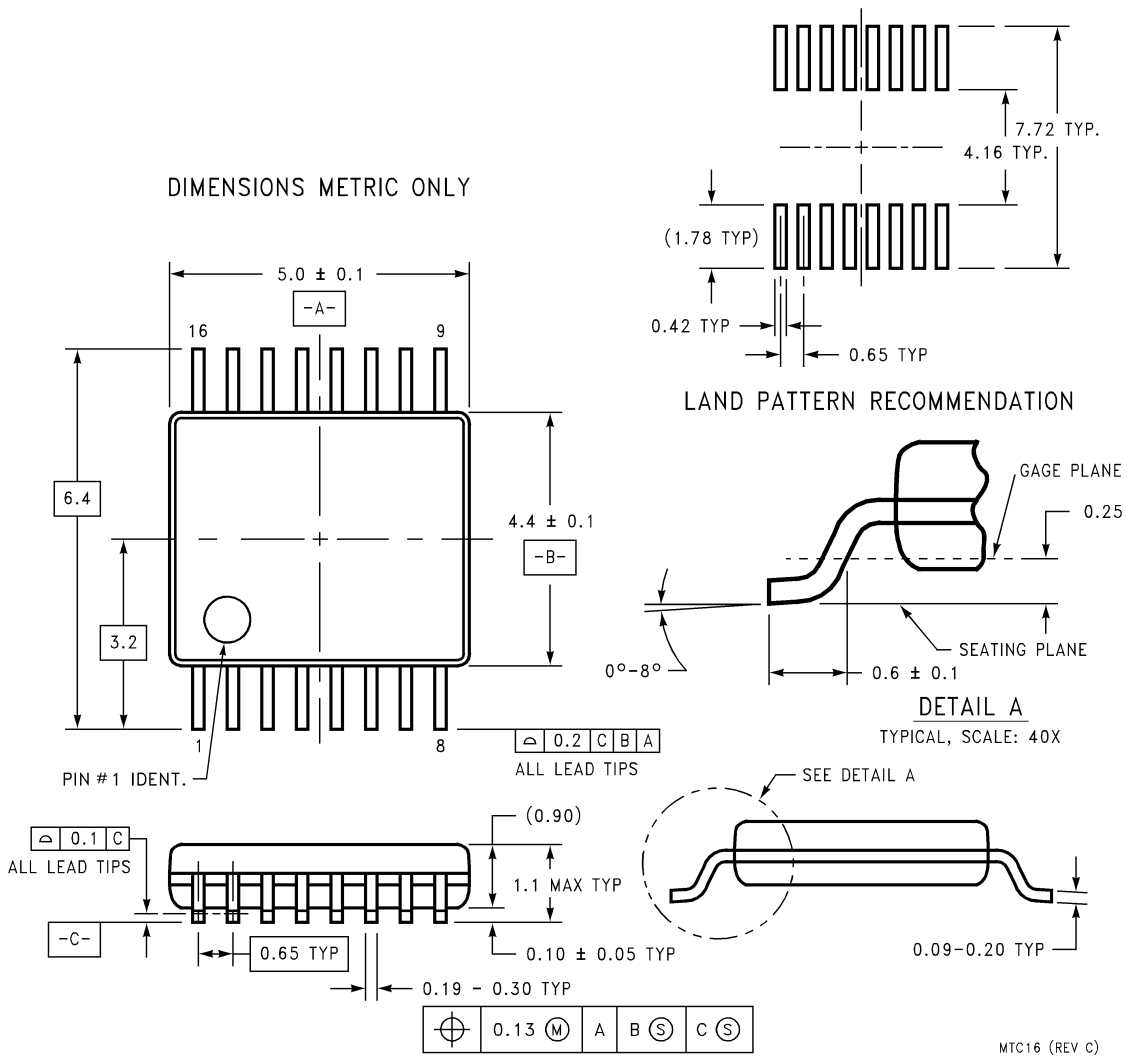
1.7.10 FastLock MODE 2 PROGRAMMING

Again, the F[1]–F[7] bits will be denoted as don't care (*) but are dependent on the desired modes of the applicable functions. To program the device for mode 2 FastLock, the F[8]–F[10] bits are programmed 101, while the N[19] bit is set to 1. The device will stay in the 4X current mode for the programmed number of phase detector cycles. Bits F[11]–F[14] program this number of cycles and are shown in *Table 6*. For our example, we will use 27 phase detector cycles, i.e. bits F[11]–F[14] will be 0110_b. After 27 phase detector cycles, the N[19] bit returns to zero, bringing the device back to low current mode. The resulting bit stream is as follows:



FastLock modes 3 and 4 are programmed in the same manner and give the added 4X gain increase as discussed in Section 1.3.4 FastLock modes.

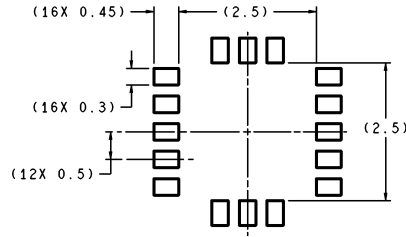
Physical Dimensions inches (millimeters) unless otherwise noted



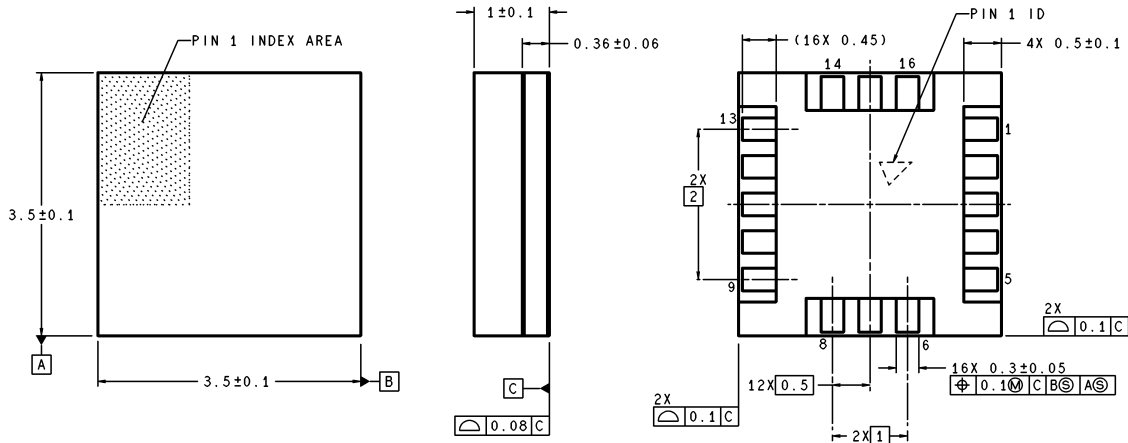
16-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)
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MTC16 (REV C)

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