LMV641 10 MHz, 12V, Low Power Amplifier

Check for Samples: LMV641

FEATURES

- **Guaranteed 2.7V, and ±5V Performance**
- **Low Power Supply Current 138 µA**
- **High Unity Gain Bandwidth 10 MHz**
- **Max Input Offset Voltage 500 µV**
- **CMRR 120 dB**
- **PSRR 105 dB**
- **Input Referred Voltage Noise 14 nV/√Hz**
- **1/f Corner Frequency 4 Hz**
- **Output Swing with 2 kΩ Load 40 mV from Rail**
- **Total Harmonic Distortion 0.002% @ 1kHz, 2kΩ**
- **Temperature Range −40°C to 125°C**

APPLICATIONS

- **Portable equipment**
- **Battery powered systems**
- **Sensors and instrumentation**

DESCRIPTION

The LMV641 is a low power, wide bandwidth operational amplifier with an extended power supply voltage range of 2.7V to 12V.

It features 10 MHz of gain bandwidth product with unity gain stability on a typical supply current of 138 µA. Other key specifications are a PSRR of 105 dB, CMRR of 120 dB, V_{OS} of 500 µV, input referred voltage noise of 14 nV/√Hz, and a THD of 0.002%. This amplifier has a rail-to-rail output stage, and a common mode input voltage which includes the negative supply.

The LMV641 operates over a temperature range of −40°C to +125°C and is offered in the board space saving 5-Pin SC70, SOT-23, and 8-Pin SOIC packages.

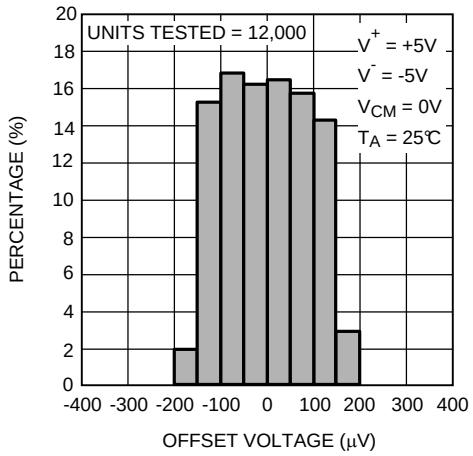


Figure 1. Offset Voltage Distribution

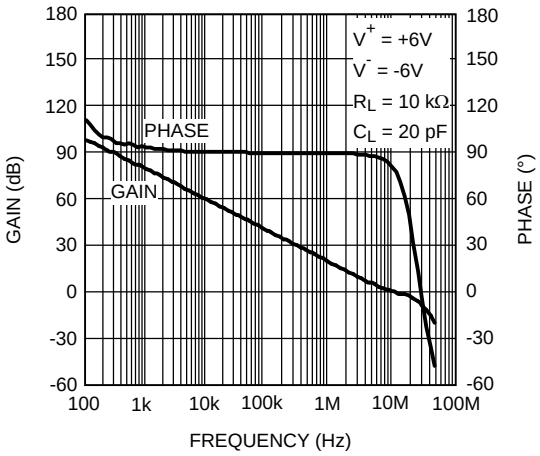


Figure 2. Open Loop Gain and Phase vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Differential Input V_{ID}	±0.3V
Supply Voltage ($V_S = V^+ - V^-$)	13.2V
Input/Output Pin Voltage	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (4)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Temperature Range (2)	−40°C to 125°C
Supply Voltage ($V_S = V^+ - V^-$)	2.7V to 12V
Package Thermal Resistance (θ_{JA})(2)	
5-Pin SC70	456°C/W
8-Pin SOIC	166°C/W
5-Pin SOT-23	325°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.7V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			30	500 **750**	µV
TC V_{OS}	Input Offset Average Drift			0.1		µV/°C
I_B	Input Bias Current	(3)		75	95 **110**	nA
I_{OS}	Input Offset Current			0.9	5	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	89 **84**	114		dB

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Positive current corresponds to current flowing into the device.

2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.7V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 10V, V_{CM} = 0.5		94.5 **92.5**	105		dB
		2.7V ≤ V^+ ≤ 12V, V_{CM} = 0.5		94 **92**	100		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB **CMRR ≥ 68 dB**		0		1.8	V
A_{VOL}	Large Signal Voltage Gain	0.3V ≤ V_O ≤ 2.4V, R_L = 2 kΩ to $V^+/2$ **0.4V ≤ V_O ≤ 2.3V, R_L = 2 kΩ to $V^+/2$**		82 **78**	88		dB
		0.3V ≤ V_O ≤ 2.4V, R_L = 10 kΩ to $V^+/2$ **0.4V ≤ V_O ≤ 2.3V, R_L = 10 kΩ to $V^+/2$**		86 **82**	98		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$, V_{IN} = 100 mV			42	58 **68**	mV from rail
		R_L = 10 kΩ to $V^+/2$, V_{IN} = 100 mV			22	35 **40**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$, V_{IN} = 100 mV			38	48 **58**	
		R_L = 10 kΩ to $V^+/2$, V_{IN} = 100 mV			18	30 **35**	
I_{OUT}	Sourcing and Sinking Output Current	V_{IN_DIFF} = 100 mV to $V_O = V^+/2$ (4)	Sourcing		22		mA
			Sinking		25		
I_S	Supply Current				138	170 **220**	µA
SR	Slew Rate	A_V = +1, V_O = 1 V_{PP}	Rising (10% to 90%)		2.3		V/µs
			Falling (90% to 10%)		1.6		
GBW	Gain Bandwidth Product				10		MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz			14		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz			0.15		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ			0.014		%

(4) The part is not short circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in the Typical Performance Characteristics and should be consulted before designing for heavy loads.

10V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 10V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			5	500 **750**	µV
TC V_{OS}	Input Offset Average Drift			0.1		µV/°C
I_B	Input Bias Current	(3)		70	90 **105**	nA
I_{OS}	Input Offset Current			0.7	5	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 9V	94 **90**	120		dB

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Positive current corresponds to current flowing into the device.

10V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 10V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 10V, V_{CM} = 0.5V		94.5 **92.5**	105		dB
		2.7V ≤ V^+ ≤ 12V, V_{CM} = 0.5V		94 **92**	100		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB **CMRR ≥ 76 dB**		0		9.1	V
A_{VOL}	Large Signal Voltage Gain	0.3V ≤ V_O ≤ 9.7V, R_L = 2 kΩ to $V^+/2$ **0.4V ≤ V_O ≤ 9.6V, R_L = 2 kΩ to $V^+/2$**		90 **85**	99		dB
		0.3V ≤ V_O ≤ 9.7V, R_L = 10 kΩ to $V^+/2$ **0.4V ≤ V_O ≤ 9.6V, R_L = 10 kΩ to $V^+/2$**		97 **92**	104		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$, V_{IN} = 100 mV			68	95 **125**	mV from rail
		R_L = 10 kΩ to $V^+/2$, V_{IN} = 100 mV			37	55 **65**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$, V_{IN} = 100 mV			65	90 **110**	
		R_L = 10 kΩ to $V^+/2$, V_{IN} = 100 mV			32	42 **52**	
I_{OUT}	Sourcing and Sinking Output Current	V_{IN_DIFF} = 100 mV to $V_O = V^+/2$ (4)	Sourcing		26		mA
			Sinking		112		
I_S	Supply Current				158	190 **240**	µA
SR	Slew Rate	A_V = +1, V_O = 2V to 8 V_{PP}	Rising (10% to 90%)		2.6		V/µs
			Falling (90% to 10%)		1.6		
GBW	Gain Bandwidth Product				10		MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz			14		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz			0.15		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ			0.002		%

(4) The part is not short circuit protected and is not recommended for operation with low resistive loads. Typical sourcing and sinking output current curves are provided in the Typical Performance Characteristics and should be consulted before designing for heavy loads.

CONNECTION DIAGRAMS

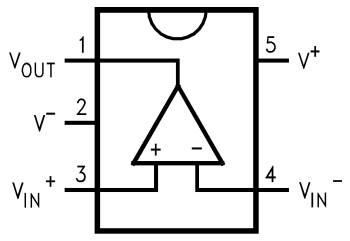


Figure 3. 5-Pin SOT-23/SC70
Top View

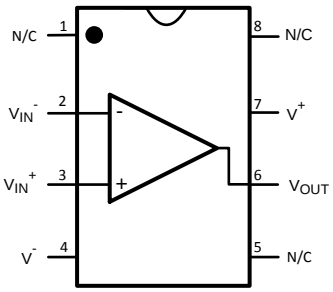


Figure 4. 8-Pin SOIC
Top View

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_S/2.

Supply Current vs. Supply Voltage

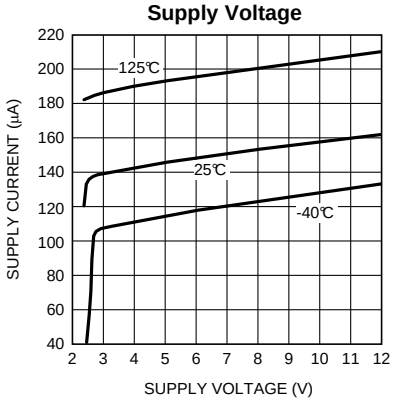


Figure 5.

Offset Voltage vs. Supply Voltage

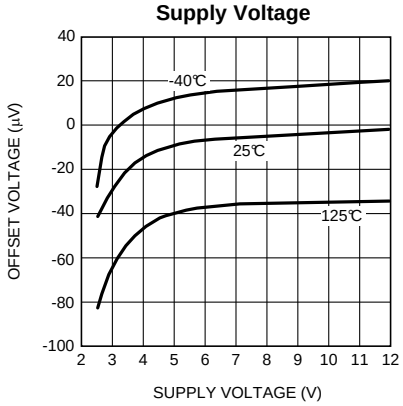


Figure 6.

Offset Voltage vs. V_{CM}

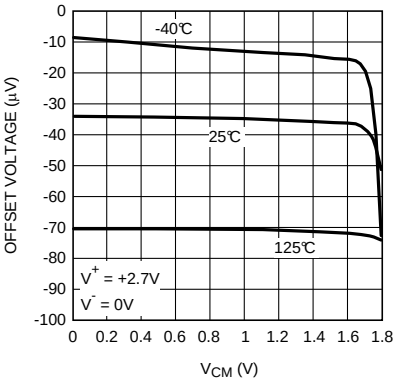


Figure 7.

Offset Voltage vs. V_{CM}

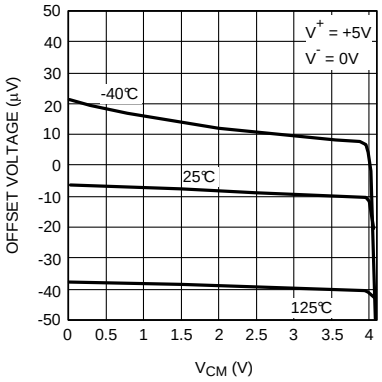


Figure 8.

Offset Voltage vs. V_{CM}

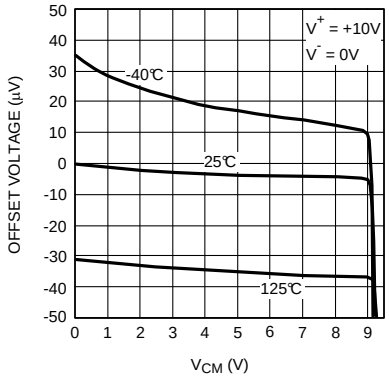


Figure 9.

Offset Voltage vs. V_{CM}

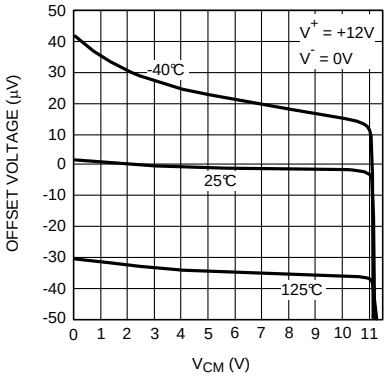


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_S/2.

Offset Voltage Distribution

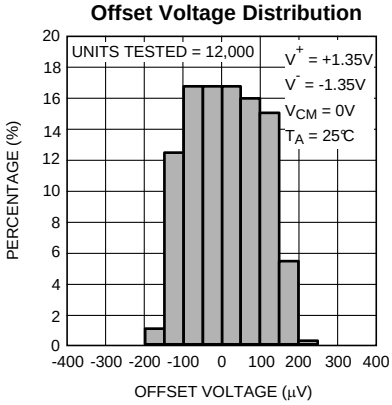


Figure 11.

Offset Voltage Distribution

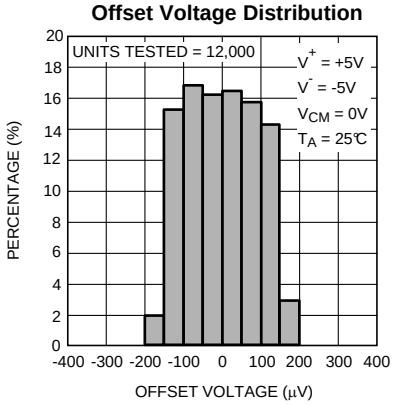


Figure 12.

CMRR vs. Frequency

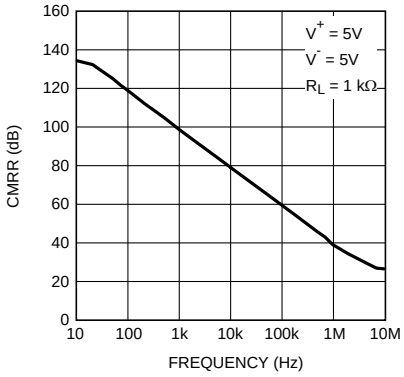


Figure 13.

PSRR vs. Frequency

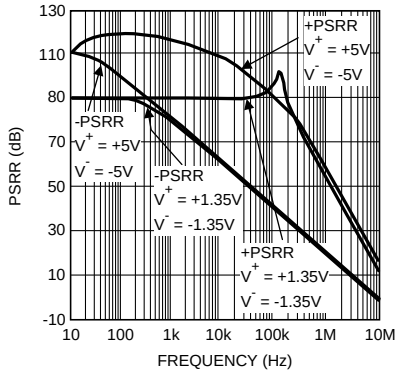


Figure 14.

Input Bias Current vs. V_{CM}

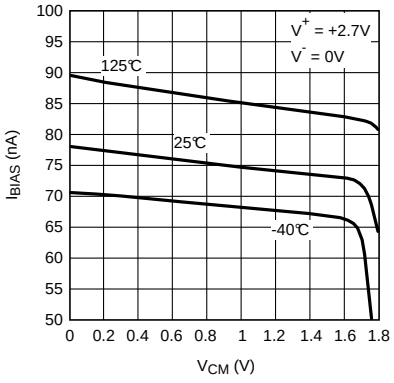


Figure 15.

Input Bias Current vs. V_{CM}

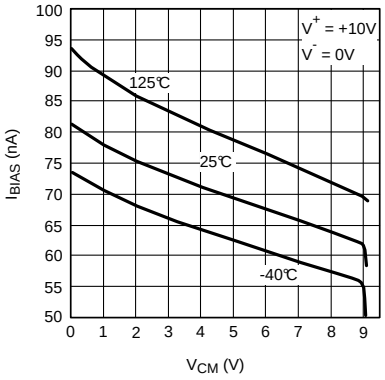


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_S/2.

Open Loop Gain and Phase with Capacitive Load

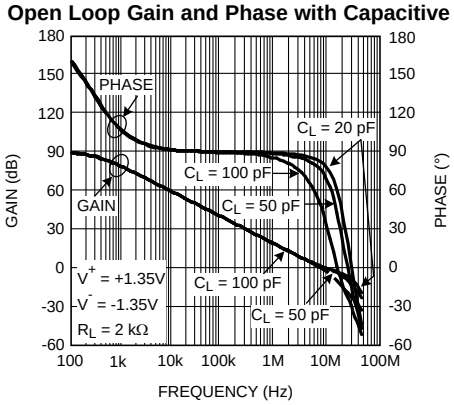


Figure 17.

Open Loop Gain and Phase with Capacitive Load

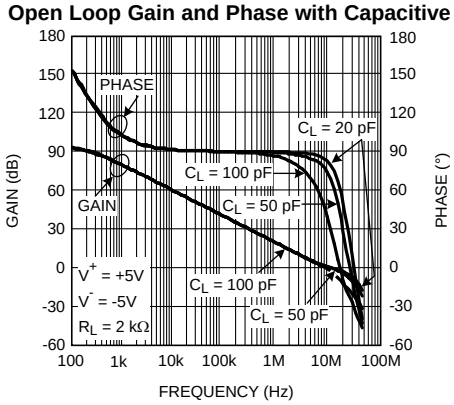


Figure 18.

Open Loop Gain and Phase with Resistive Load

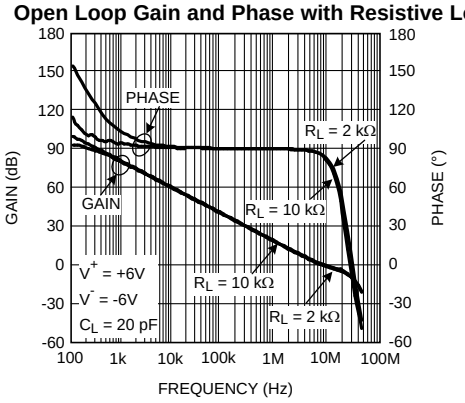


Figure 19.

Open Loop Gain and Phase with Supply Voltage

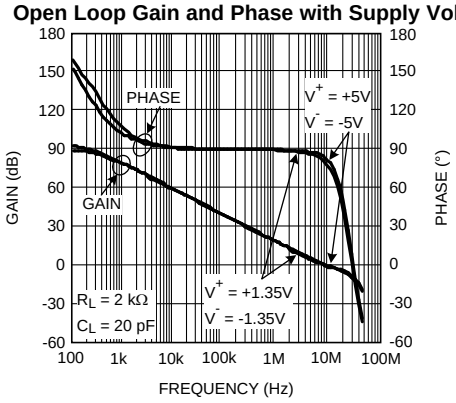


Figure 20.

Input Referred Noise Voltage vs. Frequency

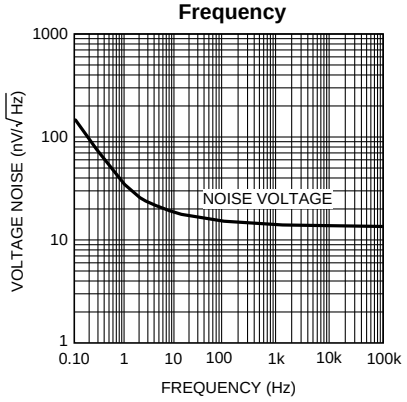


Figure 21.

Close Loop Output Impedance vs. Frequency

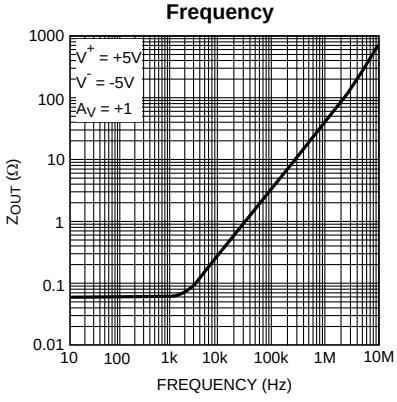


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_S/2.

THD+N vs. Frequency

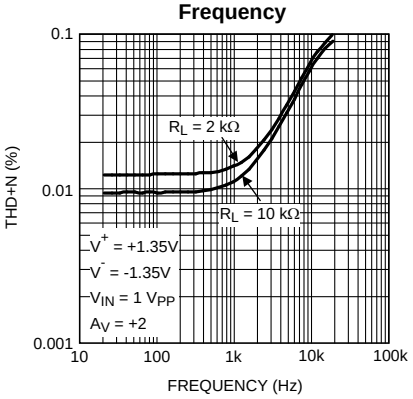


Figure 23.

THD+N vs. Frequency

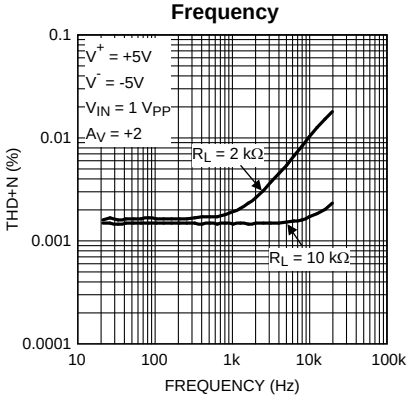


Figure 24.

THD+N vs. V_{OUT}

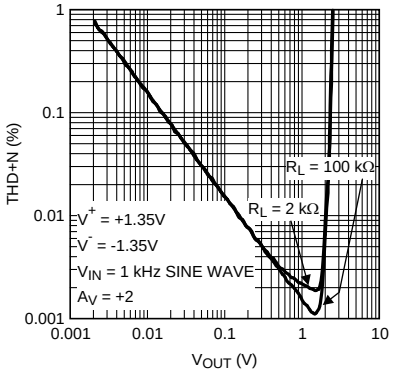


Figure 25.

THD+N vs. V_{OUT}

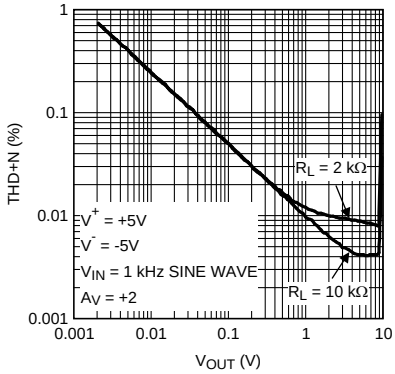


Figure 26.

Sourcing Current vs. Supply Voltage

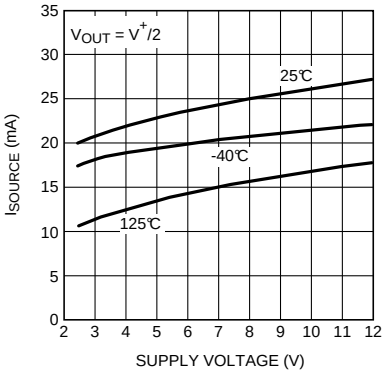


Figure 27.

Sinking Current vs. Supply Voltage

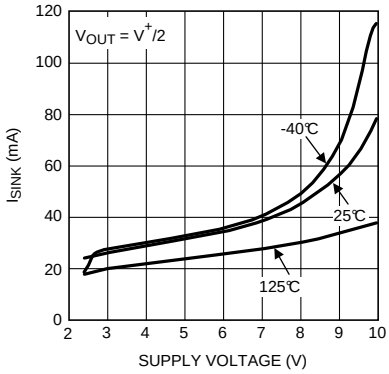


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_S/2.

Sourcing Current vs. V_{OUT}

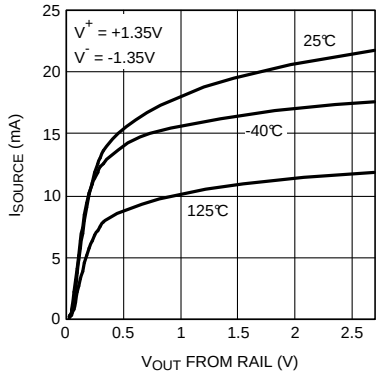


Figure 29.

Sinking Current vs. V_{OUT}

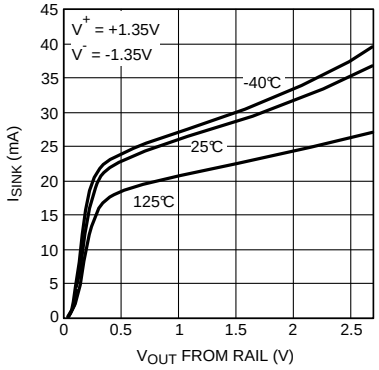


Figure 30.

Sourcing Current vs. V_{OUT}

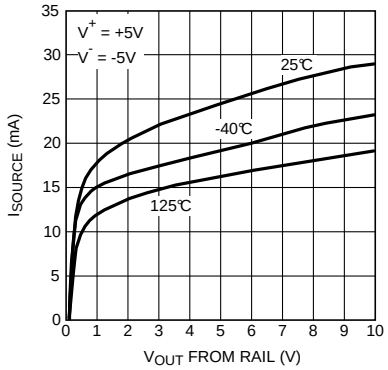


Figure 31.

Large Signal Transient

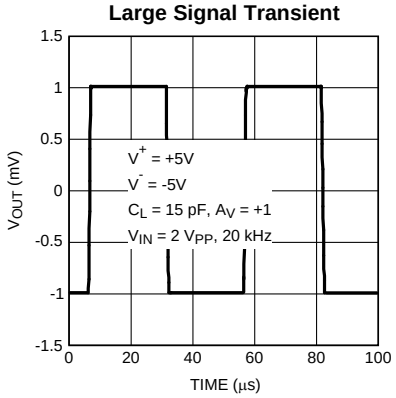


Figure 32.

Small Signal Transient Response

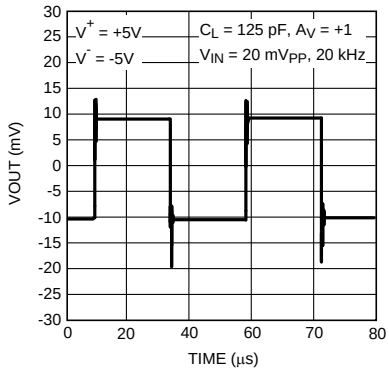


Figure 33.

Small Signal Transient Response

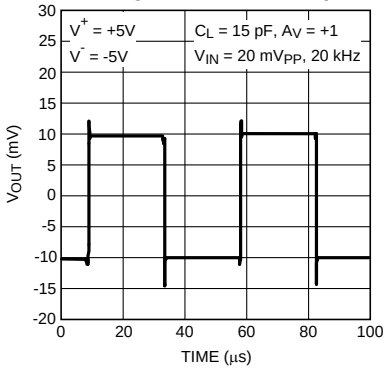


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_S/2.

Output Swing High vs. Supply Voltage

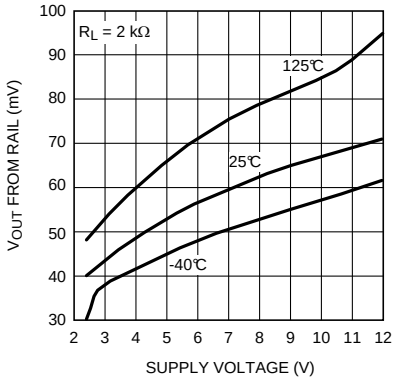


Figure 35.

Output Swing Low vs. Supply voltage

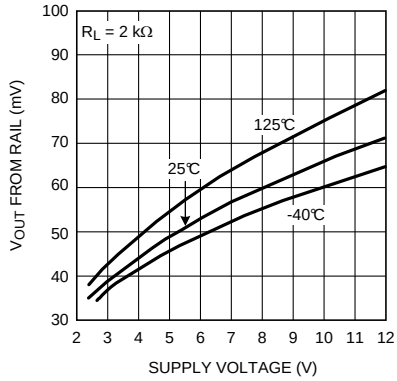


Figure 36.

Output Swing High vs. Supply Voltage

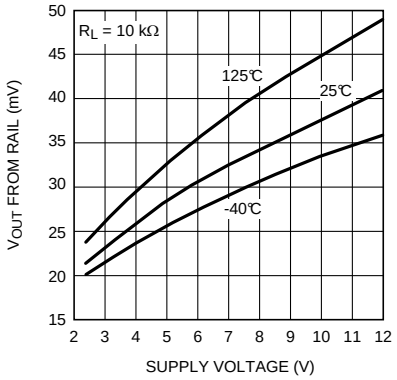


Figure 37.

Output Swing Low and Supply Voltage

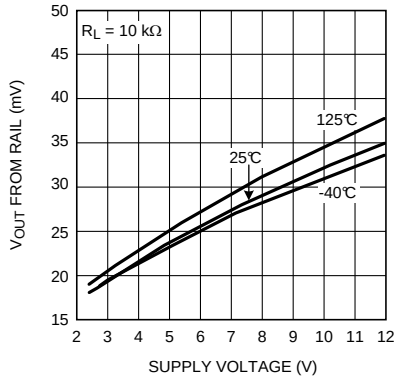


Figure 38.

Slew Rate vs. Supply Voltage

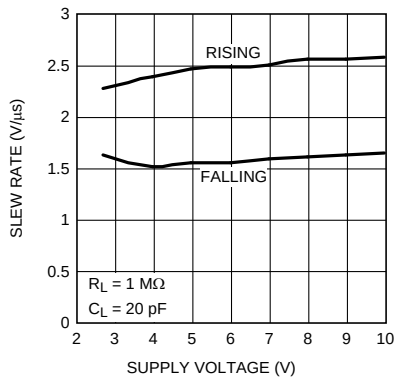


Figure 39.

APPLICATION INFORMATION

ADVANTAGES OF THE LMV641

Low Voltage and Low Power Operation

The LMV641 has performance guaranteed at supply voltages of 2.7V and 10V. It is guaranteed to be operational at all supply voltages between 2.7V and 12.0V. The LMV641 draws a low supply current of 138 µA. The LMV641 provides the low voltage and low power amplification which is essential for portable applications.

Wide Bandwidth

Despite drawing the very low supply current of 138 µA, the LMV641 manages to provide a wide unity gain bandwidth of 10 MHz. This is easily one of the best bandwidth to power ratios ever achieved, and allows this op amp to provide wideband amplification while using the minimum amount of power. This makes the LMV641 ideal for low power signal processing applications such as portable media players and other accessories.

Low Input Referred Noise

The LMV641 provides a flatband input referred voltage noise density of 14 nV/$\sqrt{\text{Hz}}$, which is significantly better than the noise performance expected from a low power op amp. This op amp also feature exceptionally low 1/f noise, with a very low 1/f noise corner frequency of 4 Hz. Because of this the LMV641 is ideal for low power applications which require decent noise performance, such as PDAs and portable sensors.

Ground Sensing and Rail-to-Rail Output

The LMV641 has a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing. The input common mode range of this part includes the negative supply rail which allows direct sensing at ground in a single supply operation.

Small Size

The small footprint of the packages for the LMV641 saves space on printed circuit boards, and enables the design of smaller and more compact electronic products. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using a physically smaller package, these op amps can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity.

STABILITY OF OP AMP CIRCUITS

If the phase margin of the LMV641 is plotted with respect to the capacitive load (C_L) at its output, and if C_L is increased beyond 100 pF then the phase margin reduces significantly. This is because the op amp is designed to provide the maximum bandwidth possible for a low supply current. Stabilizing the LMV641 for higher capacitive loads would have required either a drastic increase in supply current, or a large internal compensation capacitance, which would have reduced the bandwidth. Hence, if this device is to be used for driving higher capacitive loads, it will have to be externally compensated.

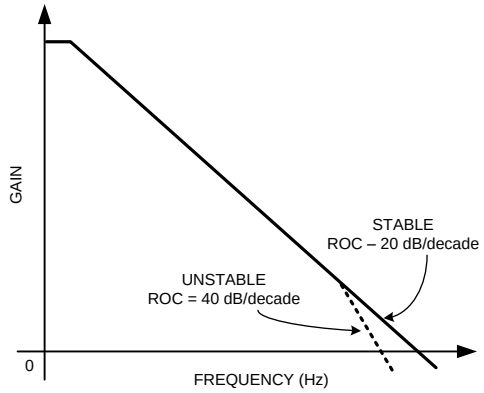


Figure 40. Gain vs. Frequency for an Op Amp

An op amp, ideally, has a dominant pole close to DC which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains the same until the op amp's unity gain bandwidth, then the op amp is stable. If, however, a large capacitance is added to the output of the op amp, it combines with the output impedance of the op amp to create another pole in its frequency response before its unity gain frequency (Figure 40). This increases the ROC to 40 dB/decade and causes instability.

In such a case, a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to an ROC of 20 dB/decade, which ensures stability.

In The Loop Compensation

Figure 41 illustrates a compensation technique, known as *in the loop* compensation, that employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

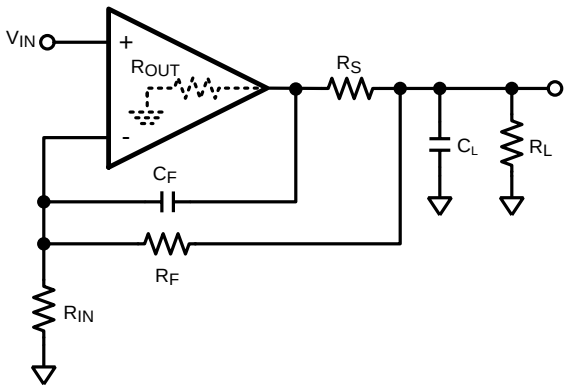


Figure 41. In the Loop Compensation

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/ decade. For the circuit shown in Figure 41 the values of R_S and C_F are given by Equation 1. Values of R_S and C_F required for maintaining stability for different values of C_L, as well as the phase margins obtained, are shown in Table 1. R_F and R_{IN} are 10 kΩ, R_L is 2 kΩ, while R_{OUT} is 680Ω.

$$R_S = \frac{R_{OUT} R_{IN}}{R_F}$$

$$C_F = \left(\frac{R_F + 2R_{IN}}{R_F^2} \right) C_L R_{OUT} \tag{1}$$

Table 1.

C_L (nF)	R_S (Ω)	C_F (pF)	Phase Margin (°)
0.5	680	10	17.4
1	680	20	12.4
1.5	680	30	10.1

The LMV641 is capable of driving heavy capacitive loads of up to 1 nF without oscillating, however it is recommended to use compensation should the load exceed 1 nF. Using this methodology will reduce any excessive ringing and help maintain the phase margin for stability. The values of the compensation network tabulated above illustrate the phase margin degradation as a function of the capacitive load.

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed loop bandwidth of the circuit is now limited by R_F and C_F.

Compensation by External Resistor

In some applications it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 42. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. This introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance, and ensures stability. The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5Ω to 50Ω are usually sufficient to ensure stability. A larger value of R_{ISO} will result in a system with less ringing and overshoot, but will also limit the output swing and the short circuit current of the circuit.

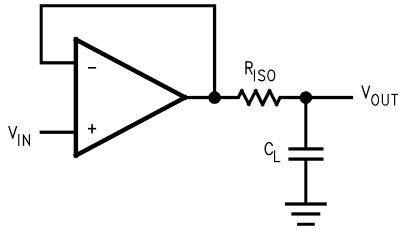


Figure 42. Compensation by Isolation Resistor

TYPICAL APPLICATIONS

ANISOTROPIC MAGNETORESISTIVE SENSOR

The low operating current of the LMV641 makes it a good choice for battery operated applications. Figure 43 shows two LMV641s in a portable application with a magnetic field sensor. The LMV641s condition the output from an anisotropic magnetoresistive (AMR) sensor. The sensor is arranged in the form of a Wheatstone bridge. This type of sensor can be used to accurately measure the current (either DC or AC) flowing in a wire by measuring the magnetic flux density, **B**, emanating from the wire.

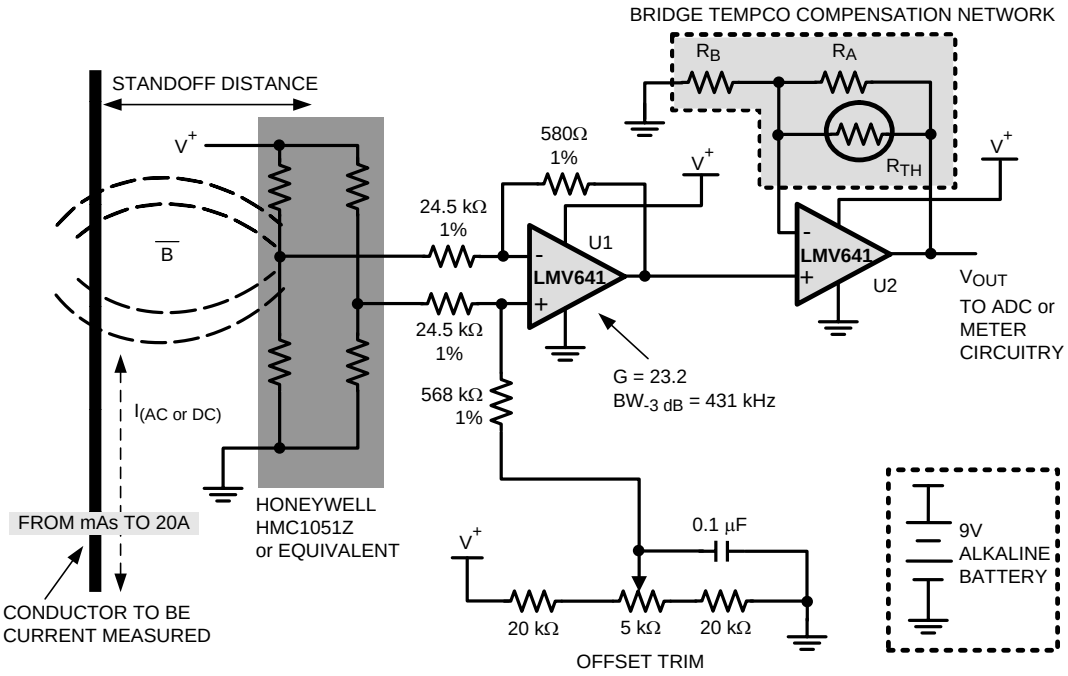


Figure 43. A Battery Operated System for Contact-Less Current Sensing Using an Anisotropic Magnetoresistive Sensor

In this circuit, the use of a 9-volt alkaline battery exploits the LMV641's high voltage and low supply current for a low power, portable current sensing application. The sensor converts an incident magnetic field (via the magnetic flux linkage) in the sensitive direction, to a balanced voltage output. The LMV641 can be utilized for moderate to high current sensing applications (from a few milliamps and up to 20A) using a nearby external conductor providing the sensed magnetic field to the bridge. The circuit shows a Honeywell HMC1051Z used as a current sensor. Note that the circuit must be calibrated based on the final displacement of the sensed conductor relative to the measurement bridge. Typically, once the sensor has been oriented properly, with respect to the conductor to be measured, the conductor can be placed about one centimeter away from the bridge and have reasonable capability of measuring from tens of milliamperes to beyond 20 amperes.

In Figure 43, U1 is configured as a single differential input amplifier. Its input impedance is relatively low, however, and requires that the source impedance of the sensor be considered in the gain calculations. Also, the asymmetrical loading on the bridge will produce a small offset voltage that can be cancelled out with the offset trim circuit shown in Figure 43.

Figure 44 shows a typical magnetoresistive Wheatstone bridge and the Thevenin equivalent of its resistive elements. As we shall see, the Thevenin equivalent model of the sensor is useful in calculating the gain needed in the differential amplifier.

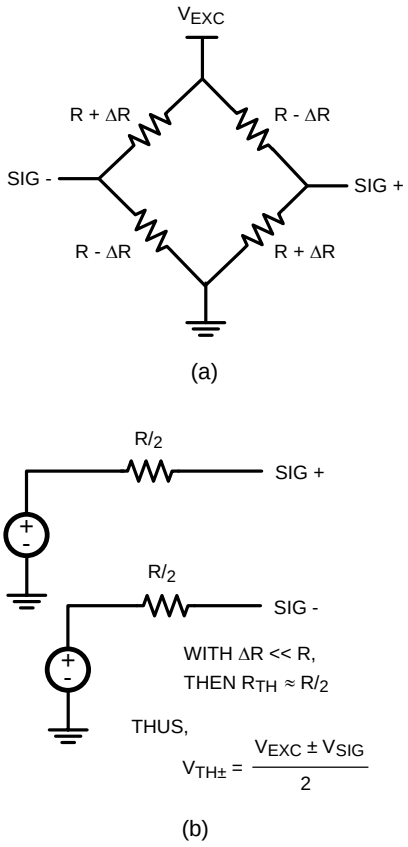


Figure 44. Anisotropic Magnetoresistive Wheatstone Bridge Sensor, (a), and Thevenin Equivalent Circuit, (b)

Using Thevenin's Theorem, the bridge can be reduced to two voltage sources with series resistances. ΔR is normally very small in comparison to R, thus the Thevenin equivalent resistance, commonly called the source resistance, can be taken to be R. When a bias voltage is applied between V_{EXC} and ground, in the absence of a magnetic field, all of the resistances are considered equal. The voltage at Sig+ and Sig− is half V_{EXC}, or 4.5V, and Sig+ - Sig− = 0. Bridges are designed such that, when immersed in a magnetic field, opposite resistances in the bridge change by ±ΔR with an amount proportional to the strength of the magnetic field. This causes the bridge's output differential voltage, to change from its half V_{EXC} value. Thus Sig+ - Sig− = Vsig ≠ 0. With four active elements, the output voltage is:

$$V_{SIG} = V_{EXC} \times \frac{\Delta R}{R} \quad (2)$$

Since ΔR is proportional to the field strength, B_S, the amount of output voltage from the sensor is a function of sensor sensitivity, S. This expression can rewritten as $V_{SIG} = V_{EXC} \cdot S \cdot B_S$, where

S = material constant (nominally 1 mV/V/gauss)

B_S = magnetic flux in gauss

A simplified schematic of a single op amp, differential amplifier is shown in Figure 45. The Thevenin equivalent circuit of the sensor can be used to calculate the gain of this amplifier.

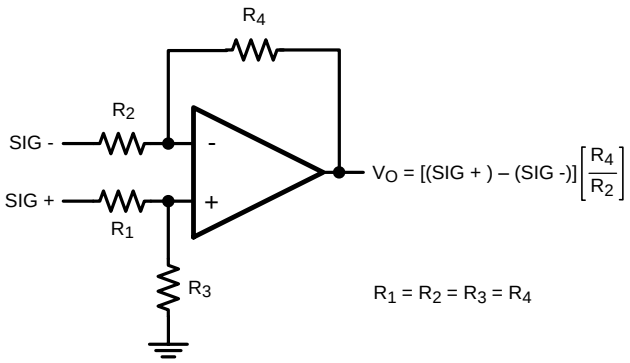


Figure 45. Differential Input Amplifier

The Honeywell HMC1051Z AMR sensor has nominal 1 kΩ elements and a sensitivity of 1 mV/V/gauss and is being used with 9V of excitation with a full scale magnetic field range of ±6 gauss. At full-scale, the resistors will have ΔR ≈ 12Ω and 108 mV will be seen from Sig− to Sig+ (refer to Figure 46).

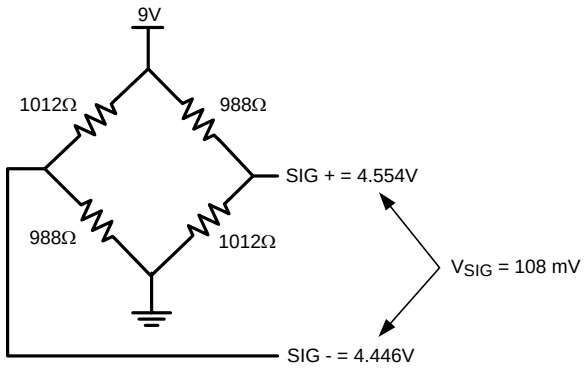


Figure 46. Sensor Output with No Load

Referring to the simplified diagram in Figure 45, and assuming that required full scale at the output of the amplifier is 2.5V, a gain of 23.2 is needed for U1. It is clear from the Thevenin equivalent circuit in Figure 47 that a sensor Thevenin equivalent source resistance, R_{THEV}, of 500Ω will be in series with both the inverting and non-inverting inputs of the LMV641. Therefore, the required gain is:

$$A_{VCL} = \frac{R_4}{R_{THEV} + R_2} = 23.2 \quad (3)$$

Choosing $R_1 = R_2 = 24.5$ kΩ, then R_4 will be approximately 580 kΩ. The actual values chosen will depend on the full-scale needs of the succeeding circuitry as well as bandwidth requirements. The values shown here provide a −3 dB bandwidth of approximately 431 kHz, and are found as follows.

$$BW_{-3\ dB} = \frac{\text{GAIN-BANDWIDTH PRODUCT}}{A_{VCL}} = \frac{10\ MHz}{23.2} = 431\ kHz$$

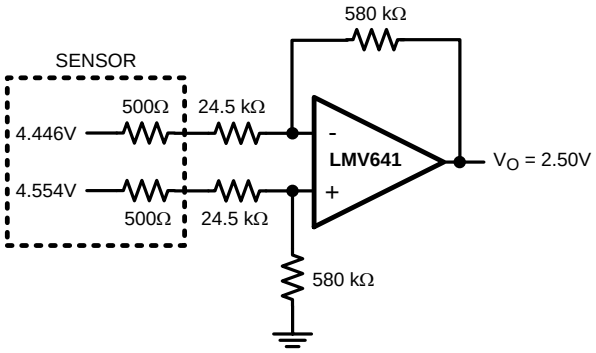


Figure 47. Thevenin Equivalent Showing Required Gain

By choosing input resistor values for R_1 and R_2 that are four to ten times the bridge element resistance, the bridge is minimally loaded and the offset errors induced by the op amp stages are minimized. These resistors should have 1% tolerance, or better, for the best noise rejection and offset minimization.

Referring once again to Figure 43, U2 is an additional gain stage with a thermistor element, R_{TH}, in the feedback loop. It performs a temperature compensation function for the bridge so that it will have greater accuracy over a wide range of operational temperatures. With mangetoresistive sensors, temperature drift of the bridge sensitivity is negative and linear, and in the case of the sensor used here, is nominally −3000 PP/M. Thus the gain of U2 needs to increase proportionally with increasing temperature, suggesting a thermistor with a positive temperature coefficient. Selection of the temperature compensation resistor, R_{TH}, depends on the additional gain required, on the thermistor chosen, and is dependent on the thermistor's %/°C shift in resistance. For best op amp compatibility, the thermistor resistance should be greater than 1000Ω. R_{TH} should also be much less than R_A, the feedback resistor. Because the temperature coefficient of the AMR bridge is largely linear, R_{TH} also needs to behave in a linear fashion with temperature, thus R_A is placed in parallel with R_{TH}, which acts to linearize the thermistor.

Gain Error and Bandwidth Consideration if Using an Analog to Digital Converter

The bandwidth available from Figure 43 is dependent on the system closed loop gain required and the maximum gain-error allowed if driving an analog to digital converter (ADC). If the output from the sensor is intended to drive an ADC, the bandwidth will be considerably reduced from the closed-loop corner frequency. This is because the gain error of the pre-amplifier stage needs to be taken into account when calculating total error budget. Good practice dictates that the gain error of the amplifier be less than or equal to half LSB (preferably less in order to allow for other system errors that will eat up a portion of the available error budget) of the ADC. However, at the −3 dB corner frequency the gain error for any amplifier is 29.3%. In reality, the gain starts rolling off long before the −3 dB corner is reached. For example, if the amplifier is driving an 8-bit ADC, the minimum gain error allowed for half LSB would be approximately 0.2%. To achieve this gain error with the op amp, the maximum frequency of interest can be no higher than

$$\sqrt{\frac{1}{\left(1 - \frac{1}{2^{n+1}}\right)^2} - 1} \times f_{-3\ dB} \tag{4}$$

where n is the bit resolution of the ADC and $f_{-3\ dB}$ is the closed loop corner frequency.

Given that the LMV641 has a GBW of 10 MHz, and is operating with a closed loop gain of 26.3, its closed loop bandwidth is 380 kHZ, therefore

$$\text{MAX FREQ} = \sqrt{\frac{1}{\left(1 - \frac{1}{2^{n+1}}\right)^2}} - 1 = 0.062 \times f_{-3\,dB}$$

$$= 0.062 \times 380\ \text{kHz} = 23.56\ \text{kHz} \quad (5)$$

which is the highest frequency that can be measured with required accuracy.

VOICEBAND FILTER

The majority of the energy of recognizable speech is within a band of frequencies between 200 Hz and 4 kHz. Therefore it is beneficial to design circuits which transmit telephone signals that pass only certain frequencies and eliminate unwanted signals (noise) that could interfere with conversations and introduce error into control signals. The pass band of these circuits is defined as the ranges of frequencies that are passed. A telephone system voice frequency (VF) channel has a pass band of 0 Hz to 4 kHz. Specifically for human voices most of the energy content is found from 300 Hz to 3 kHz and any signal within this range is considered an in-band signal. Alternatively, any signal outside this range but within the VF channel is considered an out-of-band signal.

To properly recover a voice signal in applications such as cellular phones, cordless phones, and voice pagers, a low power bandpass filter that is matched to the human voice spectrum can be implemented using an LMV641 op amp. Figure 48 shows a multi-feedback, multi-pole filter (2^{nd} order response) with a gain of −1. The lower 3 dB cutoff frequency which is set by the DC blocking capacitor C_1 and resistor R_1 is 60 Hz and the upper cutoff frequency is 3.5 kHz.

The total current consumption is a mere 138 µA. The LV641 is operating with a gain of −1, but the circuit is easily modified to add gain. The op amp is powered from a single supply, hence the need for offset (common-mode) adjustment of its output, which is set to ½ V_S via its non-inverting input.

This filter is also useful in applications for battery operated talking toys and games.

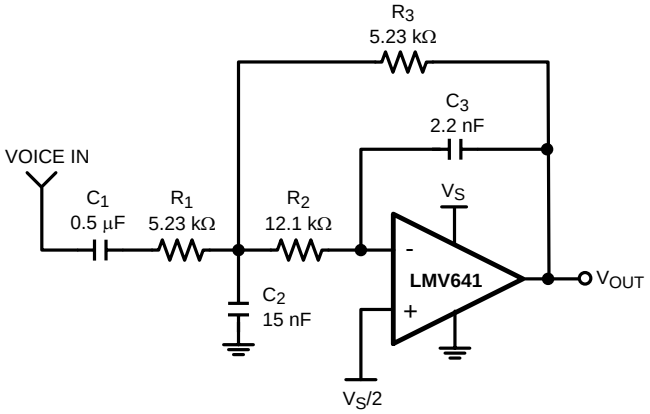


Figure 48. Low Power Voice In-Band Receive Filter for Battery-Powered Portable Use

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI Format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV641MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV64 1MA	Samples
LMV641MAE/NOPB	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV64 1MA	Samples
LMV641MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV64 1MA	Samples
LMV641MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AB9A	Samples
LMV641MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AB9A	Samples
LMV641MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AB9A	Samples
LMV641MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A99	Samples
LMV641MGE/NOPB	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A99	Samples
LMV641MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A99	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

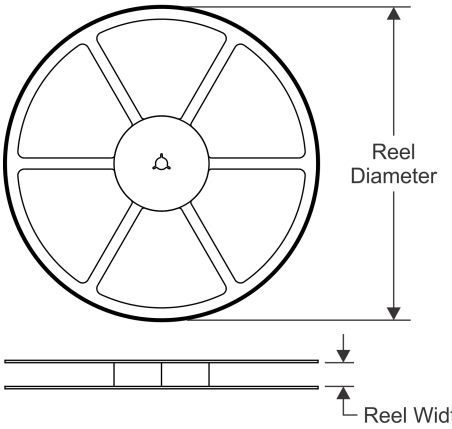
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

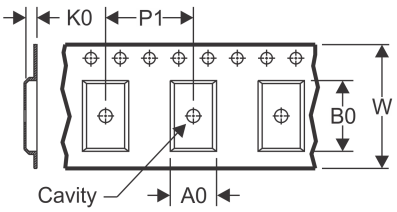
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

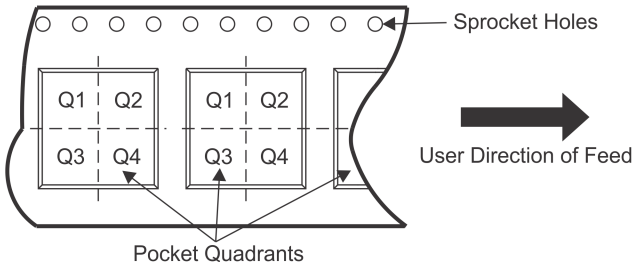


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

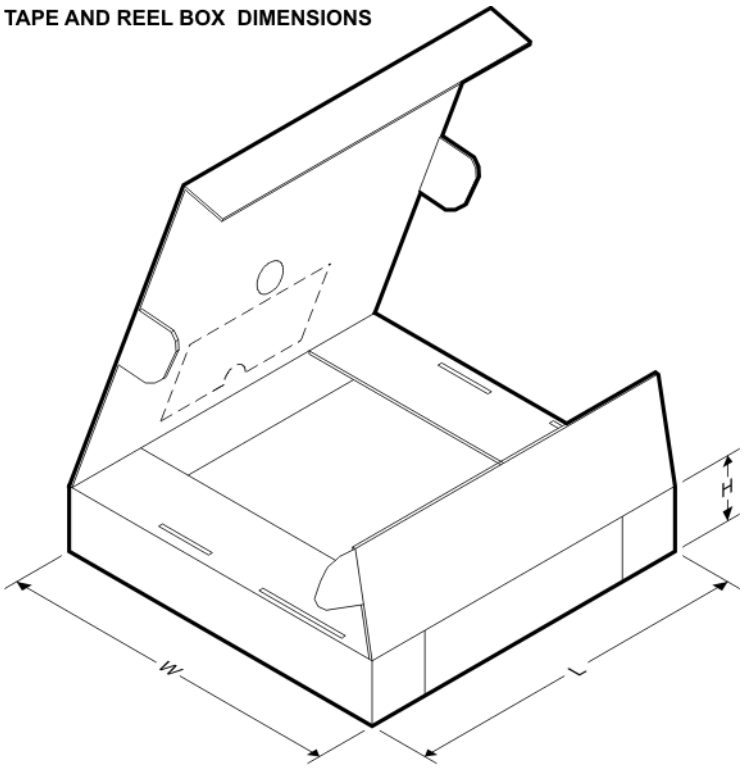
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV641MAE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV641MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV641MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV641MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV641MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV641MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV641MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV641MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

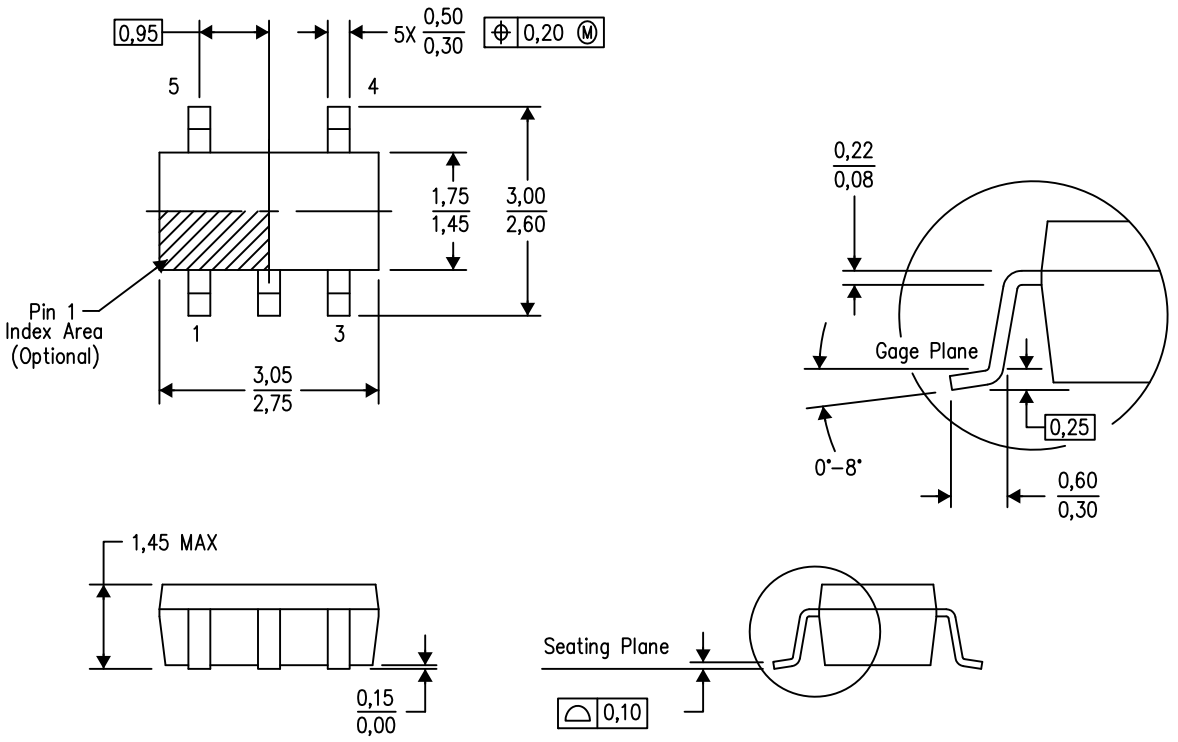
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV641MAE/NOPB	SOIC	D	8	250	210.0	185.0	35.0
LMV641MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV641MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV641MFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LMV641MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV641MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV641MGE/NOPB	SC70	DCK	5	250	210.0	185.0	35.0
LMV641MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

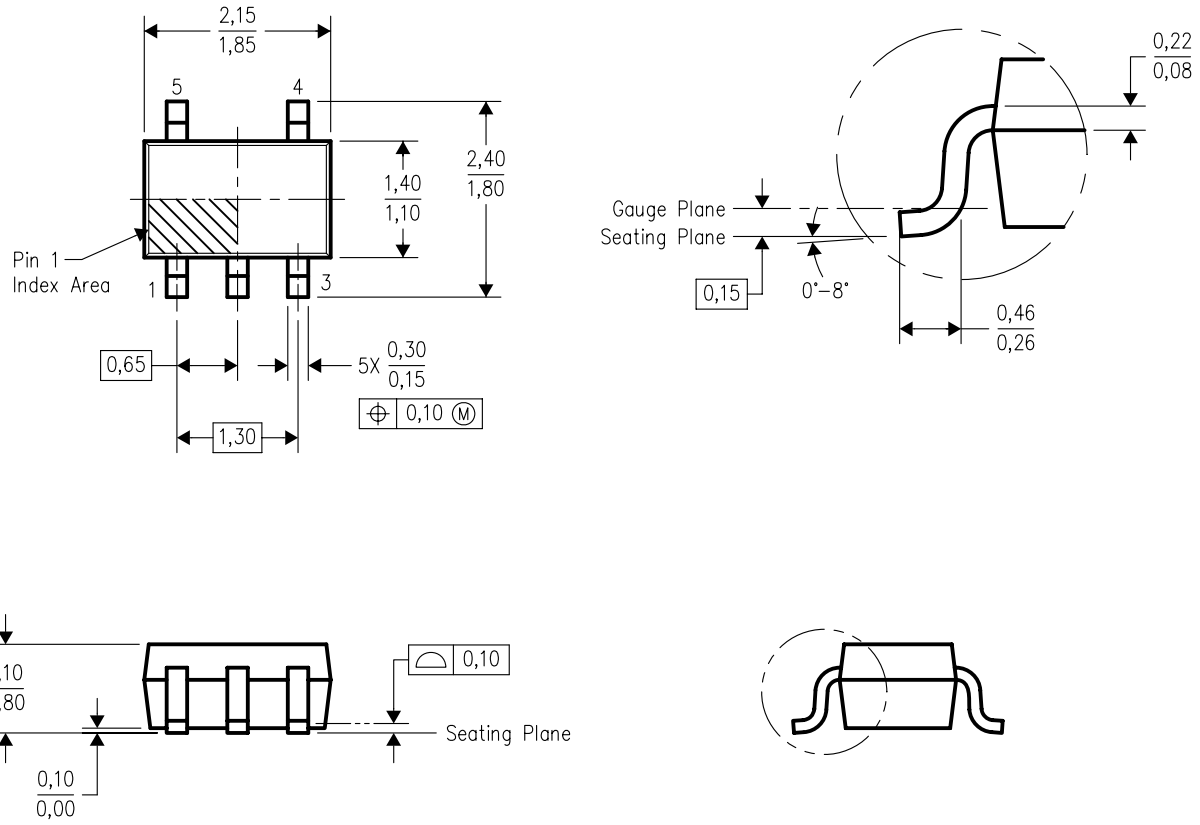
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

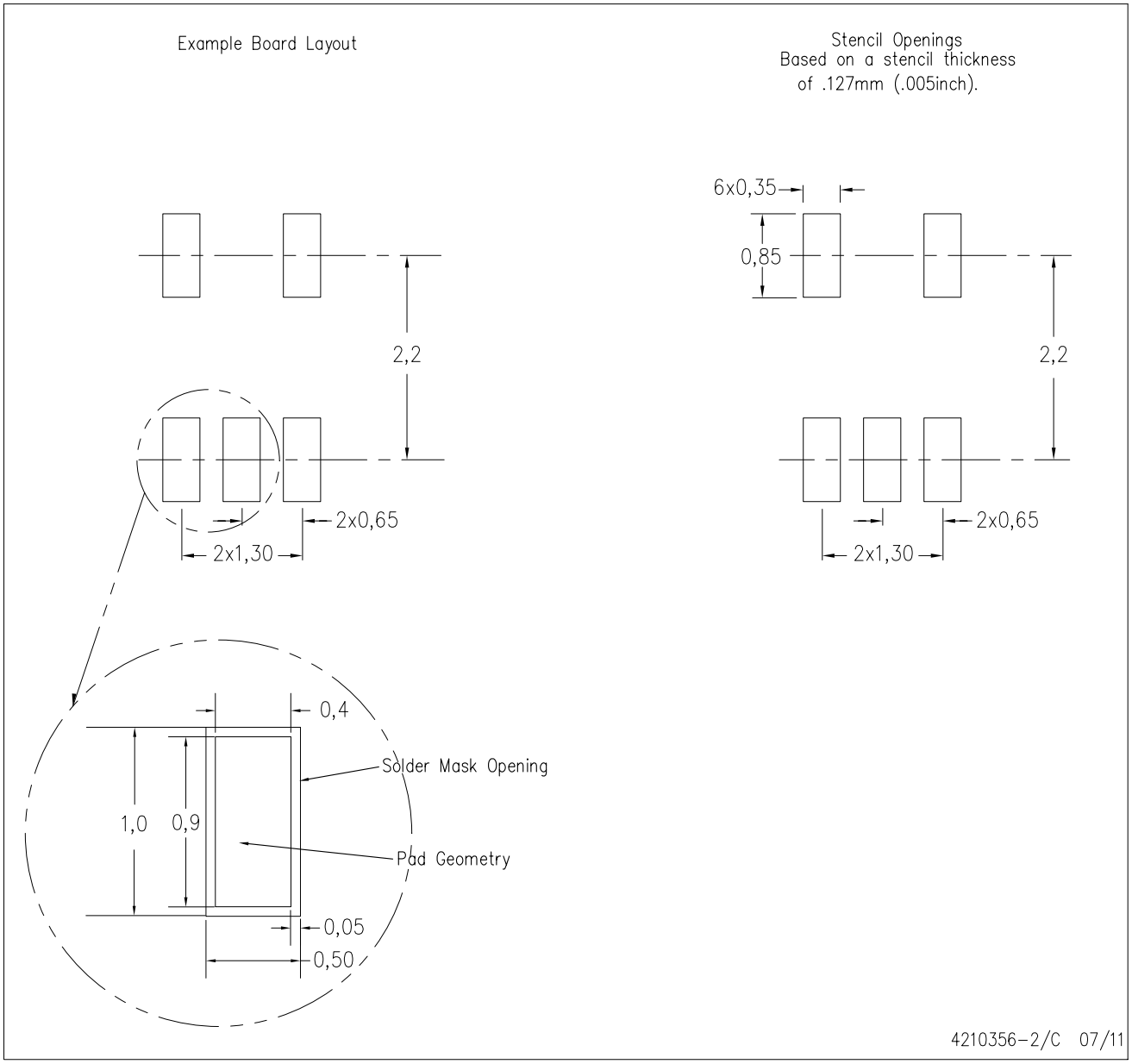
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

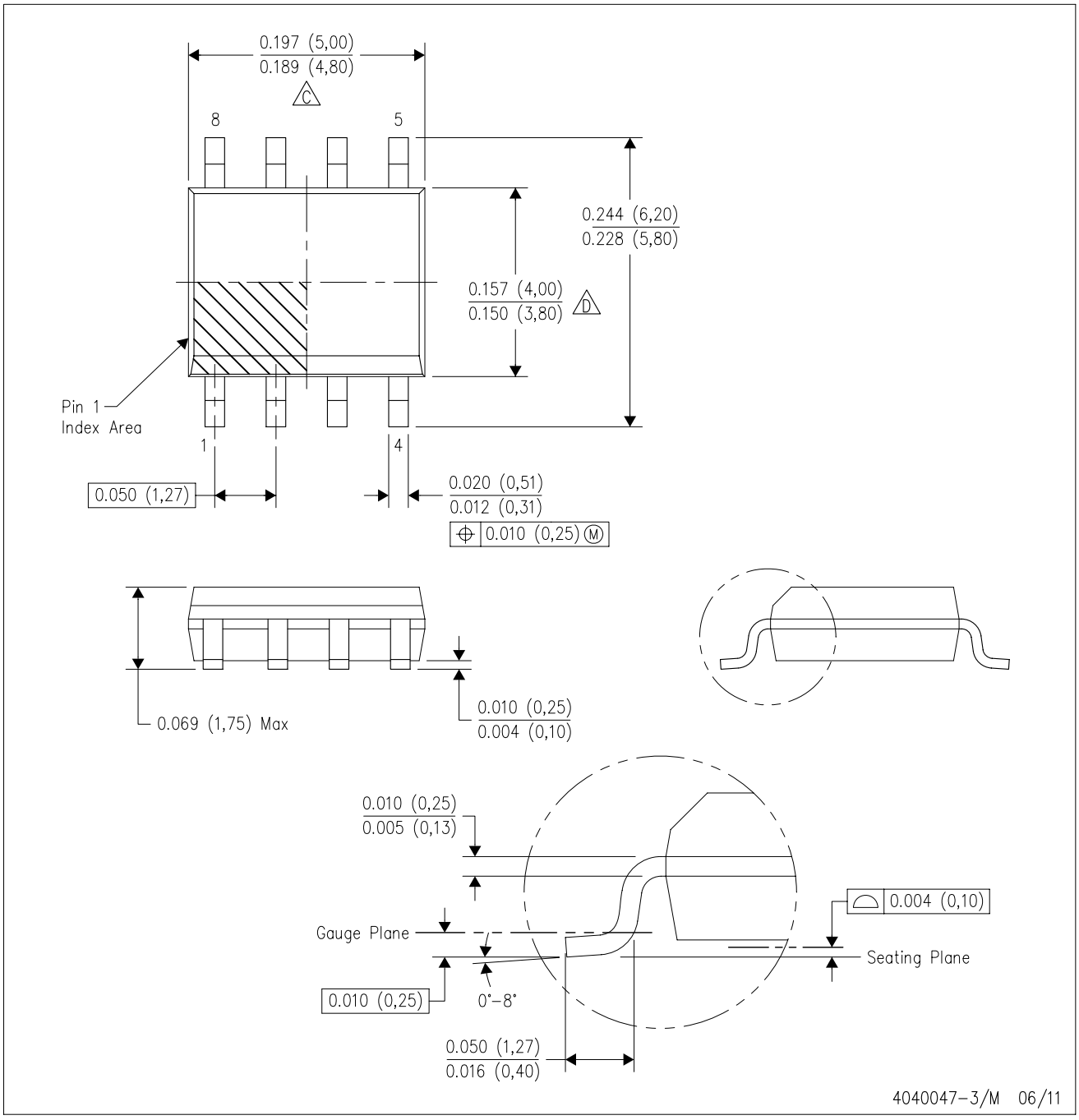
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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