LMR10510

LMR10510 SIMPLE SWITCHER ® 5.5Vin, 1A Step-Down Voltage Regulator in SOT-23 and LLP

Literature Number: SNVS727A

Texas Instruments

LMR10510

SIMPLE SWITCHER® 5.5Vin, 1A Step-Down Voltage Regulator in SOT-23 and LLP

Features

- Input voltage range of 3V to 5.5V
- Output voltage range of 0.6V to 4.5V
- Output current up to 1A
- 1.6MHz (LMR10510X) and 3 MHz (LMR10510Y) switching frequencies
- Low shutdown Iq, 30 nA typical
- Internal soft-start
- Internally compensated
- Current-Mode PWM operation
- Thermal shutdown
- SOT23-5 (2.92 x 2.84 x 1 mm) and LLP-6 (3 x 3 x 0.8 mm) packaging
- Fully enabled for WEBENCH® Power Designer

Performance Benefits

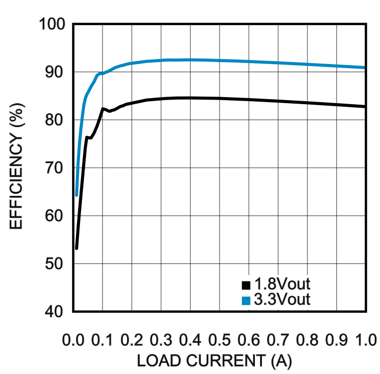
- Extremely easy to use
- Tiny overall solution reduces system cost

Applications

- Point-of-Load Conversions from 3.3V, and 5V Rails
- Space Constrained Applications
- Battery Powered Equipment
- Industrial Distributed Power Applications
- Power Meters
- Portable Hand-Held Instruments

System Performance

Efficiency vs Load Current - "X" V_{IN} = 5V



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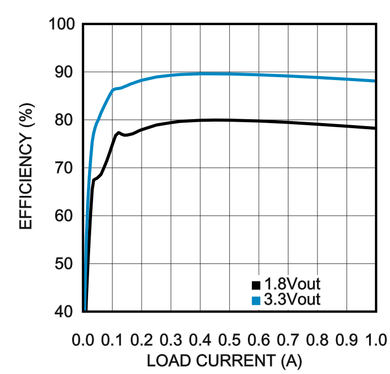
Efficiency vs Load Current - "Y" V_{IN} = 5V



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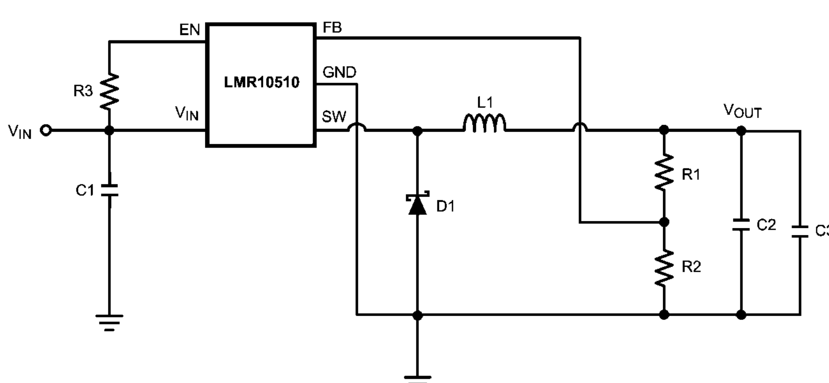
Typical Application



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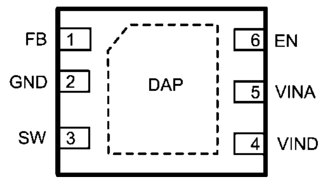
Connection Diagrams



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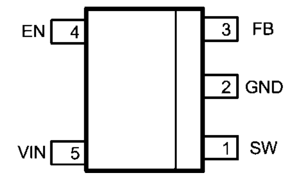
6-Pin LLP



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5-Pin SOT-23

Ordering Information

Order Number	Frequency Option	Package Type	NSC Package Drawing	Top Mark	Supplied As
LMR10510XMFE	1.6MHz	SOT23-5	MF05A	SH7B	250 units Tape and Reel
LMR10510XMF					1000 units Tape and Reel
LMR10510XMFX					3000 units Tape and Reel
LMR10510YMFE	3MHz			SH9B	250 units Tape and Reel
LMR10510YMF					1000 units Tape and Reel
LMR10510YMFX					3000 units Tape and Reel
LMR10510YSDE		LLP-6	SDE06A	L268B	250 units Tape and Reel
LMR10510YSD					1000 units Tape and Reel
LMR10510YSDX					4500 units Tape and Reel

Pin Descriptions 5-Pin SOT23

Pin	Name	Function
1	SW	Switch node. Connect to the inductor and catch diode.
2	GND	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
3	FB	Feedback pin. Connect to external resistor divider to set output voltage.
4	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than VIN + 0.3V.
5	VIN	Input supply voltage.

Pin Descriptions 6-Pin LLP

Pin	Name	Function
1	FB	Feedback pin. Connect to external resistor divider to set output voltage.
2	GND	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
3	SW	Switch node. Connect to the inductor and catch diode.
4	VIND	Power Input supply.
5	VINA	Control circuitry supply voltage. Connect VINA to VIND on PC board.
6	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than VINA + 0.3V.
DAP	Die Attach Pad	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

VIN	-0.5V to 7V
FB Voltage	-0.5V to 3V
EN Voltage	-0.5V to 7V
SW Voltage	-0.5V to 7V
ESD Susceptibility	2kV
Junction Temperature (Note 2)	150°C
Storage Temperature	−65°C to +150°C

For soldering specifications:
see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf

Operating Ratings

VIN	3V to 5.5V
Junction Temperature	−40°C to +125°C

Electrical Characteristics (Note 3), (Note 4)

VIN = 5V unless otherwise indicated under the **Conditions** column. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage		**0.588**	0.600	**0.612**	V
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 5V		0.02		%/V
I_B	Feedback Input Bias Current			0.1	**100**	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.73	**2.90**	V
		V_{IN} Falling	**1.85**	2.3		
	UVLO Hysteresis			0.43		V
F_{SW}	Switching Frequency	LMR10510-X	**1.2**	1.6	**1.95**	MHz
		LMR10510-Y	**2.25**	3.0	**3.75**	
D_{MAX}	Maximum Duty Cycle	LMR10510-X	**86**	94		%
		LMR10510-Y	**82**	90		
D_{MIN}	Minimum Duty Cycle	LMR10510-X		5		%
		LMR10510-Y		7		
$R_{DS(ON)}$	Switch On Resistance	LLP-6 Package		150		mΩ
		SOT23-5 Package		130	**195**	
I_{CL}	Switch Current Limit	V_{IN} = 3.3V	**1.2**	1.75		A
V_{EN_TH}	Shutdown Threshold Voltage				**0.4**	V
	Enable Threshold Voltage		**1.8**			
I_{SW}	Switch Leakage			100		nA
I_{EN}	Enable Pin Current	Sink/Source		100		nA
I_Q	Quiescent Current (switching)	LMR10510X V_{FB} = 0.55		3.3	**5**	mA
		LMR10510Y V_{FB} = 0.55		4.3	**6.5**	mA
	Quiescent Current (shutdown)	All Options V_{EN} = 0V		30		nA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
θ_{JA}	Junction to Ambient 0 LFPM Air Flow (*Note 5*)	LLP-6 Package		80		°C/W
		SOT23-5 Package		118		
θ_{JC}	Junction to Case	LLP-6 Package		18		°C/W
		SOT23-5 Package		80		
T_{SD}	Thermal Shutdown Temperature			165		°C

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not guarantee specfic performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

Note 3: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

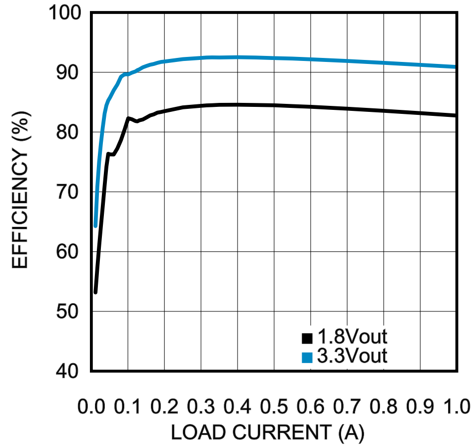
Note 4: Typical numbers are at 25°C and represent the most likely parametric norm.

Note 5: Applies for packages soldered directly onto a 3" x 3" PC board with 2oz. copper on 4 layers in still air.

Typical Performance Characteristics

Unless stated otherwise, all curves taken at VIN = 5.0V with configuration in typical application circuit shown in *Figure 3*. T_J = 25°C, unless otherwise specified.

η vs Load "X" Vin = 5V, Vo = 1.8V & 3.3V



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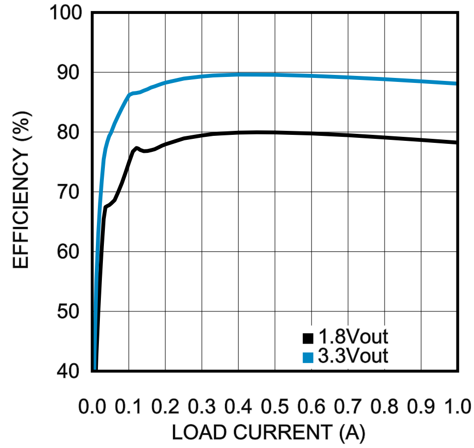
η vs Load "Y" Vin = 5V, Vo = 3.3V & 1.8V



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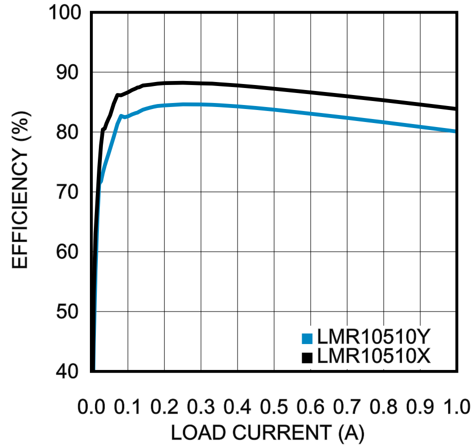
η vs Load "X and Y" Vin = 3.3V, Vo = 1.8V



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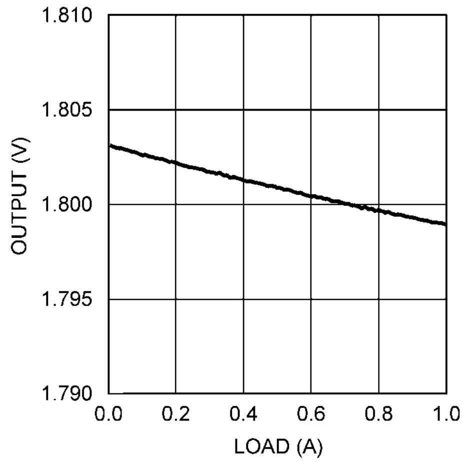
Load Regulation
Vin = 3.3V, Vo = 1.8V (All Options)



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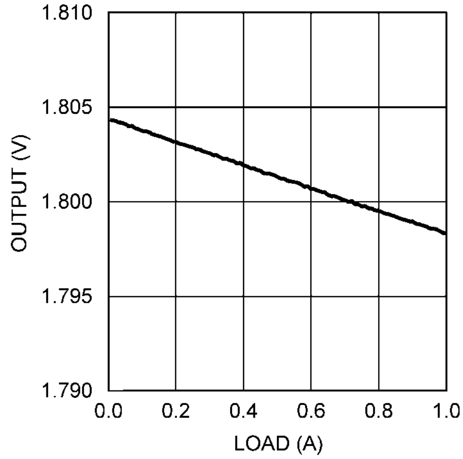
Load Regulation Vin = 5V, Vo = 1.8V (All Options)



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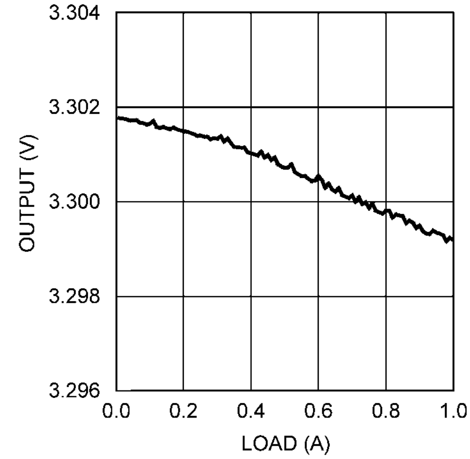
Load Regulation Vin = 5V, Vo = 3.3V (All Options)



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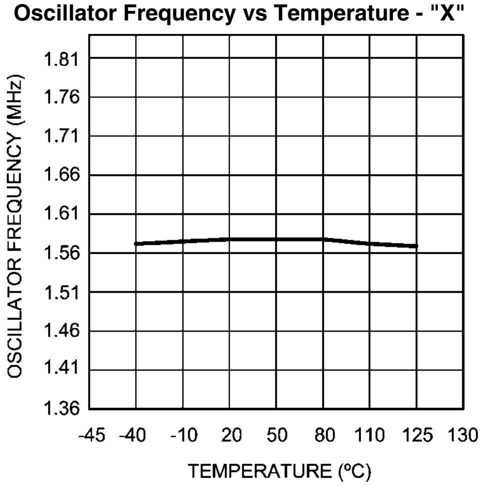
Oscillator Frequency vs Temperature - "X"



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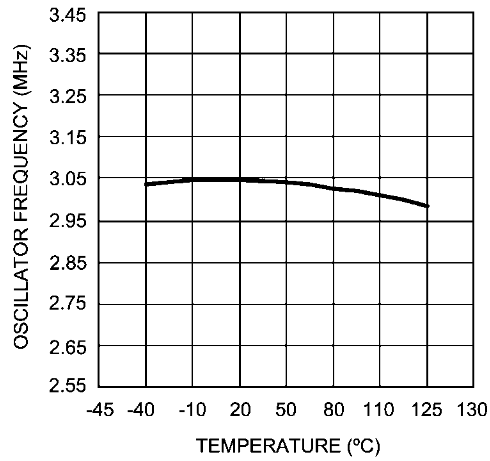
Oscillator Frequency vs Temperature - "Y"



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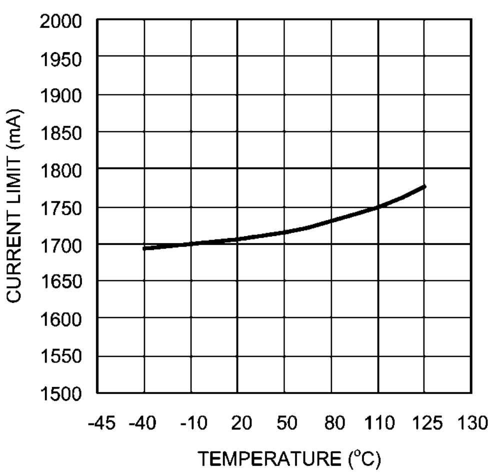
Current Limit vs Temperature Vin = 3.3V



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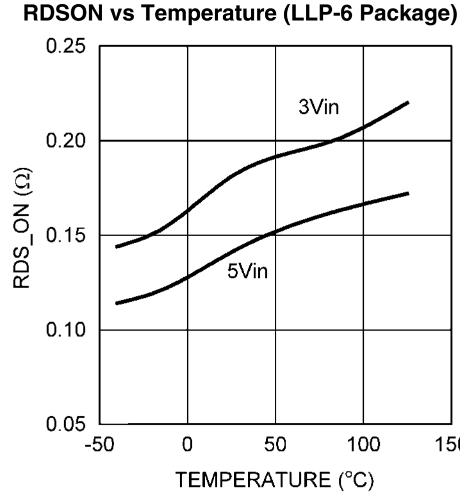
RDSON vs Temperature (LLP-6 Package)



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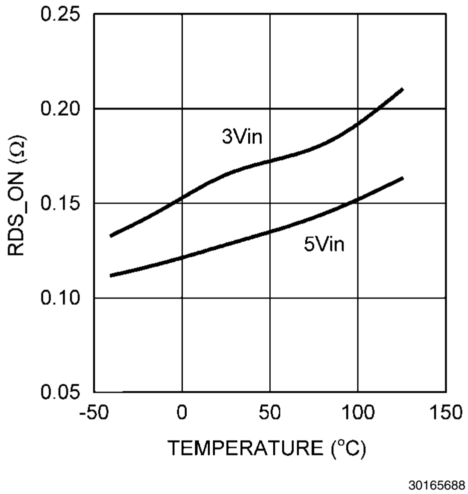
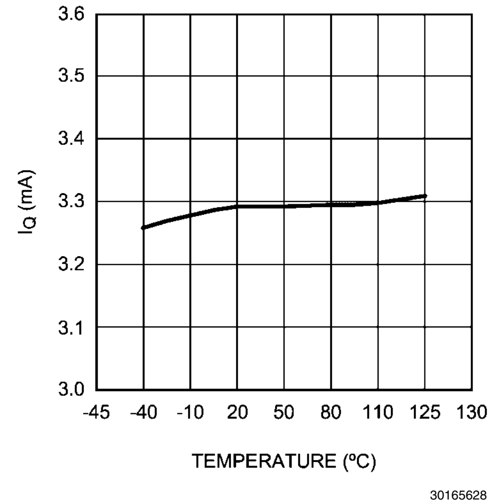
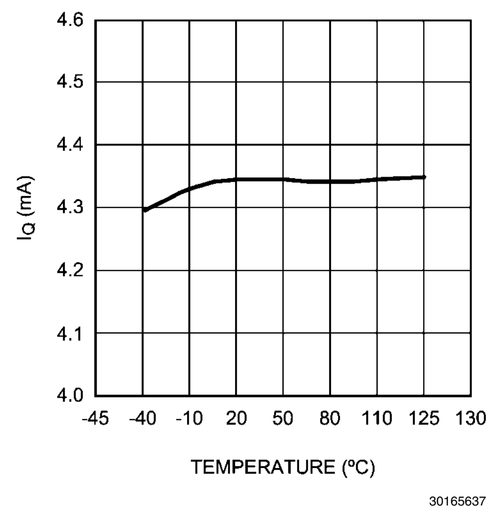
RDSON vs Temperature (SOT23-5 Package)



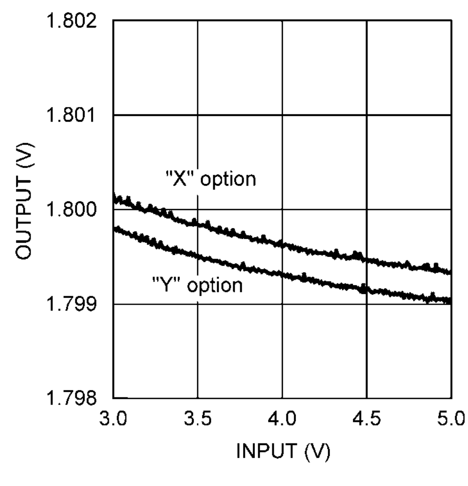
LMR10510X I_Q (Quiescent Current)



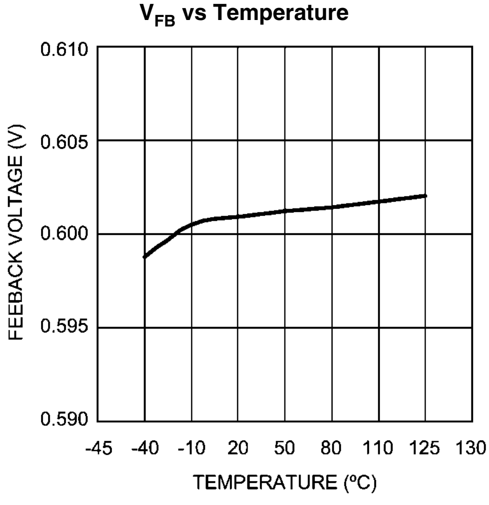
LMR10510Y I_Q (Quiescent Current)



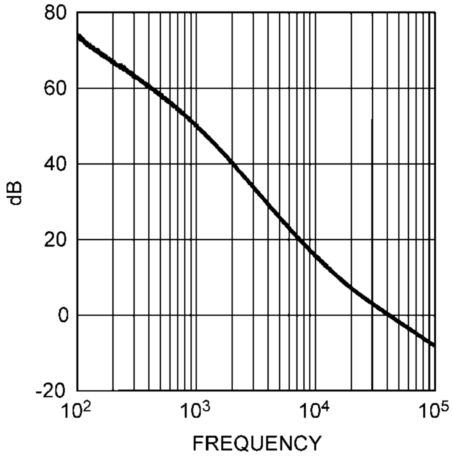
Line Regulation
Vo = 1.8V, Io = 500mA



V_{FB} vs Temperature



Gain vs Frequency
(Vin = 5V, Vo = 1.2V @ 1A)



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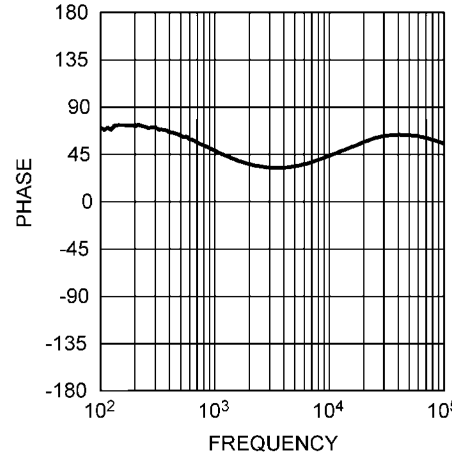
Phase Plot vs Frequency
(Vin = 5V, Vo = 1.2V @ 1A)



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Simplified Block Diagram

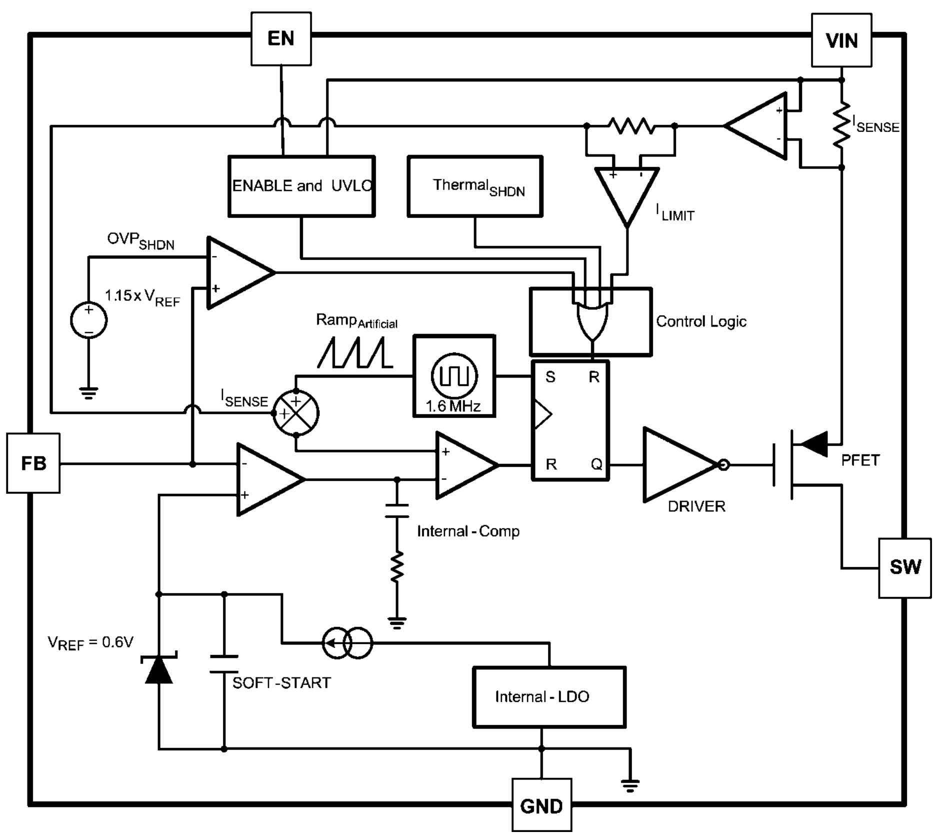

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FIGURE 1.

General Description

The LMR10510 regulator is a monolithic, high frequency, PWM step-down DC/DC converter in a 5 pin SOT23 and a 6 Pin LLP package. It provides all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area. With a minimum of external components, the LMR10510 is easy to use. The ability to drive 1.0A loads with an internal 130 mΩ PMOS switch results in the best power density available. The world-class control circuitry allows on-times as low as 30ns, thus supporting exceptionally high frequency conversion over the entire 3V to 5.5V input operating range down to the minimum output voltage of 0.6V. The LMR10510 is a constant frequency PWM buck regulator IC that delivers a 1.0A load current. The regulator has a preset switching frequency of 1.6MHz or 3.0MHz. This high frequency allows the LMR10510 to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space. The LMR10510 is internally compensated, so it is simple to use and requires few external components. Even though the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low stand-by current of 30 nA. The LMR10510 utilizes current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output over-voltage protection.

Applications Information

THEORY OF OPERATION

The following operating description of the LMR10510 will refer to the Simplified Block Diagram (Figure 1) and to the waveforms in Figure 2. The LMR10510 supplies a regulated output voltage by switching the internal PMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal PMOS control switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through the Schottky catch diode, which forces the SW pin to swing below ground by the forward voltage (V_D) of the Schottky catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

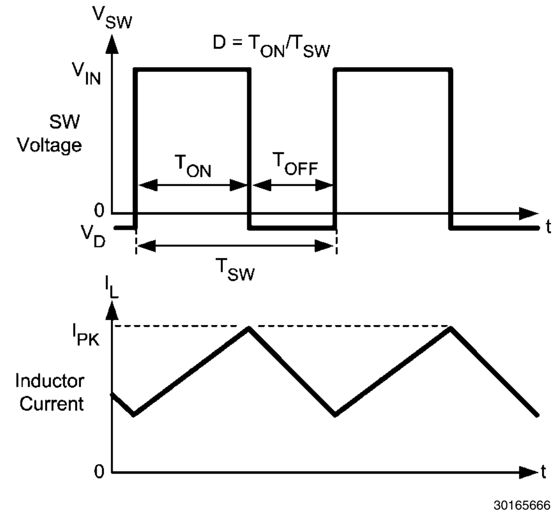


FIGURE 2. Typical Waveforms

SOFT-START

This function forces V_{OUT} to increase at a controlled rate during start up. During soft-start, the error amplifier's reference voltage ramps from 0V to its nominal value of 0.6V in approximately 600 µs. This forces the regulator output to ramp up in a controlled fashion, which helps reduce inrush current.

OUTPUT OVERVOLTAGE PROTECTION

The over-voltage comparator compares the FB pin voltage to a voltage that is 15% higher than the internal reference V_{REF}. Once the FB pin voltage goes 15% above the internal reference, the internal PMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

UNDERVOLTAGE LOCKOUT

Under-voltage lockout (UVLO) prevents the LMR10510 from operating until the input voltage exceeds 2.73V (typ). The UVLO threshold has approximately 430 mV of hysteresis, so the part will operate until V_{IN} drops below 2.3V (typ). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

CURRENT LIMIT

The LMR10510 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 1.75A (typ), and turns off the switch until the next switching cycle begins.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

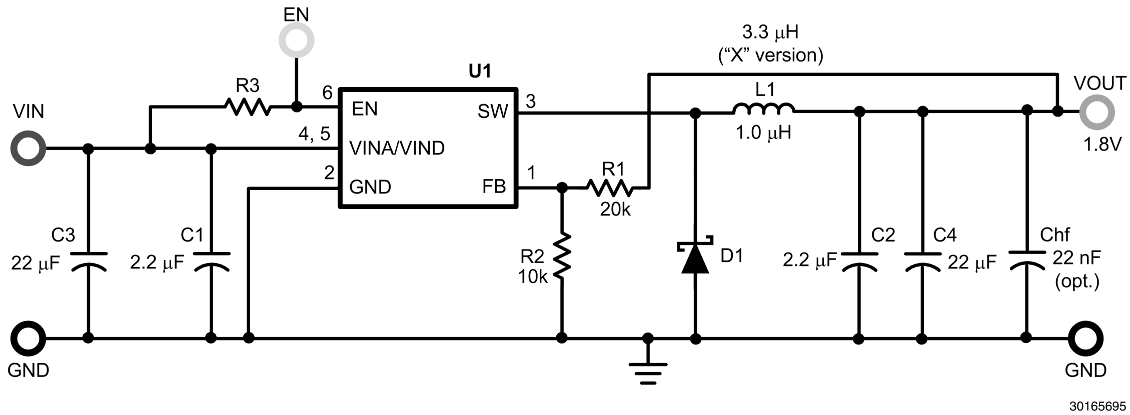


FIGURE 3. Typical Application Schematic

Design Guide

INDUCTOR SELECTION

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal PMOS must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}}$$

V_{SW} can be approximated by:

$$V_{SW} = I_{OUT} \times R_{DSON}$$

The diode forward drop (V_D) can range from 0.3V to 0.7V depending on the quality of the diode. The lower the V_D, the higher the operating efficiency of the converter. The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current.

One must ensure that the minimum current limit (1.2A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L$$

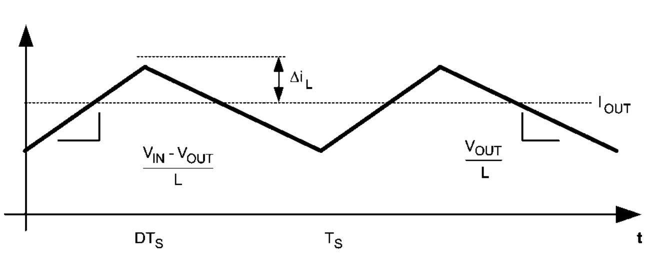


FIGURE 4. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S}$$

In general,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT})$$

If Δi_L = 20% of 1A, the peak current in the inductor will be 1.2A. The minimum guaranteed current limit over all operating conditions is 1.2A. One can either reduce Δi_L, or make the engineering judgment that zero margin will be safe enough. The typical current limit is 1.75A.

The LMR10510 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the output capacitor section for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by:

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times (V_{IN} - V_{OUT})$$

Where

$$T_S = \frac{1}{f_S}$$

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum output current. For example, if the designed maximum output current is 1.0A and the peak current is 1.25A, then the inductor should be specified with a saturation current limit of > 1.25A. There is no need to specify the saturation or peak current of the inductor at the 1.75A typical switch current limit. The difference in inductor size is a factor of 5. Because of the operating frequency of the LMR10510, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (R_{DCR}) will provide better operating efficiency. For recommended inductors see Example Circuits.

INPUT CAPACITOR

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and ESL (Equivalent Series Inductance). The recommended input capacitance is 22 µF.The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS\_IN} \sqrt{D\left[I_{OUT}^{2}\ (1\text{-}D) + \frac{\Delta i^{2}}{3}\right]}$$

Neglecting inductor ripple simplifies the above equation to:

$$I_{RMS\_IN} = I_{OUT} \times \sqrt{D(1 - D)}$$

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LMR10510, leaded capacitors may have an ESL so large that the resulting impedance (2πfL) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended.

Sanyo POSCAP, Tantalum or Niobium, Panasonic SP, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs it is recommended to use X7R or X5R type capacitors due to their tolerance and temperature characteristics. Consult capacitor manufacturer datasheets to see how rated capacitance varies over operating conditions.

OUTPUT CAPACITOR

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_{OUT} = \Delta I_{L}\left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LMR10510, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum of 22 µF of output capacitance. Capacitance often, but not always, can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types.

CATCH DIODE

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_{OUT} \times (1\text{-}D)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

OUTPUT VOLTAGE

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10kΩ. When designing a unity gain converter (Vo = 0.6V), R1 should be between 0Ω and 100Ω, and R2 should be equal or greater than 10kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2$$

$$V_{REF} = 0.60V$$

PCB LAYOUT CONSIDERATIONS

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor and the catch diode D1. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the output capacitor, which should be near the GND connections of CIN and D1. There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R1 placed as close as possible to the GND of the IC. The V_{OUT} trace to R2 should be routed away from the inductor and any other traces that are switching. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-1229 for further considerations and the LMR10510 demo board as an example of a good layout.

Calculating Efficiency, and Junction Temperature

The complete LMR10510 DC/DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter: switching and conduction. Conduction losses usually dominate at higher output loads, whereas switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}}$$

V_{SW} is the voltage drop across the internal PFET when it is on, and is equal to:

$$V_{SW} = I_{OUT} \times R_{DSON}$$

V_D is the forward voltage drop across the Schottky catch diode. It can be obtained from the diode manufactures Electrical Characteristics section. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_D + V_{DCR}}{V_{IN} + V_D + V_{DCR} - V_{SW}}$$

The conduction losses in the free-wheeling Schottky diode are calculated as follows:

$$P_{DIODE} = V_D \times I_{OUT} \times (1\text{-}D)$$

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode that has a low forward voltage drop.

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR}$$

The LMR10510 conduction loss is mainly associated with the internal PFET:

$$P_{COND} = (I_{OUT}^2 \times D)\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON}$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D$$

Switching losses are also associated with the internal PFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE})$$

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL})$$

$$P_{SW} = P_{SWR} + P_{SWF}$$

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN}$$

I_Q is the quiescent operating current, and is typically around 3.3mA for the 1.6MHz frequency option.

Typical Application power losses are:

Power Loss Tabulation

V_{IN}	5.0V		
V_{OUT}	3.3V	P_{OUT}	3.3W
I_{OUT}	1.0A		
V_D	0.45V	P_{DIODE}	150mW
F_{SW}	1.6MHz		
I_Q	3.3mA	P_Q	17mW
T_{RISE}	4nS	P_{SWR}	16mW
T_{FALL}	4nS	P_{SWF}	16mW
$R_{DS(ON)}$	150mΩ	P_{COND}	100mW
IND_{DCR}	70mΩ	P_{IND}	70mW
D	0.667	P_{LOSS}	369mW
η	88%	$P_{INTERNAL}$	149mW

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q = P_{LOSS}$$

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q = P_{INTERNAL}$$

$$P_{INTERNAL} = 149\text{mW}$$

Thermal Definitions

T_J = Chip junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from chip junction to device case

$R_{\theta JA}$ = Thermal resistance from chip junction to ambient air

Heat in the LMR10510 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs. conductor).

Heat Transfer goes as:

Silicon → package → lead frame → PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{Power}$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{Power}$$

The PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB can greatly effect $R_{\theta JA}$. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Four to six thermal vias should be placed under the exposed pad to the ground plane if the LLP package is used.

Thermal impedance also depends on the thermal properties of the application operating conditions (Vin, Vo, Io etc), and the surrounding circuitry.

Silicon Junction Temperature Determination Method 1:

To accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to case temperature.

$R_{\theta JC}$ is approximately 18°C/Watt for the 6-pin LLP package with the exposed pad. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench we have:

$$R_{\theta JC} = \frac{T_J - T_C}{Power}$$

where T_C is the temperature of the exposed pad and can be measured on the bottom side of the PCB.

Therefore:

$$T_j = (R_{\theta JC} \times P_{LOSS}) + T_C$$

From the previous example:

$$T_j = (R_{\theta JC} \times P_{INTERNAL}) + T_C$$

$$T_j = 18°C/W \times 0.149W + T_C$$

The second method can give a very accurate silicon junction temperature.

The first step is to determine $R_{\theta JA}$ of the application. The LMR10510 has over-temperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of about 15°C. Once the silicon temperature has decreased to approximately 150°C, the device will start to switch again. Knowing this, the $R_{\theta JA}$ for any application can be characterized during the early stages of the design one may calculate the $R_{\theta JA}$ by placing the PCB circuit into a thermal chamber. Raise the ambient temperature in the given working application until the circuit enters thermal shutdown. If the SW-pin is monitored, it will be obvious when the internal PFET stops switching, indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature, and the ambient temperature $R_{\theta JA}$ can be determined.

$$R_{\theta JA} = \frac{165° - Ta}{P_{INTERNAL}}$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

An example of calculating $R_{\theta JA}$ for an application using the LMR10510 is shown below.

A sample PCB is placed in an oven with no forced airflow. The ambient temperature was raised to 147°C, and at that temperature, the device went into thermal shutdown.

From the previous example:

$$P_{INTERNAL} = 149 \text{ mW}$$

$$R_{\theta JA} = \frac{165°C - 147°C}{149 \text{ mW}} = 121°C/W$$

Since the junction temperature must be kept below 125°C, then the maximum ambient temperature can be calculated as:

$$T_j - (R_{\theta JA} \times P_{LOSS}) = T_A$$

$$125°C - (121°C/W \times 149 \text{ mW}) = 107°C$$

LLP Package

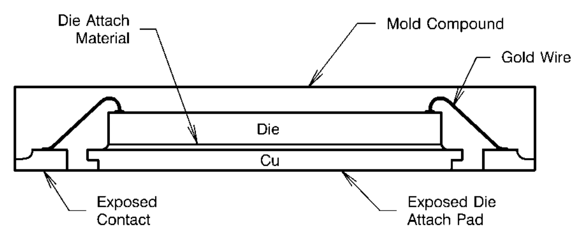


FIGURE 5. Internal LLP Connection

For certain high power applications, the PCB land may be modified to a "dog bone" shape (see Figure 6). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

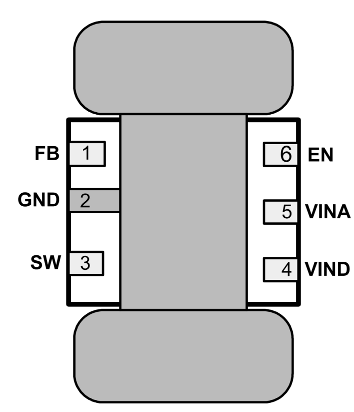


FIGURE 6. 6-Lead LLP PCB Dog Bone Layout

LMR10510X Design Example 1

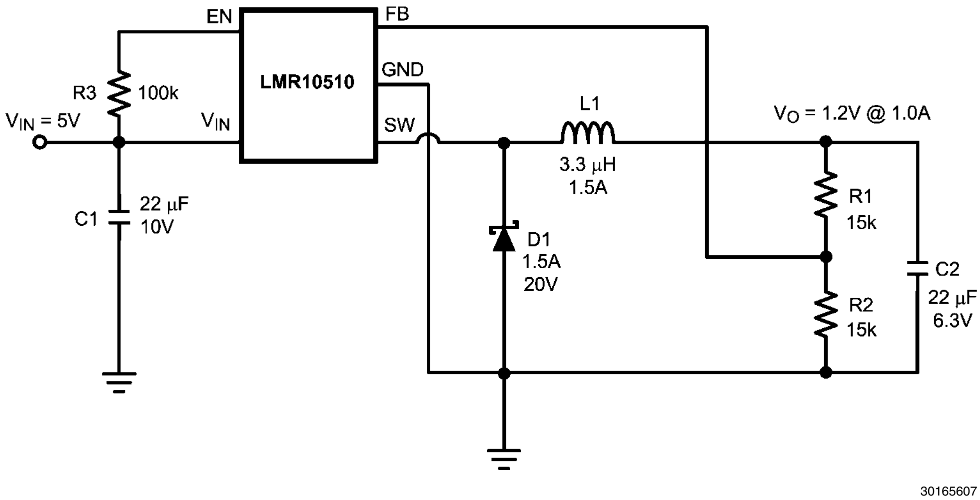


FIGURE 7. LMR10510X (1.6MHz): Vin = 5V, Vo = 1.2V @ 1.0A

LMR10510X Design Example 2

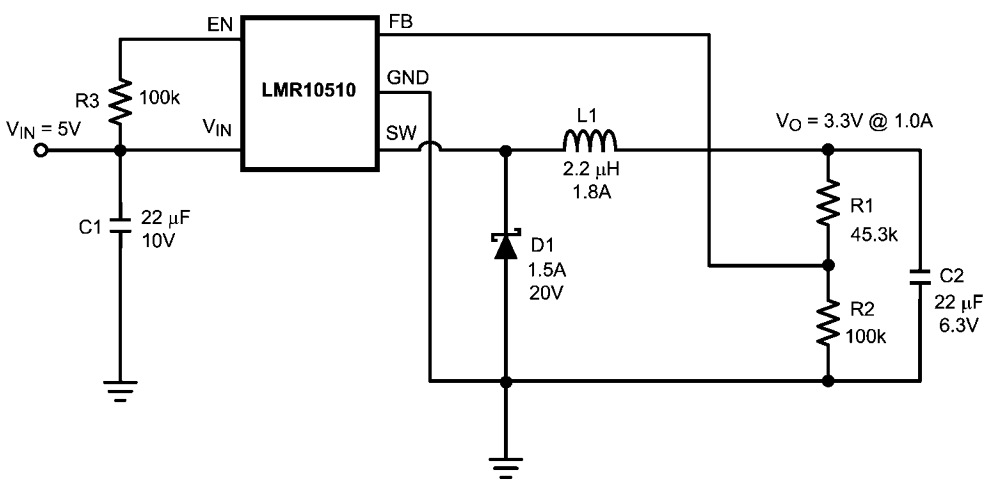


FIGURE 8. LMR10510X (1.6MHz): Vin = 5V, Vo = 3.3V @ 1.0A

LMR10510Y Design Example 3

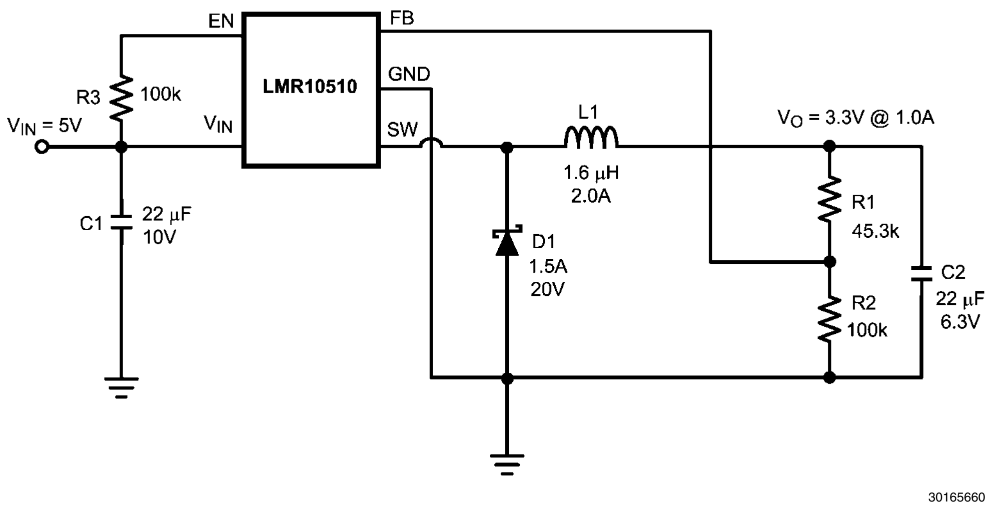


FIGURE 9. LMR10510Y (3MHz): Vin = 5V, Vo = 3.3V @ 1.0A

LMR10510Y Design Example 4

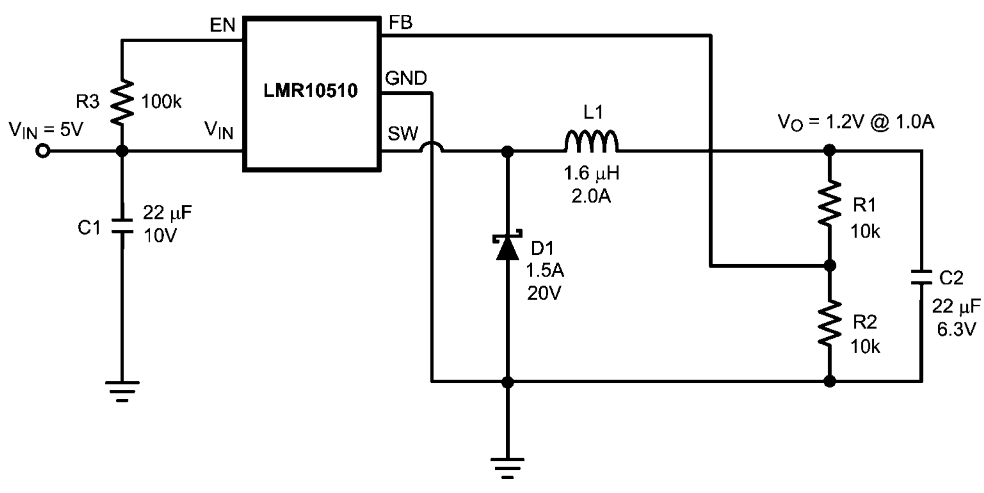
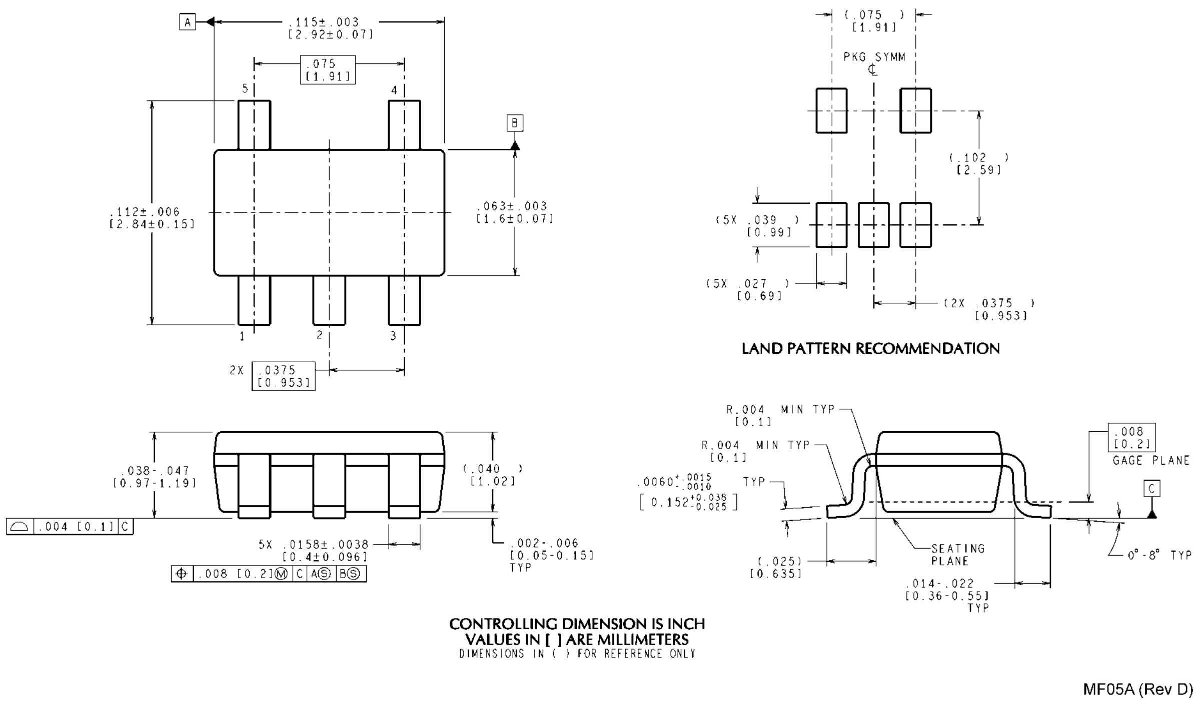
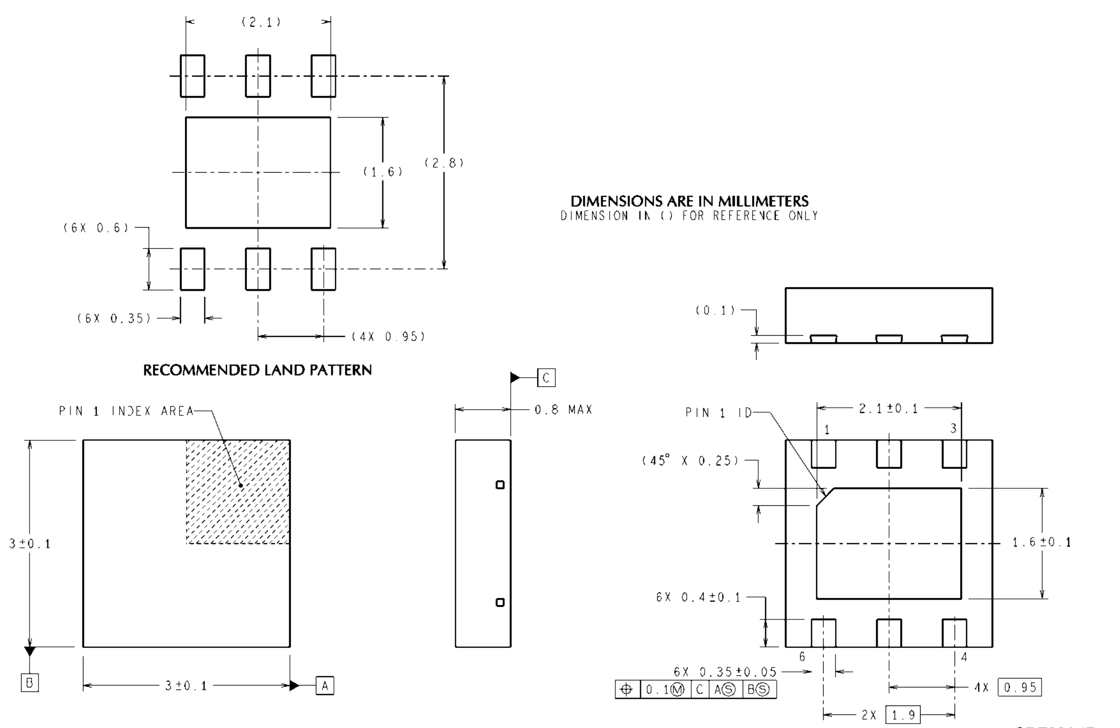


FIGURE 10. LMR10510Y (3MHz): Vin = 5V, Vo = 1.2V @ 1.0A

Physical Dimensions inches (millimeters) unless otherwise noted



5-Lead SOT-23 Package
NS Package Number MF05A



6-Lead LLP Package
NS Package Number SDE06A

Notes

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