March 12, 2012

LMK00304

3-GHz 4-Output Differential Clock Buffer/Level Translator

1.0 General Description

The LMK00304 is a 3-GHz 4-output differential fanout buffer intended for high-frequency, low-jitter clock/data distribution and level translation. The input clock can be selected from two universal inputs or one crystal input. The selected input clock is distributed to two banks of 2 differential outputs and one LVCMOS output. The differential output banks can be mutually configured as LVPECL, LVDS, or HCSL drivers, or disabled. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The LMK00304 operates from a 3.3 V core supply and 3 independent 3.3 V/2.5 V output supplies.

The LMK00304 provides high performance, versatility, and power efficiency, making it ideal for replacing fixed-output buffer devices while increasing timing margin in the system.

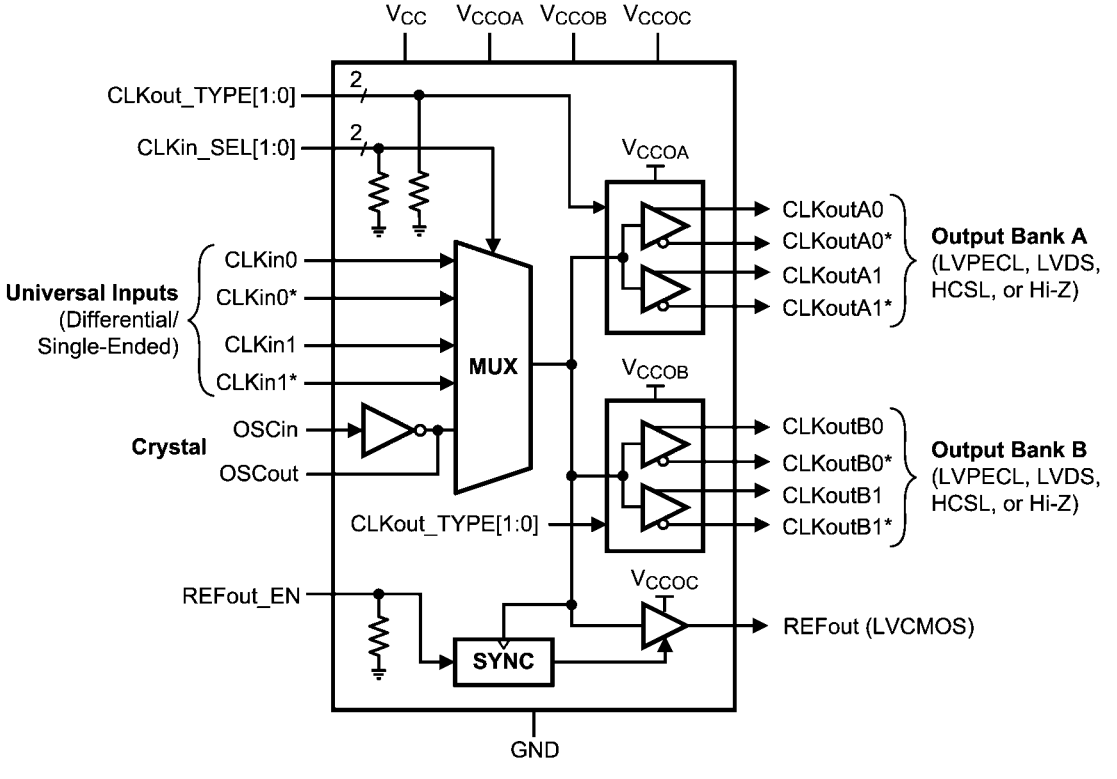
2.0 Target Applications

- Clock Distribution and Level Translation for high-speed ADCs, DACs, Serial Interfaces (Multi-Gigabit Ethernet, XAUI, Fibre Channel, PCIe, SATA/SAS, SONET/SDH, CPRI), and high-frequency backplanes
- Remote Radio Units (RRU) and Baseband Units (BBU)
- Switches and Routers
- Servers, Workstations, and Computing

3.0 Features

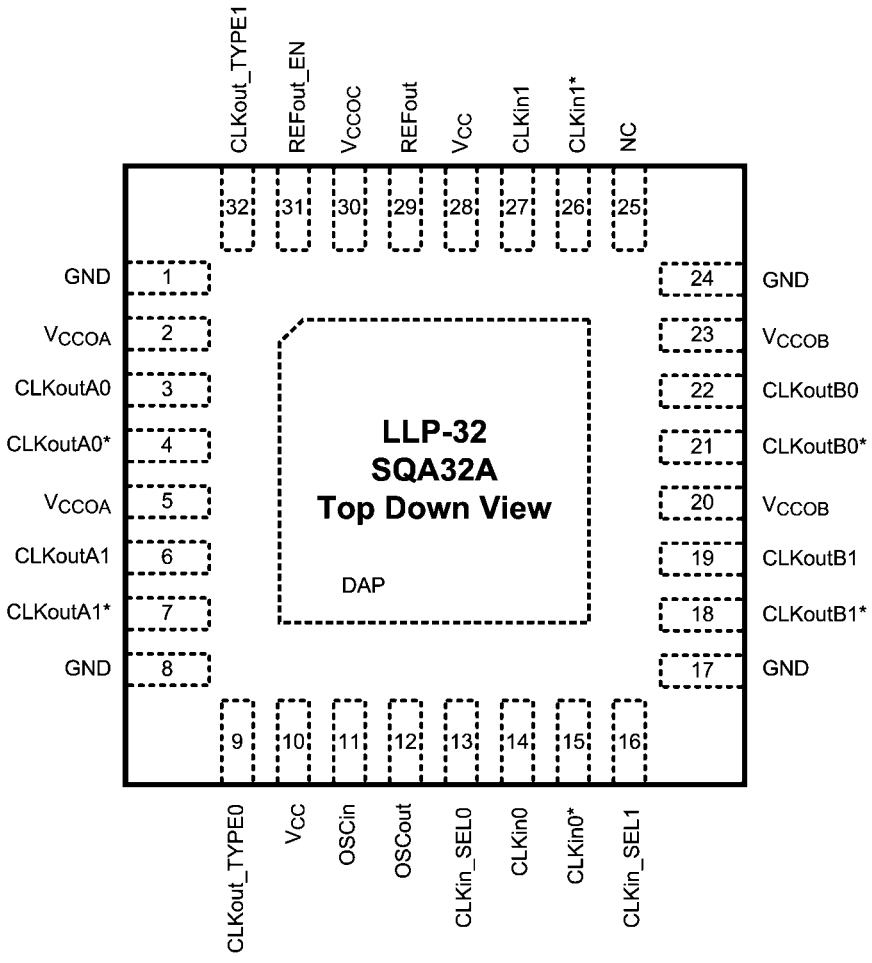
- 3:1 Input Multiplexer
  - Two universal inputs operate up to 3.1 GHz and accept LVPECL, LVDS, CML, SSTL, HSTL, HCSL (AC-coupled), or single-ended clocks
  - One crystal input accepts a 10 to 40 MHz crystal or single-ended clock
- Two Banks with 2 Differential Outputs each
  - LVPECL, LVDS, HCSL, or Hi-Z (selectable)
  - LVPECL Additive Jitter with LMK03806 clock source:
    - 20 fs RMS at 156.25 MHz (10 kHz – 1 MHz)
    - 51 fs RMS at 156.25 MHz (12 kHz – 20 MHz)
- High PSRR: -65 / -76 dBc (LVPECL/LVDS) at 156.25 MHz
- LVCMOS output with synchronous enable input
- Pin-controlled configuration
- V_{CC} Core Supply: 3.3 V ± 5%
- 3 Independent V_{CCO} Output Supplies: 3.3 V/2.5 V ± 5%
- Industrial temperature range: -40°C to +85°C
- Package: 32-pin LLP (5.0 x 5.0 x 0.8 mm)

4.0 Functional Block Diagram



5.0 Connection Diagram

32-Pin LLP Package



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6.0 Pin Descriptions

Pin #	Pin Name(s)	Type	Description
DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
1, 8 17, 24	GND	GND	Ground
2, 5	V_{CCOA}	PWR	Power supply for Bank A Output buffers. V_{CCOA} operates from 3.3 V or 2.5 V. The V_{CCOA} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. (*Note 1*)
3, 4	CLKoutA0, CLKoutA0*	O	Differential clock output A0. Output type set by CLKout_TYPE pins.
6, 7	CLKoutA1, CLKoutA1*	O	Differential clock output A1. Output type set by CLKout_TYPE pins.
9, 32	CLKout_TYPE0, CLKout_TYPE1	I	Bank A and Bank B output buffer type selection pins (*Note 2*)
10, 28	Vcc	PWR	Power supply for Core and Input Buffer blocks. The Vcc supply operates from 3.3 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcc pin.
11	OSCin	I	Input for crystal. Can also be driven by a XO, TCXO, or other external single-ended clock.
12	OSCout	O	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
13, 16	CLKin_SEL0, CLKin_SEL1	I	Clock input selection pins (*Note 2*)
14, 15	CLKin0, CLKin0*	I	Universal clock input 0 (differential/single-ended)
18, 19	CLKoutB1*, CLKoutB1	O	Differential clock output B1. Output type set by CLKout_TYPE pins.
20, 23	V_{CCOB}	PWR	Power supply for Bank B Output buffers. V_{CCOB} operates from 3.3 V or 2.5 V. The V_{CCOB} pins are internally tied together. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. (*Note 1*)
21, 22	CLKoutB0*, CLKoutB0	O	Differential clock output B0. Output type set by CLKout_TYPE pins.
25	NC	—	Not connected internally. Pin may be floated, grounded, or otherwise tied to any potential within the Supply Voltage range stated in the *Section 8.0 Absolute Maximum Ratings*.
26, 27	CLKin1*, CLKin1	I	Universal clock input 1 (differential/single-ended)
29	REFout	O	LVCMOS reference output. Enable output by pulling REFout_EN pin high.
30	V_{CCOC}	PWR	Power supply for REFout buffer. V_{CCOC} operates from 3.3 V or 2.5 V. Bypass with a 0.1 uF low-ESR capacitor placed very close to each Vcco pin. (*Note 1*)
31	REFout_EN	I	REFout enable input. Enable signal is internally synchronized to selected clock input. (*Note 2*)

Note 1: The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

Note 2: CMOS control input with internal pull-down resistor.

Note 3: Any unused output pins should be left floating with minimum copper length (*Note 5*), or properly terminated if connected to a transmission line, or disabled/Hi-Z if possible. See *Section 7.3 Clock Outputs* for output configuration and *Section 14.3 Termination and Use of Clock Drivers* for output interface and termination techniques.

7.0 Functional Description

The LMK00304 is a 4-output differential clock fanout buffer with low additive jitter that can operate up to 3.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 2 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 32-pin LLP package and leverages much of the high-speed, low-noise circuit design employed in the LMK04800 family of clock conditioners.

7.1 V_{CC} and V_{CCO} Power Supplies

The LMK00304 has separate 3.3 V core supply (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}). Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to its respective Vcco supply, while the output levels for LVDS and HCSL are relatively constant over the specified Vcco range. Refer to *Section 14.4 Power Supply and Thermal Considerations* for additional supply related considerations, such as power dissipation, power supply bypassing, and power supply ripple rejection (PSRR).

Note 4: Care should be taken to ensure the Vcco voltages do not exceed the Vcc voltage to prevent turning-on the internal ESD protection circuitry.

7.2 Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in *Table 1*. Refer to *Section 14.1 Driving the Clock Inputs* for clock input requirements. When CLKin0 or CLKin1 is selected, the crystal circuit is powered down. When OSCin is selected, the crystal oscillator circuit will start-up and its clock will be distributed to all outputs. Refer to *Section 14.2 Crystal Interface* for more information. Alternatively, OSCin may be driven by a single-ended clock (up to 250 MHz) instead of a crystal.

TABLE 1. Input Selection

CLKin_SEL1	CLKin_SEL0	Selected Input
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	X	OSCin

Table 2 shows the output logic state vs. input state when either CLKin0/CLKin0* or CLKin1/CLKin1* is selected. When OSCin is selected, the output state will be an inverted copy of the OSCin input state.

TABLE 2. CLKin Input vs. Output States

State of Selected CLKin	State of Enabled Outputs
CLKinX and CLKinX* inputs floating	Logic low
CLKinX and CLKinX* inputs shorted together	Logic low
CLKin logic low	Logic low
CLKin logic high	Logic high

7.3 Clock Outputs

The differential output buffer type for both Bank A and B outputs are configured using the CLKout_TYPE[1:0] as shown in *Table 3*. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length ((*Note 5*)) to minimize capacitance and potential coupling and reduce power consumption. If all differential outputs are not used, it is recommended to disable (Hi-Z) the banks to reduce power. Refer to *Section 14.3 Termination and Use of Clock Drivers* for more information on output interface and termination techniques.

Note 5: For best soldering practices, the minimum trace length for any unused pin should extend to include the pin solder mask. This way during reflow, the solder has the same copper area as connected pins. This allows for good, uniform fillet solder joints helping to keep the IC level during reflow.

TABLE 3. Differential Output Buffer Type Selection

CLKout_ TYPE1	CLKout_ TYPE0	CLKoutX Buffer Type (Bank A and B)
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Disabled (Hi-Z)

7.3.1 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the Vcco voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN, as shown in *Table 4*.

TABLE 4. Reference Output Enable

REFout_EN	REFout State
0	Disabled (Hi-Z)
1	Enabled

The REFout_EN input is internally synchronized with the selected input clock by the SYNC block. This synchronizing function prevents glitches and runt pulses from occurring on the REFout clock when enabled or disabled. REFout will be enabled within 3 cycles (t_{EN}) of the input clock after REFout_EN is toggled high. REFout will be disabled within 3 cycles (t_{DIS}) of the input clock after REFout_EN is toggled low.

When REFout is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout is configured with a 1 kΩ load to ground, then the output will be pulled to low when disabled.

8.0 Absolute Maximum Ratings (Note 6, Note 7)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Supply Voltages	V_{CC}, V_{CCO}	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to (V_{CC} + 0.3)	V
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (solder 4 s)	T_L	+260	°C
Junction Temperature	T_J	+150	°C

9.0 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature Range	T_A	-40	25	85	°C
Junction Temperature	T_J			125	°C
Core Supply Voltage Range	V_{CC}	3.15	3.3	3.45	V
Output Supply Voltage Range (Note 8, Note 9)	V_{CCO}	3.3 – 5% 2.5 – 5%	3.3 2.5	3.3 + 5% 2.5 + 5%	V

Note 6: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see *Section 11.0 Electrical Characteristics*. The guaranteed specifications apply only to the test conditions listed.

Note 7: This device is a high-performance integrated circuit with an ESD rating up to 2 kV Human Body Model, up to 150 V Machine Model, and up to 750 V Charged Device Model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

Note 8: The output supply voltages or pins (V_{CCOA}, V_{CCOB}, and V_{CCOC}) will be called V_{CCO} in general when no distinction is needed, or when the output supply can be inferred from the output bank/type.

Note 9: Vcco for any output bank should be less than or equal to Vcc (Vcco ≤ Vcc).

10.0 Package Thermal Resistance

Package	θ_{JA}	$\theta_{JC\ (DAP)}$
32-Lead LLP (Note 10)	38.1 °C/W	7.2 °C/W

Note 10: Specification assumes 5 thermal vias connect the die attach pad (DAP) to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the LLP. It is recommended that the maximum number of vias be used in the board layout.

11.0 Electrical Characteristics

Unless otherwise specified: Vcc = 3.3 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed. (Note 8, Note 11)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Consumption						
I_{CC_CORE}	Core Supply Current, All Outputs Disabled	CLKinX selected		8.5	10.5	mA
		OSCin selected		10	13.5	mA
I_{CC_PECL}	Additive Core Supply Current, LVPECL Banks Enabled			38	48	mA
I_{CC_LVDS}	Additive Core Supply Current, LVDS Banks Enabled			43	52	mA
I_{CC_HCSL}	Additive Core Supply Current, HCSL Banks Enabled			50	58.5	mA
I_{CC_CMOS}	Additive Core Supply Current, LVCMOS Output Enabled			3.5	5.5	mA
I_{CCO_PECL}	Additive Output Supply Current, LVPECL Banks Enabled	Includes Output Bank Bias and Load Currents for both banks, R_T = 50 Ω to Vcco - 2V on all outputs		135	163	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCO_LVDS}	Additive Output Supply Current, LVDS Banks Enabled				25	34.5	mA
I_{CCO_HCSL}	Additive Output Supply Current, HCSL Banks Enabled	Includes Output Bank Bias and Load Currents for both banks, R_T = 50 Ω on all outputs			65	81.5	mA
I_{CCO_CMOS}	Additive Output Supply Current, LVCMOS Output Enabled	200 MHz, C_L = 5 pF	Vcco = 3.3 V ± 5%		9	10	mA
			Vcco = 2.5 V ± 5%		7	8	mA
Power Supply Ripple Rejection (PSRR)							
$PSRR_{PECL}$	Ripple-Induced Phase Spur Level (*Note 13*) Differential LVPECL Output	100 kHz, 100 mVpp Ripple Injected on Vcco, Vcco = 2.5 V	156.25 MHz		-65		dBc
			312.5 MHz		-63		
$PSRR_{LVDS}$	Ripple-Induced Phase Spur Level (*Note 13*) Differential LVDS Output		156.25 MHz		-76		dBc
			312.5 MHz		-74		
$PSRR_{HCSL}$	Ripple-Induced Phase Spur Level (*Note 13*) Differential HCSL Output		156.25 MHz		-72		dBc
			312.5 MHz		-63		
CMOS Control Inputs (CLKin_SELn, CLKout_TYPEn, REFout_EN)							
V_{IH}	High-Level Input Voltage			1.6		Vcc	V
V_{IL}	Low-Level Input Voltage			GND		0.4	V
I_{IH}	High-Level Input Current	V_{IH} = Vcc, Internal pull-down resistor				50	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V, Internal pull-down resistor		-5	0.1		µA
Clock Inputs (CLKin0/CLKin0*, CLKin1/CLKin1*)							
f_{CLKin}	Input Frequency Range (*Note 20*)	Functional up to 3.1 GHz Output frequency range and timing specified per output type (refer to LVPECL, LVDS, HCSL, LVCMOS output specifications)		DC		3.1	GHz
V_{IHD}	Differential Input High Voltage	CLKin driven differentially				Vcc	V
V_{ILD}	Differential Input Low Voltage			GND			V
V_{ID}	Differential Input Voltage Swing (*Note 14*)			0.15		1.3	V
V_{CMD}	Differential Input Common Mode Voltage	V_{ID} = 150 mV		0.5		Vcc - 1.2	V
		V_{ID} = 350 mV		0.5		Vcc - 1.1	
		V_{ID} = 800 mV		0.5		Vcc - 0.9	
V_{IH}	Single-Ended Input High Voltage	CLKinX driven single-ended, CLKinX* AC coupled to GND		V_{CM} + 0.15		Vcc	V
V_{IL}	Single-Ended Input Low Voltage			GND		V_{CM} -0.15	V
V_{CM}	Single-Ended Input Common Mode Voltage			0.5		Vcc - 1.2	V
ISO_{MUX}	Mux Isolation, CLKin0 to CLKin1	f_{OFFSET} > 50 kHz, P_{CLKinX} = 0 dBm	f_{CLKin0} = 100 MHz		-84		dBc
			f_{CLKin0} = 200 MHz		-82		
			f_{CLKin0} = 500 MHz		-71		
			f_{CLKin0} = 1000 MHz		-65		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Crystal Interface (OSCin, OSCout)							
F_{CLK}	External Clock Frequency Range (*Note 20*)	OSCin driven single-ended, OSCout floating				250	MHz
F_{XTAL}	Crystal Frequency Range	Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) (*Note 15*)		10		40	MHz
C_{IN}	OSCin Input Capacitance				1		pF
LVPECL Outputs (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing (*Note 20*, *Note 21*)	V_{OD} ≥ 600 mV, R_L = 100 Ω differential	Vcco = 3.3 V ± 5%, R_T = 160 Ω to GND	1.0	1.2		GHz
			Vcco = 2.5 V ± 5%, R_T = 91 Ω to GND	0.75	1.0		
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing (*Note 20*, *Note 21*)	V_{OD} ≥ 400 mV, R_L = 100 Ω differential	Vcco = 3.3 V ± 5%, R_T = 160 Ω to GND	1.5	3.1		GHz
			Vcco = 2.5 V ± 5%, R_T = 91 Ω to GND	1.5	2.3		
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (*Note 16*)	Vcco = 3.3 V, R_T = 160 Ω to GND, R_L = 100 Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		59		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		64		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		30		
$Jitter_{ADD}$	Additive RMS Jitter with LVPECL clock source from LMK03806 (*Note 16*, *Note 17*)	Vcco = 3.3 V, R_T = 160 Ω to GND, R_L = 100 Ω differential	CLKin: 156.25 MHz, J_{SOURCE} = 190 fs RMS (10 kHz to 1 MHz)		20		fs
			CLKin: 156.25 MHz, J_{SOURCE} = 195 fs RMS (12 kHz to 20 MHz)		51		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	Vcco = 3.3 V, R_T = 160 Ω to GND, R_L = 100 Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		-162.5		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		-158.1		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		-154.4		
DUTY	Duty Cycle (*Note 20*)	50% input clock duty cycle		45		55	%
V_{OH}	Output High Voltage	T_A = 25 °C, DC Measurement, R_T = 50 Ω to Vcco - 2 V		Vcco - 1.2	Vcco - 0.9	Vcco - 0.7	V
V_{OL}	Output Low Voltage			Vcco - 2.0	Vcco - 1.75	Vcco - 1.5	V
V_{OD}	Output Voltage Swing (*Note 14*)			600	830	1000	mV
t_R	Output Rise Time 20% to 80%	R_T = 160 Ω to GND, R_L = 100 Ω differential			175		ps
t_F	Output Fall Time 80% to 20%				175		ps

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS Outputs (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout_FS}	Maximum Output Frequency Full V_{OD} Swing (*Note 20*, *Note 21*)	V_{OD} ≥ 250 mV, R_L = 100 Ω differential		1.0	1.6		GHz
f_{CLKout_RS}	Maximum Output Frequency Reduced V_{OD} Swing (*Note 20*, *Note 21*)	V_{OD} ≥ 200 mV, R_L = 100 Ω differential		1.5	2.1		GHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (*Note 16*)	Vcco = 3.3 V, R_L = 100 Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		89		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		77		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		37		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	Vcco = 3.3 V, R_L = 100 Ω differential	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		-159.5		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		-157.0		
			CLKin: 625 MHz, Slew rate ≥ 3 V/ns		-152.7		
DUTY	Duty Cycle (*Note 20*)	50% input clock duty cycle		45		55	%
V_{OD}	Output Voltage Swing (*Note 14*)	T_A = 25 °C, DC Measurement, R_L = 100 Ω differential		250	400	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States			-50		50	mV
V_{OS}	Output Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States			-35		35	mV
I_{SA} I_{SB}	Output Short Circuit Current Single Ended	T_A = 25 °C, Single ended outputs shorted to GND		-24		24	mA
I_{SAB}	Output Short Circuit Current Differential	Complementary outputs tied together		-12		12	mA
t_R	Output Rise Time 20% to 80%	R_L = 100 Ω differential			175		ps
t_F	Output Fall Time 80% to 20%				175		ps

Symbol	Parameter	Conditions		Min	Typ	Max	Units
HCSL Outputs (CLKoutAn/CLKoutAn*, CLKoutBn/CLKoutBn*)							
f_{CLKout}	Output Frequency Range (*Note 20*)	R_L = 50 Ω to GND, C_L ≤ 5 pF		DC		400	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (*Note 16*)	Vcco = 3.3 V, R_T = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		77		fs
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		86		
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	Vcco = 3.3 V, R_T = 50 Ω to GND	CLKin: 100 MHz, Slew rate ≥ 3 V/ns		-161.3		dBc/Hz
			CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns		-156.3		
DUTY	Duty Cycle (*Note 20*)	50% input clock duty cycle		45		55	%
V_{OH}	Output High Voltage	T_A = 25 °C, DC Measurement, R_T = 50 Ω to GND		520	810	920	mV
V_{OL}	Output Low Voltage			-150	0.5	150	mV
V_{CROSS}	Absolute Crossing Voltage (*Note 20*, *Note 22*)	R_L = 50 Ω to GND, C_L ≤ 5 pF		160	350	460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} (*Note 20*, *Note 22*)					140	mV
t_R	Output Rise Time 20% to 80% (*Note 22*)	250 MHz, R_L = 50 Ω to GND, C_L ≤ 5 pF			300		ps
t_F	Output Fall Time 80% to 20% (*Note 22*)				300		ps
LVCMOS Output (REFout)							
f_{CLKout}	Output Frequency Range (*Note 20*)	C_L ≤ 5 pF		DC		250	MHz
$Jitter_{ADD}$	Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz (*Note 16*)	Vcco = 3.3 V, C_L ≤ 5 pF	100 MHz, Input Slew rate ≥ 3 V/ns		95		fs
Noise Floor	Noise Floor f_{OFFSET} ≥ 10 MHz	Vcco = 3.3 V, C_L ≤ 5 pF	100 MHz, Input Slew rate ≥ 3 V/ns		-159.3		dBc/Hz
DUTY	Duty Cycle (*Note 20*)	50% input clock duty cycle		45		55	%
V_{OH}	Output High Voltage	1 mA load		Vcco - 0.1			V
V_{OL}	Output Low Voltage					0.1	V
I_{OH}	Output High Current (Source)	Vo = Vcco / 2	Vcco = 3.3 V		28		mA
			Vcco = 2.5 V		20		
I_{OL}	Output Low Current (Sink)		Vcco = 3.3 V		28		mA
			Vcco = 2.5 V		20		
t_R	Output Rise Time 20% to 80% (*Note 22*)	250 MHz, R_L = 50 Ω to GND, C_L ≤ 5 pF			225		ps
t_F	Output Fall Time 80% to 20% (*Note 22*)				225		ps
t_{EN}	Output Enable Time (*Note 23*)	C_L ≤ 5 pF				3	cycles
t_{DIS}	Output Disable Time (*Note 23*)					3	cycles

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Propagation Delay and Output Skew							
t_{PD_PECL}	Propagation Delay CLKin-to-LVPECL	R_T = 160 Ω to GND, R_L = 100 Ω differential			360		ps
t_{PD_LVDS}	Propagation Delay CLKin-to-LVDS	R_L = 100 Ω differential			400		ps
t_{PD_HCSL}	Propagation Delay CLKin-to-HCSL (*Note 22*)	R_T = 50 Ω to GND, $C_L \leq$ 5 pF			590		ps
t_{PD_CMOS}	Propagation Delay CLKin-to-LVCMOS (*Note 22*)	$C_L \leq$ 5 pF	Vcco = 3.3 V		1475		ps ps
			Vcco = 2.5 V		1550		
$t_{SK(O)}$	Output Skew LVPECL/LVDS/HCSL (*Note 20*, *Note 22*, *Note 24*)	Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications.			30	50	ps
$t_{SK(PP)}$	Part-to-Part Output Skew LVPECL/LVDS/HCSL (*Note 22*, *Note 24*)				80		ps

Note 11: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 12: See *Section 14.4 Power Supply and Thermal Considerations* for more information on current consumption and power dissipation calculations.

Note 13: Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [(2 * $10^{(PSRR / 20)}$) / (π * f^{CLK})] * 1E12

Note 14: See *Section 12.1 Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.

Note 15: The ESR requirements stated must be met to ensure that the oscillator circuitry has no startup issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal. Refer to *Section 14.2 Crystal Interface* for crystal drive level considerations.

Note 16: For the 100 MHz and 156.25 MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method #1: J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2), where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKin. For the 625 MHz clock input condition, Additive RMS Jitter is approximated using Method #2: J_{ADD} = SQRT(2*$10^{dBc/10}$) / (2*π*f_{CLK}), where dBc is the phase noise power of the Output Noise Floor integrated from 1 to 20 MHz bandwidth. The phase noise power can be calculated as: dBc = Noise Floor + 10*$\log_{10}$(20 MHz - 1 MHz). The additive RMS jitter was approximated for 625 MHz using Method #2 because the RMS jitter of the clock source was not sufficiently low enough to allow practical use of Method #1. Refer to the "Noise Floor vs. CLKin Slew Rate" and "RMS Jitter vs. CLKin Slew Rate" plots in *Section 13.0 Typical Performance Characteristics*.

Note 17: 156.25 MHz LVPECL clock source from LMK03806 with 20 MHz crystal reference (crystal part number: ECS-200-20-30BU-DU). J_{SOURCE} = 190 fs RMS (10 kHz to 1 MHz) and 195 fs RMS (12 kHz to 20 MHz). Refer to the LMK03806 datasheet for more information.

Note 18: The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is ≥ 10 MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations.

Note 19: Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, it is recommended to use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

Note 20: Specification is guaranteed by characterization and is not tested in production.

Note 21: See *Section 13.0 Typical Performance Characteristics* for output operation over frequency.

Note 22: AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.

Note 23: Output Enable Time is the number of input clock cycles it takes for the output to be enabled after REFout_EN is pulled high. Similarly, Output Disable Time is the number of input clock cycles it takes for the output to be disabled after REFout_EN is pulled low. The REFout_EN signal should have an edge transition much faster than that of the input clock period for accurate measurement.

Note 24: Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

12.0 Measurement Definitions

12.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 1 illustrates the two different definitions side-by-side for inputs and *Figure 2* illustrates the two different definitions side-by-side for outputs. The V_{ID} (or V_{OD}) definition show the DC levels, V_{IH} and V_{OL} (or V_{OH} and V_{OL}), that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

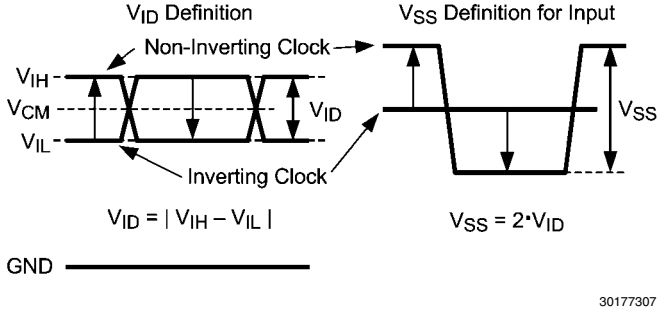


FIGURE 1. Two Different Definitions for Differential Input Signals

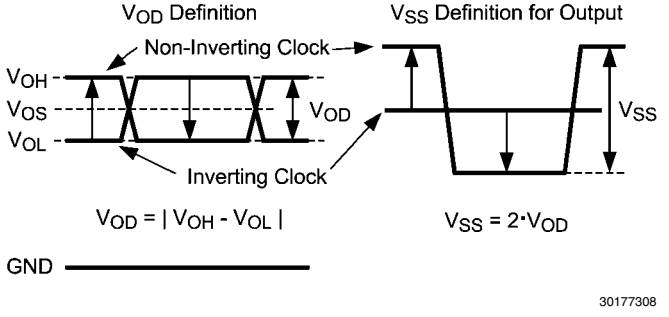


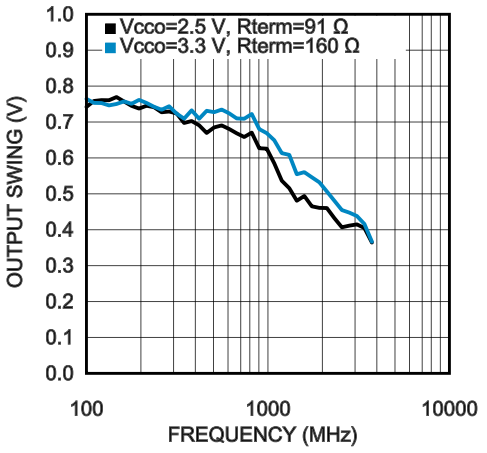
FIGURE 2. Two Different Definitions for Differential Output Signals

Note 25: Refer to Application Note AN-912 Common Data Transmission Parameters and their Definitions for more information.

13.0 Typical Performance Characteristics

Unless otherwise specified: Vcc = 3.3 V, Vcco = 3.3 V, T_A = 25 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns.

LVPECL Output Swing (V_{OD}) vs. Frequency



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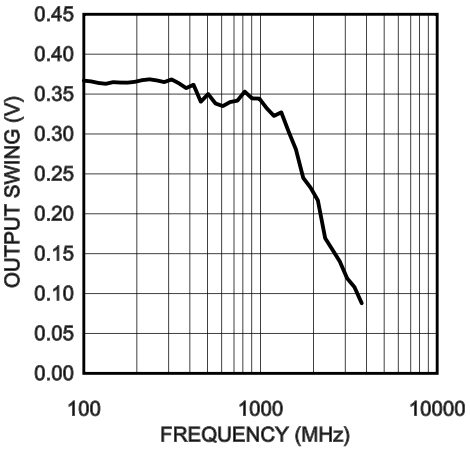
LVDS Output Swing (V_{OD}) vs. Frequency



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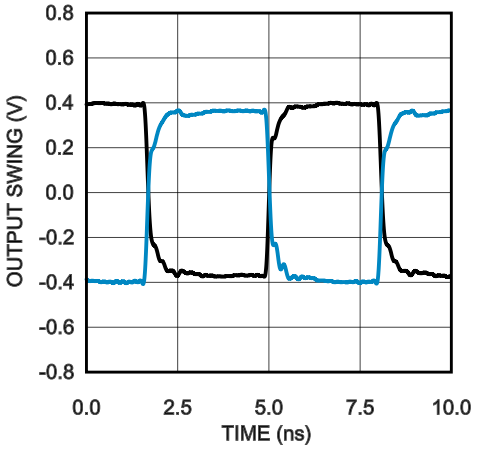
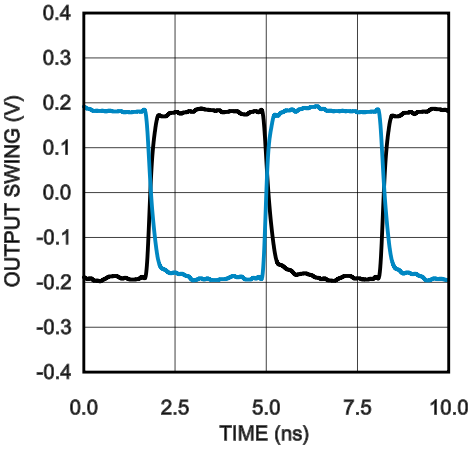
LVPECL Output Swing @ 156.25 MHz



30177391

LVDS Output Swing @ 156.25 MHz



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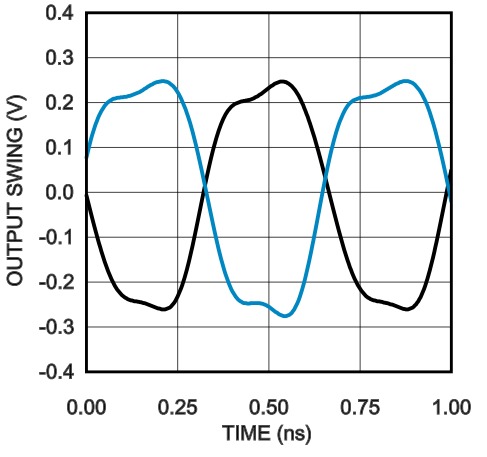
LVPECL Output Swing @ 1.5 GHz



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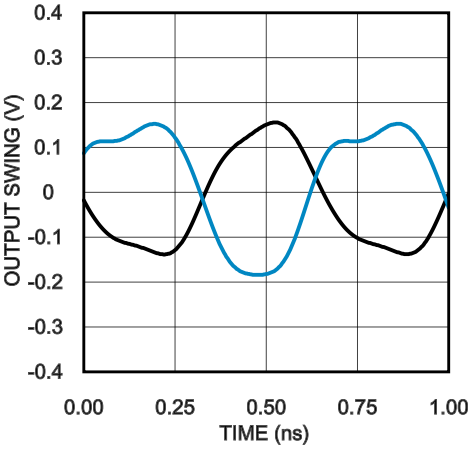
LVDS Output Swing @ 1.5 GHz



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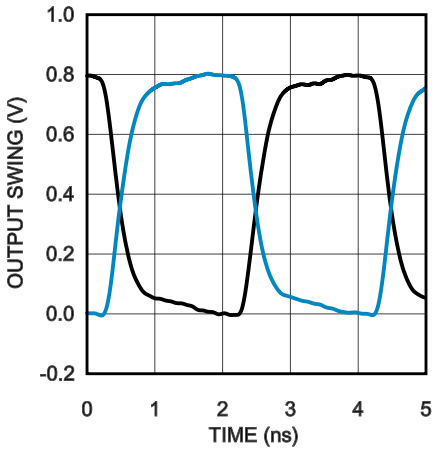
HCSL Output Swing @ 250 MHz



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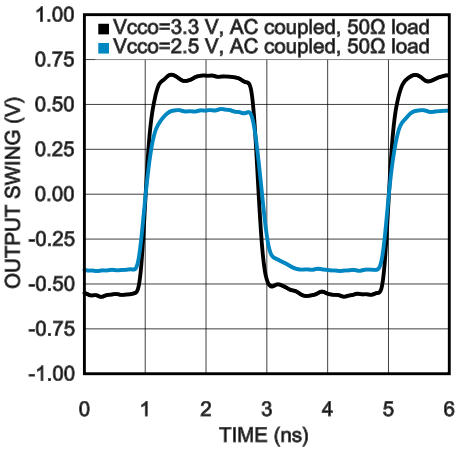
LVCMOS Output Swing @ 250 MHz



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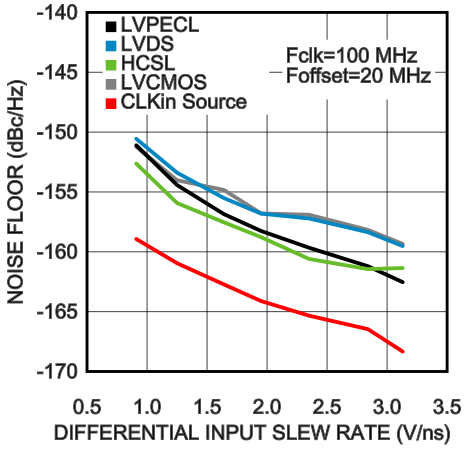
Noise Floor vs. CLKin Slew Rate @ 100 MHz



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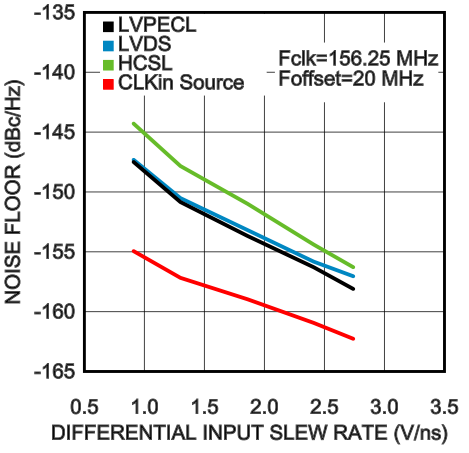
Noise Floor vs. CLKin Slew Rate @ 156.25 MHz



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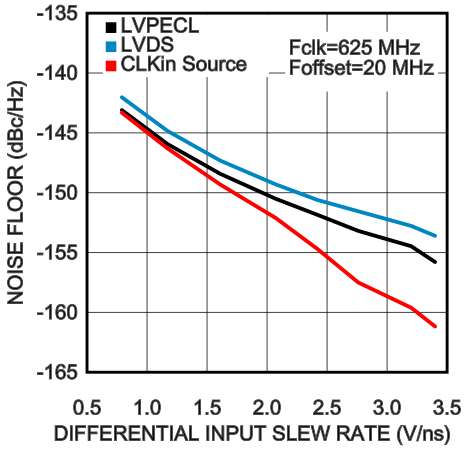
Noise Floor vs. CLKin Slew Rate @ 625 MHz



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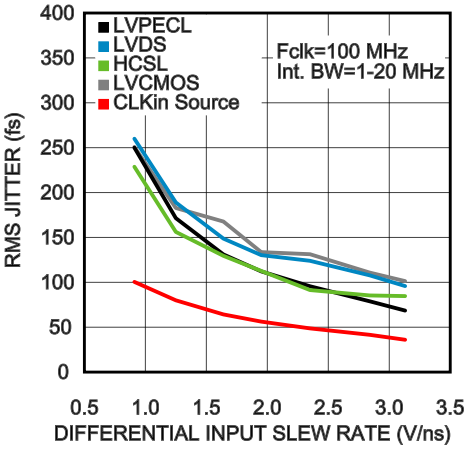
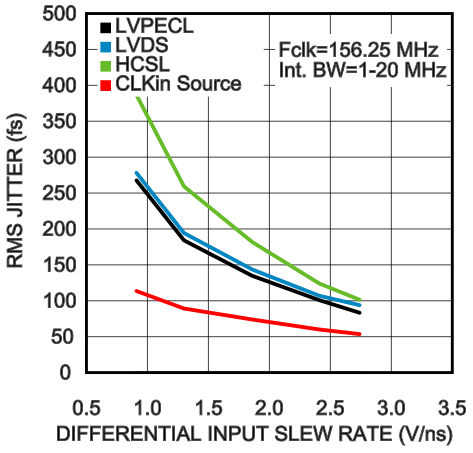
RMS Jitter vs. CLKin Slew Rate @ 100 MHz (*Note 26*)



30177380

RMS Jitter vs. CLKin Slew Rate @ 156.25 MHz (*Note 26*)



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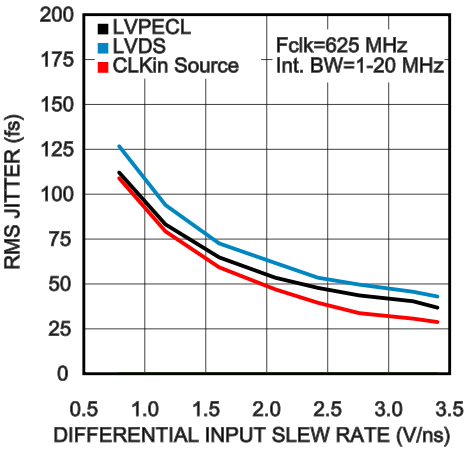
RMS Jitter vs. CLKin Slew Rate @ 625 MHz



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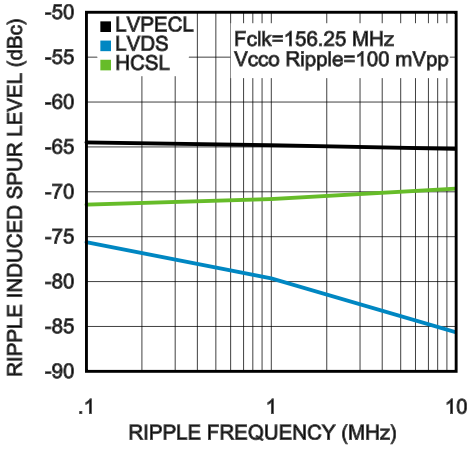
PSRR vs. Ripple Frequency @ 156.25 MHz



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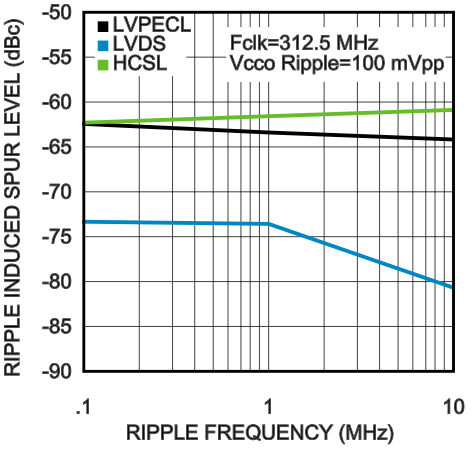
PSRR vs. Ripple Frequency @ 312.5 MHz



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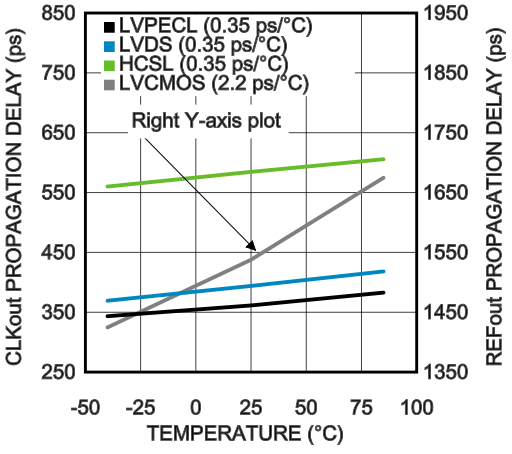
Propagation Delay vs. Temperature



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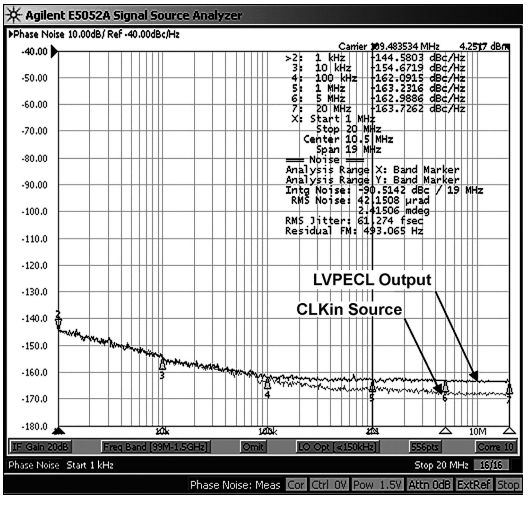
LVPECL Phase Noise @ 100 MHz (*Note 26*)



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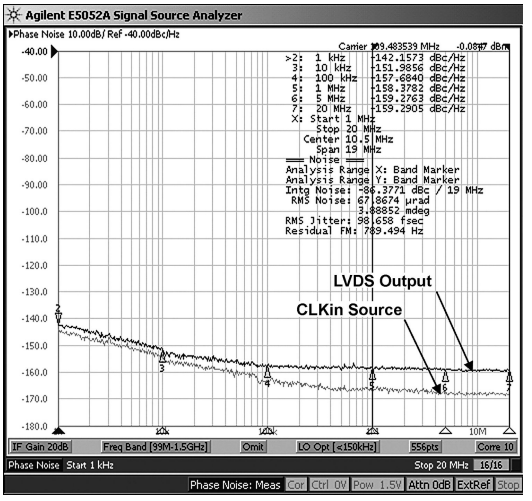
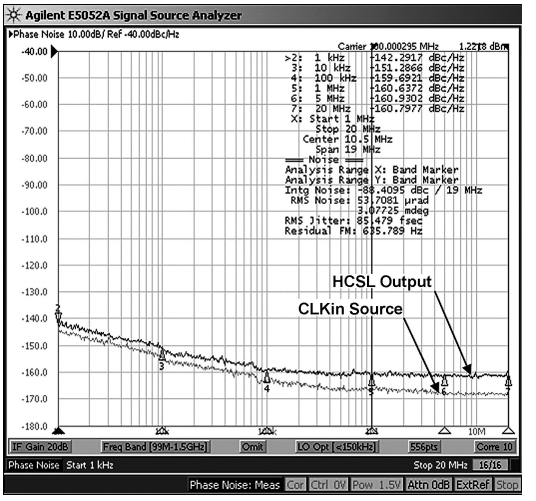
LVDS Phase Noise @ 100 MHz (*Note 26*)



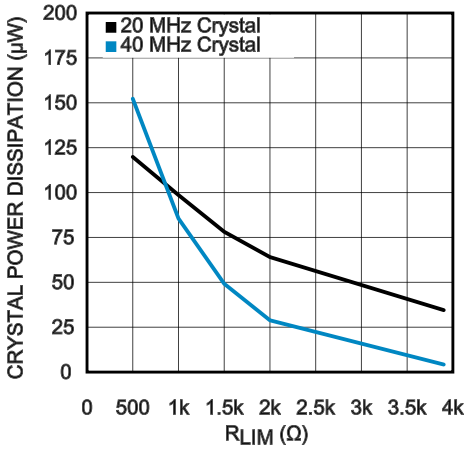
30177396

HCSL Phase Noise @ 100 MHz (*Note 26*)



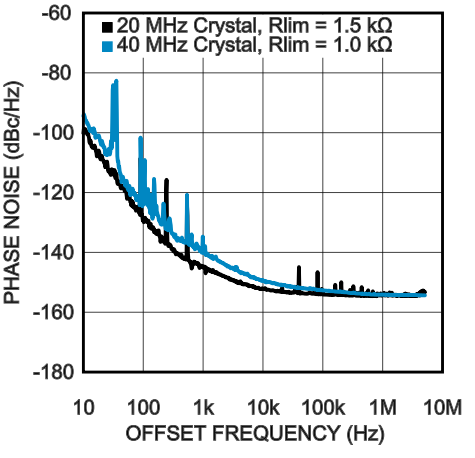
30177397

Crystal Power Dissipation vs. R_{LIM}
(*Note 27*, *Note 28*)



30177331

LVDS Phase Noise in Crystal Mode
(*Note 27*, *Note 28*)



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Note 26: The typical RMS jitter values in the plots show the total output RMS jitter (J_{OUT}) for each output buffer type and the source clock RMS jitter (J_{SOURCE}). From these values, the Additive RMS Jitter can be calculated as: $J_{ADD} = SQRT(J_{OUT}^2 - J_{SOURCE}^2)$.

Note 27: 20 MHz crystal characteristics: Abracon ABL series, AT cut, C_L = 18 pF , C_0 = 4.4 pF measured (7 pF max), ESR = 8.5 Ω measured (40 Ω max), and Drive Level = 1 mW max (100 µW typical).

Note 28: 40 MHz crystal characteristics: Abracon ABLS2 series, AT cut, C_L = 18 pF , C_0 = 5 pF measured (7 pF max), ESR = 5 Ω measured (40 Ω max), and Drive Level = 1 mW max (100 µW typical).

14.0 Application Information

14.1 Driving the Clock Inputs

The LMK00304 has two universal inputs (CLKin0/CLKin0* and CLKin1/CLKin1*) that can accept DC-coupled 3.3V/2.5V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet the input requirements specified in *Section 11.0 Electrical Characteristics*. The device can accept a wide range of signals due to its wide input common mode voltage range (V_{CM}) and input voltage swing (V_{ID}) / dynamic range. For 50% duty cycle and DC-balanced signals, AC coupling may also be employed to shift the input signal to within the V_{CM} range. Refer to *Section 14.3 Termination and Use of Clock Drivers* for signal interfacing and termination techniques.

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. For this reason, a differential signal input is recommended over single-ended because it typically provides higher slew rate and common-mode-rejection. Refer to the “Noise Floor vs. CLKin Slew Rate” and “RMS Jitter vs. CLKin Slew Rate” plots in *Section 13.0 Typical Performance Characteristics*.

While it is recommended to drive the CLKin0 and CLKin1 with a differential signal input, it is possible to drive them with a single-ended clock. Again, the single-ended input slew rate should be as high as possible to minimize performance degradation. The CLKin input has an internal bias voltage of about 1.4 V, so the input can be AC coupled as shown in *Figure 3*.

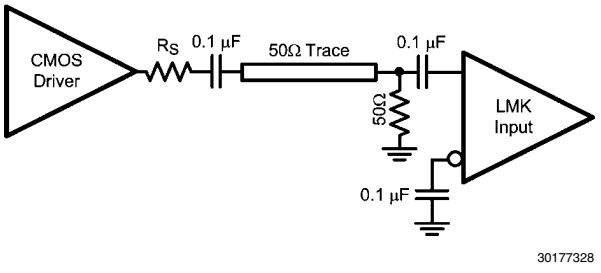


FIGURE 3. Single-Ended LVCMOS Input, AC Coupling

A single-ended clock may also be DC coupled to CLKinX as shown in *Figure 4*. If the DC coupled input swing has a common mode level near the device's internal bias voltage of 1.4 V, then only a 0.1 uF bypass cap is required on CLKinX*. Otherwise, if the input swing is not optimally centered near the internal bias voltage, then CLKinX* should be externally biased to the midpoint voltage of the input swing. This can be achieved using external biasing resistors, R_{B1} and R_{B2}, or another low-noise voltage reference. The external bias voltage should be within the specified input common voltage (V_{CM}) range. This will ensure the input swing crosses the threshold voltage at a point where the input slew rate is the highest.

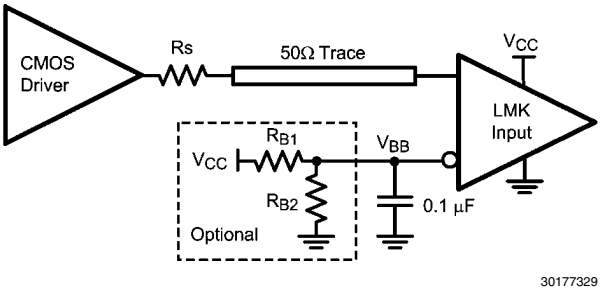


FIGURE 4. Single-Ended LVCMOS Input, DC Coupling with Common Mode Biasing

If the crystal oscillator circuit is not used, it is possible to drive the OSCin input with an single-ended external clock as shown in *Figure 5*. The input clock should be AC coupled to the OSCin pin, which has an internally-generated input bias voltage, and the OSCout pin should be left floating. While OSCin provides an alternative input to multiplex an external clock, it is recommended to use either universal input (CLKinX) since it offers higher operating frequency, better common mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.

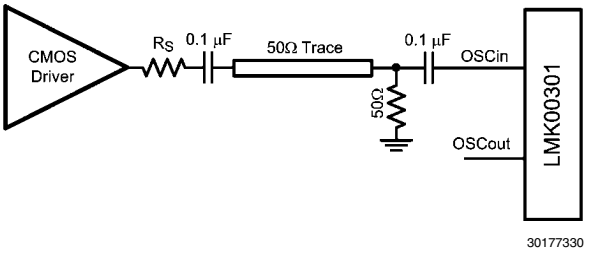


FIGURE 5. Driving OSCin with a Single-Ended Input

14.2 Crystal Interface

The LMK00304 has an integrated crystal oscillator circuit that supports a fundamental mode, AT-cut crystal. The crystal interface is shown in *Figure 6*.

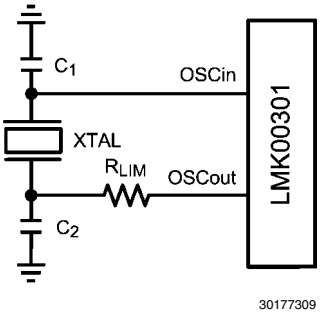


FIGURE 6. Crystal Interface

The load capacitance (C_L) is specific to the crystal, but usually on the order of 18 - 20 pF. While C_L is specified for the crystal, the OSCin input capacitance (C_{IN} = 1 pF typical) of the device and PCB stray capacitance (C_{STRAY} ~ 1~3 pF) can affect the discrete load capacitor values, C_1 and C_2.

For the parallel resonant circuit, the discrete capacitor values can be calculated as follows:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{IN} + C_{STRAY} \quad (1)$$

Typically, $C_1 = C_2$ for optimum symmetry, so *Equation 1* can be rewritten in terms of C_1 only:

$$C_L = C_1^2 / (2 * C_1) + C_{IN} + C_{STRAY} \quad (2)$$

Finally, solve for C_1:

$$C_1 = (C_L - C_{IN} - C_{STRAY})*2 \quad (3)$$

Section 11.0 Electrical Characteristics provides crystal interface specifications with conditions that ensure start-up of the crystal, but it does not specify crystal power dissipation. The designer will need to ensure the crystal power dissipation does not exceed the maximum drive level specified by the crystal manufacturer. Overdriving the crystal can cause premature aging, frequency shift, and eventual failure. Drive level should be held at a sufficient level necessary to start-up and maintain steady-state operation.

The power dissipated in the crystal, P_{XTAL}, can be computed by:

$$P_{XTAL} = I_{RMS}^2 * R_{ESR}*(1 + C_0/C_L)^2 \quad (4)$$

Where:

- I_{RMS} is the RMS current through the crystal.
- R_{ESR} is the max. equivalent series resistance specified for the crystal
- C_L is the load capacitance specified for the crystal
- C_0 is the min. shunt capacitance specified for the crystal

I_{RMS} can be measured using a current probe (e.g. Tektronix CT-6 or equivalent) placed on the leg of the crystal connected to OSCout with the oscillation circuit active.

As shown in *Figure 6*, an external resistor, R_{LIM}, can be used to limit the crystal drive level, if necessary. If the power dissipated in the selected crystal is higher than the drive level specified for the crystal with R_{LIM} shorted, then a larger resistor value is mandatory to avoid overdriving the crystal. However, if the power dissipated in the crystal is less than the drive level with R_{LIM} shorted, then a zero value for R_{LIM} can be used. As a starting point, a suggested value for R_{LIM} is 1.5 kΩ.

14.3 Termination and Use of Clock Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads.
  - LVDS outputs are current drivers and require a closed current loop.
  - HCSL drivers are switched current outputs and require a DC path to ground via 50 Ω termination.
  - LVPECL outputs are open emitter and require a DC path to ground.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level; in this case, the signal should normally be AC coupled.

It is possible to drive a non-LVPECL or non-LVDS receiver with a LVDS or LVPECL driver as long as the above guidelines are followed. Check the datasheet of the receiver or input being driven to determine the best termination and coupling method to be sure the receiver is biased at the optimum DC voltage (common mode voltage).

14.3.1 Termination for DC Coupled Differential Operation

For DC coupled operation of an LVDS driver, terminate with 100 Ω as close as possible to the LVDS receiver as shown in *Figure 7*.

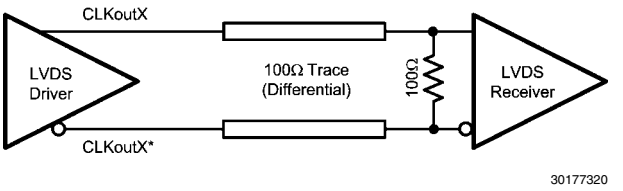


FIGURE 7. Differential LVDS Operation, DC Coupling, No Biasing by the Receiver

For DC coupled operation of an HCSL driver, terminate with 50 Ω to ground near the driver output as shown in *Figure 8*. Series resistors, Rs, may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a DC path to ground, AC coupling is not allowed between the output drivers and the 50 Ω termination resistors.

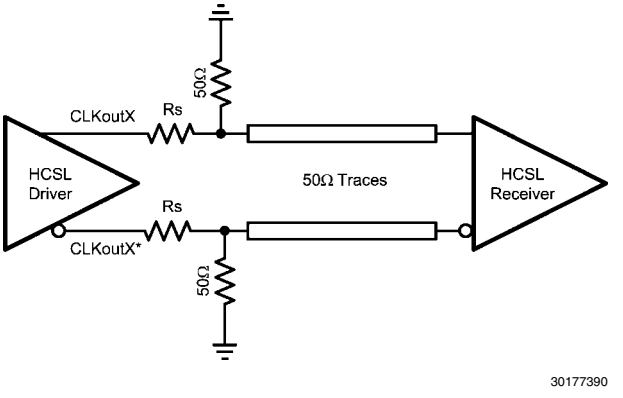


FIGURE 8. HCSL Operation, DC Coupling

For DC coupled operation of an LVPECL driver, terminate with 50 Ω to Vcco - 2 V as shown in *Figure 9*. Alternatively terminate with a Thevenin equivalent circuit as shown in *Figure 10* for Vcco (output driver supply voltage) = 3.3 V and 2.5 V. In the Thevenin equivalent circuit, the resistor dividers set the output termination voltage (V_{TT}) to Vcco – 2 V.

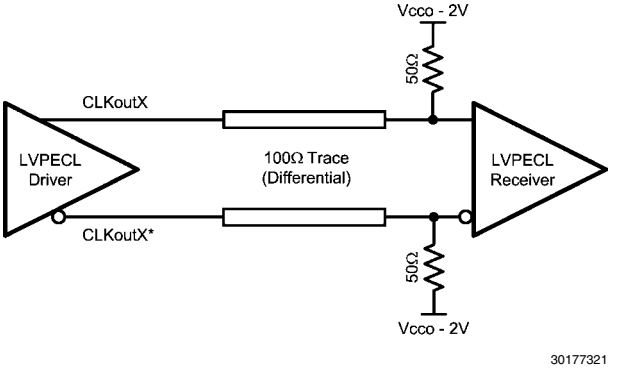
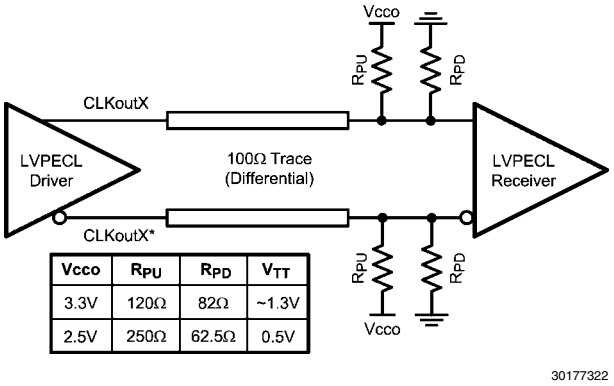


FIGURE 9. Differential LVPECL Operation, DC Coupling



Vcco	RPU	RPD	VTT
3.3V	120Ω	82Ω	~1.3V
2.5V	250Ω	62.5Ω	0.5V

FIGURE 10. Differential LVPECL Operation, DC Coupling, Thevenin Equivalent

14.3.2 Termination for AC Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common mode voltage) when driving different receiver standards. Since AC coupling prevents the driver from providing a DC bias voltage at the receiver, it is important to ensure the receiver is biased to its ideal DC level.

When driving non-biased LVDS receivers with an LVDS driver, the signal may be AC coupled by adding DC blocking capacitors; however the proper DC bias point needs to be established at the receiver. One way to do this is with the termination circuitry in *Figure 11*. When driving self-biased LVDS receivers, the circuit shown in *Figure 11* may be modified by replacing the 50 Ω terminations to Vbias with a single 100 Ω resistor across the input pins of the receiver. When using AC coupling with LVDS outputs, there may be a startup delay observed in the clock output due to capacitor charging. The previous example uses a 0.1 µF capacitor, but this may need to be adjusted to meet the startup requirements for the particular application. Another variant of AC coupling to a self-biased LVDS receiver is to move the 0.1 uF capacitors between the 100 Ω differential termination and the receiver inputs.

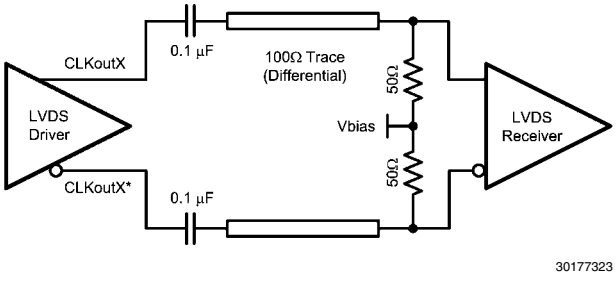


FIGURE 11. Differential LVDS Operation, AC Coupling, No Biasing by the Receiver

LVPECL drivers require a DC path to ground. When AC coupling an LVPECL signal use 160 Ω emitter resistors (or 91 Ω for Vcco = 2.5 V) close to the LVPECL driver to provide a DC path to ground as shown in *Figure 15*. For proper receiver operation, the signal should be biased to the DC bias level (common mode voltage) specified by the receiver. The typical DC bias voltage (common mode voltage) for LVPECL receivers is 2 V. Alternatively, a Thevenin equivalent circuit forms a valid termination as shown in *Figure 12* for Vcco = 3.3 V and 2.5 V. Note: this Thevenin circuit is different from the DC coupled example in *Figure 10*, since the voltage divider is setting the input common mode voltage of the receiver.

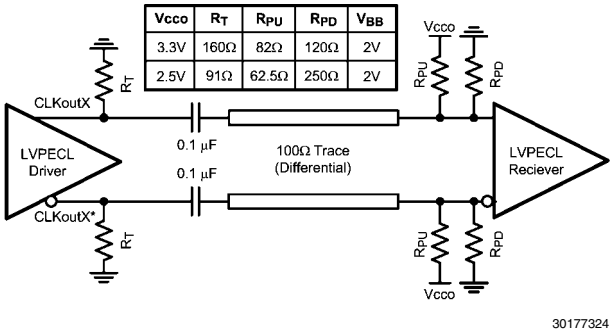


FIGURE 12. Differential LVPECL Operation, AC Coupling, Thevenin Equivalent

14.3.3 Termination for Single-Ended Operation

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal.

It is possible to use an LVPECL driver as one or two separate 800 mV p-p signals. When DC coupling one of the LMK00304 LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminate the unused driver. When DC coupling on of the LMK00304 LVPECL drivers, the termination should be 50 Ω to Vcco - 2 V as shown in *Figure 13*. The Thevenin equivalent circuit is also a valid termination as shown in *Figure 14* for Vcco = 3.3 V.

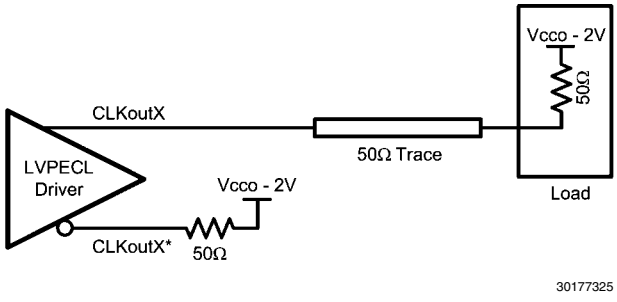
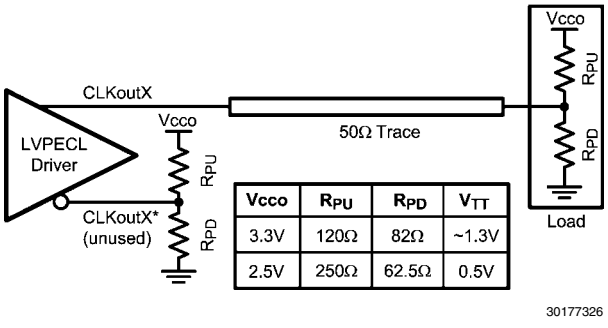


FIGURE 13. Single-Ended LVPECL Operation, DC Coupling

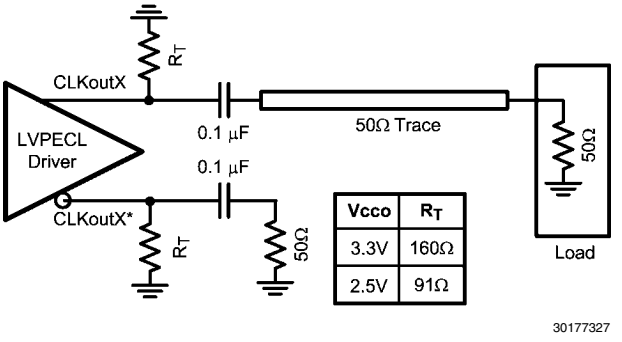


Vcco	RPU	RPD	VTT
3.3V	120Ω	82Ω	~1.3V
2.5V	250Ω	62.5Ω	0.5V

FIGURE 14. Single-Ended LVPECL Operation, DC Coupling, Thevenin Equivalent

When AC coupling an LVPECL driver use a 160 Ω emitter resistor (or 91 Ω for Vcco = 2.5 V) to provide a DC path to ground and ensure a 50 Ω termination with the proper DC bias level for the receiver. The typical DC bias voltage for LVPECL

receivers is 2 V. If the companion driver is not used, it should be terminated with either a proper AC or DC termination. This latter example of AC coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment no DC bias point (0 VDC) is required for safe and proper operation. The internal 50 Ω termination the test equipment correctly terminates the LVPECL driver being measured as shown in *Figure 15*. When using only one LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminated the unused driver.



Vcco	R_T
3.3V	160Ω
2.5V	91Ω

FIGURE 15. Single-Ended LVPECL Operation, AC Coupling

14.4 Power Supply and Thermal Considerations

14.4.1 Current Consumption and Power Dissipation Calculations

The current consumption values specified in *Section 11.0 Electrical Characteristics* can be used to calculate the total power dissipation and IC power dissipation for any device configuration. The total V_{CC} core supply current (I_{CC_TOTAL}) can be calculated using *Equation 5*:

$$I_{CC\_TOTAL} = I_{CC\_CORE} + I_{CC\_BANKS} + I_{CC\_CMOS} \quad (5)$$

Where:

- I_{CC_CORE} is the V_{CC} current for core logic and input blocks and depends on selected input (CLKinX or OSCin).
- I_{CC_BANKS} is the V_{CC} current for Banks A & B and depends on the selected output type (I_{CC_PECL}, I_{CC_LVDS}, I_{CC_HCSL}, or 0 mA if disabled).
- I_{CC_CMOS} is the V_{CC} current for the LVCMOS output (or 0 mA if REFout is disabled).

Since the output supplies (V_{CCOA}, V_{CCOB}, V_{CCOC}) can be powered from 3 independent voltages, the respective output supply currents ($I_{CCO\_BANK\_A}$, $I_{CCO\_BANK\_B}$, and I_{CCO_CMOS}) should be calculated separately.

I_{CCO_BANK} for either Bank A or B may be taken as 50% of the corresponding output supply current specified for two banks (I_{CCO_PECL}, I_{CCO_LVDS}, or I_{CCO_HCSL}) **provided the output loading matches the specified conditions**. Otherwise, I_{CCO_BANK} should be calculated per bank as follows:

$$I_{CCO\_BANK} = I_{BANK\_BIAS} + (N * I_{OUT\_LOAD}) \quad (6)$$

Where:

- I_{BANK_BIAS} is the output bank bias current (fixed value).
- I_{OUT_LOAD} is the DC load current per loaded output pair.
- N is the number of loaded output pairs (N = 0 to 2).

Table 5 shows the typical I_{BANK_BIAS} values and I_{OUT_LOAD} expressions for LVPECL, LVDS, and HCSL.

For LVPECL, it is possible to use a larger termination resistor (R_T) to ground instead of terminating with 50 Ω to V_{TT} = Vcco - 2 V; this technique is commonly used to eliminate the extra termination voltage supply (V_{TT}) and potentially reduce device power dissipation at the expense of lower output swing. For example, when Vcco is 3.3 V, a R_T value of 160 Ω to ground will eliminate the 1.3 V termination supply without sacrificing much output swing. In this case, the typical I_{OUT_LOAD} is 25 mA, so I_{CCO_BANK} for one LVPECL bank reduces to 63 mA (vs. 67.5 mA with 50 Ω resistors to Vcco - 2 V).

TABLE 5. Typical Output Bank Bias and Load Currents

Current Parameter	LVPECL	LVDS	HCSL
I_{BANK_BIAS}	13 mA	11.6 mA	2.4 mA
I_{OUT_LOAD}	$(V_{OH} - V_{TT})/R_T + (V_{OL} - V_{TT})/R_T$	0 mA (No DC load current)	V_{OH}/R_T

Once the current consumption is known for each supply, the total power dissipation (P_{TOTAL}) can be calculated:

$$P_{TOTAL} = (V_{CC}*I_{CC\_TOTAL}) + (V_{CCOA}*I_{CCO\_BANK}) + (V_{CCOB}*I_{CCO\_BANK}) + (V_{CCOC}*I_{CCO\_CMOS}) \quad (7)$$

If the device is configured with LVPECL and/or HCSL outputs, then it is also necessary to calculate the power dissipated in any termination resistors (P_{RT_PECL} and P_{RT_HCSL}) and in any LVPECL termination voltages (P_{VTT_PECL}). The external power dissipation values can be calculated as follows:

$$P_{RT\_PECL} \text{ (per LVPECL pair)} = (V_{OH} - V_{TT})^2/R_T + (V_{OL} - V_{TT})^2/R_T \quad (8)$$

$$P_{VTT\_PECL} \text{ (per LVPECL pair)} = V_{TT} * [(V_{OH} - V_{TT})/R_T + (V_{OL} - V_{TT})/R_T] \quad (9)$$

$$P_{RT\_HCSL} \text{ (per HCSL pair)} = V_{OH}^2 / R_T \quad (10)$$

Finally, the IC power dissipation (P_{DEVICE}) can be computed by subtracting the external power dissipation values from P_{TOTAL} as follows:

$$P_{DEVICE} = P_{TOTAL} - N_1*(P_{RT\_PECL} + P_{VTT\_PECL}) - N_2*P_{RT\_HCSL} \quad (11)$$

Where:

- N_1 is the number of LVPECL output pairs with termination resistors to V_{TT} (usually Vcco - 2 V or GND).
- N_2 is the number of HCSL output pairs with termination resistors to GND.

14.4.1.1 Power Dissipation Example: Worst-Case Dissipation

This example shows how to calculate IC power dissipation for a configuration to estimate **worst-case power dissipation**. In this case, the maximum supply voltage and supply current values specified in *Section 11.0 Electrical Characteristics* are used.

- Max V_{CC} = V_{CCO} = 3.465 V. Max I_{CC} and I_{CCO} values.
- CLKin0/CLKin0* input is selected.
- Banks A and B are configured for LVPECL: all outputs terminated with 50 Ω to V_T = Vcco - 2 V.
- REFout is enabled with 5 pF load.
- T_A = 85 °C

Using the power calculations from the previous section and *maximum* supply current specifications, we can compute P_{TOTAL} and P_{DEVICE}.

- From *Equation 5*: I_{CC_TOTAL} = 10.5 mA + 48 mA + 5.5 mA = 64 mA
- From I_{CCO_PECL} max spec: I_{CCO_BANK} = 50% of I_{CCO_PECL} = 81.5 mA
- From *Equation 7*: P_{TOTAL} = (3.465 V * 64 mA) + (3.465 V * 81.5 mA)+ (3.465 V * 81.5 mA) + (3.465 V * 10 mA) = 821 mW
- From *Equation 8*: P_{RT_PECL} = ((2.57 V - 1.47 V)²/50 Ω) + ((1.72 V - 1.47 V)²/50 Ω) = 25.5 mW (per output pair)
- From *Equation 9*: P_{VTT_PECL} = 1.47 V * [((2.57 V - 1.47 V) / 50 Ω) + ((1.72 V - 1.47 V) / 50 Ω)] = 39.5 mW (per output pair)
- From *Equation 10*: P_{RT_HCSL} = 0 mW (no HCSL outputs)
- From *Equation 11*: P_{DEVICE} = 821 mW - (4 * (25.5 mW + 39.5 mW)) - 0 mW = 561 mW

In this worst-case example, the IC device will dissipate about 561 mW or 68% of the total power (821 mW), while the remaining 32% will be dissipated in the emitter resistors (102 mW for 4 pairs) and termination voltage (158 mW into Vcco - 2 V). Based on θ_{JA} of 38.1 °C/W, the estimate die junction temperature would be about 21.4 °C above ambient, or 106.4 °C when T_A = 85 °C.

14.4.2 Power Supply Bypassing

The Vcc and Vcco power supplies should have a high-frequency bypass capacitor, such as 0.1 uF or 0.01 uF, placed very close to each supply pin. 1 uF to 10 uF decoupling capacitors should also be placed nearby the device between the supply and ground planes. All bypass and decoupling capacitors should have short connections to the supply and ground plane through a short trace or via to minimize series inductance.

14.4.2.1 Power Supply Ripple Rejection

In practical system applications, power supply noise (ripple) can be generated from switching power supplies, digital ASICs or FPGAs, etc. While power supply bypassing will help filter out some of this noise, it is important to understand the effect of power supply ripple on the device performance. When a single-tone sinusoidal signal is applied to the power supply of a clock distribution device, such as LMK00304, it can produce narrow-band phase modulation as well as amplitude modulation on the clock output (carrier). In the single-side band phase noise spectrum, the ripple-induced phase modulation appears as a phase spur level relative to the carrier (measured in dBc).

For the LMK00304, power supply ripple rejection, or PSRR, was measured as the single-sideband phase spur level (in dBc) modulated onto the clock output when a ripple signal was injected onto the Vcco supply. The PSRR test setup is shown in *Figure 16*.

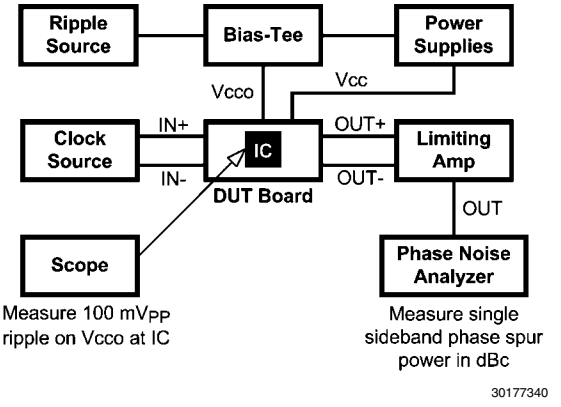


FIGURE 16. PSRR Test Setup

A signal generator was used to inject a sinusoidal signal onto the Vcco supply of the DUT board, and the peak-to-peak ripple amplitude was measured at the Vcco pins of the device. A limiting amplifier was used to remove amplitude modulation on the differential output clock and convert it to a single-ended signal for the phase noise analyzer. The phase spur level measurements were taken for clock frequencies of 156.25 MHz and 312.5 MHz under the following power supply ripple conditions:

- Ripple amplitude: 100 mVpp on Vcco = 2.5 V
- Ripple frequencies: 100 kHz, 1 MHz, and 10 MHz

Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows:

$$DJ\ (ps\ pk\text{-}pk) = [(2*10^{(PSRR\ /\ 20)}) / (\pi * f_{CLK})] * 10^{12} \quad (12)$$

The “PSRR vs. Ripple Frequency” plots in *Section 13.0 Typical Performance Characteristics* show the ripple-induced phase spur levels for the differential output types at 156.25 MHz and 312.5 MHz . The LMK00304 exhibits very good and well-behaved PSRR characteristics across the ripple frequency range for all differential output types. The phase spur levels for LVPECL are below -64 dBc at 156.25 MHz and below -62

dBc at 312.5 MHz. Using *Equation 12*, these phase spur levels translate to Deterministic Jitter values of 2.57 ps pk-pk at 156.25 MHz and 1.62 ps pk-pk at 312.5 MHz. Testing has shown that the PSRR performance of the device improves for Vcco = 3.3 V under the same ripple amplitude and frequency conditions.

14.4.3 Thermal Management

Power dissipation in the LMK00304 device can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate, T_A (ambient temperature) plus device power dissipation times θ_{JA} should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended land and via pattern is shown in *Figure 17*. More information on soldering LLP packages can be obtained at: *http://www.national.com/analog/packaging/*.

A recommended footprint including recommended solder mask and solder paste layers can be found at: *http://www.national.com/analog/packaging/gerber* for the SQA32A package.

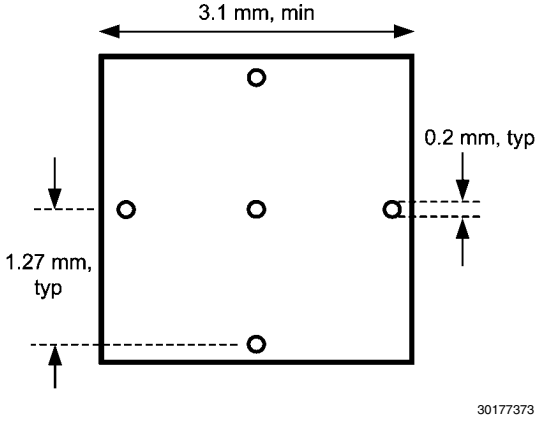
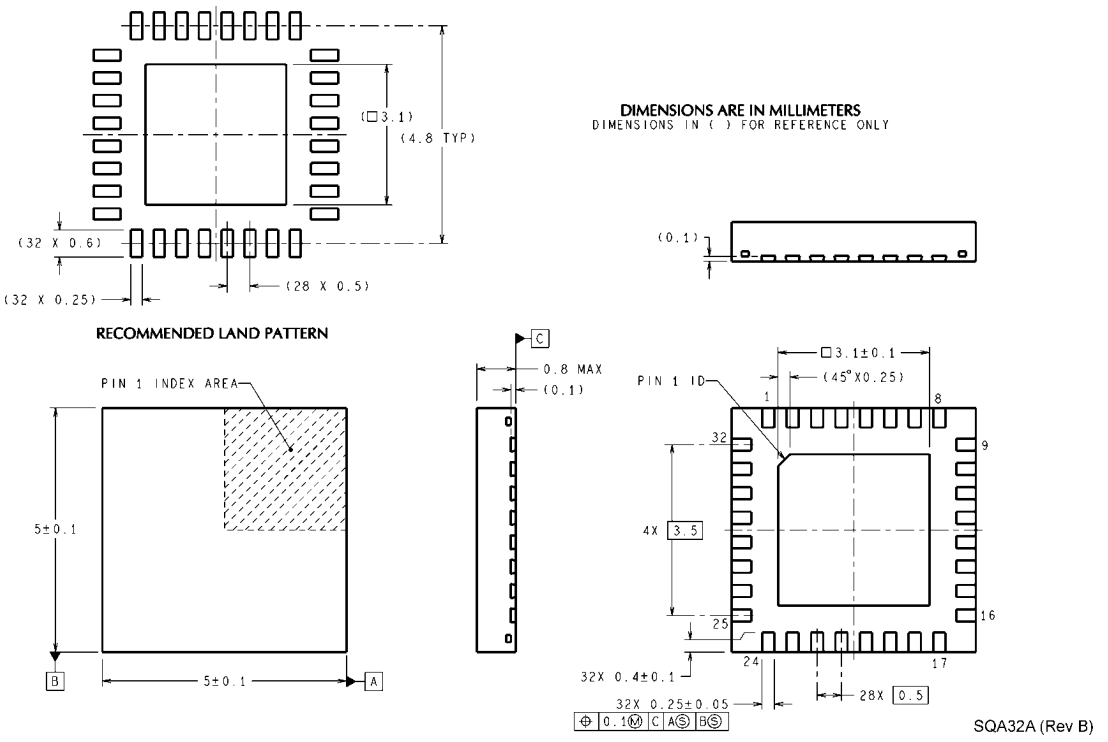


FIGURE 17. Recommended Land and Via Pattern

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in *Figure 17* should connect these top and bottom copper layers and to the ground layer. These vias act as "heat pipes" to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

15.0 Physical Dimensions inches (millimeters) unless otherwise noted



32-Pin LLP (SQA32A) Package

Order Number	Package Marking	Packing
LMK00304SQX	LMK00304	2500 Unit Tape and Reel
LMK00304SQ		1000 Unit Tape and Reel
LMK00304SQE		250 Unit Tape and Reel

Notes

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