National Semiconductor

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LM5033
100V Push-Pull Voltage Mode PWM Controller

General Description

The LM5033 High Voltage PWM controller contains all the features needed to implement Push-Pull, Half-Bridge, and Full-Bridge topologies. Applications include closed loop voltage mode converters with a highly regulated output voltage, or an open loop "DC transformer" such as an Intermediate Bus Converter (IBC) with an efficiency >95%. Two alternating gate driver outputs with a guaranteed deadtime are provided. The LM5033 includes a start-up regulator that operates over a wide input range of 15V to 100V. Additional features include: precision voltage reference output, current limit detection, remote shutdown, softstart, sync capability and thermal shutdown. This high speed IC has total propagation delays less than 100 ns and a 1MHz capable oscillator.

Features

- Internal high voltage (100V) start-up regulator
- Single resistor oscillator setting
- Synchronizable
- Precision reference output
- Adjustable soft-start
- Over-current protection
- Direct optocoupler interface
- 1.5A peak gate drivers
- Thermal Shutdown

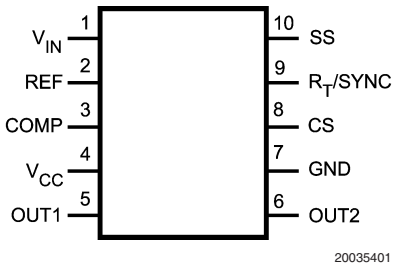
Applications

- Intermediate DC/DC Bus Converter
- Telecommunication Power Converters
- Industrial Power Converters
- +42V Automotive Systems

Package

- MSOP-10
- LLP-10

Connection Diagram



10-Lead MSOP, LLP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5033MM	MSOP-10	MUB10A	1000 Units on Tape and Reel
LM5033MMX	MSOP-10	MUB10A	3500 Units on Tape and Reel
LM5033SD	LLP-10 (4 x 4 mm)	SDC10A	1000 Units on Tape and Reel
LM5033SDX	LLP-10 (4 x 4 mm)	SDC10A	4500 Units on Tape and Reel

Pin Description

PIN	NAME	DESCRIPTION	APPLICATION INFORMATION
1	Vin	Input Voltage	Input to the start-up regulator. Input range is 15V to 90V, with transient capability to 100V .
2	REF	2.5V precision reference output	Sink only, requires an external pull-up resistor. This can be used as a reference for external circuitry.
3	COMP	PWM Input	Feedback to the PWM comparator's inverting input, through a 3:1 divider. The output duty cycle increases as this pin's voltage increases. Internally there is a 5kΩ pullup to +5.2V.
4	VCC	9.6V output from the internal high voltage series pass regulator	An external voltage (10V - 15V) can be applied to this pin to shutdown the internal regulator, thereby reducing internal dissipation. An internal diode connects Vcc to Vin.
5	OUT1	Gate Driver Output #1	Alternating output gate driver, which can source and sink 1.5A.
6	OUT2	Gate Driver Output #2	Alternating output gate driver, which can source and sink 1.5A.
7	GND	Ground pin for all internal circuitry	Connections to external ground must be done with care for optimum performance. See the Functional Description and Applications Section for more information.
8	CS	Current sense input	Current sense input for the current limit detection. If CS exceeds 0.5V the outputs are disabled and the softstart pin is discharged to ground.
9	R_T/ SYNC	Oscillator timing resistor pin and synchronization input	An external resistor to ground sets the oscillator frequency. This pin will also accept ac-coupled synchronization pulses from an external source.
10	SS	Softstart pin	An internal 10µA current source and an external capacitor set the soft-start timing. This pin can be externally pulled to below 0.5V to disable the output drivers.
LLP DAP	SUB	Die Substrate	The exposed die attach pad on the LLP package should be connected to a PCB thermal pad at ground potential. For additional information on using National Semiconductor's No Pull Back LLP package, please refer to LLP Application Note AN-1187.

Block Diagram

Functional Block Diagram

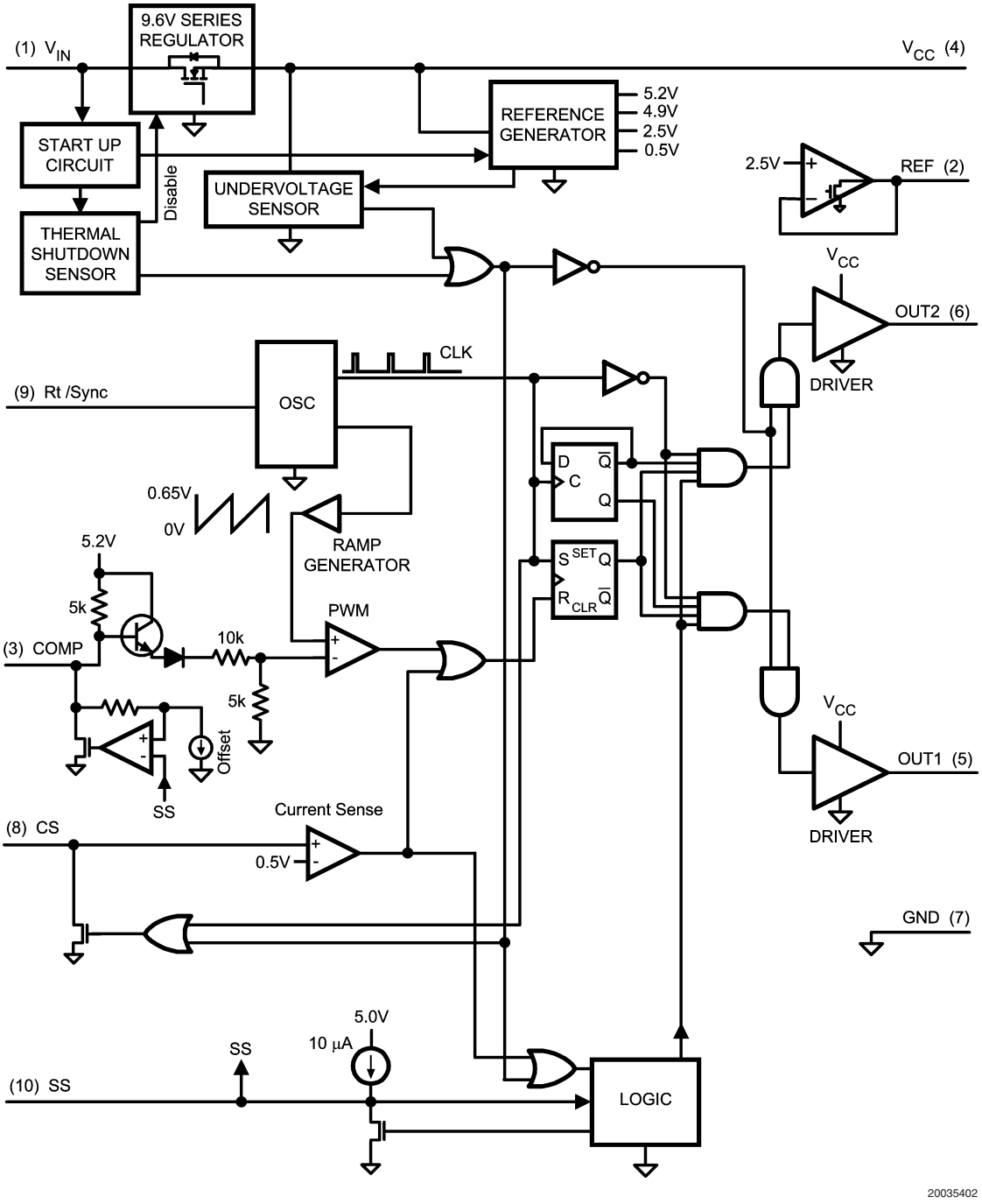


FIGURE 1.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} to GND	-0.3V to 100V
V_{CC} to GND	-0.3V to 16V
Rt/Sync to GND	-0.3V to 5.5V
Pins 3, 8, 10 to GND	-0.3V to 7.0V
ESD Rating (Note 3)	
Human Body Model	2kV
Storage Temperature Range	-65˚C to 150˚C
Junction Temperature	150˚C
Power Dissipation (Note 2)	Internally Limited

Operating Ratings (Note 1)

V_{IN} Voltage (Pin1)	15 to 90V
Operating Junction Temperature	-40˚C to 125˚C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, V_{CC} = 10V applied externally, R_T = 26.7kΩ, unless otherwise stated. See (Note 4) and (Note 5).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} Startup Regulator (Pins 1, 4)						
V_{CC}Reg	V_{CC} Voltage	Pin 4 open	**9.2**	9.6	**10.0**	V
Icc-out	V_{CC} Current Limit	Out1, Out2 disabled. Ext. supply to Vcc disconnected.	**20**	34		mA
Iin	Startup Regulator Current into V_{IN}	Normal Operation V_{IN} = 90V		150	**500**	µA
		Ext. V_{CC} Supply Disconnected and Output Load = 1800pF		7		mA
		SS Pin = 0V		3		mA
UVT	V_{CC} Undervoltage Threshold (increasing V_{CC})		**VccReg - 300mV**	VccReg - 100 mV		V
	UVT Hysteresis (decreasing V_{CC})		**2.3**	2.8	**3.3**	
Icc-in	Supply Current from external source to V_{CC}	SS Pin = 0V		2	**3**	mA
		SS Pin = open and Output Load = 1800pF		7		
2.5V Reference (Pin 2)						
Vref	Output voltage	Pin 2 sink current = 5mA	**2.44**	2.50	**2.56**	V
	Current sink capability		**5.0**	13		mA
Current Sense (Pin 8)						
CS	Threshold voltage		**0.45**	0.50	**0.55**	V
	CS delay to output	Pin 8 taken from zero to 0.6V. Time for Out1 or Out2 to fall to 90% of Vcc. CLoad = 0 @ Out1, Out2		30		ns
	Current sink capability (clocked)	Pin 8 ≤ 0.3V	**3**	6		mA
Softstart (Pin 10)						
	Softstart current source		**7**	10	**13**	µA
	Softstart to Comp offset		**0.25**	0.50	**0.75**	V
	Open Circuit Voltage			5.0		V

Electrical Characteristics (Continued)

Specifications with standard typeface are for T_J = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, V_{CC} = 10V applied externally, R_T = 26.7kΩ, unless otherwise stated. See (Note 4) and (Note 5).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Oscillator (Pin 9)						
Fs1	Internal frequency	Rt = 26.7 kΩ	**175**	200	**225**	kHz
Fs2	Internal frequency	Rt = 8.2 kΩ		600		kHz
Vsync	Sync threshold			3.2	**3.8**	V
	R_t/Sync DC voltage			2.0		V
PWM Comparator Input (Pin 3)						
t_{PWM}	Gain from pin 3 to PWM comparator			0.34		V/V
	Maximum duty cycle at Out1, Out2	See PWM Comparator text		100 x $(0.5T_S-T_D)/T_S$		%
	Minimum duty cycle at Out1, Out2	Pin 3 = 0V.			**0**	%
	Open Circuit Voltage		**4.2**	5.2	**6.2**	V
	Short circuit current	Pin 3 = 0V	**0.6**	1.1	**1.5**	mA
Output Drivers (Pin 5, 6)						
	Deadtime (T_D)	CLoad = 0 @ OUT1, OUT2. Time measured from 10% of falling output to 10% of rising output.	**85**	135	**185**	ns
	Rise Time	C_{Load} = 1nF		16		ns
	Fall Time	C_{Load} = 1nF		16		ns
	Output High Voltage	Iout = 50 mA (source)	**Vcc-0.75**	Vcc-0.25		V
	Output Low Voltage	Iout = 100 mA (sink)		0.25	**0.75**	V
	Max. source current			1.5		A
	Max. sink current			1.5		A
Thermal Shutdown						
T_{SD}	Shutdown temperature			165		˚C
	Shutdown temperature hysteresis			15		˚C
Thermal Resistance						
θ_{JA}	Junction to Ambient	MUB10A Package		200		˚C/W
		SDC10A Package		38		

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation is a function of the maximum allowed junction temperature ($T_{J(max)}$), the ambient temperature (T_A), and the junction-to-ambient thermal resistance (θ_{JA}). The maximum allowable power dissipation can be calculated from PD = ($T_{J(max)}$ - T_A) / θ_{JA}. Excessive power dissipation will cause the thermal shutdown to activate.

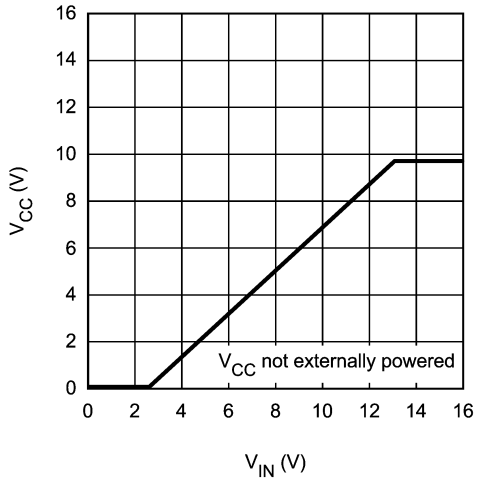
Note 3: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 4: Min and Max limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: Typical specifications represent the most likely parametric norm at 25˚C operation.

Typical Performance Characteristics

V_{CC} vs V_{IN}



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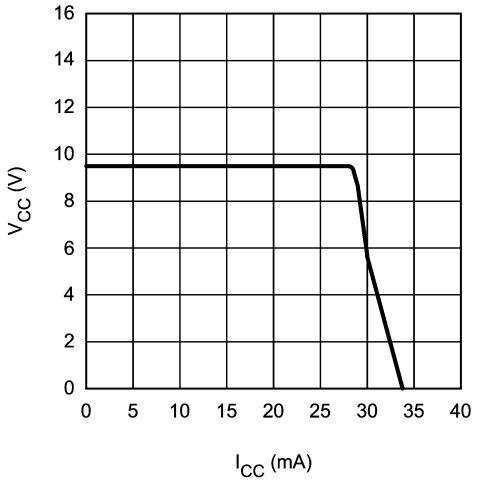
V_{CC} vs I_{CC} (V_{IN} = 48V)



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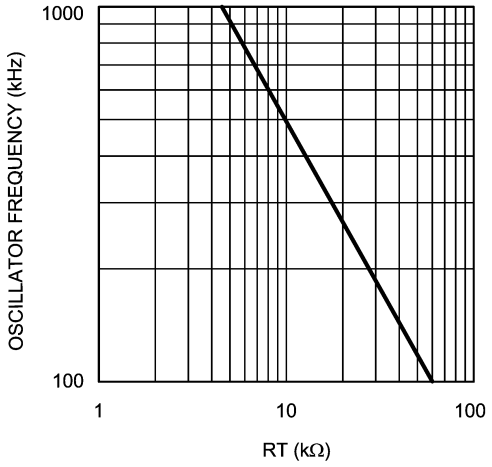
Oscillator Frequency vs R_T



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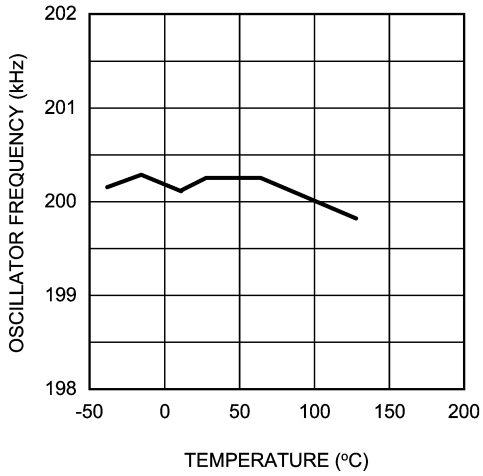
Oscillator Frequency vs Temperature
R_T = 26.7kΩ



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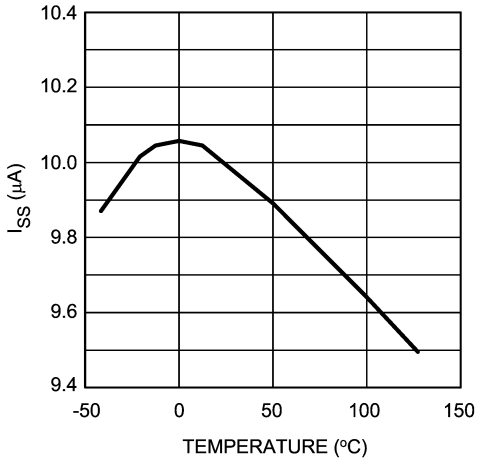
Soft Start Current vs Temperature



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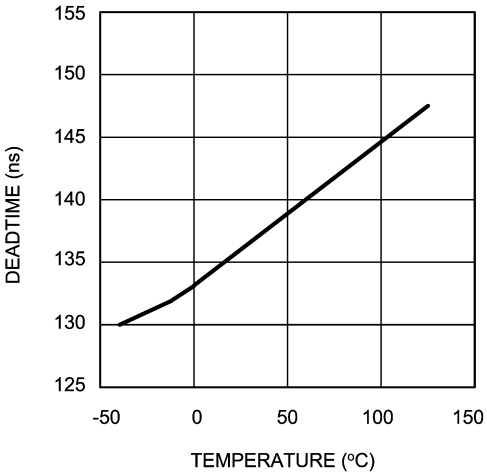
Dead Time vs Temperature



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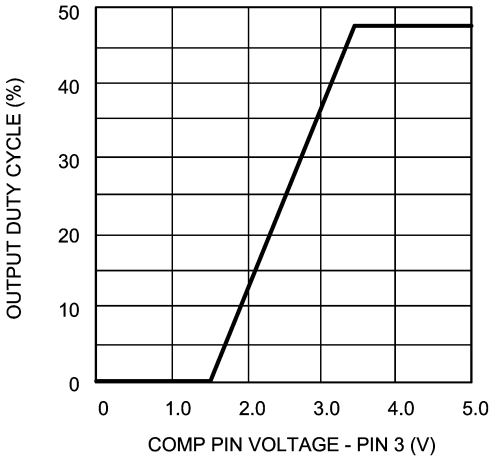
Typical Performance Characteristics (Continued)

Output Duty Cycle vs Comp Voltage
R_T = 16.5kΩ



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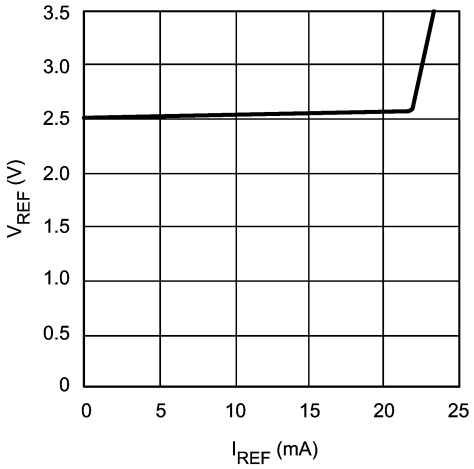
V_{REF} vs I_{REF}



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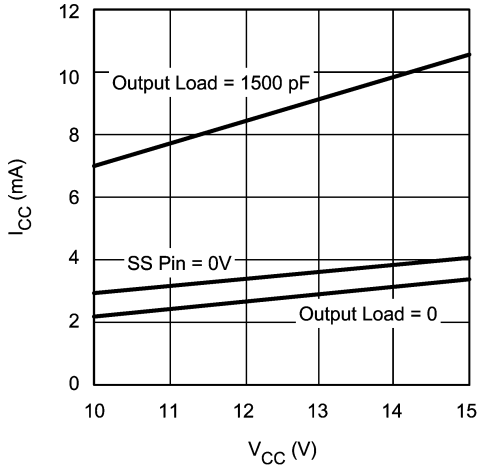
I_{CC} vs V_{CC}
(V_{CC} Powered Externally)



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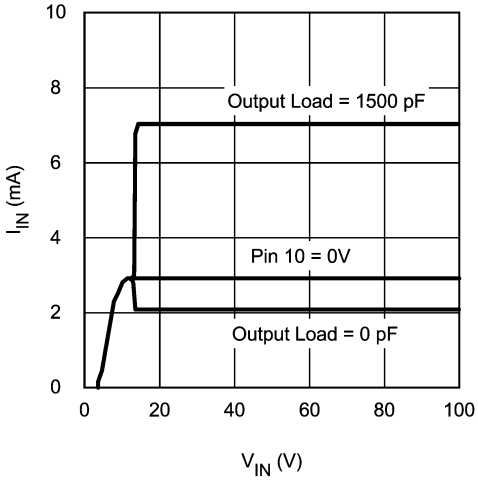
I_{IN} vs V_{IN}
(V_{CC} Not Powered Externally)



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Functional Description

The LM5033 High Voltage PWM controller contains all of the features needed to implement Push-Pull and Bridge topologies, using voltage-mode control in a small 10 pin package. Features included are: startup regulator, precision 2.5V reference output, current limit detection, alternating gate drivers, sync capability, thermal shutdown, softstart, and remote shutdown. This high speed IC has total propagation delays <100 ns. These features simplify the design of an open loop DC-DC converter, or a voltage controlled closed loop converter. The Functional Block Diagram is shown in *Figure 1*.

High Voltage Start-Up Regulator (Pins 1, 4)

The LM5033 contains an internal high voltage startup regulator. The input pin (V_{IN}) can be connected directly to line voltages as high as 90V for normal operation, and can withstand transients to 100V. The regulator output at V_{CC} (9.6V) is internally current limited and sources a minimum of 20mA. Upon power up, the capacitor at V_{CC} will charge up, providing a time delay while internal circuits stabilize. When V_{CC} reaches the upper threshold of the under-voltage sensor (typically 9.5V), the under-voltage sensor resets, enabling the output drivers, although the PWM duty cycle will initially be at zero. As the Softstart capacitor then charges up (described below) the output duty cycle will increase until regulated by the PWM control loop. The value of the V_{CC} capacitor which affects the above mentioned delay depends on the total system design and its start-up characteristics. The recommended range of values for the V_{CC} capacitor is 0.1 to 50µF.

The lower threshold of the under-voltage sensor is typically at 6.8V. If V_{CC} falls below this value the outputs are disabled and the softstart capacitor is discharged. When V_{CC} is again increased above the upper threshold the outputs are enabled, and the softstart sequence repeats.

The LM5033's internal power dissipation can be reduced by powering V_{CC} from an external supply. Typically this is done by means of an auxiliary transformer winding which is diode connected to the V_{CC} pin to provide 10-15V to V_{CC} as the controller completes the start-up sequence. The externally applied V_{CC} voltage will cause the internal regulator to shut off. The under-voltage sensor circuit will still function in this mode, requiring that the external V_{CC} capacitor be sized so that V_{CC} never falls below 6.8V. The required current into the V_{CC} pin from the external source is shown in Typical Performance Characteristics (I_{CC} vs. V_{CC}).

If a fault condition occurs such that the external supply to V_{CC} fails, external current draw from the V_{CC} pin must be limited as to not exceed the regulator's current limit, or the maximum power dissipation of the IC. An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{IN} pins together and feeding the external bias voltage (10-15V) into that node.

A thermal shutdown protection will activate if the die temperature exceeds 165°C, disabling the outputs (OUT1 and OUT2), and shutting down the V_{CC} regulator. When the die temperature has reduced below 150°C (typical hysteresis = 15°C) the V_{CC} regulator is enabled and a softstart sequence will initiate.

Reference (Pin 2)

The Ref pin provides a reference voltage of 2.5V, ±2.4%. The pin is internally connected to an NMOS FET drain at the buffer amplifier's output, allowing it to sink, but not source current. An external pullup resistor is required. Current into the pin must be limited to less than 20 mA to maintain regulation. See the graph in the Typical Performance Characteristics.

During start-up if the pullup voltage is present before the reference amplifier establishes regulation, the voltage on pin 2 must not exceed 5.5V. If this reference is not used the Ref pin can float or be connected to ground.

PWM Comparator (Pin 3), Duty Cycle and Deadtime

The PWM comparator compares an internal ramp signal (0 - 0.65V) with the loop error voltage derived from the Comp pin (pin 3). The Comp voltage is typically set by an external error amplifier through an optocoupler for closed loop applications. Internally, the voltage at the Comp pin passes through two level shifting diodes, and a gain reducing 3:1 resistor divider. The output of the PWM comparator provides the pulse width information to the output drivers (Out1 and Out2). This comparator is optimized for speed in order to achieve minimum discernable duty cycles. The output duty cycle is 0% for V_{COMP} < 1.5V, and maximum for V_{COMP} > 3.5V. See the Typical Performance Characteristics. The maximum duty cycle for each output is limited to less than 50% due to the forced deadtime. The typical deadtime between the falling edge of one gate driver output and the rising edge of the other gate driver output is 135 ns, and does not vary with frequency. The maximum duty cycle for each output can be calculated from:

$$DC = \frac{(0.5 \times T_S) - T_D}{T_S}$$

where T_S is the period of each output, and T_D is the deadtime. For example, if the oscillator frequency is 200 kHz, each output will cycle at 100 kHz, and T_S = 10 µs. Using the nominal deadtime of 135 ns, the maximum duty cycle at this frequency is 48.65%. Using the minimum deadtime of 85 ns, the maximum duty cycle increases to 49.15%.

When the Softstart pin (pin 10) is pulled down (internally or externally) the Comp pin voltage is pulled down with it, with a difference of 0.5V. When the Softstart pin voltage increases the Comp voltage is allowed to increase, pulled up by an internal 5.2V supply through a 5kΩ resistor.

In an open loop application, such as an intermediate bus converter, pin 3 can be left open resulting in maximum duty cycle at the output drivers .

Current Sense (Pin 8)

The current sense circuit is intended to protect the power converter when an abnormal primary current is sensed by initiating a low duty cycle hiccup mode. When the threshold (0.5V) at Pin 8 is exceeded the outputs are disabled, and the softstart capacitor (at pin 10) is internally discharged. When the softstart capacitor is fully discharged **and** the voltage at the CS pin is below 0.5V, the outputs are re-enabled allowing the softstart capacitor voltage and the output duty cycle to increase.

Current Sense (Pin 8) (Continued)

The external current sensing circuit should include an RC filter located near the IC to prevent false triggering of the Current Sense comparator due to transients or noise. An internal MOSFET discharges the external filter capacitor at the conclusion of each PWM cycle to improve dynamic performance. The discharge time is equal to the deadtime between Out1 and Out2 at maximum duty cycle. Additionally, pin 8 is pulled low when V_{CC} is below the under-voltage threshold or when an over temperature condition occurs.

Oscillator, Sync Capability (Pin 9)

The LM5033 oscillator frequency is set by a single external resistor connected between Rt/Sync and ground. The required Rt resistor is calculated from:

$$Rt = \frac{(1/F) - 172^{*}10^{-9}}{182^{*}10^{-12}}$$

The outputs (Out1 and Out2) alternate at half the oscillator frequency. The voltage at the Rt/Sync pin is internally regulated to a nominal 2.0V. The Rt resistor should be located as close as possible to the IC, and connected directly to the pins (Rt and GND).

The LM5033 can be synchronized to an external clock by applying a narrow pulse to pin 9. The external clock must be a higher frequency than the free running frequency set by the Rt resistor, and the pulse width must be between 15 and 150 ns. The clock signal must be coupled into the Rt/Sync pin through a 100 pF capacitor. When the synchronizing pulse transitions low-to-high, the voltage at pin 9 must exceed 3.8V from its nominal 2.0V dc level. During the clock signal's low time the voltage at pin 9 will be clamped at 2.0V by an internal regulator. The Rt resistor is always required, whether the oscillator is free running or externally synchronized.

Soft Start (Pin 10)

The softstart feature allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turn-on, after the under-voltage sensor resets at V_{CC}, an internal 10 µA current source charges an external capacitor at pin 10 to generate a ramping voltage (0 to + 5V) which allows the voltage on the Comp pin (pin 3) to increase gradually. As the COMP voltage increases the output duty cycle will increase from zero to the value required for regulation. Internally, the softstart pin is pulled low when a current fault is detected at pin 8, the V_{CC} voltage is below the lower threshold of the under-voltage sensor, or when a thermal shutdown occurs. Additionally, the softstart pin can be pulled low by an external device.

In the event of a current fault, (see Current Sense section) the softstart capacitor will be discharged by an internal pull-down device. The falling voltage at pin 10 will pull down the COMP pin, thereby ensuring a minimum output duty cycle when the outputs are re-enabled. The softstart capacitor will then begin to ramp up, allowing the COMP voltage to increase. As the COMP voltage increases, the output duty cycle increases from zero to the value required for regulation. However, if the fault condition is still present the above sequence repeats until the fault is removed.

If the V_{CC} voltage falls below the lower under-voltage sensor threshold (typically 6.8V) the outputs are disabled, and the softstart capacitor is discharged. The falling voltage at pin 10 will pull down the COMP pin, thereby ensuring minimum output duty cycle when the outputs are re-enabled. After the V_{CC} voltage increases above the upper threshold (typically 9.5V), the outputs are enabled, and the softstart capacitor will begin to ramp up, allowing the COMP pin voltage to increase. The output duty cycle will then increase from zero to the value required for regulation.

In the event of a fault which results in an excessively high die temperature, an internal Thermal Shutdown circuit is provided to protect the IC. When activated (at 165˚C) the IC is forced into a low power reset state, disabling the output drivers and the V_{CC} regulator. When the die temperature has reduced (typical hysteresis = 15˚C), the V_{CC} regulator is enabled and a softstart sequence will initiate.

Using an externally controlled switch, the outputs (Pins 5 & 6) can be disabled at any time by pulling pin 10 below 0.5V. This will pull down the COMP pin to near ground, causing the output duty cycle to go to zero. Upon releasing pin 10, the softstart capacitor will ramp up, allowing the COMP pin voltage to increase. The output duty cycle then increases from zero to the value required for regulation.

OUT1, OUT2 (Pins 5, 6)

The LM5033 provides two alternating outputs, OUT1 and OUT2, each capable of sourcing and sinking 1.5A peak. Each will toggle at one-half the internal oscillator frequency. The voltage output levels are nominally ground and V_{CC}, minus a saturation voltage at each level which depends on the current flow.

The outputs can drive power MOSFETs directly in a push-pull application, or they can drive a high voltage gate driver (e.g., LM5100) in a bridge application.

The outputs are disabled when any of the following conditions occur:

1. An overcurrent condition is detected at pin 8,
2. The V_{CC} under-voltage sensor is active,
3. An over-temperature condition is detected, or
4. The voltage at Pin 10 is below 0.5V

Thermal Protection

The system design should limit the LM5033 junction temperature to not exceed 125˚C during normal operation. However, in the event of a fault which results in a higher die temperature, an internal Thermal Shutdown circuit is provided to protect the IC. When thermal shutdown is activated, typically at 165˚C, the IC is forced into a low power reset state disabling the output drivers and the V_{CC} regulator. This feature helps prevent catastrophic failures from accidental device overheating. When the die temperature has reduced (typical hysteresis = 15˚C) the V_{CC} regulator is enabled and a softstart sequence initiates.

Application Information

The following information is intended to provide guidelines for implementing the LM5033. However, final selection of all external components is dependent on the configuration and operating characteristics of the complete power conversion system.

Application Information (Continued)

V_{IN} (PIN 1)

The voltage applied at pin 1, normally the same as that applied to the main transformer's primary, can be in the range of 15 to 90V, with transient capability to 100V. The current into pin 1 depends not only on V_{IN}, but also on the load on the output driver pins, any load on V_{CC}, and whether or not an external voltage is applied to V_{CC}. If Vin is close to the absolute maximum rating of the LM5033, it is recommended the circuit of Figure 2 be used to filter transients which may occur at the input supply.

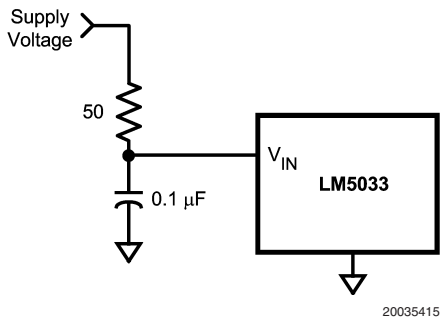


FIGURE 2. Input Transient Protection

If V_{CC} is not powered externally, requiring all internal bias currents for the LM5033, and output driver currents, to be supplied at Vin and through the internal regulator, the required input current (Iin) is shown in the Typical Performance Characteristics (I_{IN} vs. V_{IN}).

If V_{CC} is powered externally, Iin will increase with V_{IN} as shown in the above mentioned graph until the external voltage is applied to V_{CC}. In most applications, this occurs once the outputs are enabled and load current begins to flow. The current into Vin will then drop to a nominal 150µA (Pin 10 = open or grounded).

V_{CC} (PIN 4)

The capacitor at the V_{CC} pin provides not only noise filtering and stability, but also a necessary time delay during start-up. The time delay allows the internal circuitry of the LM5033, and associated external circuitry, to stabilize before V_{CC} reaches its final value, at which time the outputs are enabled and the softstart sequence begins. Any external circuitry connected to the REF output (Pin 2) and Softstart (Pin 10) should be designed to stabilize during the time delay.

The current limit of the V_{CC} regulator, and the external capacitor, determine the V_{CC} turn-on time delay. Typically, a 1µF capacitor will provide approximately 300 µs of delay, with larger capacitors providing proportionately longer delays. Experimentation with the final design may be necessary to determine the minimum value for the V_{CC} capacitor.

SOFTSTART (PIN 10)

The capacitor at pin 10 determines the time required for the output duty cycle to increase from zero to the final value for regulation. The minimum acceptable time is dependent on the response of the feedback loops to the COMP pin, as well as the characteristics of the magnetic components. If the Softstart time is too quick, the system output could significantly overshoot its intended voltage before the loop has a chance to establish regulation, possibly adversely affecting the load. Experimentation with the final design is usually necessary to determine the minimum value for the SS capacitor.

CURRENT SENSE (PIN 8)

This pin typically receives an input representative of the primary current from the current sense elements of the external circuitry. The peak amplitude at this pin must be less than 0.5V for normal operation. Filtering at this pin should be sufficient to prevent false triggering of the Current Sense comparator, but not significantly delay detection of an overcurrent condition. The filter's capacitor at pin 8 should not be larger than 2200 pF.

OSCILLATOR, SYNC INPUT (PIN 9)

The internal oscillator frequency is generally selected in conjunction with the system magnetic components, and any other aspects of the system which may be affected by the frequency. The R_t resistor at pin 9 sets the frequency according to the formula in the Functional Description. Each output (OUT1 and OUT2) switches at half the oscillator frequency. If the required frequency value is critical in a particular application, the tolerance of the external resistor, and the frequency tolerance indicated in the Electrical Characteristics, must be taken into account when selecting the resistor.

If the LM5033 is to be synchronized to an external clock, that signal must be coupled into pin 9 through a 100 pF capacitor. The R_t resistor is still required in this case, and it must be selected to set the internal oscillator to a frequency lower than the external synchronizing frequency. The amplitude of the external pulses must take pin 9 above 3.8V on the low-to-high transition but no higher than 5.5V. The clock pulse width should be between 15 and 150 ns.

DEADTIME ADJUSTMENT

If the application requires a change in the minimum deadtime between the outputs, the circuits in *Figure 3* are recommended. Suggested values for the resistor and capacitor at each output are 500Ω, and 100 pF, respectively for a nominal 50 ns change. The diodes can be 1N4148, or similar.

Application Information (Continued)

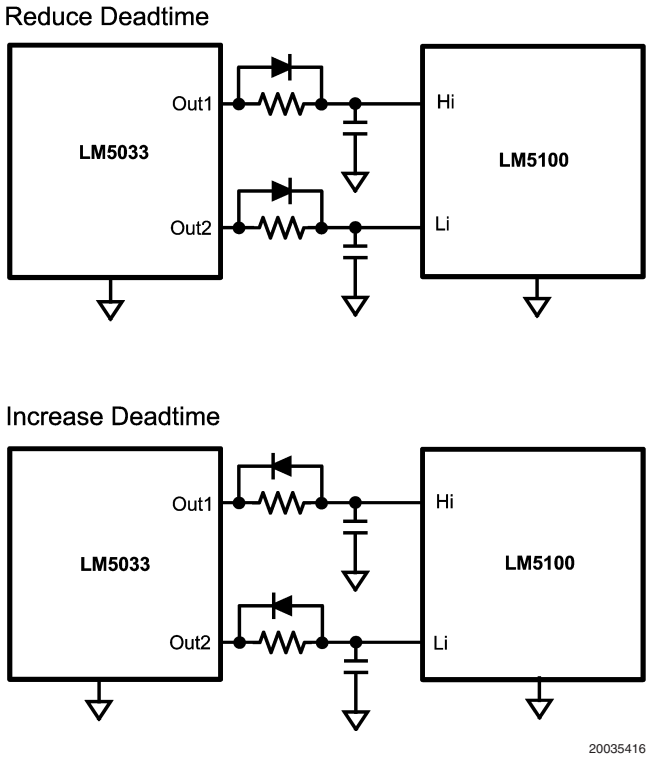


FIGURE 3. Deadtime Adjustment

PC BOARD LAYOUT

The LM5033 current sense and PWM comparators are very fast, and as such will respond to short duration noise pulses. Layout considerations are critical for the current sense filter. The components at pins 3, 8, 9, and 10 should be as physically close as possible to the IC, thereby minimizing noise pickup in the PC tracks.

If a current sense transformer is used both leads of the transformer secondary should be routed to the sense filter components, and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board track to pin 7 of the IC rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor sources, a low inductance resistor should be used. In this case all the noise sensitive low power grounds should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

The outputs of the LM5033, or of the high voltage gate driver (if used), should have short direct paths to the power MOSFETs in order to minimize the effects of inductance in the PC board traces.

If the internal dissipation of the LM5033 and any of the power devices produces high junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the LLP-10 package can be soldered to ground plane on the PC board, and the ground plane should extend out from beneath the IC to help dissipate the heat. The exposed pad is internally connected to the IC substrate.

Additionally, the use of wide PC board traces where possible can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

APPLICATION CIRCUIT EXAMPLE

Figure 6 shows an example circuit for a half-bridge 200W DC/DC converter built in a quarter brick format. The circuit is that of an intermediate bus converter (IBC) which operates open-loop (unregulated output), converting a nominal 48V input to a nominal 9.0V output with a 30 mΩ output impedance. The current sense transformer (T2), and the associated filter at the CS pin, provide overcurrent detection at approximately 23A. The auxiliary winding on T1 powers V_{CC} and the LM5100's V+ pin (once the outputs are enabled) to reduce power dissipation within the LM5033. The LM5100 provides appropriate level shifting for Q1. Synchronous rectifiers Q3 and Q4 minimize conduction losses in the output stage. Dual comparators U2 and U3 provide under-voltage and over-voltage sensing at Vin. The under-voltage sense levels are 37V increasing, and 33V decreasing. The over-voltage sense levels are 63V increasing, and 61.5V decreasing. The circuit can be shut down by taking the ON/OFF input below 0.8V. An external synchronizing frequency can be applied to the SYNC input. Measured efficiency and output characteristics for this circuit are shown in *Figure 4* and *Figure 5*.

Application Information (Continued)

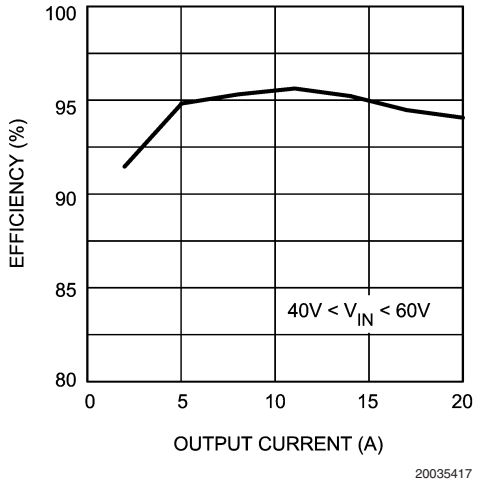


FIGURE 4. Efficiency vs Output Current
Circuit of *Figure 6*

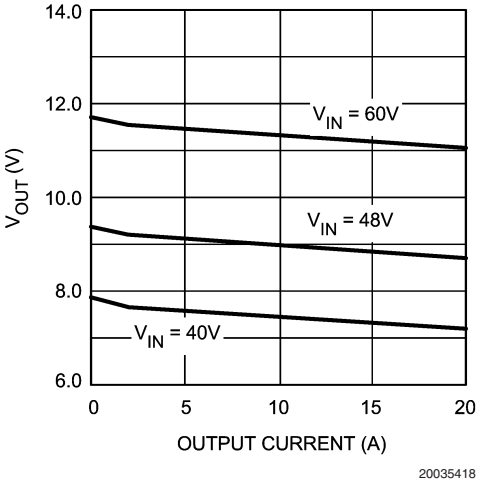


FIGURE 5. V_{OUT} vs Load Current and V_{IN}
for the circuit of *Figure 6*

Application Information (Continued)

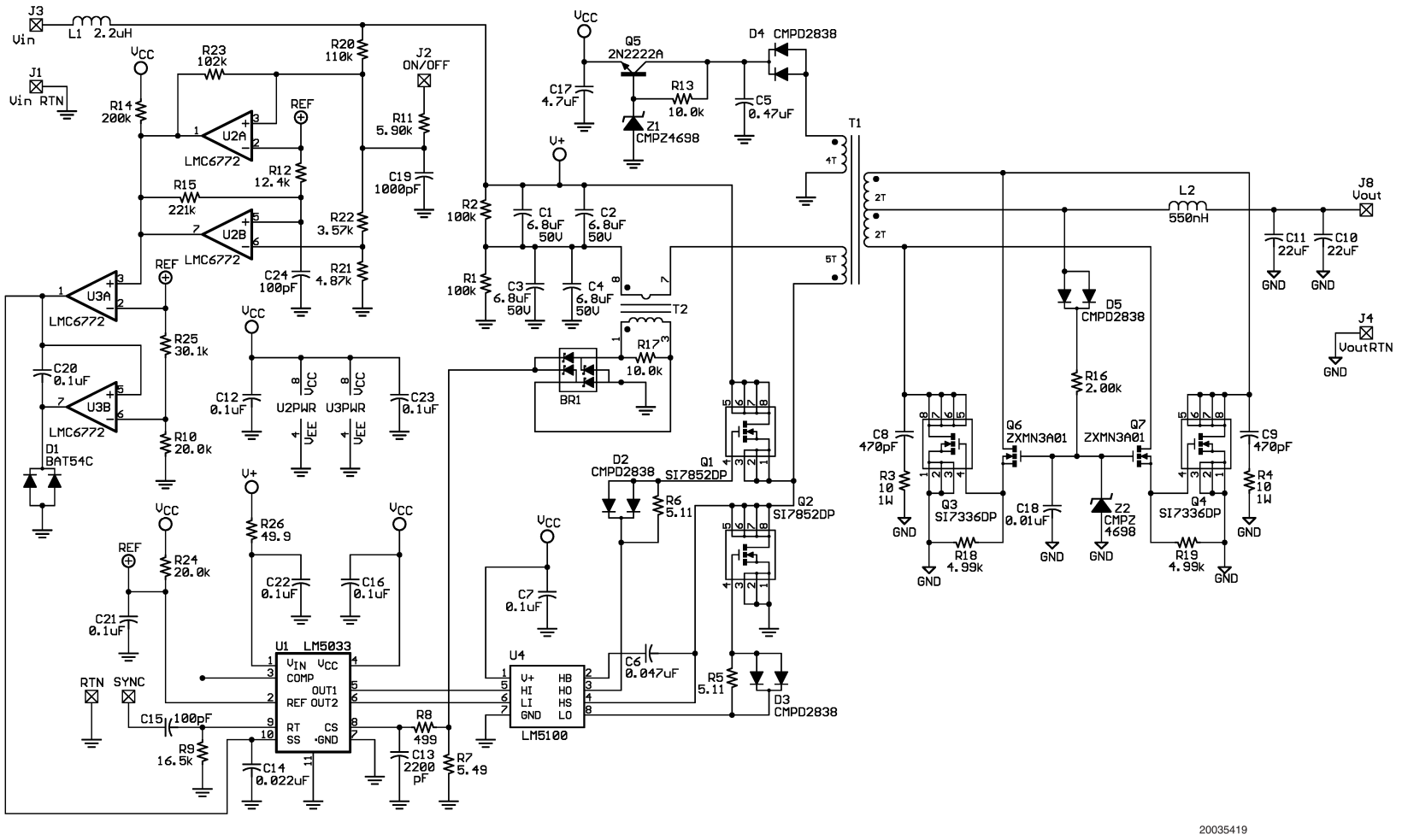


FIGURE 6. Intermediate Bus Converter
40V - 60V Input; 7.5 - 11.3V, 20A Output

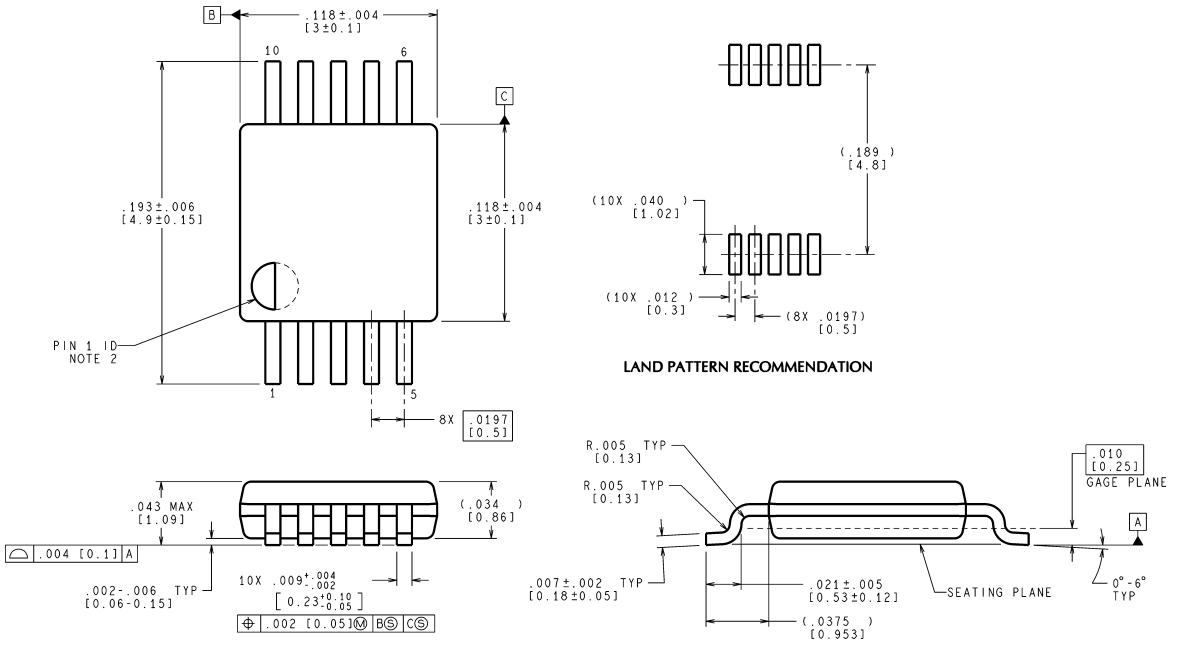
Bill of Materials (for the circuit of *Figure 6*)

Item	Device	Package	Value
BR1	Schottky diode bridge, Diodes, Inc. BAT54BRW	SOT-363	30V, 0.2A
C1-4	Capacitor	1812	6.8 µF, 50V
C5	Capacitor	0805	0.47 µF, 25V
C6	Capacitor	0805	0.047 µF, 25V
C7, 12, 16, 20-23	Capacitor	0805	0.1 µF, 16V
C8, 9	Capacitor	0805	470 pF, 50V
C10, 11	Capacitor	1210	22 µF, 16 V
C13	Capacitor	0805	2200 pF, 16V
C14	Capacitor	0805	0.022 µF. 16V
C15, 24	Capacitor	0805	100 pF, 16V
C17	Capacitor	1206	4.7 µF, 16V
C18	Capacitor	0805	0.01 µF, 16V
C19	Capacitor	0805	1000 pF, 16V
D1	Dual Schottky diode, Vishay BAT54C	SOT-23	30V, 0.2A
D2-5	Dual diode, Central Semi CMPD2838	SOT-23	75V, 0.2A
L1	Inductor, TDK RLF7030T-2R2M5R4	SMD	2.2 µH, 5.5A
L2	Inductor, TDK SPM12535T-R60M220	SMD	550 nH, 22A
Q1, 2	N Channel MOSFET, Vishay Si7852DP	PowerPAK SO-8	80V, 12.5A
Q3, 4	N Channel MOSFET, Vishay Si7336DP	PowerPAK SO-8	30V, 30A
Q5	NPN 2N2222A Transistor	SOT-23	75V, 0.6A
Q6, 7	N Channel MOSFET, Zetex ZXMN3A01	SOT-23	30V, 2 A
R1, 2	Resistor	1206	100 kΩ, 1/4W
R3, 4	Resistor	2512	10Ω, 1W
R5, 6	Resistor	0805	5.11Ω
R7	Resistor	0805	5.49Ω
R8	Resistor	0805	499Ω
R9	Resistor	0805	16.5 kΩ
R10, 24	Resistor	0805	20 kΩ
R11	Resistor	0805	5.9 kΩ
R12	Resistor	0805	12.4 kΩ
R13, 17	Resistor	0805	10 kΩ
R14	Resistor	0805	200 kΩ
R15	Resistor	0805	221 kΩ
R16	Resistor	0805	2.0 kΩ
R18, 19	Resistor	0805	4.99 kΩ
R20	Resistor	1206	110 kΩ, 1W
R21	Resistor	0805	4.87 kΩ

Bill of Materials (for the circuit of *Figure 6*) (Continued)

Item	Device	Package	Value
R22	Resistor	0805	3.57 kΩ
R23	Resistor	0805	102 kΩ
R25	Resistor	0805	30.1 kΩ
R26	Resistor	0805	49.9 Ω
T1	Power Transformer, Coilcraft B0853-A	Planar	
T2	Current sense transformer, Pulse Eng. P8208	SMD	100:1, 10A
U1	PWM Controller, National Semi LM5033D	LLP-10	
U2, 3	Dual Micropower Comparator, Nat'l Semi LMC6772	Mini SO-8	
U4	Gate driver, National Semi LM5100M	SO-8	
Z1, 2	Zener diode, Central Semi CMPZ4698	SOT-23	11V, 350 mW

Physical Dimensions inches (millimeters)
unless otherwise noted



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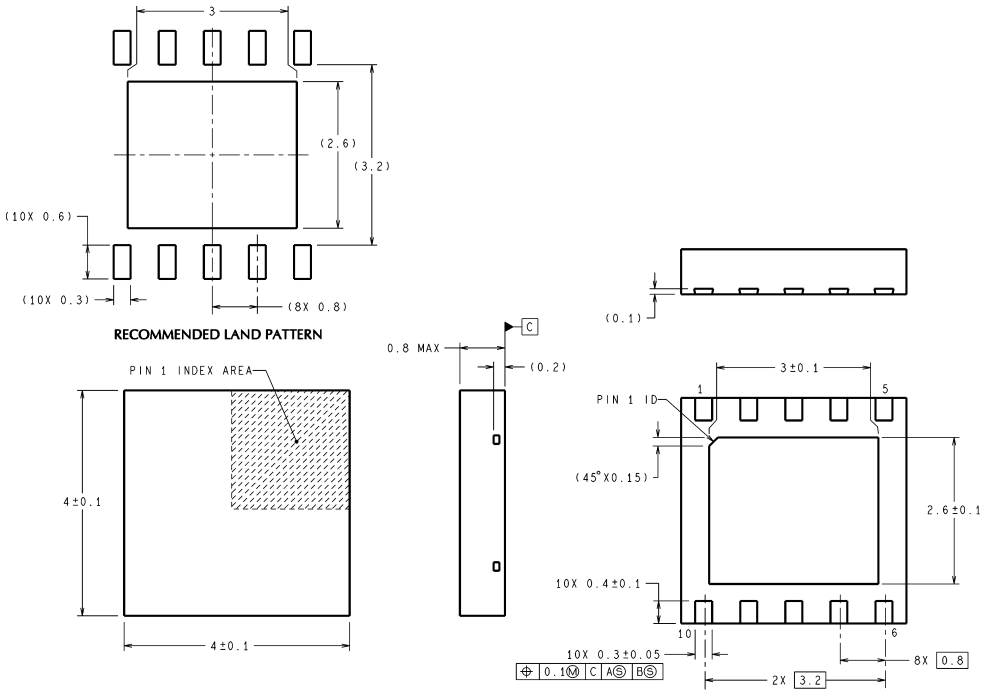
MUB10A (Rev B)

10-Lead MSOP Package
NS Package Number MUB10A



SDC10A (Rev A)

10-Lead LLP Plastic Dual Package
NS Package Number SDC10A

Notes

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