LM48560

LM48560 High Voltage Class H Ceramic Speaker Driver with Automatic Level Control

Literature Number: SNAS513B

November 10, 2011

LM48560

Boomer® Audio Power Amplifier Series

High Voltage Class H Ceramic Speaker Driver with Automatic Level Control

General Description

The LM48560 is a high voltage, high efficiency, Class H driver for ceramic speakers and piezo actuators. The LM48560's Class H architecture offers significant power savings compared to traditional Class AB amplifiers. The device provides $30V_{P-P}$ output drive while consuming just 4mA of quiescent current from a 3.6V supply.

The LM48560 features National's unique automatic level control (ALC) that provides output limiter functionality. The LM48560 features two fully differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I²C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs.

The LM48560 has a low power shutdown mode that reduces quiescent current consumption to 0.1µA. The LM48560 is a available in an ultra-small 16–bump micro SMD package (1.97mm x 1.97mm).

Key Specifications

- Output Voltage at V_{DD} = 3.6V
  R_L = 1.5µF+10Ω, THD+N ≤ 1% — $30V_{P-P}$ (typ)
- Quiescent Power Supply Current at 3.6V (ALC enabled) — 4mA (typ)
- Power Dissipation at $25V_{P-P}$ — 1W (typ)
- Shutdown current — 0.1µA (typ)

Features

- Class H Topology
- Integrated Boost Converter
- Bridge-Tied Load (BTL) Output
- Selectable Differential Inputs
- Selectable Control Interfaces (Hardware or Software mode)
- I²C Programmable ALC
- Low Supply Current
- Minimum External Components
- Micro-Power Shutdown
- Available in Space-Saving micro SMD Package

Applications

- Touch screen Smart Phones
- Tablet PCs
- Portable Electronic Devices
- MP3 Players

Typical Application

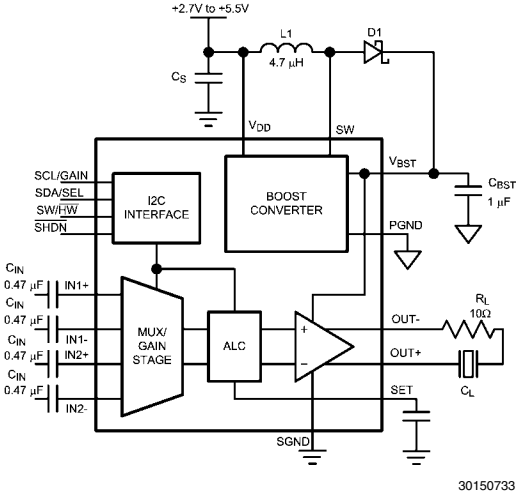

FIGURE 1. Typical Application Circuit

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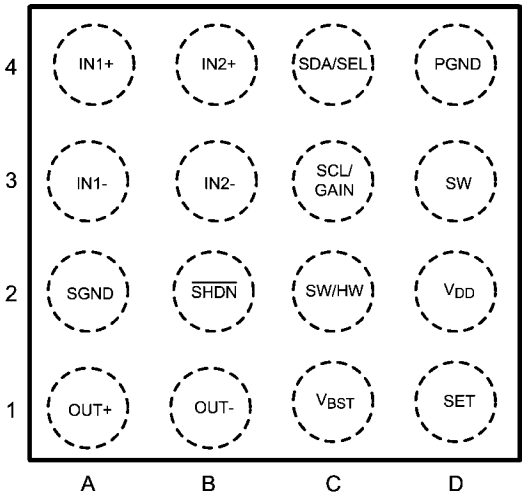
Connection Diagrams

TL Package
1.97mm x 1.97mm x 0.6mm



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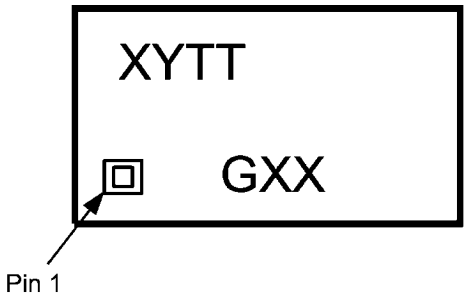
Top View
Order Number LM48560TL
See NS Package Number TLA16Z1A

16–Bump micro SMD Marking



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Top View
XY = Date code
TT = Die traceability
G = Boomer Family
XX = LM48560TL

Ordering Information

Ordering Information Table

Order Number	Package	Package Drawing Number	Transport Media	MSL Level	Green Status
LM48560TL	16 Bump µSMD	TLA16Z1A	250 units on tape and reel	1	RoHS & no Sb/Br
LM48560TLX	16 Bump µSMD	TLA16Z1A	2500 units on tape and reel	1	RoHS & no Sb/Br

TABLE 1. Bump Descriptions

Bump	Name	Description
A1	OUT+	Amplifier Non-Inverting Output
A2	SGND	Amplifier Ground
A3	IN1–	Amplifier Inverting Input 1
A4	IN1+	Amplifier Non-Inverting Input 1
B1	OUT-	Amplifier Inverting Output
B2	$\overline{SHDN}$	Active Low Shutdown. Connect $\overline{SHDN}$ to GND to disable device. Connect $\overline{SHDN}$ to V_{DD} for normal operation
B3	IN2–	Amplifier Inverting Input 2
B4	IN2+	Amplifier Non-Inverting Input 2
C1	V_{BST}	Boost Converter Output
C2	SW/$\overline{HW}$	Mode Selection Control: SW/$\overline{HW}$ = 0 → Hardware Mode SW/$\overline{HW}$ = 1 → Software Mode
C3	SCL/GAIN	I²C Serial Clock Input (Software Mode) Gain Select Input (Hardware Mode) see (*Table 3*)
C4	SDA/SEL	I²C Serial Data Input (Software Mode) Amplifier Input Select (Hardware Mode) see (*Table 3*)
D1	SET	ALC Timing Input
D2	V_{DD}	Power Supply
D3	SW	Boost Converter Switching Node
D4	PGND	Boost Converter Ground

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 1)	6V
SW Voltage	25V
V_{BST} Voltage	21V
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Rating, Human Body Model (Note 4)	2kV
ESD Rating, Machine Model (Note 5)	100V
ESD Rating, Charge Device Model (Note 6)	500V
Storage Temperature	−65°C to + 150°C
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (TLA16Z1A)	55 °C/W
Soldering Information	
See AN-1112 "Micro SMD Wafer Level Chip Scale Package."	

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	
V_{DD}	$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 3.6V (Note 1, Note 2)

The following specifications apply for R_L = 1.5µF + 10Ω, C_{BST} = 1µF, C_{IN} = 0.47µF, A_V = 24dB unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48560 Min (Note 8)	LM48560 Typ (Note 7)	LM48560 Max (Note 8)	Units (Limits)
V_{DD}	Supply Voltage Range		2.7		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = ∞				
		ALC Enabled		4	6	mA
		ALC Disabled		3.6		mA
P_D	Power Consumption	V_{OUT} = 25V_{P-P}, f = 1kHz		1		W
I_{SD}	Shutdown Current	Software Mode		2.5	4.4	µA
		Hardware Mode		0.1	2	µA
T_{WU}	Wake-up Time	From Shutdown		15		ms
V_{OS}	Differential Output Offset Voltage	A_V = 24V		10	90	mV
		A_V = 0dB (Boost Disabled)		5	20	mV
A_V	Gain (Hardware Mode)	IN1				
		GAIN = 0	0.5	0	0.5	dB
		GAIN = 1	5.5	6	6.5	dB
		IN2				
		GAIN = 0	23.5	24	24.5	dB
		GAIN = 1	29.5	30	30.5	dB
	Gain (Software Mode)	Boost Disabled				
		GAIN1 = 0, GAIN0 = 0	−0.5	0	0.5	dB
		GAIN1 = 0, GAIN0 = 1	5.5	6	6.5	dB
		GAIN1 = 1, GAIN0 = 0	11.5	12	12.5	dB
		GAIN1 = 1, GAIN0 = 1	17.5	18	18.5	dB
		Boost Enabled				
		GAIN1 = 0, GAIN0 = 0	20.5	21	21.5	dB
		GAIN1 = 0, GAIN0 = 1	23.5	24	24.5	dB
		GAIN1 = 1, GAIN0 = 0	26.5	27	27.5	dB
		GAIN1 = 1, GAIN0 = 1	29.5	30	30.5	dB
	Gain Step Size (Software Mode)			3		dB
R_{IN}	Input Resistance	A_V = 0dB	46	50	58	kΩ
		A_V = 30dB	46	50	58	kΩ

Symbol	Parameter	Conditions	LM48560			Units (Limits)
			Min (Note 8)	Typ (Note 7)	Max (Note 8)	
V_{OUT}	Output Voltage	THD+N = 1%				
		f = 200Hz		30		V_{P-P}
		f = 1kHz	25	30		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 18V_{P-P}, f = 1kHz		0.08		%
PSRR	Power Supply Rejection Ratio (Figure 2)	V_{DD} = 3.6V + 200mV_{P-P} sine, Inputs = AC GND				
		f_{RIPPLE} = 217Hz	55	78		dB
		f_{RIPPLE} = 1kHz		76		dB
CMRR	Common Mode Rejection Ratio (Figure 3)	V_{CM} = 200mV_{P-P} sine				
		f_{RIPPLE} = 217Hz		68		dB
		f_{RIPPLE} = 1kHz		78		dB
SNR	Signal-to-Noise-Ratio	Boost Disabled, A-weighted		107		dB
		Boost Enabled A-weighted		98		dB
ε_{OS}	Output Noise	A-weighted				
		A_V = 24dB		134		μV_{RMS}
		A_V = 0dB (Boost Disabled)		16		μV_{RMS}
T_A	Attack Time	ATK1:ATK0 = 00		0.75		ms
T_R	Release time	RLT1:RLT0 = 00		1		s
f_{SW}	Boost Converter Switching Frequency			2		MHz
I_{LIMIT}	Boost Converter Current Limit			1.5		A
V_{IH}	Logic High Input Threshold	$\overline{SHDN}$	1.4			V
V_{IL}	Logic Low Input Threshold	$\overline{SHDN}$			0.5	V
I_{IN}	Input Leakage Current	$\overline{SHDN}$		0.1	0.2	µA

I²C Interface Characteristics (Note 1, Note 2)

The following specifications apply for R_{PU} = 1kΩ to V_{DD}, SW/$\overline{HW}$ = 1 (Software Mode) unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48560			Units (Limits)
			Min (Note 7)	Typ (Note 6)	Max (Note 7)	
V_{IH}	Logic Input High Threshold	SDA, SCL	1.1			V
V_{IL}	Logic Input Low Threshold	SDA, SCL			0.5	V
	SCL Frequency				400	kHz
t_1	SCL Period		2.5			µs
t_2	SDA Setup Time		250			ns
t_3	SDA Stable Time		250			ns
t_4	Start Condition Time		250			ns
t_5	Stop Condition Time		250			ns

Note 1: "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Charge device model, applicable std. JESD22-C101-C.

Note 7: Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

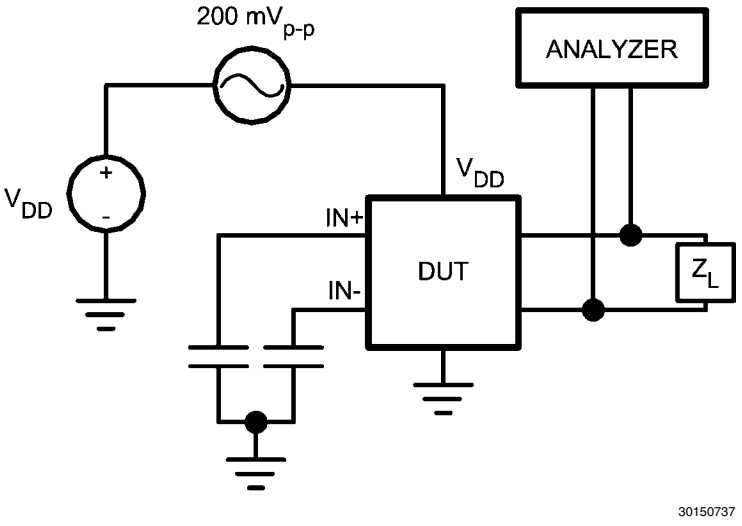


FIGURE 2. PSRR Test Circuit

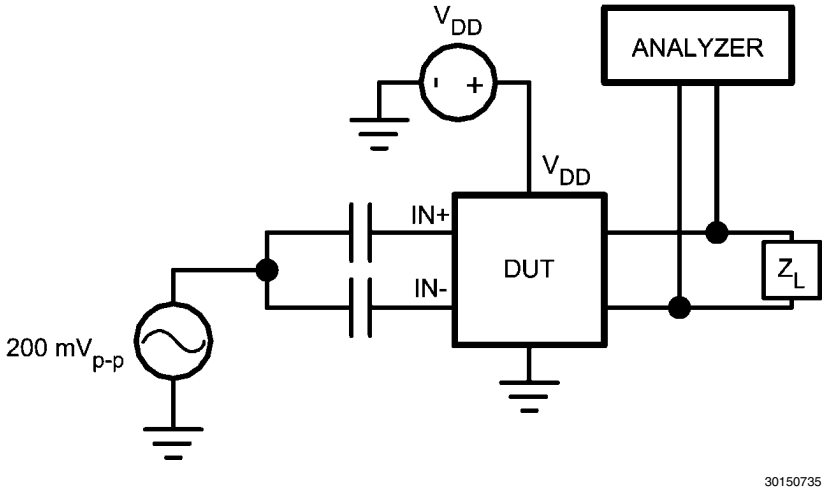
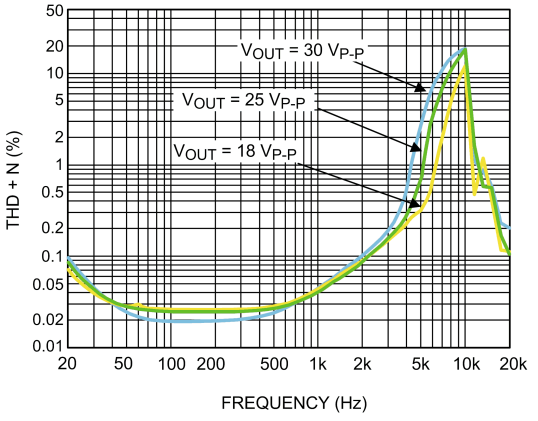


FIGURE 3. CMRR Test Circuit

Typical Performance Characteristics

All typical performance curves are taken with conditions seen in *Figure 1* (Typical Application Circuit), unless otherwise specified.

THD+N vs FREQUENCY
C_L = 0.6µF, V_{DD} = 3.6V, Boosted, A_V = 24dB



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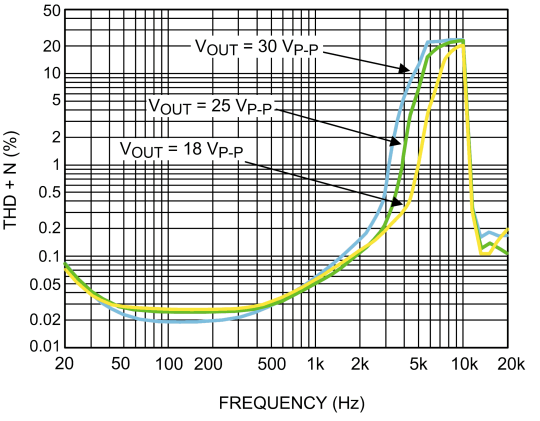
THD+N vs FREQUENCY
C_L = 1.0µF, V_{DD} = 3.6V, Boosted, A_V = 24dB



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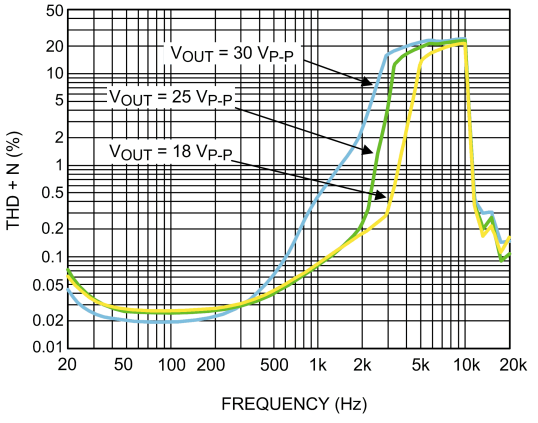
THD+N vs FREQUENCY
C_L = 1.5µF, V_{DD} = 3.6V, Boosted, A_V = 24dB



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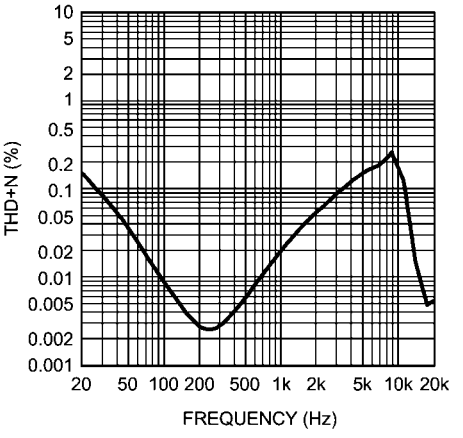
THD+N vs FREQUENCY
V_{DD} = 3.6V, C_L = 0.6µF, V_{OUT} = 5V_{P-P}
Unboosted, A_V = 0dB



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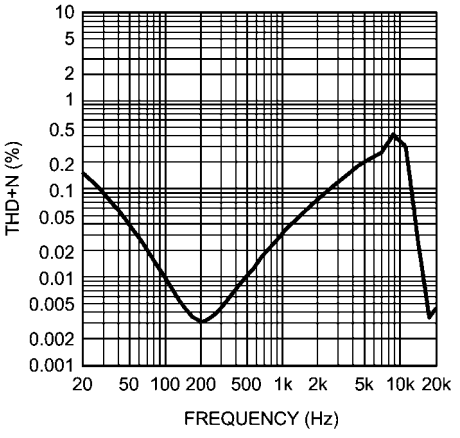
THD+N vs FREQUENCY
V_{DD} = 3.6V, C_L = 1µF, V_{OUT} = 5V_{P-P}
Unboosted , A_V = 0dB



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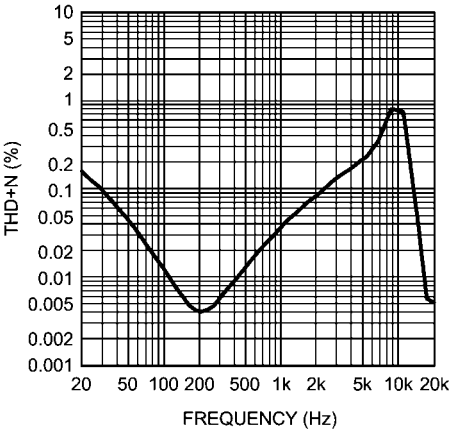
THD+N vs FREQUENCY
V_{DD} = 3.6V, C_L = 1.5µF, V_{OUT} = 5V_{P-P}
Unboosted, A_V = 0dB



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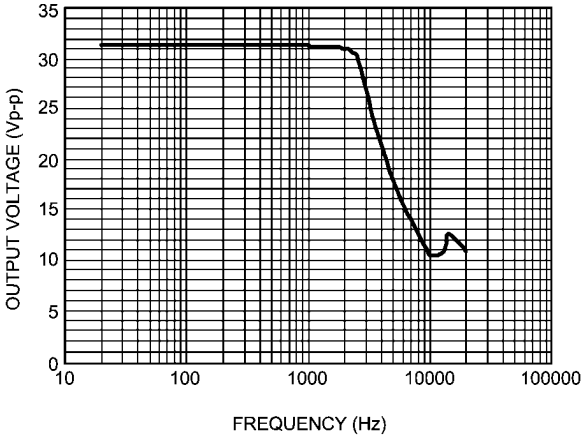
OUTPUT VOLTAGE vs FREQUENCY
C_L = 1.5µF, THD+N ≤ 1%, Boosted



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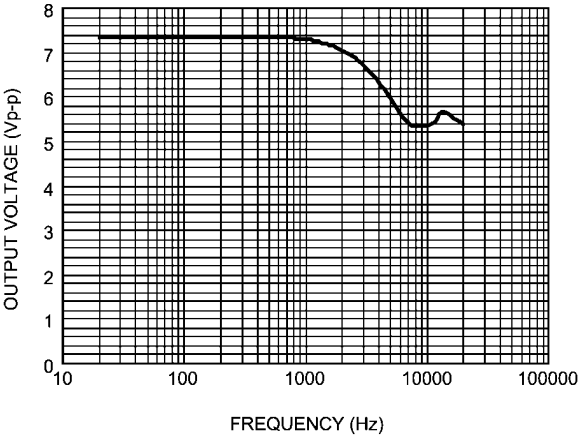
OUTPUT VOLTAGE vs FREQUENCY
C_L = 1.5µF, THD+N ≤ 1%, Unboosted



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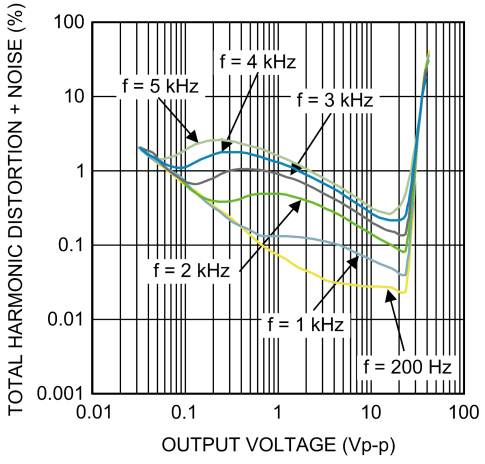
THD+N vs OUTPUT VOLTAGE
C_L = 0.6µF, V_{DD} = 3.6V, Boosted, A_V = 24dB



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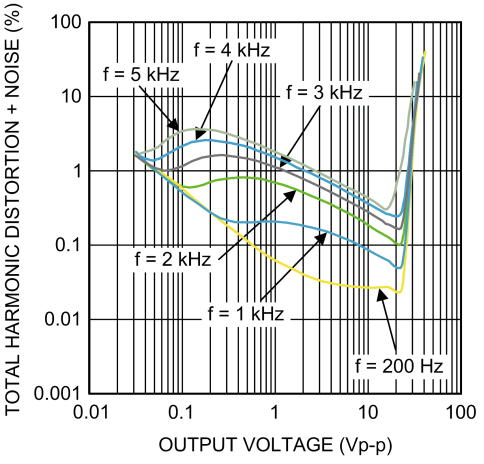
THD+N vs OUTPUT VOLTAGE
C_L = 1.0µF, V_{DD} = 3.6V, Boosted, A_V = 24dB



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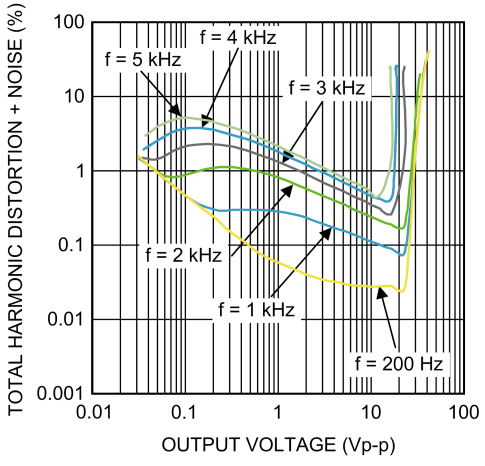
THD+N vs OUTPUT VOLTAGE
C_L = 1.5µF, V_{DD} = 3.6V, Boosted, A_V = 24dB



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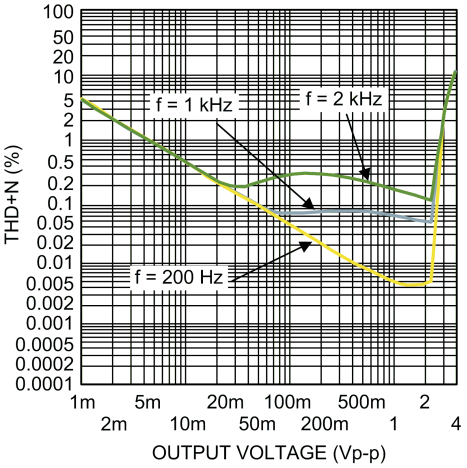
THD+N vs OUTPUT VOLTAGE
C_L = 1.5µF, V_{DD} = 3.6V, Unboosted, A_V = 0dB



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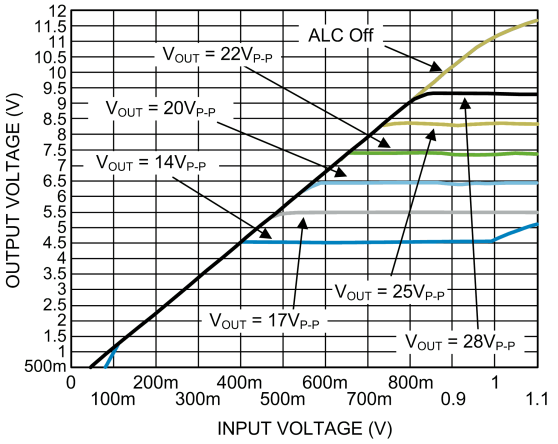
INPUT VOLTAGE vs OUTPUT VOLTAGE
ALC Enabled, A_V = 21dB, V_{DD} = 3.6V



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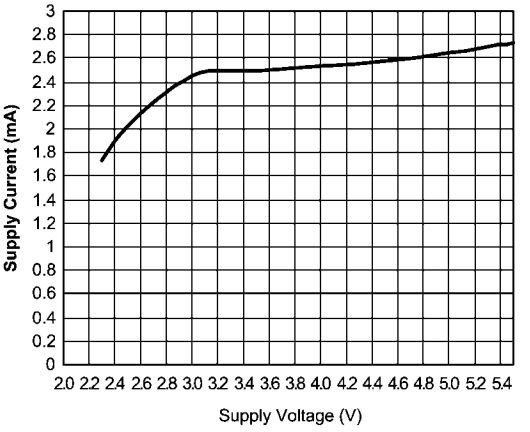
SUPPLY CURRENT vs SUPPLY VOLTAGE
R_L = ∞



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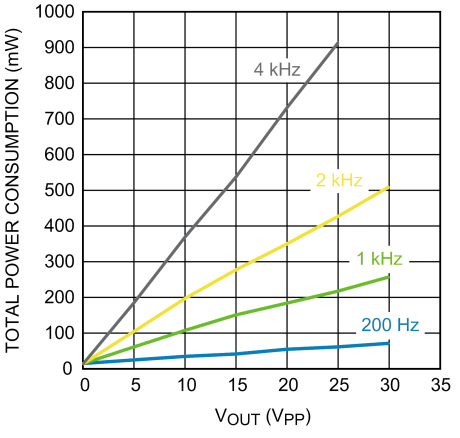
TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE
V_{DD} = 3.6V, C_L = 0.6µF



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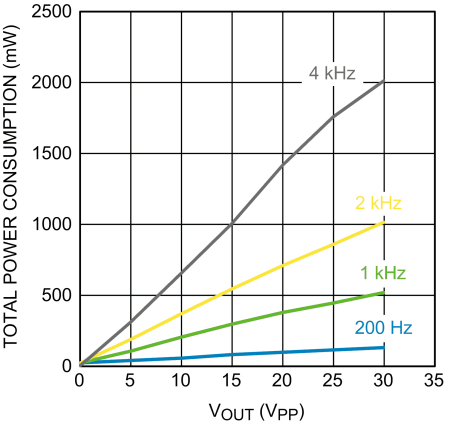
TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE
V_{DD} = 3.6V, C_L = 1.0µF



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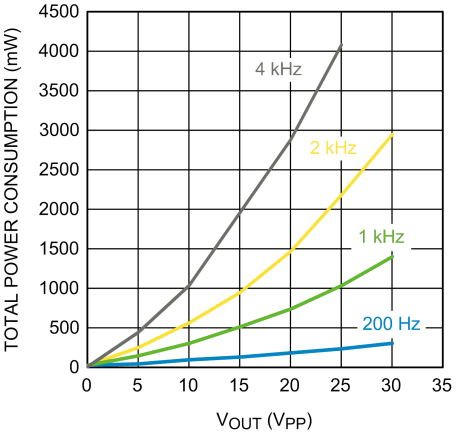
TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE
V_{DD} = 3.6V, C_L = 1.5µF



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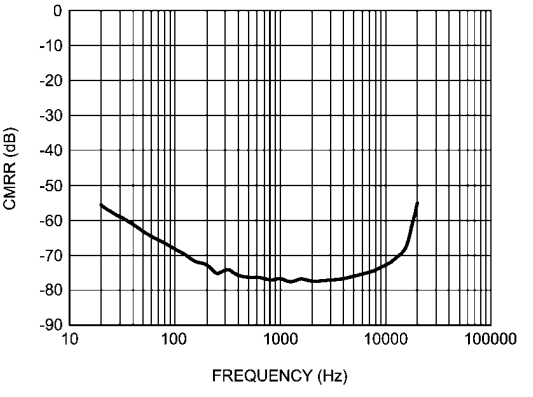
COMMON MODE REJECTION RATIO vs FREQUENCY
V_{CM}= 200mV$_{P-P}$, C_{IN} = 10µF, V_{DD} = 3.6V, C_L = 1.5µF



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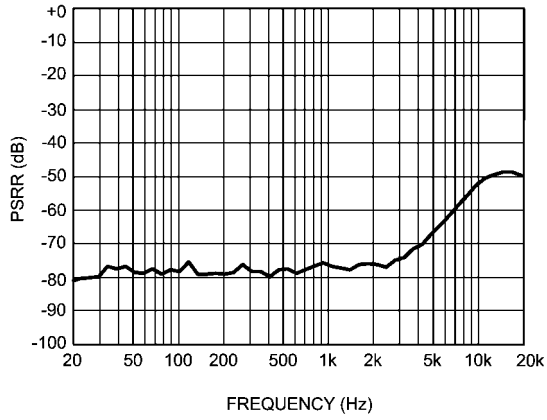
POWER SUPPLY REJECTION RATIO vs FREQUENCY
V_{RIPPLE} = 200mV_{P-P}, V_{DD} = 3.6V, C_L = 1.5µF



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Application Information

READ/WRITE I²C COMPATIBLE INTERFACE

The LM48560 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48560 and the master can communicate at clock rates up to 400kHz. *Figure 4* shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48560 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition *Figure 5*. Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse *Figure 6*. The LM48560 device address is 1101111.

I²C BUS FORMAT

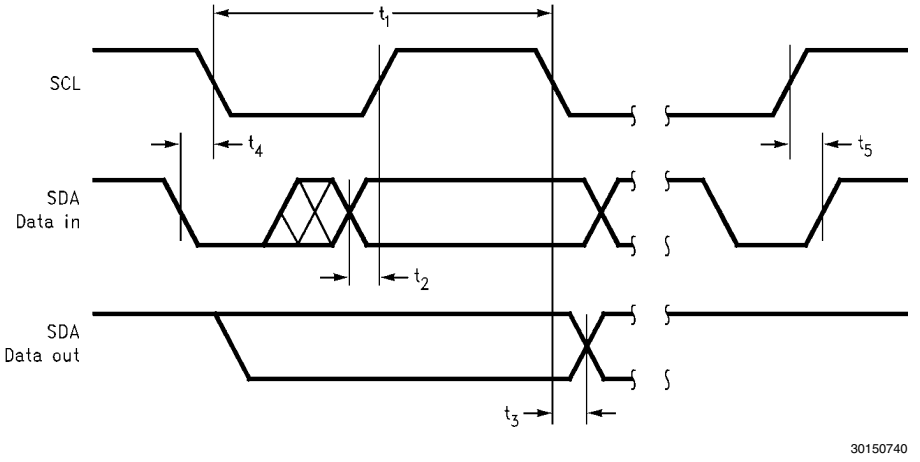


FIGURE 4. I²C Timing Diagram

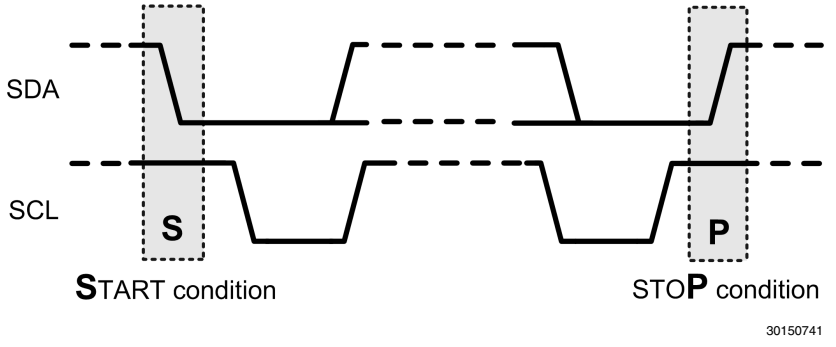


FIGURE 5. Start and Stop Diagram

WRITE SEQUENCE

The example write sequence is shown in *Figure 6*. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit (R/$\overline{W}$ = 0 indicating the master is writing to the LM48560). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM48560 sends another ACK bit. Upon receipt of the acknowledge, the 8-bit register data is sent, MSB first. The register data word is followed by an ACK, upon receipt of which, the master issues a STOP bit, allowing SDA to go high while SDA is high.

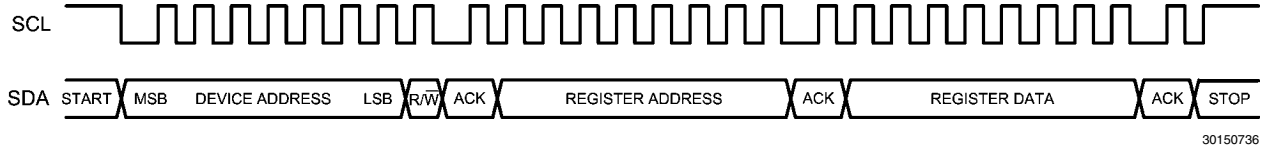


FIGURE 6. Example I²C Write Cycle

READ SEQUENCE

The example read sequence is shown in *Figure 7*. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, followed by the R/$\overline{W}$ = 1 (R/$\overline{W}$ = 1 indicating the master wants to read data from the LM48560). After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK). Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first, followed by an ACK and selected register data from the LM48560. The register data is sent MSB first. Following the acknowledgement of the register data word [7:0], the master issues a STOP bit, allowing SDA to go high while SDA is high.

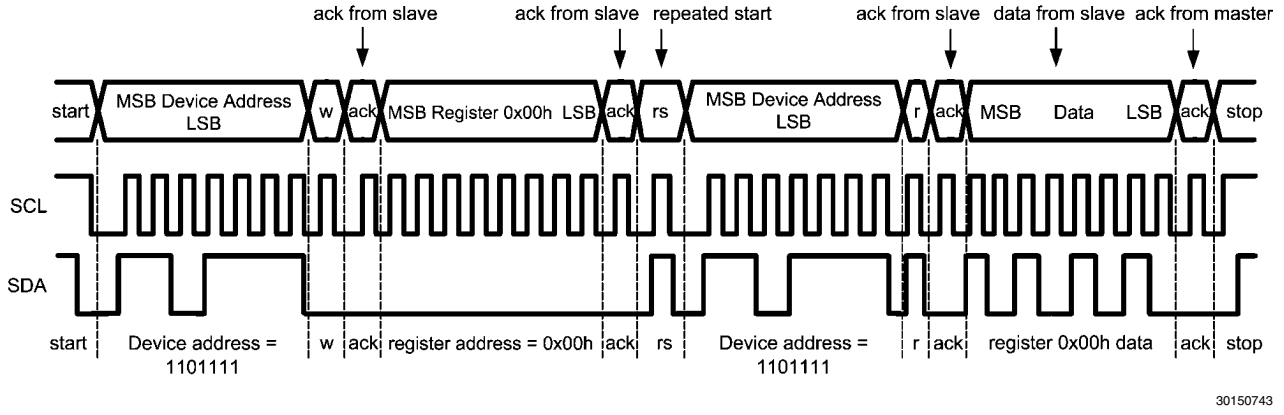


FIGURE 7. Example I²C Read Cycle

TABLE 2. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 (R/$\overline{W}$)
Device Address	1	1	0	1	1	1	1	0

TABLE 3. Mode Selection

SW/HW	SDA/SEL	SCL/GAIN	MODE
0	0 (Boost Disabled)	0	IN1, A_V = 0
		1	IN1, A_V = 6
	1 (Boost Enabled)	0	IN2, A_V = 24
		1	IN2, A_V = 30
1	X	X	I²C Mode

TABLE 4. I²C Control Registers

REGISTER ADDRESS	Register Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00h	SHUTDOWN CONTROL	X	X	X	X	TURN_ON	IN_SEL	BOOST_EN	$\overline{SHDN}$
0x01h	NO CLIP CONTROL	X	RLT1	RLT0	ATK1	ATK0	PLEV2	PLEV1	PLEV0
0x02h	GAIN CONTROL	X	X	X	X	X	X	GAIN1	GAIN0
0x03h	TEST MODE	X	X	X	X	X	X	X	X

TABLE 5. Shutdown Control Register

BIT	NAME	VALUE	DESCRIPTION
B7:B4	UNUSED	X	Unused, set to 0
B3	TURN_ON	0	Normal turn on time, t_{WU} = 15ms
		1	Fast turn on time, t_{WU} = 5ms
B2	IN_SEL	0	Input 1 selected
		1	Input 2 selected
B1	BOOST_EN	0	Boost disabled
		1	Boost enabled
B0	$\overline{SHDN}$	0	Device shutdown
		1	Device enabled

TABLE 6. No Clip Control Register

BIT	NAME	VALUE			DESCRIPTION
B7	UNUSED	X			Unused, set to 0
B6:B5	RLT1 (B6) RLT0 (B5)	B6	B5		Sets Release Time based on C_{SET}. See “Release Time” section.
		0	0		T_R = 0.5s
		0	1		T_R = 0.38s
		1	0		T_R = 0.21s
		1	1		T_R = 0.17s
B4:B3	ATK1 (B4) ATK0 (B3)	B4	B3		Sets Attack Time based on C_{SET}. See ”Attack Time” section.
		0	0		T_A = 0.83ms
		0	1		T_A = 1.2ms
		1	0		T_A = 1.5ms
		1	1		T_A = 2.2ms
B2:B0	PLEV2 (B2) PLEV1 (B1) PLEV0 (B0)	B2	B1	B0	Sets output voltage limit level.
		0	0	0	Voltage Limit disabled
		0	0	1	$V_{TH(VLIM)} = 14V_{P-P}$
		0	1	0	$V_{TH(VLIM)} = 17V_{P-P}$
		0	1	1	$V_{TH(VLIM)} = 20V_{P-P}$
		1	0	0	$V_{TH(VLIM)} = 22V_{P-P}$
		1	0	1	$V_{TH(VLIM)} = 25V_{P-P}$
		1	1	0	$V_{TH(VLIM)} = 28V_{P-P}$
		1	1	1	Voltage Limit disabled

TABLE 7. Gain Control Register

BIT	NAME	VALUE		DESCRIPTION
B7:B2	UNUSED	X		Unused, set to 0
B1:B0	GAIN1(B1) GAIN0 (B0)	B1	B0	Sets amplifier gain. Boost disabled (BOOST_EN = 0)
		0	0	0dB
		0	1	6dB
		1	0	12dB
		1	1	18dB
B1:B0	GAIN1(B1) GAIN0 (B0)	B1	B0	Sets amplifier gain. Boost enabled (BOOST_EN = 1)
		0	0	21dB
		0	1	24dB
		1	0	27dB
		1	1	30dB

GENERAL AMPLIFIER FUNCTION

The LM48560 is a fully differential, Class H piezo driver for ceramic speakers and haptic actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal, increasing headroom and improving efficiency compared to a conventional Class AB driver. The fully differential amplifier takes advantage of the increased headroom and bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended amplifier.

CLASS H OPERATION

Class H is a modification of another amplifier class (typically Class B or Class AB) to increase efficiency and reduce power dissipation. To decrease power dissipation, Class H uses a tracking power supply that monitors the output signal and adjusts the supply accordingly. When the amplifier output is below $3V_{P-P}$, the nominal boost voltage is 6V. As the amplifier output increases above $3V_{P-P}$, the boost voltage tracks the amplifier output as shown in *Figure 8*. When the amplifier output falls below $3V_{P-P}$, the boost converter returns to its nominal output voltage. Power dissipation is greatly reduced compared to conventional Class AB drivers.

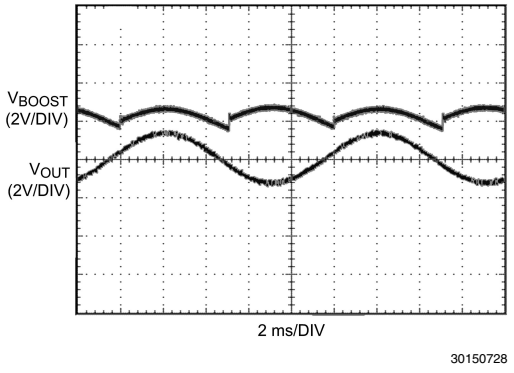


FIGURE 8. Class H Operation

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM48560 features a fully differential amplifier. A differential amplifier amplifies the difference between the two input signals. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

AUTOMATIC LEVEL CONTROL (ALC)

The ALC is available in software mode only, and only in boosted mode. In hardware mode ALC is always disabled. The ALC limits the peak output voltage to the programmed value. Consequently, it limits the peak boost voltage, as this is derived from the output voltage. The ALC is continuous, in that it provides a continuous adjustment of the voltage gain in order to limit the output voltage to the programmed value. The available gain adjustment range is typically 8dB. When the input amplitude is further increased beyond the ALC attenuation range, the output will again increase. This is illustrated in the Typical Performance Graphs, as seen on the $14V_{PP}$ plot in the Input voltage vs Output Voltage curve. The attack and decay of the ALC is programmed by software and works in conjunction with the external capacitor C_{SET}. Typically C_{SET} is 1µF, although it can be changed from 0.1µF to 4.7µF to select other ranges of attack and decay time.

ATTACK TIME

Attack time ($t_{ATK)}$ is the time it takes for the gain to be reduced by 6dB once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by equation (2):

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK} \quad (1)$$

Where α_{ATK} is the attack time coefficient () set by bits B4:B3 in the Voltage Limit Control Register (see). The attack time coefficient allows the user to set a nominal attack time. The internal 20kΩ resistor is subject to temperature change, and it has tolerance between -11% to +20%.

TABLE 8. Attack Time Coefficient

B5	B4	α_{ATK}
0	0	2.4
0	1	1.7
1	0	1.3
1	1	0.9

RELEASE TIME

Release time (t_{RL}) is the time it takes for the gain to return from 6dB to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by equation (3):

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL} \quad (s) \qquad (2)$$

where α_{RL} is the release time coefficient (Table 11) set by bits B4:B3 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20MΩ is subject to temperature change, and it has tolerance between -11% to +20%.

TABLE 9. Release Time Coefficient

B5	B4	α_{RL}
0	0	4
0	1	5.3
1	0	9.5
1	1	11.8

BOOST CONVERTER

The LM48560 features an integrated boost converter with a dynamic output control. The device monitors the output signal of the amplifier, and adjusts the output voltage of the boost converter to maintain sufficient headroom while improving efficiency.

SOFTWARE/HARDWARE MODE

Device operation in hardware or software mode is determined by the state of the SW/$\overline{HW}$ pin. Connect SW/$\overline{HW}$ to ground for hardware mode, and connect to V_{DD} for software mode.

SW/$\overline{HW}$	SDA/SEL	SCL/GAIN	MODE
0	0 (Boost Disabled)	0	IN1, Av = 0
		1	IN1, Av = 6
	1 (Boost Enabled)	0	IN2, Av = 24
		1	IN2, Av = 30
1	SDA	SCL	I²C Mode

GAIN SETTING

The LM48560 features four internally configured gain settings 0db, 6dB, and 30dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in *Table 10*.

TABLE 10. Gain Setting

GAIN	GAIN SETTING IN1	GAIN SETTING IN2
0	0dB	24dB
1	6dB	30dB

SHUTDOWN FUNCTION

The LM48560 features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and boost converter and reduce supply current to 0.01µA.

SINGLE-ENDED INPUT CONFIGURATION

The LM48560 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. *Figure 9* shows the typical single-ended applications circuit.

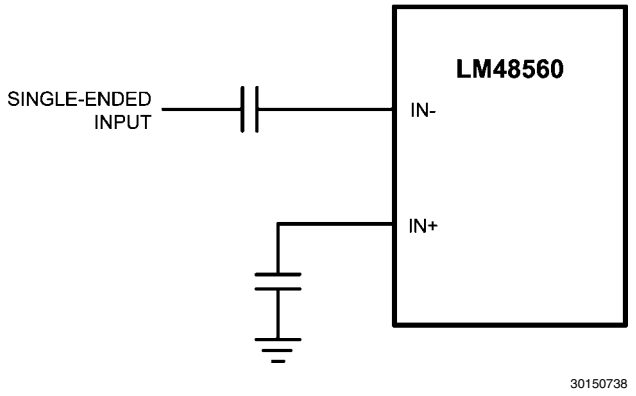


FIGURE 9. Single-Ended Input Configuration

PROPER SELECTION OF EXTERNAL COMPONENTS

ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between .01µF to 1µF. Lowering the value below .01µF can increase the attack time but LM48560 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

Power Selection of External Components

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Boost Converter Capacitor Selection

The LM48560 boost converter requires three external capacitors for proper operation: a 1µF supply bypass capacitor, and 1µF + 100pF output reservoir capacitors. Place the supply bypass capacitor as close to V_{DD} as possible. Place the reservoir capacitors as close to VBST and VAMP as possible. Low ESR surface-mount multi-layer ceramic capacitors with X7R or X5R temperature characteristics are recommended. Select output capacitors with voltage rating of 25V or higher. Tantalum, OS-CON and aluminum electrolytic capacitors are not recommended. See Table 4 for suggested capacitor manufacturers.

Inductor Selection

The LM48560 boost converter is designed for use with a 4.7µH inductor. Choose an inductor with a saturation current rating greater than the maximum operating peak current of the LM48560 (> 1A). This ensures that the inductor does not saturate, preventing excess efficiency loss, over heating and possible damage to the inductor. Additionally, choose an inductor with the lowest possible DCR (series resistance) to further minimize efficiency losses.

Diode Selection

Use a Schottkey diode as shown in *Figure 1*. A 20V diode such as the NSR0520V2T1G from On Semiconductor is recommended. The NSR0520V2T1G is designed to handle a maximum average current of 500mA.

PCB LAYOUT GUIDELINES

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48560 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

DEMO BOARD USER GUIDE

Quick Start Guide (Hardware Mode):

1. Short pins 1 (VDD) and 2 of JU1 for normal operation.
2. Short pins 2 and 3(GND) of JU7 to set the device in hardware mode.
3. Short pins 2 and 3 (GND) of JU3 to select IN1.
4. Short pins 2 and 3 (GND) of JU2 for 0dB gain.
5. Connect a power supply (2.7V-5.5V) and ground reference respectively to the VDD and GND headers on the demo board.
6. Connect a differential audio input to IN1+ and IN2-
7. Power on the board and observe the output on OUT+ and OUT-

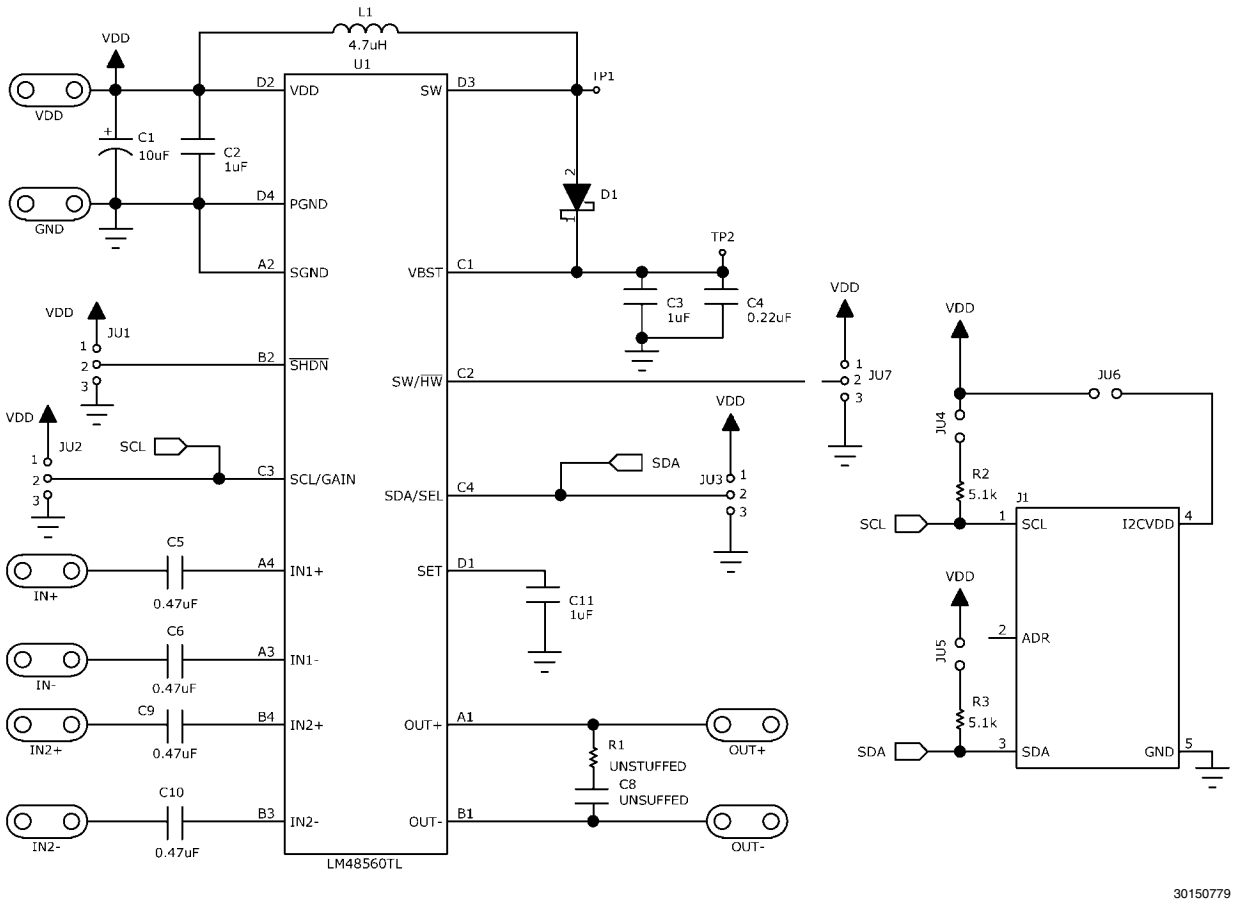
Quick Start Guide (Software Mode):

1. Short pins 1 (VDD) and 2 of JU1 for normal operation.
2. Short pins 1 (VDD) and 2 of JU7 to set the device in software mode.
3. Short pins 1 (VDD) and 2 of JU3 to select IN2.
4. Short pins 2 and 3 (GND) of JU2 for 24dB gain.
5. Connect a power supply (2.7V-5.5V) and ground reference respectively to the VDD and GND headers on the demo board.
6. Connect a differential audio input to IN1+ and IN2-
7. Connect the USB/I2C board to the LM48560 demo board.
8. Connect the USB/I2C board to a PC
9. Turn on the power supply
10. Launch the LM48560 software GUI
11. Verify that the bottom left corner of the GUI reads “USB Connected ALL ACK” (note 1)
12. Select the following:
    a. INPUT SELECT = INPUT 1
    b. BOOST = ON
    c. TURN ON TIME = NORMAL
    d. GAIN = 0dB

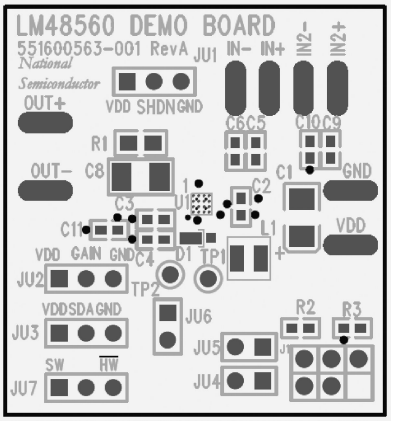
Note: If the GUI reads “USB I/O error NAK” the device has not been acknowledged, please double check your connections.

Header Functionality		
Designator	**Function**	**Notes**
VDD	VDD	Power Supply
GND	GND	Ground reference
OUT+	OUTPUT	Positive output terminal
OUT-	OUTPUT	Negative output terminal
IN1+	INPUT 1	Positive input terminal 1
IN1-	INPUT 1	Negative input terminal 1
IN2+	INPUT 2	Positive input terminal 2
IN2-	INPUT 2	Negative input terminal 2
JU1	Shutdown	Short pin 1 (VDD) and pin 2 for normal operation Short pin 2 and pin 3 (GND) for device shutdown
JU2	SCL/Gain Select	Hardware mode: Short pin 2 to pin 1 (VDD) for higher gain. Short pin 2 to pin 3(GND) for lower gain. (See Table 10) Software mode: Keep pins 1-3 open. Pin 2 = SCL for I2C communication
JU3	SDA/Input Select	Hardware mode: Short pin 2 to pin 1 (VDD) to select IN2. Short pin 2 to pin 3 (GND) to select IN1. (See Table 10) Software mode: Keep pins 1-3 open. Pin 2 = SCL for I2C communication
JU4	SCL Pullup	Short JU4 to connect pullup resistor to VDD. Open to use external I2C supply voltage
JU5	SDA pullup	Short JU5 to connect pullup resistor to VDD. Open to use external I2C supply voltage
JU6	I2C VDD	Short JU6 to use VDD as I2C VDD. Open to use external I2C supply voltage
JU7	SW/HW	Software Mode: Short pins 1 (VDD) and 2 Hardware Mode: Short pins 2 and 3(GND)

Demo Board Schematic



PC Board Layout



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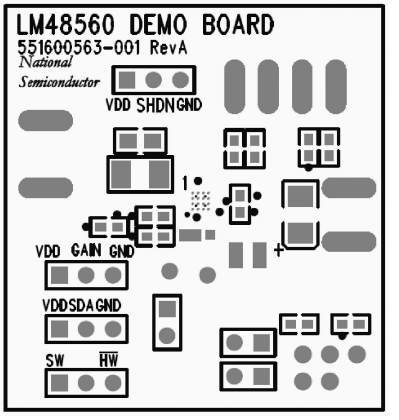
Top Silk Screen



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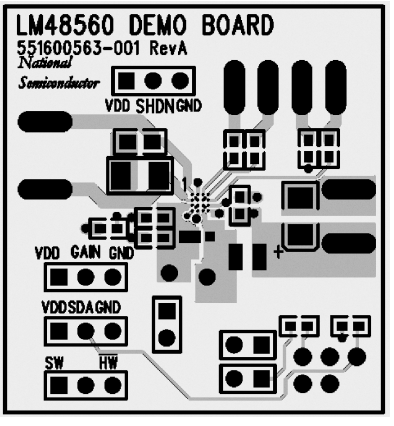
Solder Mask Top



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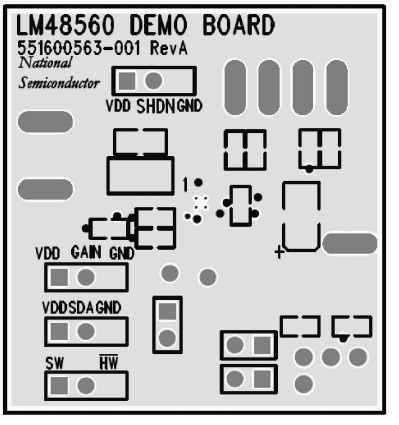
Top Layer



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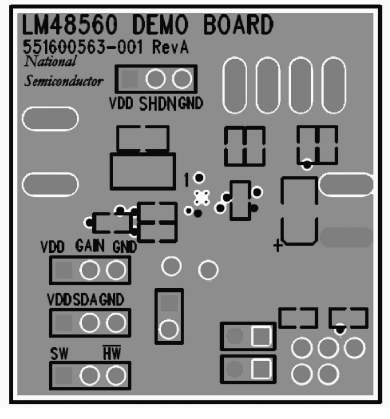
Layer 2



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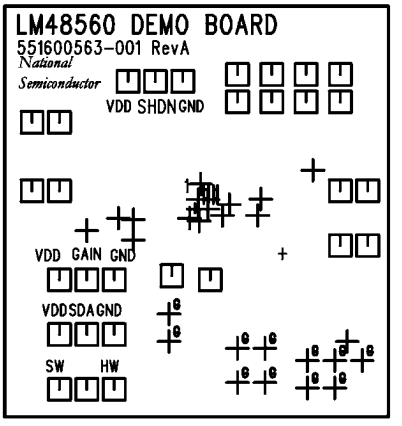
Layer 3



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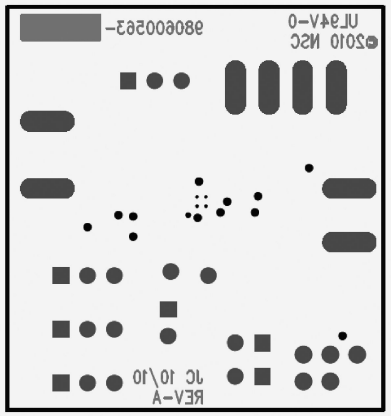
Drill Drawing



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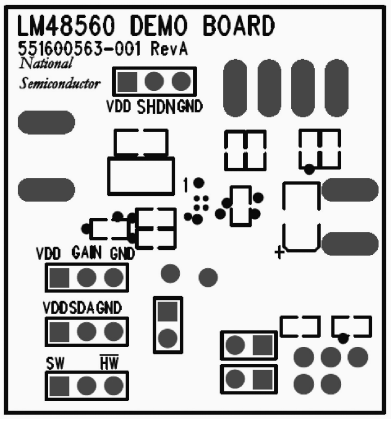
Silk Bottom



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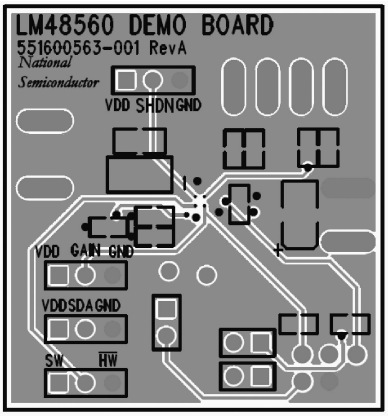
Solder Mask Bottom



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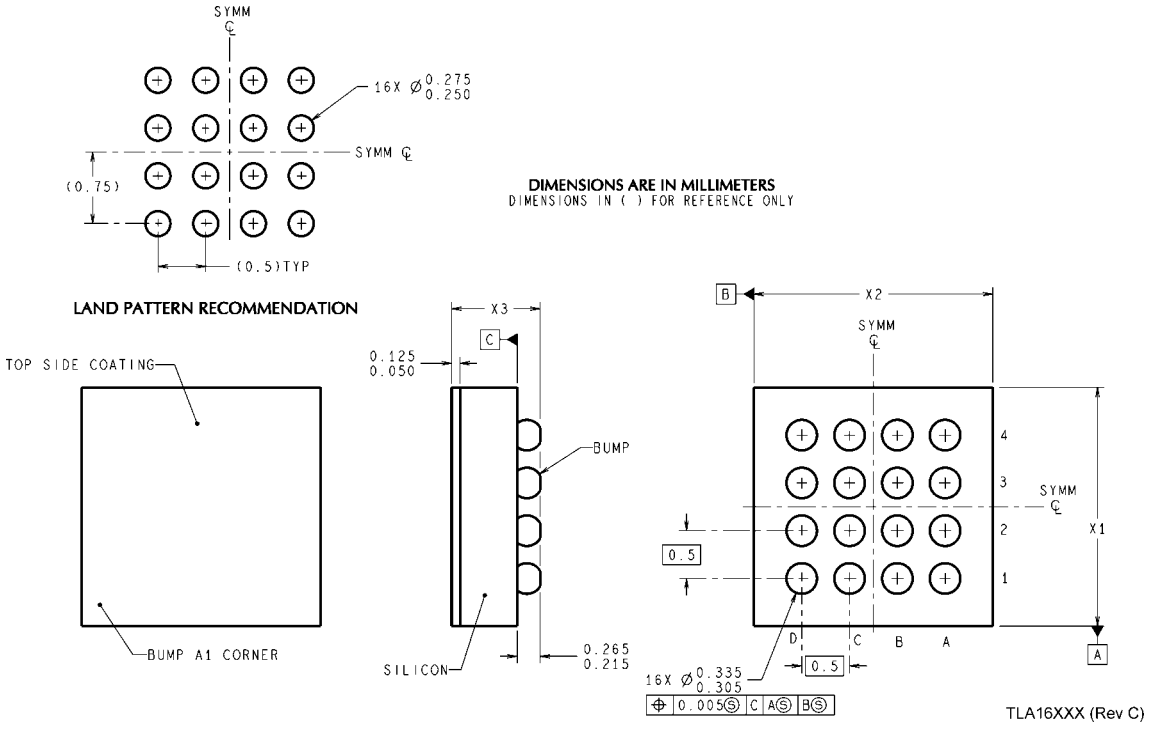
Bottom Layer

Revision History

Rev	Date	Description
1.0	08/16/11	Initial WEB released.
1.01	09/21/11	Input edits under CLASS H OPERATION.
1.02	11/01/11	Edited curves 30150753, 54, 55, 56, and Figure 7 (I^2C Read Cycle).
1.03	11/10/11	Edited Figure 7.

Physical Dimensions inches (millimeters) unless otherwise noted



Thin micro SMD
Order Number LM48560TL
NS Package Number TLA16Z1A
X1 = 1.970±0.03mm X2 = 1.970±0.03mm X3 = 0.600±0.075mm

Notes

Notes

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