

# LM4818 Boomer® Audio Power Amplifier Series **350mW Audio Power Amplifier with Shutdown Mode**

Check for Samples: [LM4818](#)

## FEATURES

- **SOIC Surface Mount Packaging.**
- **Switch On/Off Click Suppression.**
- **Unity-Gain Stable.**
- **Minimum External Components.**

## APPLICATIONS

- **General Purpose Audio**
- **Portable Electronic Devices**
- **Information Appliances (IA)**

## KEY SPECIFICATIONS

- **THD+N at 1kHz, 350mW Continuous Average Output Power into 16Ω 10% (max)**
- **THD+N at 1kHz, 300mW Continuous Average Output Power into 8Ω 10% (max)**
- **Shutdown Current 0.7μA (typ)**

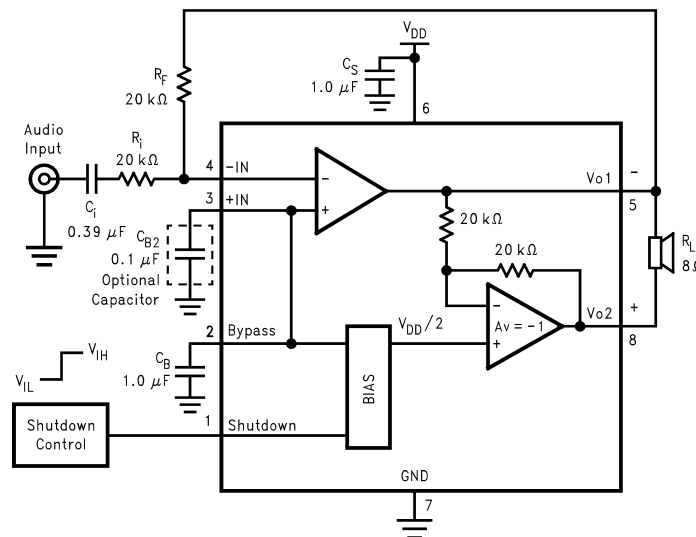
## DESCRIPTION

The LM4818 is a mono bridged power amplifier that is capable of delivering 350mW<sub>RMS</sub> output power into a 16Ω load or 300mW<sub>RMS</sub> output power into an 8Ω load with 10% THD+N from a 5V power supply.

The LM4818 Boomer™ audio power amplifier is designed specifically to provide high quality output power and minimize PCB area with surface mount packaging and a minimal amount of external components. Since the LM4818 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable applications.

The closed loop response of the unity-gain stable LM4818 can be configured using external gain-setting resistors. The device is available in SOIC package type to suit various applications.

## Typical Application



**Figure 1. Typical Audio Amplifier Application Circuit**

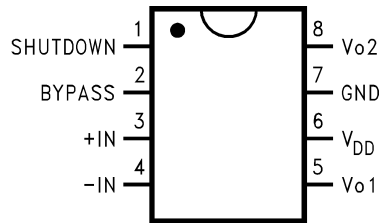


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## Connection Diagram



**Figure 2. SOIC Package - Top View**  
See Package Number D



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)(3)</sup>

Supply Voltage		6.0V	
Storage Temperature		-65°C to +150°C	
Input Voltage		-0.3V to $V_{DD} + 0.3V$	
Power Dissipation ( $P_D$ ) <sup>(4)</sup>		Internally Limited	
ESD Susceptibility <sup>(5)</sup>		2.5kV	
ESD Susceptibility <sup>(6)</sup>		200V	
Junction Temperature ( $T_J$ )		150°C	
Soldering Information	Small Outline Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Thermal Resistance	$\theta_{JC}$ (SOIC)	35°C/W	
	$\theta_{JA}$ (SOIC)	170°C/W	

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ . For the LM4818,  $T_{JMAX} = 150^\circ\text{C}$  and the typical junction-to-ambient thermal resistance ( $\theta_{JA}$ ) when board mounted is 170°C/W for the SOIC package.
- (5) Human body model, 100pF discharged through a 1.5 k $\Omega$  resistor.
- (6) Machine Model, 220pF–240pF capacitor is discharged through all pins.

## OPERATING RATINGS<sup>(1)(2)</sup>

Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
Supply Voltage	$2.0V \leq V_{CC} \leq 5.5V$

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the *Operating Ratings*. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.

**ELECTRICAL CHARACTERISTICS  $V_{DD} = 5V^{(1)(2)}$** 

 The following specifications apply for  $V_{DD} = 5V$ ,  $R_L = 16\Omega$  unless otherwise stated. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM4818		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)(5)</sup>	
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V$ , $I_o = 0A$	1.5	3.0	mA (max)
$I_{SD}$	Shutdown Current	$V_{PIN1} = V_{DD}^{(6)}$	1.0	5.0	$\mu A$ (max)
$I_{SDIH}$	Shutdown Voltage Input High			4.0	V (min)
$I_{SDIL}$	Shutdown Voltage Input Low			1.0	V (max)
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$	5	50	mV (max)
$P_O$	Output Power	THD = 10%, $f_{IN} = 1kHz$	350		mW
		THD = 10%, $f_{IN} = 1kHz$ , $R_L = 8\Omega$	300		mW
THD+N	Total Harmonic Distortion + Noise	$P_O = 270mW_{RMS}$ , $A_{VD} = 2$ , $f_{IN} = 1kHz$	1		%

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.
- (3) Typical specifications are specified at  $25^\circ C$  and represent the parametric norm.
- (4) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
- (5) Datasheet min/max specification limits are specified by designs, test, or statistical analysis.
- (6) The Shutdown pin (pin 1) should be driven as close as possible to  $V_{DD}$  for minimum current in Shutdown Mode.

**ELECTRICAL CHARACTERISTICS  $V_{DD} = 3V^{(1)(2)}$** 

 The following specifications apply for  $V_{DD} = 3V$  and  $R_L = 16\Omega$  load unless otherwise stated. Limits apply to  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM4818		Units (Limits)
			Typical <sup>(3)</sup>	Limit <sup>(4)(5)</sup>	
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V$ , $I_o = 0A$	1.0	3.0	mA (max)
$I_{SD}$	Shutdown Current	$V_{PIN1} = V_{DD}^{(6)}$	0.7	5.0	$\mu A$ (max)
$I_{SDIH}$	Shutdown Voltage Input High			2.4	V (min)
$I_{SDIL}$	Shutdown Voltage Input Low			0.6	V (max)
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$	5	50	mV
$P_O$	Output Power	THD = 10%, $f_{IN} = 1kHz$	110		mW
		THD = 10%, $f_{IN} = 1kHz$ , $R_L = 8\Omega$	90		mW
THD+N	Total Harmonic Distortion + Noise	$P_O = 80mW_{RMS}$ , $A_{VD} = 2$ , $f_{IN} = 1kHz$	1		%

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. However, the typical value is a good indication of device's performance.
- (3) Typical specifications are specified at  $25^\circ C$  and represent the parametric norm.
- (4) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
- (5) Datasheet min/max specification limits are specified by designs, test, or statistical analysis.
- (6) The Shutdown pin (pin 1) should be driven as close as possible to  $V_{DD}$  for minimum current in Shutdown Mode.

## EXTERNAL COMPONENTS DESCRIPTION

(Figure 1)

Components		Functional Description
1.	$R_i$	Combined with $R_f$ , this inverting input resistor sets the closed-loop gain. $R_i$ also forms a high pass filter with $C_i$ at $f_c = 1/(2\pi R_i C_i)$ .
2.	$C_i$	This input coupling capacitor blocks DC voltage at the amplifier's terminals. Combined with $R_i$ , it creates a high pass filter with $R_i$ at $f_c = 1/(2\pi R_i C_i)$ . Refer to the section, <a href="#">PROPER SELECTION OF EXTERNAL COMPONENTS</a> for an explanation of how to determine the value of $C_i$ .
3.	$R_f$	Combined with $R_i$ , this is the feedback resistor that sets the closed-loop gain: $A_v = 2(R_f/R_i)$ .
4.	$C_s$	This is the power supply bypass capacitor that filters the voltage applied to the power supply pin. Refer to the <a href="#">APPLICATION INFORMATION</a> section for proper placement and selection of $C_s$ .
5.	$C_B$	This is the bypass pin capacitor that filters the voltage at the BYPASS pin. Refer to the section, <a href="#">PROPER SELECTION OF EXTERNAL COMPONENTS</a> for information concerning proper placement and selection of $C_B$ .
6.	$C_{B2}$	This is an optional capacitor that is not needed in the majority of applications. If the capacitor is not used, pin 3 should be connected directly to pin2. Refer to the section <a href="#">PROPER SELECTION OF EXTERNAL COMPONENTS</a> for more information concerning $C_{B2}$ .

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency

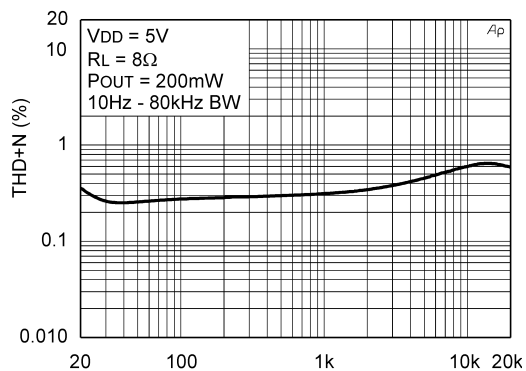


Figure 3.

THD+N vs Frequency

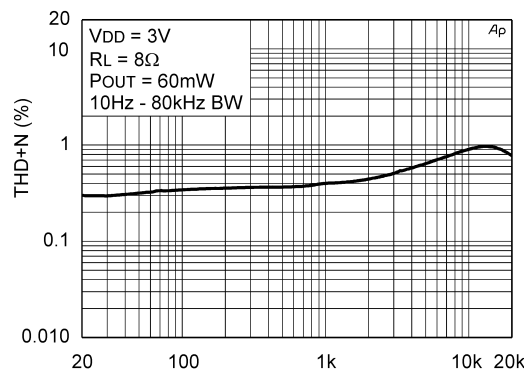


Figure 4.

THD+N vs Frequency

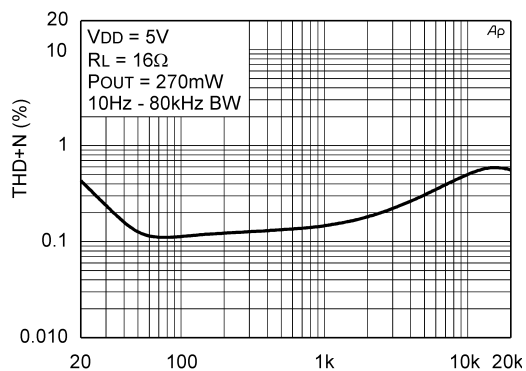


Figure 5.

THD+N vs Frequency

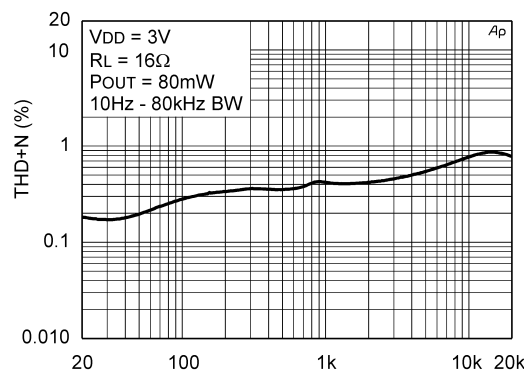


Figure 6.

THD+N vs Frequency

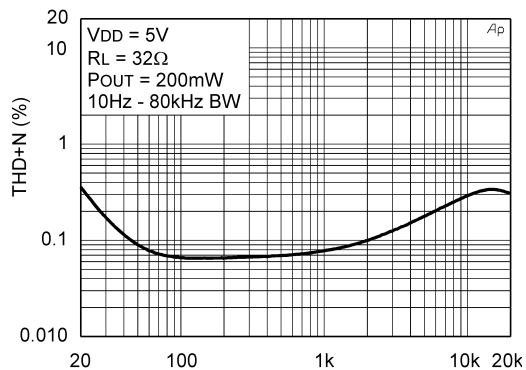


Figure 7.

THD+N vs Frequency

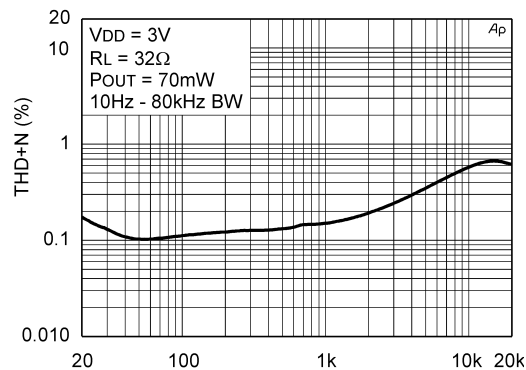


Figure 8.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

THD+N vs Output Power

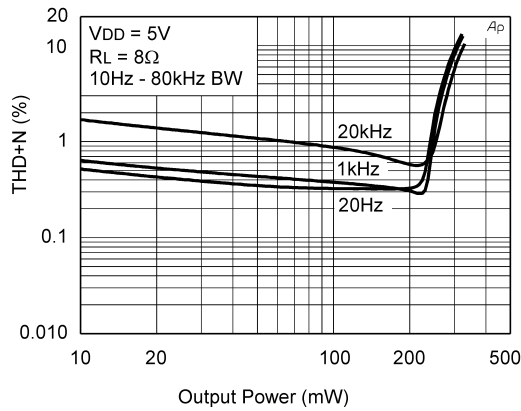


Figure 9.

THD+N vs Output Power

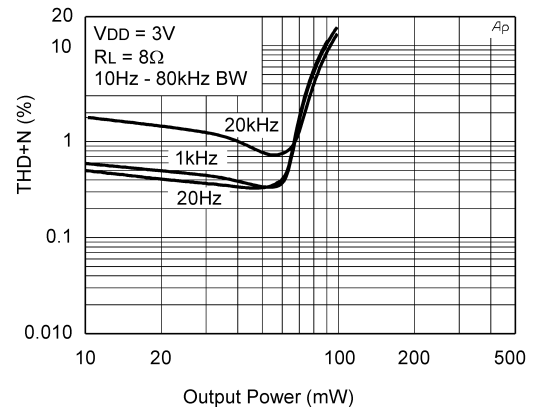


Figure 10.

THD+N vs Output Power

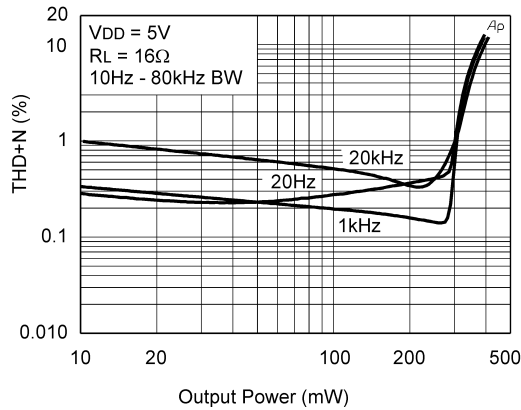


Figure 11.

THD+N vs Output Power

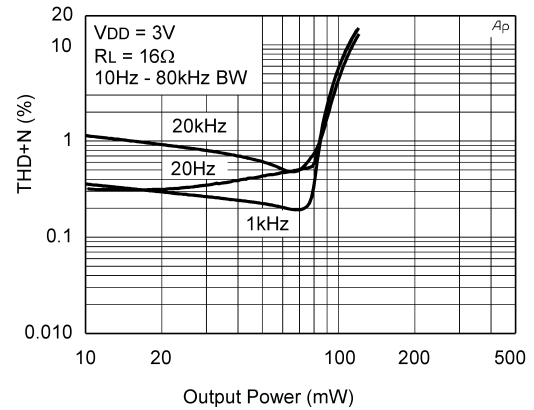


Figure 12.

THD+N vs Output Power

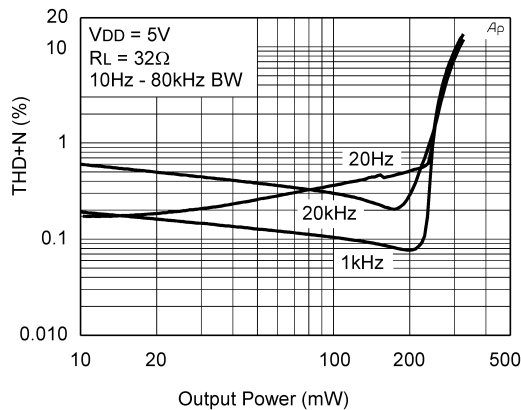


Figure 13.

THD+N vs Output Power

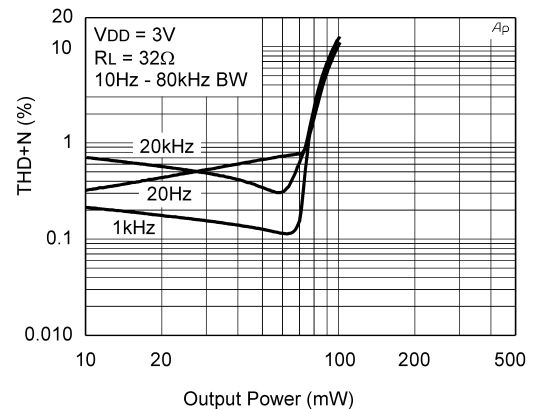
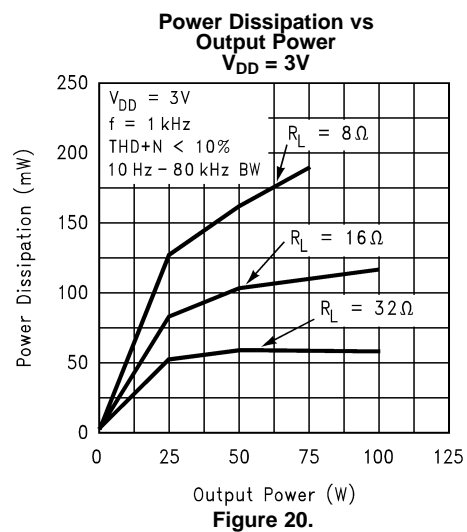
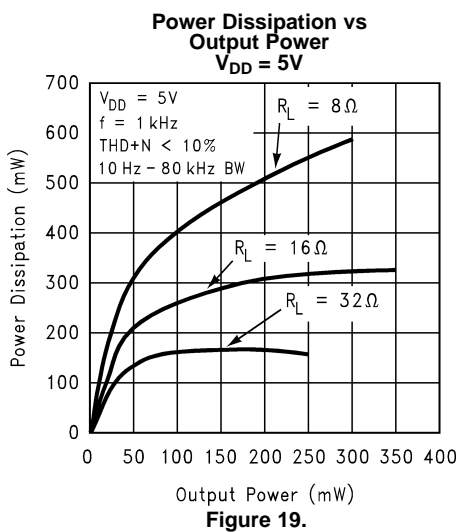
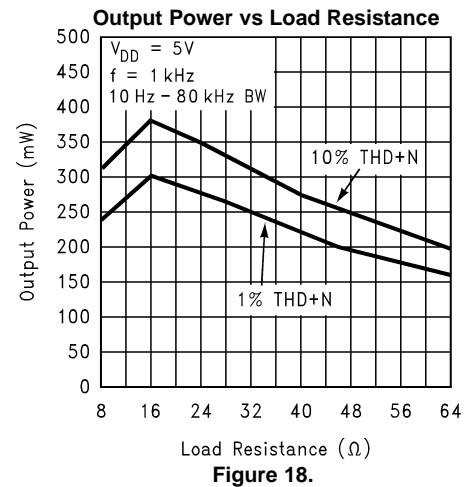
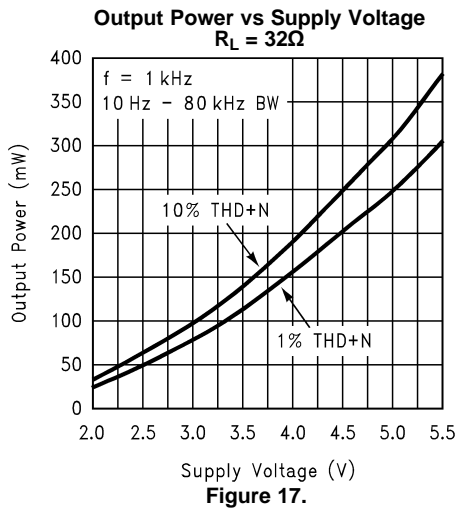
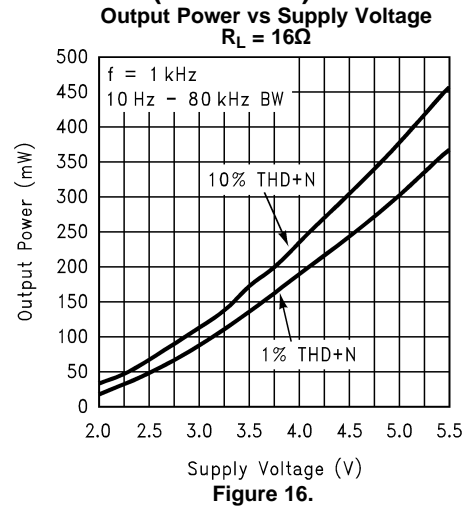
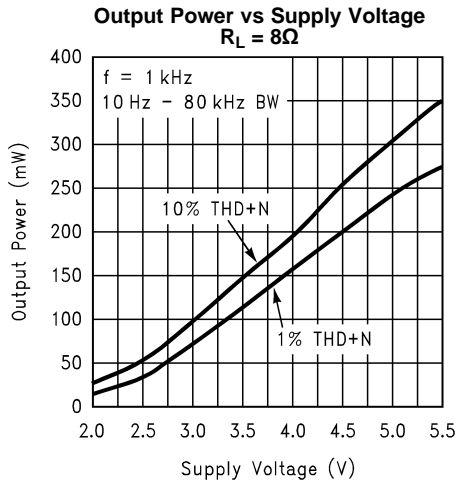


Figure 14.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

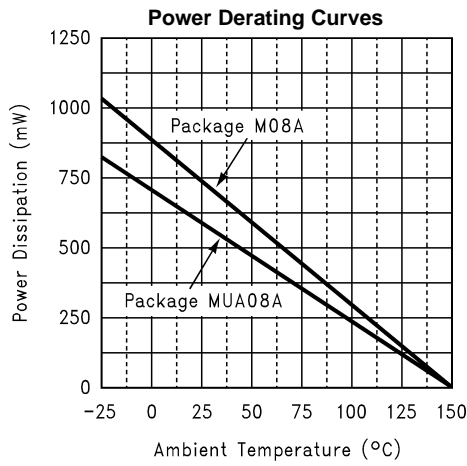


Figure 21.

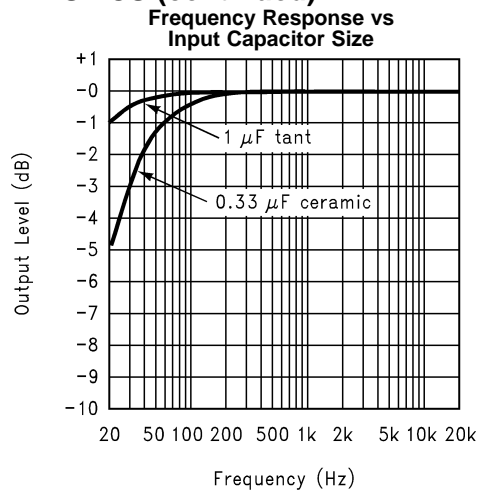


Figure 22.

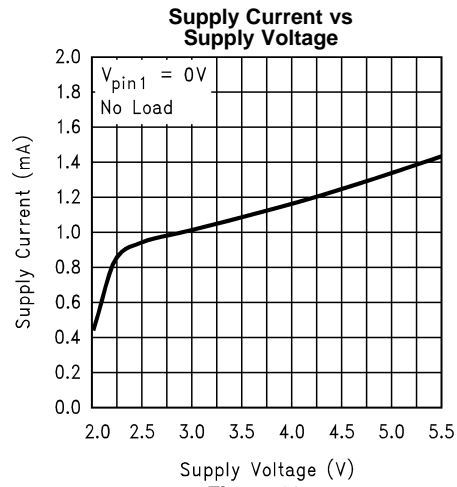


Figure 23.



## APPLICATION INFORMATION

### BRIDGE CONFIGURATION EXPLANATION

As shown in [Figure 1](#), the LM4818 consist of two operational amplifiers. External resistors,  $R_i$  and  $R_f$  set the closed-loop gain of the first amplifier (and the amplifier overall), whereas two internal 20k $\Omega$  resistors set the second amplifier's gain at -1. The LM4818 is typically used to drive a speaker connected between the two amplifier outputs.

[Figure 1](#) shows that the output of Amp1 serves as the input to Amp2, which results in both amplifiers producing signals identical in magnitude but 180° out of phase. Taking advantage of this phase difference, a load is placed between  $V_{O1}$  and  $V_{O2}$  and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode is different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This results in four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output assumes that the amplifier is not current limited or the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the [AUDIO POWER AMPLIFIER DESIGN EXAMPLE](#) section.

Another advantage of the differential bridge output is no net DC voltage across the load. This results from biasing  $V_{O1}$  and  $V_{O2}$  at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single supply amplifier's half-supply bias voltage across the load. The current flow created by the half-supply bias voltage increases internal IC power dissipation and may permanently damage loads such as speakers.

### POWER DISSIPATION

Power dissipation is a major concern when designing a successful bridged or single-ended amplifier. [Equation 2](#) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ (W) Single-ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridged amplifier is an increase in the internal power dissipation point for a bridge amplifier operating at the same given conditions. [Equation 3](#) states the maximum power dissipation point for a bridged amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = 4(V_{DD})^2 / (2\pi^2 R_L) \text{ (W) Bridge Mode} \quad (3)$$

The LM4818 has two operational amplifiers in one package and the maximum internal power dissipation is four times that of a single-ended amplifier. However, even with this substantial increase in power dissipation, the LM4818 does not require heatsinking. From [Equation 3](#), assuming a 5V power supply and an 8 $\Omega$  load, the maximum power dissipation point is 633mW. The maximum power dissipation point obtained from [Equation 3](#) must not exceed the power dissipation predicted by [Equation 4](#):

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \text{ (W)} \quad (4)$$

For the D package,  $\theta_{JA} = 170^\circ\text{C/W}$  and  $T_{JMAX} = 150^\circ\text{C}$  for the LM4818. For a given ambient temperature,  $T_A$ , [Equation 4](#) can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of [Equation 3](#) is greater than the result of [Equation 4](#), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. For a typical application using the D packaged LM4818 with a 5V power supply and an 8 $\Omega$  load, the maximum ambient temperature that does not violate the maximum junction temperature is approximately 42°C. It is assumed that a device is a surface mount part operating around the maximum power dissipation point. The assumption that the device is operating around the maximum power dissipation point is incorrect for an 8 $\Omega$  load. The maximum power dissipation point occurs when the output power is equal to the maximum power dissipation or 50% efficiency. The LM4818 is not capable of the output power level (633mW) required to operate at the maximum power dissipation point for an 8 $\Omega$  load. To find the maximum

power dissipation, the graph [Figure 20](#) must be used. From the graph, the maximum power dissipation for an 8Ω load and a 5V supply is approximately 575mW. Substituting this value back into [Equation 4](#) for  $P_{\text{DMAX}}$  and using  $\theta_{\text{JA}} = 170^{\circ}\text{C/W}$  for the D package, the maximum ambient temperature is 52°C. Refer to the [TYPICAL PERFORMANCE CHARACTERISTICS](#) curves for power dissipation information for lower output powers and maximum power dissipation for each package at a given ambient temperature.

## POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitors connected to the bypass and power supply pins should be placed as close to the LM4818 as possible. The capacitor connected between the bypass pin and ground improves the internal bias voltage's stability, producing improved PSRR. The improvements to PSRR increase as the bypass pin capacitor value increases. Typical applications employ a 5V regulator with 10μF and 0.1μF filter capacitors that aid in supply stability. Their presence, however, does not eliminate the need for bypassing the supply nodes of the LM4818. The selection of bypass capacitor values, especially  $C_B$ , depends on desired PSRR requirements, click and pop performance as explained in the section, [PROPER SELECTION OF EXTERNAL COMPONENTS](#), as well as system cost and size constraints.

## SHUTDOWN FUNCTION

The voltage applied to the LM4818's SHUTDOWN pin controls the shutdown function. Activate micro-power shutdown by applying  $V_{\text{DD}}$  to the SHUTDOWN pin. When active, the LM4818's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically  $1/2V_{\text{DD}}$ . The low 0.7μA typical shutdown current is achieved by applying a voltage that is as near as  $V_{\text{DD}}$  as possible to the SHUTDOWN pin. A voltage that is less than  $V_{\text{DD}}$  may increase the shutdown current. Avoid intermittent or unexpected micro-power shutdown by ensuring that the SHUTDOWN pin is not left floating but connected to either  $V_{\text{DD}}$  or GND.

There are a few ways to activate micro-power shutdown. These included using a single-pole, single-throw switch, a microcontroller, or a microprocessor. When using a switch, connect an external 10kΩ to 100kΩ pull-up resistor between the SHUTDOWN pin and  $V_{\text{DD}}$ . Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the shutdown pin to  $V_{\text{DD}}$  through the pull-up resistor, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor

## PROPER SELECTION OF EXTERNAL COMPONENTS

Optimizing the LM4818's performance requires properly selecting external components. Though the LM4818 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4818 is unity gain stable, giving the designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of  $1V_{\text{RMS}}$  (2.83V<sub>P-P</sub>). Please refer to the [AUDIO POWER AMPLIFIER DESIGN EXAMPLE](#) section for more information on selecting the proper gain.

Another important consideration is the amplifier's close-loop bandwidth. To a large extent, the bandwidth is dictated by the choice of external components shown in [Figure 1](#). The input coupling capacitor,  $C_i$ , forms a first order high pass filter that limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons discussed below

### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires a high value input coupling capacitor ( $C_i$  in [Figure 1](#)). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with limited frequency response reap little improvement by using a large input capacitor.

Besides affecting system cost and size,  $C_i$  has an effect on the LM4818's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's value. Higher value capacitors need more time to reach a quiescent DC voltage (usually  $1/2 V_{DD}$ ) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor,  $R_F$ . Thus, selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency can minimize pops.

As shown in [Figure 1](#), the input resistor ( $R_i$ ) and the input capacitor,  $C_i$  produce a -3dB high pass filter cutoff frequency that is found using [Equation 5](#).

$$f_{-3dB} = 1/(2 \pi R_i C_i) \text{ (Hz)} \quad (5)$$

As an example when using a speaker with a low frequency limit of 150Hz,  $C_i$ , using [Equation 5](#) is  $0.063\mu\text{F}$ . The  $0.39\mu\text{F}$   $C_i$  shown in [Figure 1](#) allows the LM4818 to drive a high efficiency, full range speaker whose response extends down to 20Hz.

Besides optimizing the input capacitor value, the bypass capacitor value,  $C_B$  requires careful consideration. The bypass capacitor's value is the most critical to minimizing turn-on pops because it determines how fast the LM4818 turns on. The slower the LM4818's outputs ramp to their quiescent DC voltage (nominally  $1/2V_{DD}$ ), the smaller the turn-on pop. While the device will function properly (no oscillations or motorboating), with  $C_B$  less than  $1.0\mu\text{F}$ , the device will be much more susceptible to turn-on clicks and pops. Thus, a value of  $C_B$  equal to or greater than  $1.0\mu\text{F}$  is recommended in all but the most cost sensitive designs.

### Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to the value of  $C_B$ , the capacitor connected to the BYPASS pin. Since  $C_B$  determines how fast the LM4818 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4818's outputs ramp to their quiescent DC voltage (nominally  $1/2V_{DD}$ ), the smaller the turn-on pop. Choosing  $C_B$  equal to  $1.0\mu\text{F}$  along with a small value of  $C_i$  (in the range of  $0.1\mu\text{F}$  to  $0.39\mu\text{F}$ ) produces a click-less and pop-less shutdown function. As discussed above, choosing  $C_i$  no larger than necessary for the desired bandwidth helps minimize clicks and pops. If using the optional capacitor,  $C_{B2}$ , the total capacitance seen at the BYPASS pin is  $C_B + C_{B2}$ . When using the values shown in [Figure 1](#) for  $C_B$  and  $C_{B2}$  the change in the capacitance seen by the BYPASS pin is not significant relative to capacitor value tolerances.

### Optimizing Click and Pop Reduction Performance

The LM4818 contains circuitry that minimizes turn-on and shutdown transients or "clicks and pops". For this discussion, turn on refers to either applying the power or supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4818's internal amplifiers are configured as unity gain buffers. An internal current source charges the voltage of the bypass capacitor,  $C_B$ , connected to the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage charging on the bypass capacitor. The gain of the internal amplifiers remains unity until the bypass capacitor is fully charged to  $1/2V_{DD}$ . As soon as the voltage on the bypass capacitor is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of the bypass capacitor,  $C_B$ , alters the device's turn-on time and magnitude of "clicks and pops". Increasing the value of  $C_B$  reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of  $C_B$  increases, the turn-on time ( $T_{ON}$ ) increases. There is a linear relationship between the size of  $C_B$  and the turn on time. If using the optional capacitor,  $C_{B2}$ , the total capacitance seen at the BYPASS pin is  $C_B$  and  $C_{B2}$ . The total capacitance seen at the BYPASS pin must be considered for the table below and when optimizing click and pop performance. Below are some typical turn-on times for various values of  $C_B$ :

$C_B$	$T_{ON}$
$0.01\mu\text{F}$	20ms
$0.1\mu\text{F}$	200ms
$0.22\mu\text{F}$	440ms
$0.47\mu\text{F}$	940ms
$1.0\mu\text{F}$	2S

In order to eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching  $V_{DD}$  may not allow the capacitors to fully discharge, which may cause "clicks and pops".

## AUDIO POWER AMPLIFIER DESIGN EXAMPLE

The following are the desired operational parameters:

Given:

Power Output	100mW
Load Impedance	16Ω
Input Level	1Vrms (max)
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. To find this minimum supply voltage, use the [Output Power vs. Supply Voltage](#) graph in the [TYPICAL PERFORMANCE CHARACTERISTICS](#) section. From the graph for a 16Ω load, (graphs are for 8Ω, 16Ω, and 32Ω loads) the supply voltage for 100mW of output power with 1% THD+N is approximately 3.15 volts.

Additional supply voltage creates the benefit of increased headroom that allows the LM4818 to reproduce peaks in excess of 100mW without output signal clipping or audible distortion. The choice of supply voltage must also not create a situation that violates maximum dissipation as explained above in the [Power Dissipation](#) section. For example, if a 3.3V supply is chosen for extra headroom then according to [Equation 3](#) the maximum power dissipation point with a 16Ω load is 138mW. Using [Equation 4](#) the maximum ambient temperature is 126°C for the D package.

After satisfying the LM4818's power dissipation requirements, the minimum differential gain is found using [Equation 6](#).

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{orms} / V_{inrms} \quad (6)$$

Thus a minimum gain of 1.27 V/V allows the LM4818 to reach full output swing and maintain low noise and THD+N performance. For this example, let  $A_{VD} = 1.27$ . The amplifier's overall gain is set using the input ( $R_i$ ) and feedback ( $R_F$ ) resistors. With the desired input impedance set to 20kΩ, the feedback resistor is found using [Equation 7](#).

$$R_F / R_i = A_{VD} / 2 \text{ (V/V)} \quad (7)$$

The value of  $R_F$  is 13kΩ.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit.

The results are:

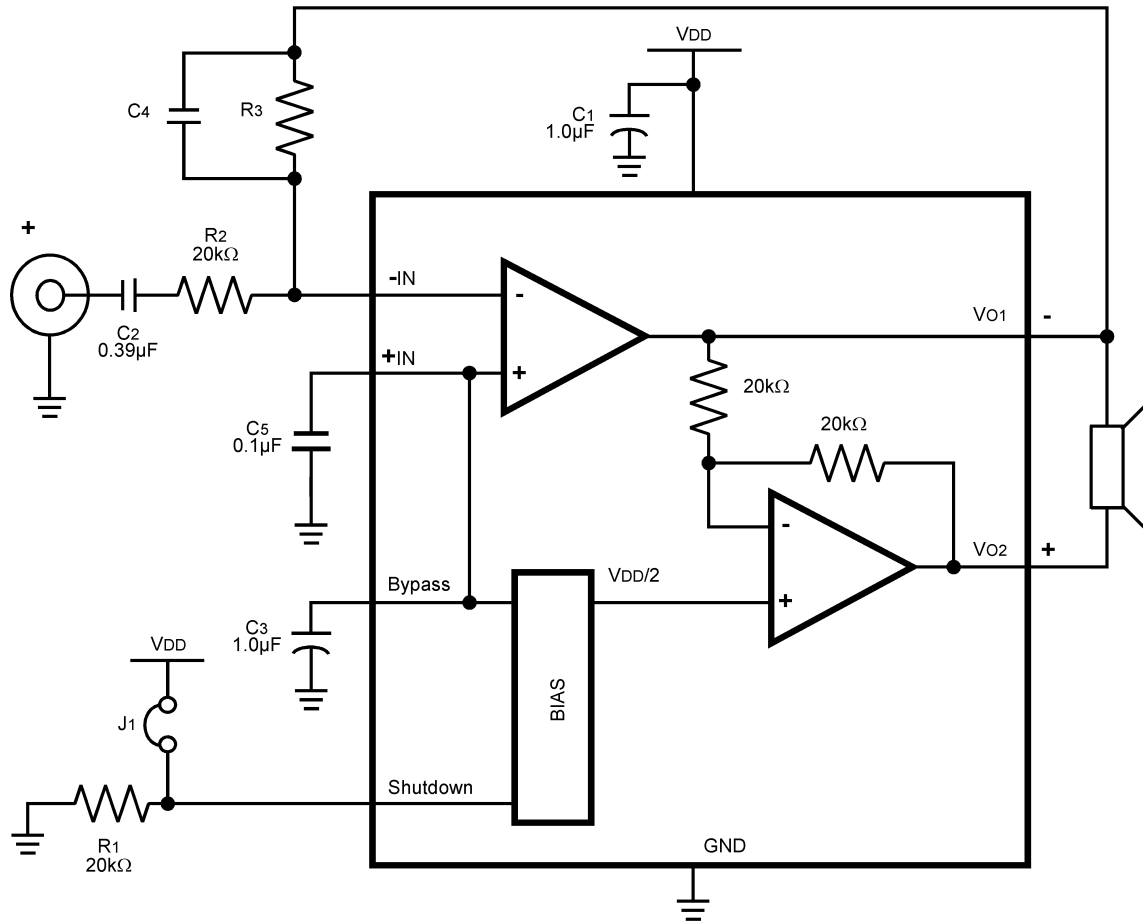
$$f_L = 100\text{Hz} / 5 = 20\text{Hz} \quad (8)$$

$$f_H = 20 \text{ kHz} * 5 = 100\text{kHz} \quad (9)$$

As mentioned in the [PROPER SELECTION OF EXTERNAL COMPONENTS](#) section,  $R_i$  and  $C_i$  create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the coupling capacitor's value using [Equation 10](#).

$$C_i \geq 1 / (2\pi R_i f_c) \text{ (F)} \quad (10)$$

$C_i \geq 0.398\mu\text{F}$ , a standard value of 0.39μF will be used. The product of the desired high frequency cutoff (100kHz in this example) and the differential gain,  $A_{VD}$ , determines the upper pass band response limit. With  $A_{VD} = 1.27$  and  $f_H = 100\text{kHz}$ , the closed-loop gain bandwidth product (GBWP) is 127kHz. This is less than the LM4818's 900kHz GBWP. With this margin the amplifier can be used in designs that require more differential gain while avoiding performance restricting bandwidth limitations.



**Figure 24. HIGHER GAIN AUDIO AMPLIFIER**

The LM4818 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor ( $C_4$ ) may be needed as shown in Figure 24 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of  $R_3$  and  $C_4$  will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is  $R_3 = 20k\Omega$  and  $C_4 = 25pF$ . These components result in a -3dB point of approximately 320 kHz. It is not recommended that the feedback resistor and capacitor be used to implement a band limiting filter below 100kHz.

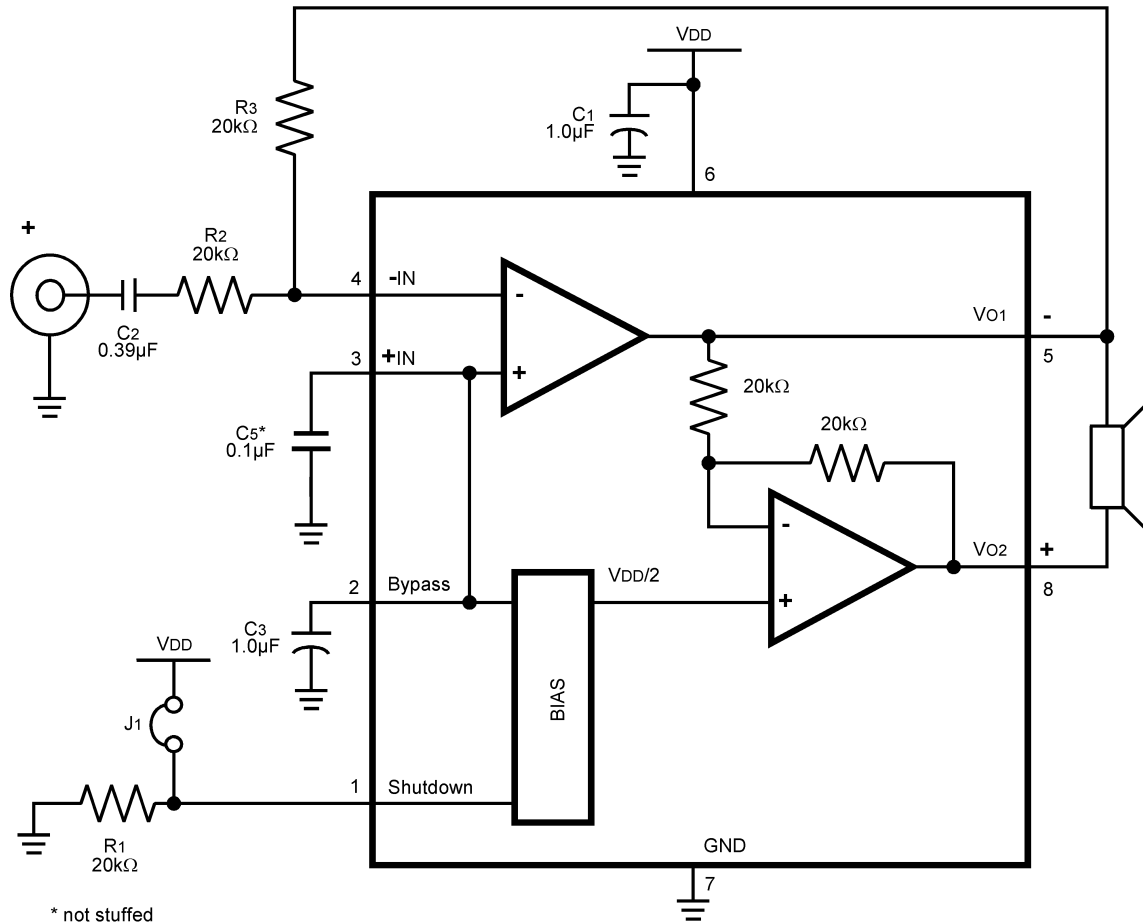
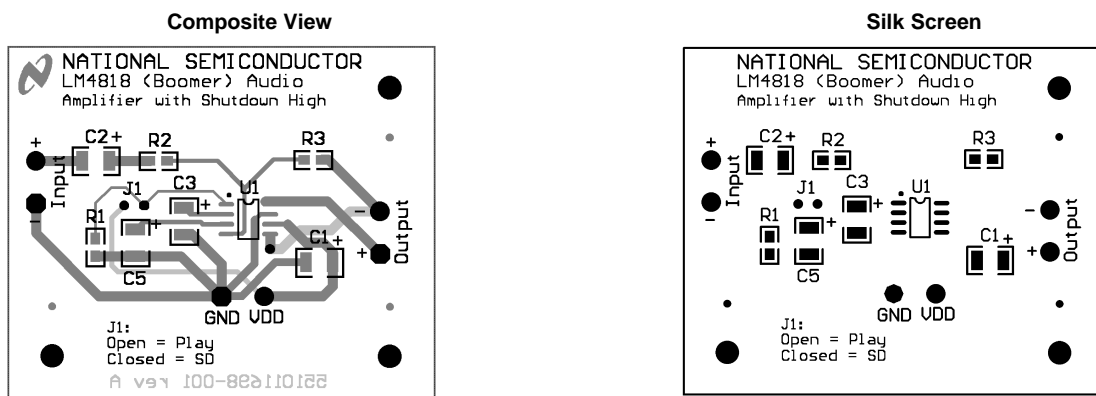
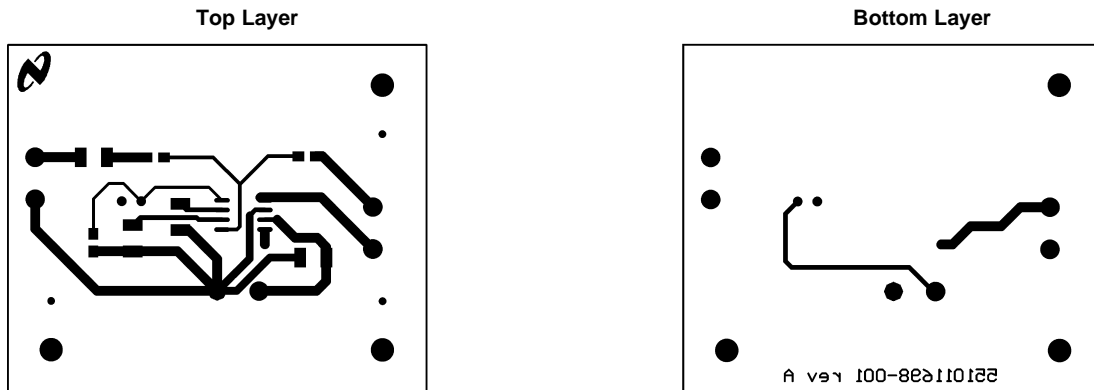


Figure 25. REFERENCE DESIGN BOARD and PCB LAYOUT GUIDELINES

LM4818 SOIC DEMO BOARD ARTWORK





**Table 1. Mono LM4818 Reference Design Boards  
Bill of Material for all Demo Boards**

Item	Part Number	Part Description	Qty	Ref Designator
1	551011208-001	LM4818 Mono Reference Design Board	1	
10	482911183-001	LM4818 Audio AMP	1	U1
20	151911207-001	Tant Cap 1uF 16V 10	1	C1
21	151911207-002	Cer Cap 0.39uF 50V Z5U 20% 1210	1	C2
25	152911207-001	Tant Cap 1uF 16V 10	1	C3
30	472911207-001	Res 20K Ohm 1/10W 5	3	R1, R2, R3
35	210007039-002	Jumper Header Vertical Mount 2X1 0.100	2	J1

## PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

### General Mixed Signal Layout Recommendation

#### *Power and Ground Circuits*

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will take require a greater amount of design time but will not increase the final price of the board. The only extra parts required will be some jumpers.

#### *Single-Point Power / Ground Connections*

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

#### *Placement of Digital and Analog Components*

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

***Avoiding Typical Design / Layout Problems***

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.



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**REVISION HISTORY**

<b>Changes from Revision A (May 2013) to Revision B</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">16</a>

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4818MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM48 18M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4818MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4818MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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