LM3704 Voltage Supervisor With Power-Fail Input, Low-Line Output and Manual Reset

1 Features

- Available Threshold Voltage of 3.08 V and 2.32 V
- No External Components Required
- Manual-Reset Input
- Available in Both Open-Drain and Push-Pull Configuration
- Reset Time-Out Delay of 200 ms
- Separate Power-Fail Comparator
- ±0.5% Reset Threshold Accuracy at Room Temperature
- ±2% Reset Threshold Accuracy Over Temperature
- 28-µA V_{CC} Supply Current

2 Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

3 Description

The LM3704 is a feature-rich, easy-to-use voltage supervisor. It is offered in both push-pull and open-drain configuration with a tight 2% accuracy over temperature.

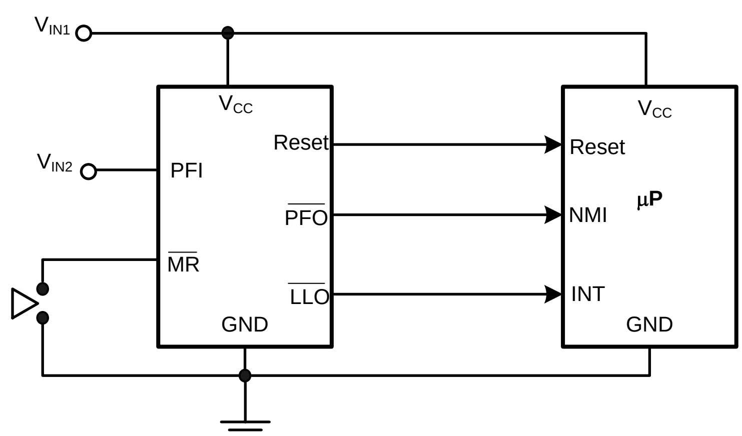
The LM3704 features include a manual reset, low-line output, and power-fail input detection. The power-fail input allows for a configurable second rail to be monitored helping detect upstream failures. The low-line output is used as a second interrupt line to indicate a fall in V_{CC} (1.02 × VRST).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3704	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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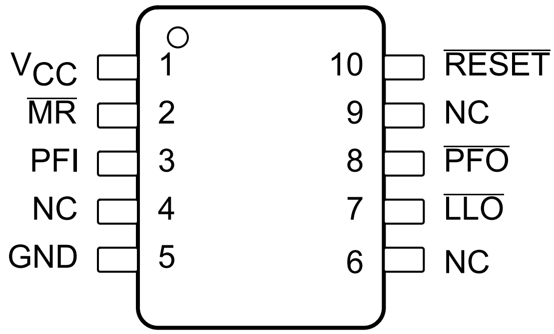
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2012) to Revision F	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{CC}	I	Power supply input.
2	$\overline{MR}$	I	Manual-reset input. When $\overline{MR}$ is less than V_{MRT} (manual reset threshold) $\overline{RESET}$/RESET is engaged.
3	PFI	I	Power-fail comparator input. When PFI is less than V_{PFT} (power-fail reset threshold), the $\overline{PFO}$ goes low. Otherwise, $\overline{PFO}$ remains high.
4	NC	—	No connection.
5	GND	—	Ground reference for all signals.
6	NC	—	No connection.
7	$\overline{LLO}$	O	Low-line logic output. Early power-fail warning output. Low when V_{CC} falls below V_{LLOT} (low-line output threshold). This output can be used to generate an NMI (non-maskable interrupt) to provide an early warning of imminent power failure.
8	$\overline{PFO}$	O	Power-fail logic output. When PFI is below V_{PFT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
9	NC	—	No connection. Test input used at factory only. Leave floating.
10	$\overline{RESET}$	O	Reset logic output. Pulses low for t_{RP} (reset time-out period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.3	6	V
All other inputs	–0.3	V_{CC} + 0.3	V
Power dissipation	See[2]		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, $\theta_{J\text{-}A}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of $\theta_{J\text{-}A}$ for the 10-pin VSSOP package is 195°C/W in a typical printed-circuit board (PCB) mounting and the DSBGA package is 220°C/W.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM3704 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_J = 25°C and V_{CC} = 2.2 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Operating voltage	LM3704, T_J = –40°C to 85°C		1		5.5	V
I_{CC}	V_{CC} supply current	All inputs = V_{CC}, all outputs floating	T_J = 25°C		28		µA
			T_J = –40°C to 85°C			50	
RESET THRESHOLD							
V_{RST}	Reset threshold	V_{CC} falling	T_J = 25°C	–0.5%	V_{RST}	0.5%	
			T_J = –40°C to 85°C	–2%		2%	
			T_J = 0°C to 70°C	–1.5%		1.5%	
V_{RSTH}	Reset threshold hysteresis				0.0032 × V_{RST}		mV
t_{RP}	Reset time-out period	Reset time-out period = C	T_J = 25°C		200		ms
			T_J = –40°C to 85°C	140		280	
t_{RD}	V_{CC} to reset delay	V_{CC} falling at 1 mV/µs			20		µs
$\overline{\text{RESET}}$							
V_{OL}	$\overline{\text{RESET}}$	V_{CC} > 1.0 V, I_{SINK} = 50 µA, T_J = –40°C to 85°C				0.3	V
		V_{CC} > 1.2 V, I_{SINK} = 100 µA, T_J = –40°C to 85°C				0.3	
		V_{CC} > 2.25 V, I_{SINK} = 900 µA, T_J = –40°C to 85°C				0.3	
		V_{CC} > 2.7 V, I_{SINK} = 1.2 mA, T_J = –40°C to 85°C				0.3	
		V_{CC} > 4.5 V, I_{SINK} = 3.2 mA, T_J = –40°C to 85°C				0.4	
V_{OH}	$\overline{\text{RESET}}$	V_{CC} > 2.25 V, I_{SOURCE} = 300 µA, T_J = –40°C to 85°C		0.8 × V_{CC}			V
		V_{CC} > 2.7 V, I_{SOURCE} = 500 µA, T_J = –40°C to 85°C		0.8 × V_{CC}			
		V_{CC} > 4.5 V, I_{SOURCE} = 800 µA, T_J = –40°C to 85°C		V_{CC} − 1.5			
PFI/$\overline{\text{MR}}$							
V_{PFT}	PFI input threshold	T_J = 25°C			1.225		V
		T_J = –40°C to 85°C		1.2		1.25	
V_{MRT}	$\overline{\text{MR}}$ Input threshold	T_J = –40°C to 85°C	$\overline{\text{MR}}$, low			0.8	V
			$\overline{\text{MR}}$, high	2			
V_{PFTH}/ V_{MRTH}	PFI/$\overline{\text{MR}}$ threshold hysteresis	PFI/$\overline{\text{MR}}$ falling, V_{CC} = $V_{RST\ MAX}$ to 5.5 V			0.0032 × V_{RST}		mV
I_{PFI}	Input current (PFI only)	T_J = –40°C to 85°C		–75		75	nA
R_{MR}	$\overline{\text{MR}}$ pullup resistance	T_J = 25°C			56		kΩ
		T_J = –40°C to 85°C		35		75	
t_{MD}	$\overline{\text{MR}}$ to reset delay				12		µS
t_{MR}	$\overline{\text{MR}}$ pulse width	T_J = –40°C to 85°C		25			µS
$\overline{\text{PFO}}$, $\overline{\text{LLO}}$							
V_{OL}	$\overline{\text{PFO}}$, $\overline{\text{LLO}}$ output low voltage	V_{CC} > 2.25 V, I_{SINK} = 900 µA, T_J = –40°C to 85°C				0.3	V
		V_{CC} > 2.7 V, I_{SINK} = 1.2 mA, T_J = –40°C to 85°C				0.3	
		V_{CC} > 4.5 V, I_{SINK} = 3.2 mA, T_J = –40°C to 85°C				0.4	

Electrical Characteristics (continued)

at T_J = 25°C and V_{CC} = 2.2 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	$\overline{PFO}$, $\overline{LLO}$ output high voltage	V_{CC} > 2.25 V, I_{SOURCE} = 300 µA, T_J = –40°C to 85°C		0.8 V_{CC}			V
		V_{CC} > 2.7 V, I_{SOURCE} = 500 µA, T_J = –40°C to 85°C		0.8 V_{CC}			
		V_{CC} > 4.5 V, I_{SOURCE} = 800 µA, T_J = –40°C to 85°C		V_{CC} − 1.5			
$\overline{LLO}$ OUTPUT							
V_{LLOT}	$\overline{LLO}$ output threshold	$V_{\overline{LLO}} - V_{RST}$, V_{CC} falling	T_J = 25°C		1.02 × V_{RST}		V
			T_J = –40°C to 85°C	1.01 × V_{RST}		1.03 × V_{RST}	
V_{LLOTH}	Low-line comparator hysteresis				0.0032 × V_{RST}		mV
t_{CD}	Low-line comparator delay	V_{CC} falling at 1 mV/µs			20		µs

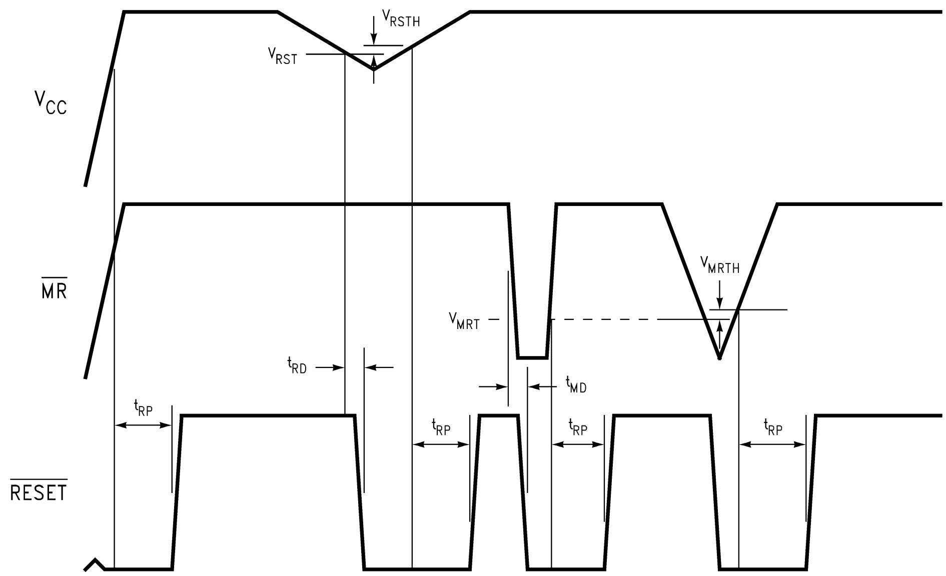


Figure 1. LM3704 Reset Time With $\overline{MR}$

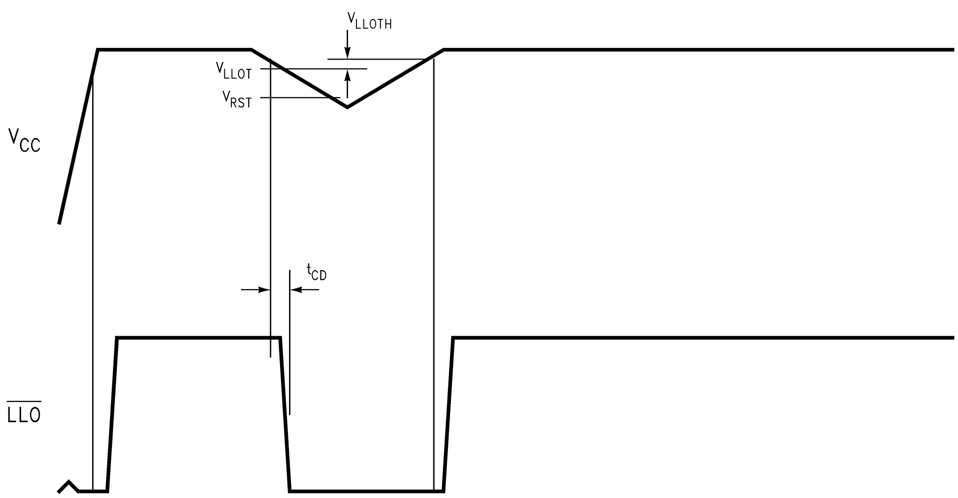


Figure 2. $\overline{LLO}$ Output

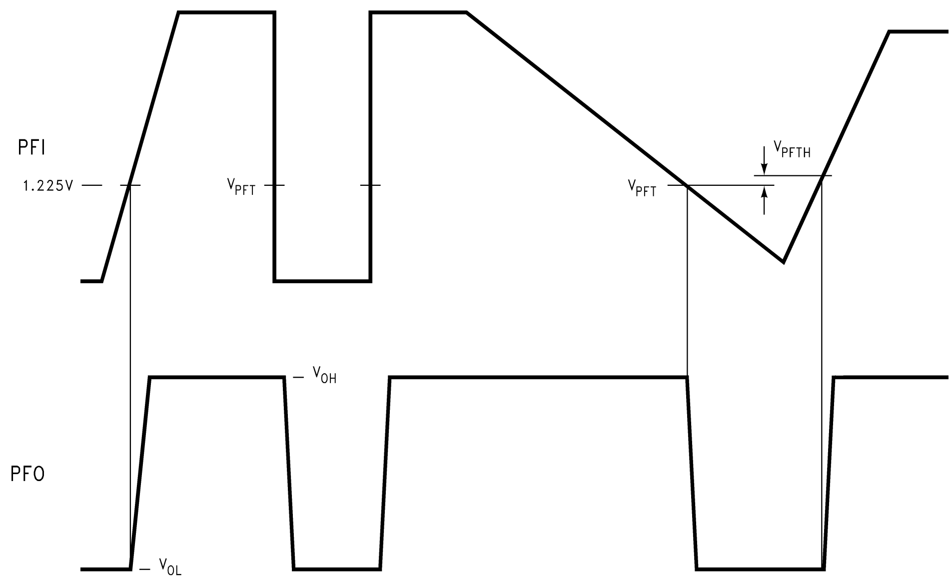


Figure 3. PFI Comparator Timing Diagram

6.6 Typical Characteristics

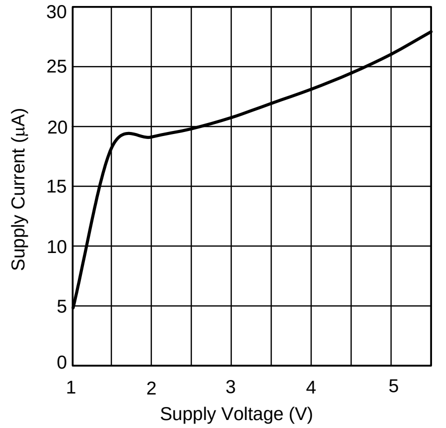


Figure 4. Supply Current vs Supply Voltage

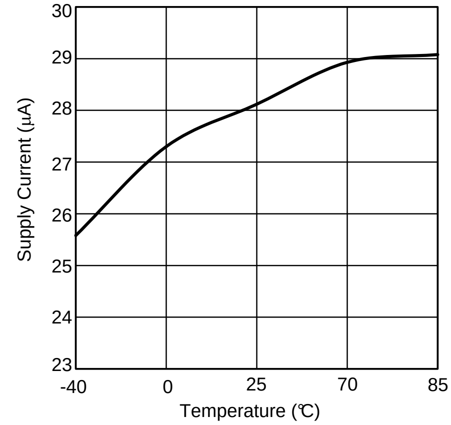


Figure 5. 3.3-V Supply Current vs Temperature

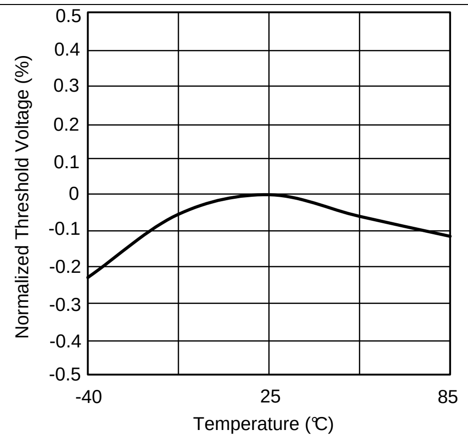


Figure 6. Normalized Reset Threshold Voltage vs Temperature

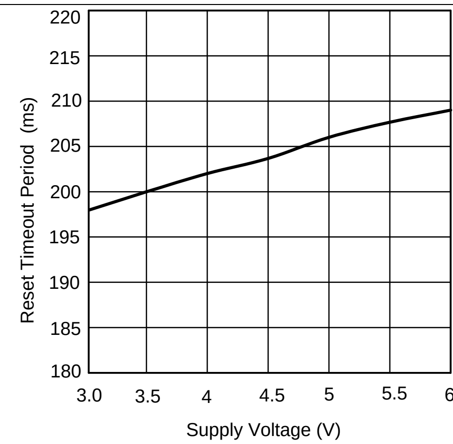


Figure 7. Reset Timeout Period vs V_{CC}

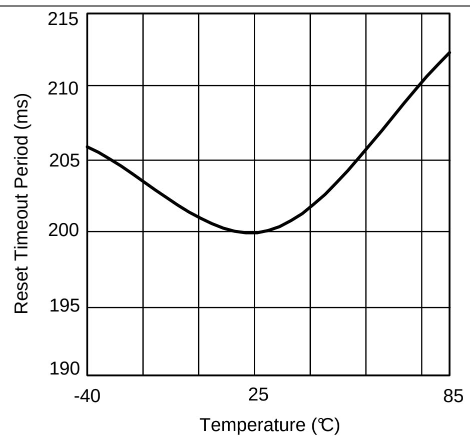
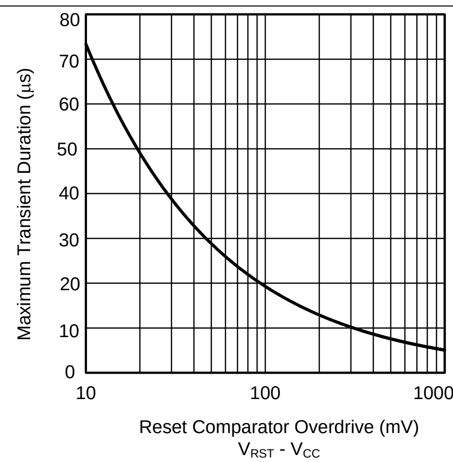


Figure 8. Reset Timeout Period vs Temperature



V_{CC} = 3.3 V

Figure 9. Maximum Transient Duration vs Reset Comparator Overdrive

Typical Characteristics (continued)

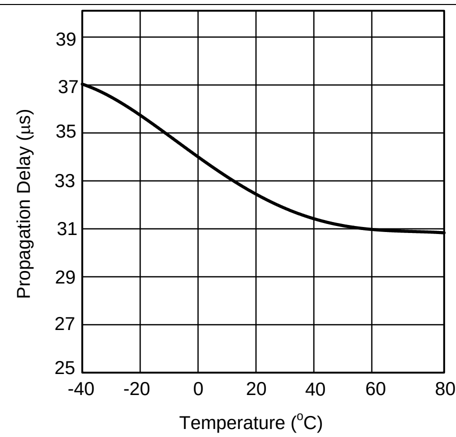


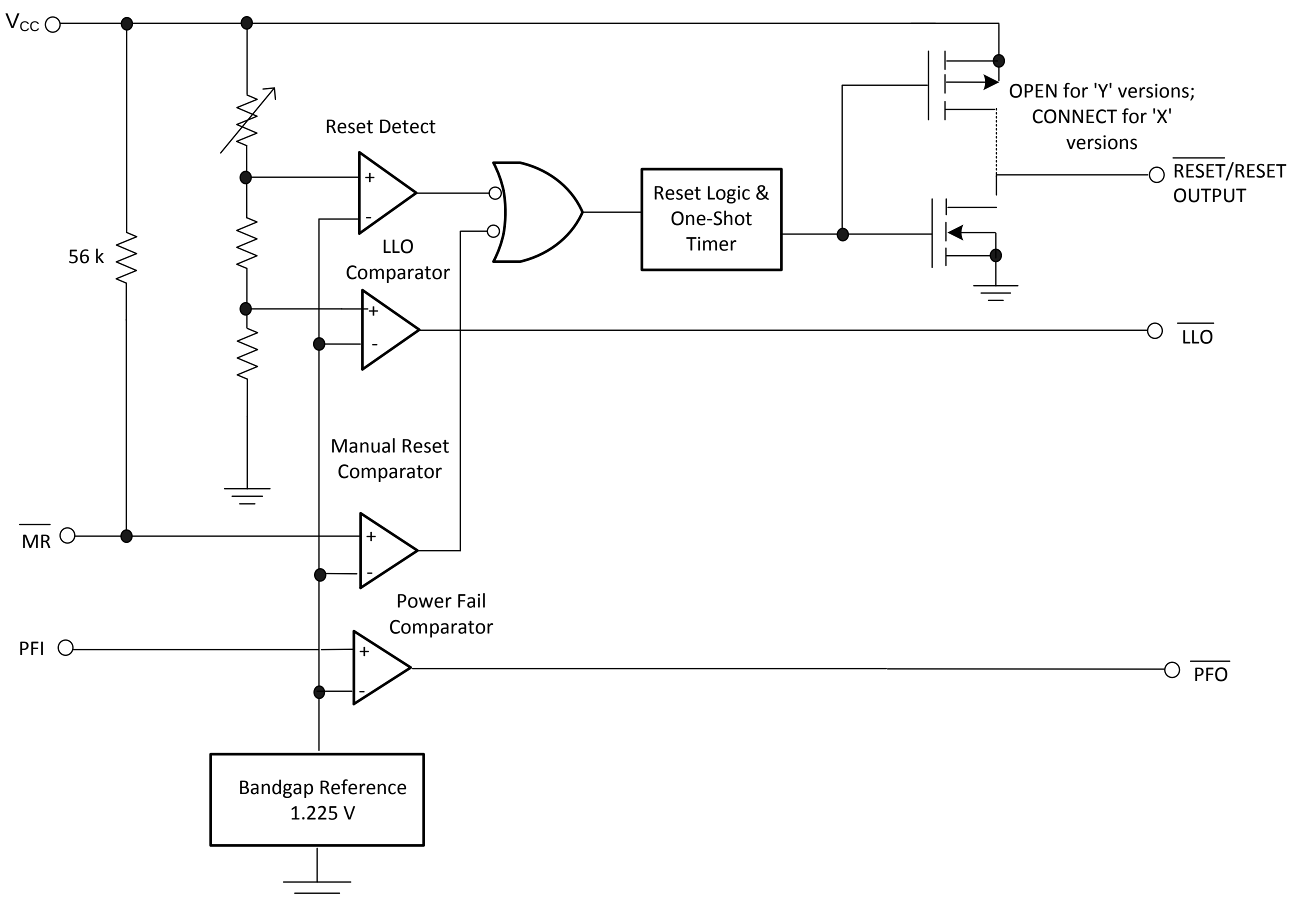
Figure 10. Low-Line Comparator Propagation Delay vs Temperature

7 Detailed Description

7.1 Overview

The LM3704 microprocessor supervisory circuit monitors power supplies and battery-controlled functions in systems and does not require external components. There is a standard reset threshold voltage of 3.08 V while other custom reset threshold voltages are available to provide maximum monitoring flexibility. The $\overline{RESET}$ pin pulses low for the reset time-out period when triggered and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. Once the V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT}, the $\overline{RESET}$ pin remains low for the reset timeout period before coming up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reset Output

The reset input of a µP initializes the device into a known state. The LM3704 microprocessor supervisory circuit asserts a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{RESET}$ is ensured valid for V_{CC} > 1 V. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset time-out period. After this interval, reset goes high. The LM3704 offers an active-low $\overline{RESET}$.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset time-out period. After this time, reset releases.

Feature Description (continued)

The Manual Reset input ($\overline{MR}$) initiates a forced reset also. See *Manual Reset Input ($\overline{MR}$)*.

7.3.2 Reset Threshold

The LM3704 is available with a reset voltage of 3.08 V. Other reset thresholds in the 2.20-V to 5-V range, in steps of 10 mV, are available; contact Texas Instruments for details.

7.3.3 Manual Reset Input ($\overline{MR}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{MR}$ input is fully debounced and provides an internal 56-kΩ pullup. When the $\overline{MR}$ input is pulled below V_{MRT} (1.225 V) for more than 25 µs, reset is asserted after a typical delay of 12 µs. Reset remains active as long as $\overline{MR}$ is held low, and releases after the reset time-out period expires after $\overline{MR}$ rises above V_{MRT}. Use $\overline{MR}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

7.3.4 Power-Fail Comparator (PFI/$\overline{PFO}$)

The PFI is compared to a 1.225-V internal reference, V_{PFT}. If PFI is less than V_{PFT}, the Power-Fail Output ($\overline{PFO}$) drops low. The power-fail comparator signals a falling power supply, and is driven typically by an external voltage divider that senses either the unregulated supply or another system supply voltage. The voltage divider generally is chosen so the voltage at PFI drops below V_{PFT} several milliseconds before the main supply voltage drops below the reset threshold, providing advanced warning of a brownout.

The voltage threshold is set by R_1 and R_2 and is calculated with Equation 1.

$$V_{PFT} = \left(\frac{R1 + R2}{R2}\right) \times 1.225V \quad (1)$$

NOTE

This comparator is completely separate from the rest of the circuitry, and may be employed for other functions as needed.

7.3.5 Low-Line Output ($\overline{LLO}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a µP when V_{CC} begins falling. $\overline{LLO}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 × V_{RST}) with hysteresis of 0.0032 × V_{RST}.

7.4 Device Functional Modes

7.4.1 $\overline{RESET}$ Output Low

Anytime V_{CC} drops below the reset threshold, the $\overline{RESET}$ output drops low and remains low until V_{CC} rises above the threshold and the reset time-out period has expired. The manual reset input ($\overline{MR}$) also causes the reset to be active. If $\overline{MR}$ input is pulled below V_{MRT} for more than 25 µs, the $\overline{RESET}$ output drops low and remains low until $\overline{MR}$ rises above the manual reset threshold (V_{MRT}) and the reset time-out period has expired.

7.4.2 $\overline{RESET}$ Output High

The $\overline{RESET}$ output remains high as long as V_{CC} is above the reset threshold and $\overline{MR}$ is above the manual reset threshold (V_{MRT}).

8 Application and Implementation

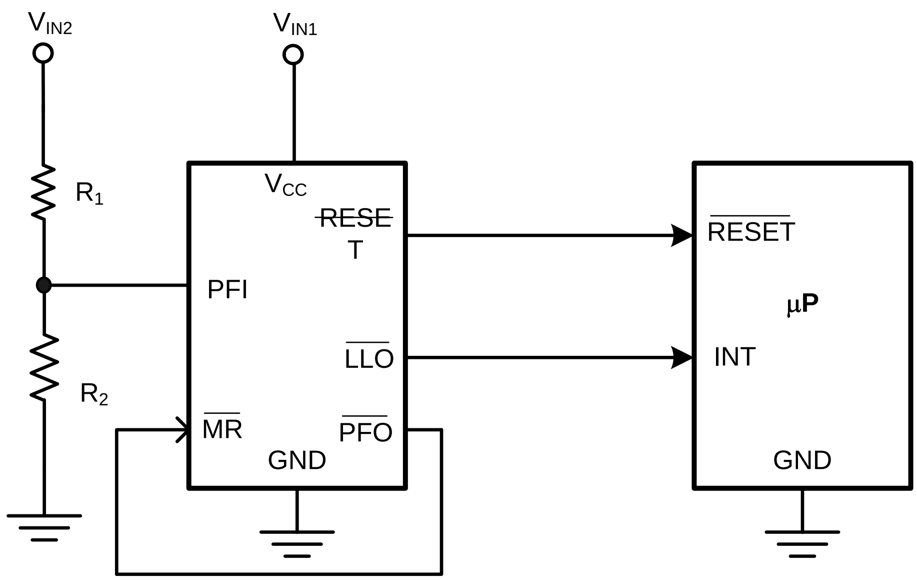
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3704 is a microprocessor supervisory circuit that provides the maximum flexibility for monitoring power supplies and battery-controlled functions. The reset threshold is typically 3.08 V but can be customized for voltages between 2.2 V and 5 V in 10-mV increments by contacting Texas Instruments. The power-fail input, which is a 1.225-V threshold detector for power-fail warning, can be adjusted using a resistor divider as shown in Figure 11. This section shows various application circuits to provide different monitoring solutions.

8.2 Typical Application



Power-Fail Reset Threshold, $V_{PFT} = 1.225\left(\frac{R_1}{R_2} + 1\right)$

Figure 11. Monitoring Two Critical Supplies

8.2.1 Design Requirements

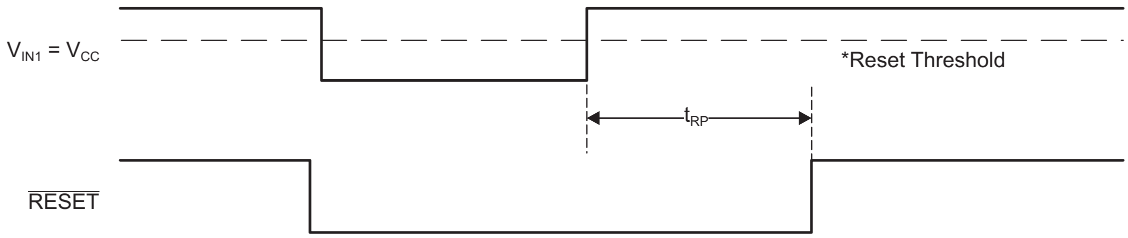
The component count is minimal; employing two resistors as part of a voltage-divider circuit is all that is needed for the typical application of monitoring two critical supplies shown in Figure 11.

8.2.2 Detailed Design Procedure

The voltage-divider circuit that connects to the power-fail reset pin is chosen such that the reset threshold at the device is 1.225 V as shown in Figure 11.

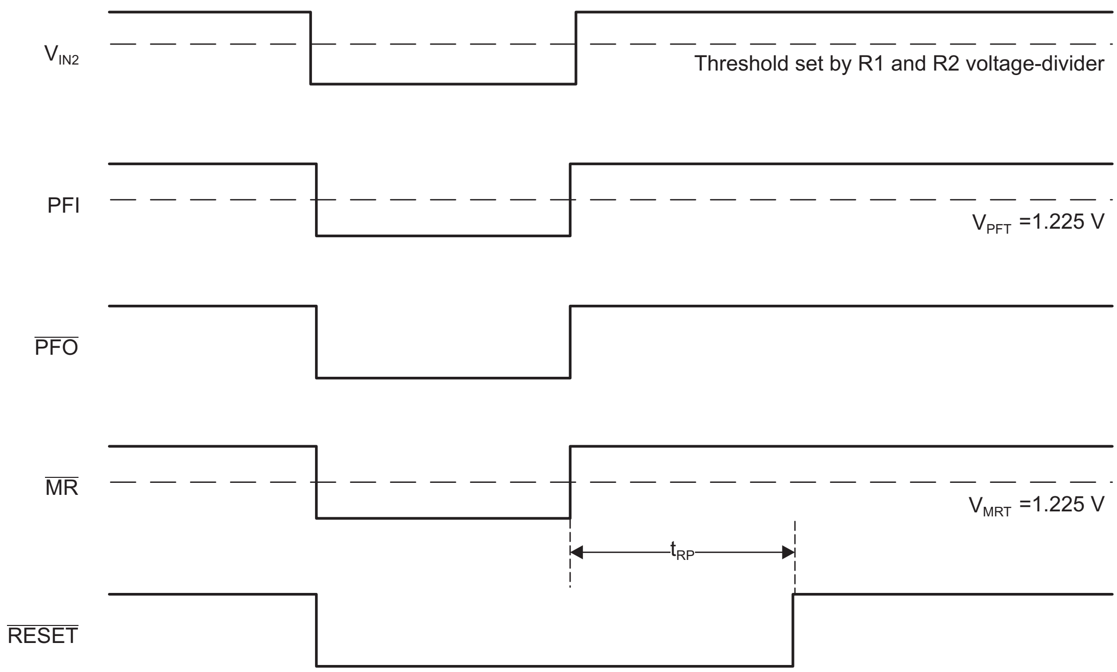
Typical Application (continued)

8.2.3 Application Curves



Standard reset threshold is 3.08 V. Custom reset voltages are available between 2.2 V and 5 V in 10-mV increments by contacting Texas Instruments.

Figure 12. Monitoring V_{IN1} for Reset Condition



See *Electrical Characteristics* for high and low levels of this specific application.

Figure 13. Monitoring V_{IN2} for Reset Condition

8.3 System Examples

The LM3704 voltage supervisor has various features such as power-fail input detection, low-line output, and manual reset while requiring few to no additional components making it versatile and easy-to-use. See Figure 14 through Figure 18 for a variety of circuit applications.

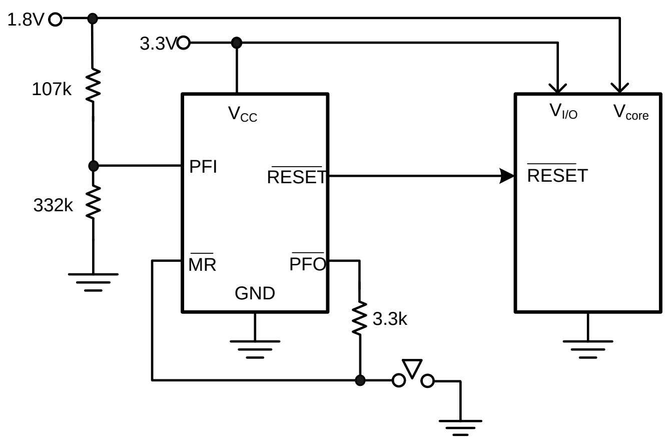


Figure 14. Monitoring Two Supplies Plus Manual Reset

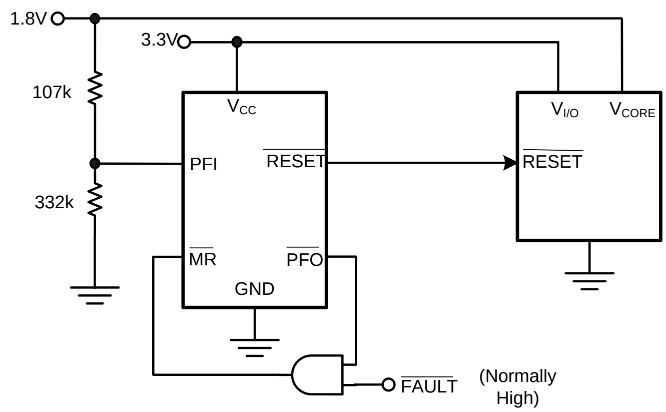
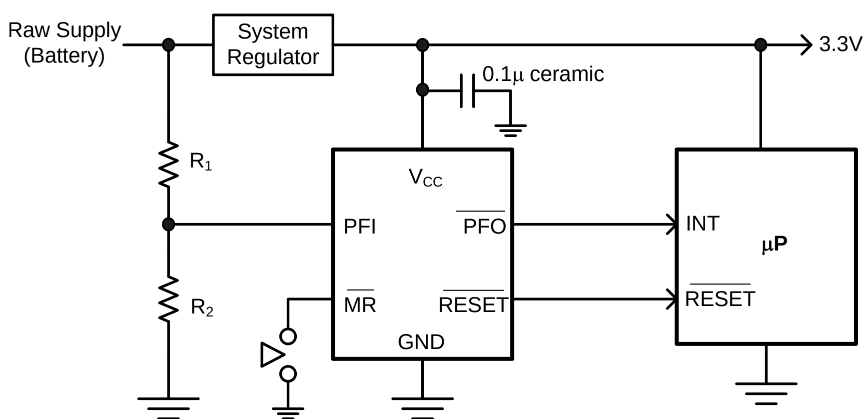


Figure 15. Monitoring Dual Supplies Plus External Fault Input



Power-Fail Reset Threshold, $V_{PFT} = 1.225 \times \left(\frac{R_1}{R_2} + 1\right)$

$\overline{MR}$ input with its 1.225-V nominal threshold, may monitor an additional supply voltage. An internal 56-kΩ pullup resistor is included on this input.

Figure 16. Microprocessor Supervisor With Early Warning Detector

System Examples (continued)

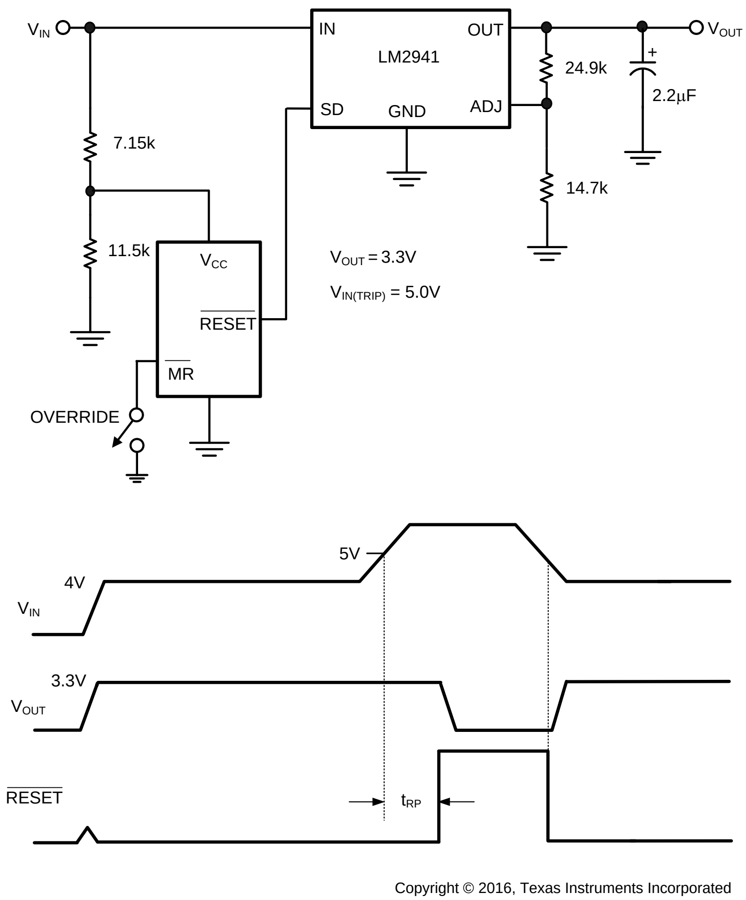


Figure 17. Regulator/Switch With Long-Term Overvoltage Lockout Prevents Overdissipation in Linear Regulator

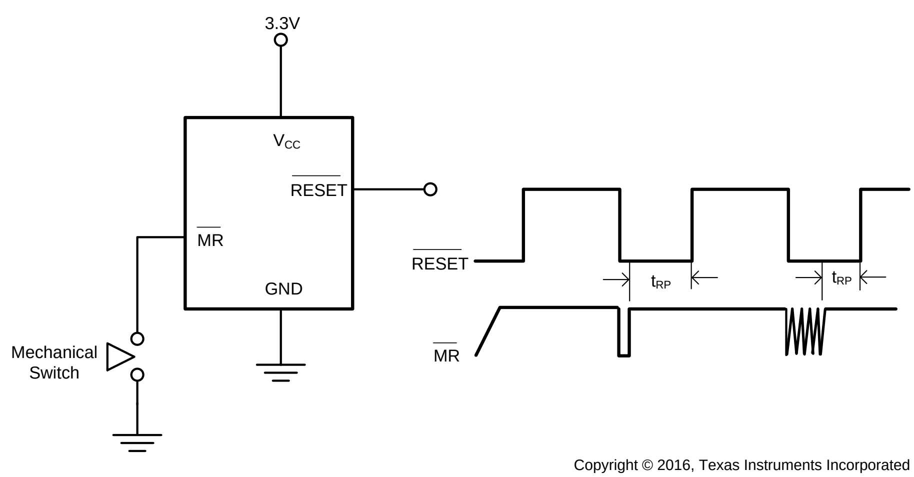


Figure 18. Switch Debouncer

9 Power Supply Recommendations

The input power supply to the V_{CC} pin of the LM3704 must be kept at a voltage lower than the recommended voltage of 5.5 V. All other input pins must be kept at a voltage lower than V_{CC} + 0.3 V. Do not exceed absolute maximum ratings found in *Absolute Maximum Ratings* in any circumstance.

10 Layout

10.1 Layout Guidelines

Keep traces short between IC and external components.

10.2 Layout Example

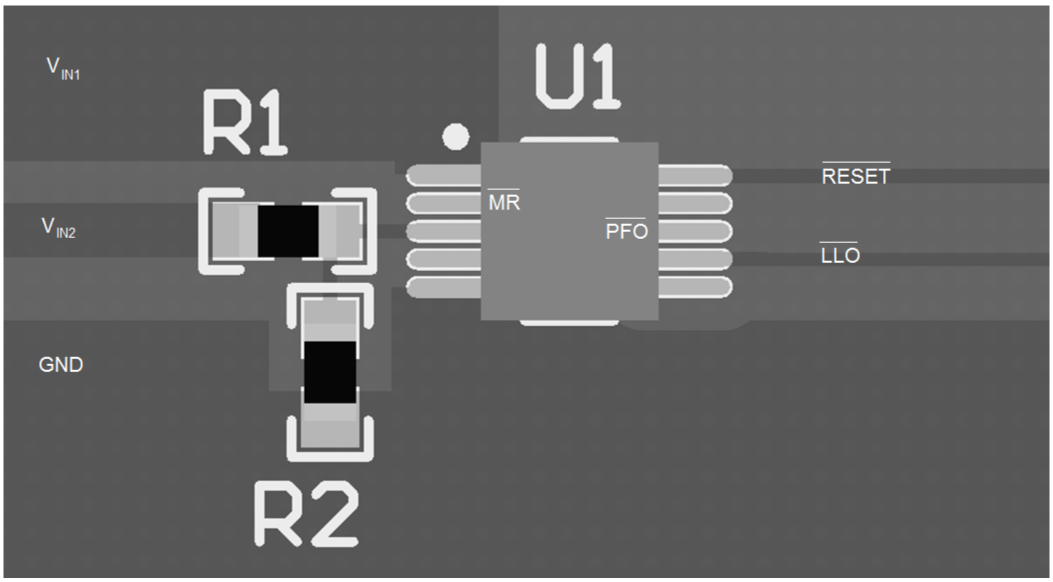


Figure 19. Layout Example for Application Circuit

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 1. Table of Functions

PART NUMBER	OUTPUT (X = TOTEM-POLE) (Y = OPEN-DRAIN)	RESET TIMEOUT PERIOD
LM3704	X, Y	200 ms

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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