LM3150 SIMPLE SWITCHER® CONTROLLER, 42V Synchronous Step-Down

Check for Samples: LM3150

FEATURES

- **PowerWise® Step-down Controller**
- **6V to 42V Wide Input Voltage Range**
- **Adjustable Output Voltage Down to 0.6V**
- **Programmable Switching Frequency up to 1 MHz**
- **No Loop Compensation Required**
- **Fully WEBENCH® Enabled**
- **Low External Component Count**
- **Constant On-Time Control**
- **Ultra-fast Transient Response**
- **Stable with Low ESR Capacitors**
- **Output Voltage Pre-bias Startup**
- **Valley Current Limit**
- **Programmable Soft-start**

TYPICAL APPLICATIONS

- **Telecom**
- **Networking Equipment**
- **Routers**
- **Security Surveillance**
- **Power Modules**

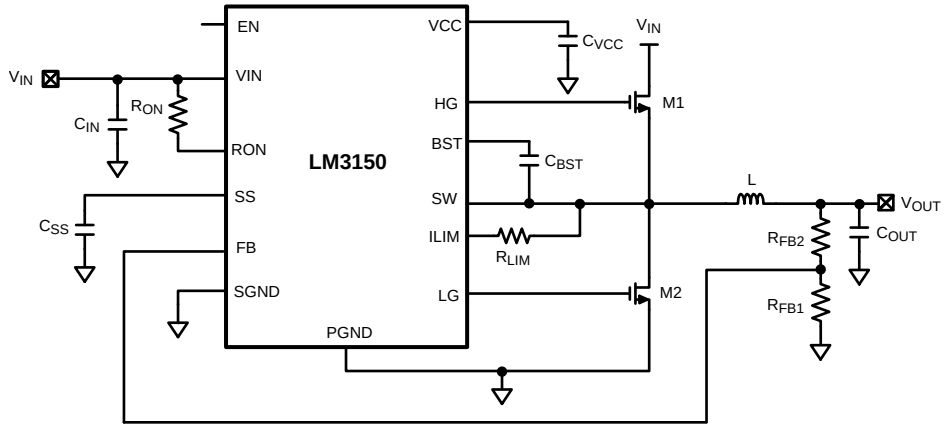
DESCRIPTION

The LM3150 SIMPLE SWITCHER® Controller is an easy to use and simplified step down power controller capable of providing up to 12A of output current in a typical application. Operating with an input voltage range of 6V-42V, the LM3150 features an adjustable output voltage down to 0.6V. The switching frequency is adjustable up to 1 MHz and the synchronous architecture provides for highly efficient designs. The LM3150 controller employs a Constant On-Time (COT) architecture with a proprietary Emulated Ripple Mode (ERM) control that allows for the use of low ESR output capacitors, which reduces overall solution size and output voltage ripple. The Constant On-Time (COT) regulation architecture allows for fast transient response and requires no loop compensation, which reduces external component count and reduces design complexity.

Fault protection features such as thermal shutdown, under-voltage lockout, over-voltage protection, short-circuit protection, current limit, and output voltage pre-bias startup allow for a reliable and robust solution.

The LM3150 SIMPLE SWITCHER® concept provides for an easy to use complete design using a minimum number of external components and TI's WEBENCH® online design tool. WEBENCH® provides design support for every step of the design process and includes features such as external component calculation with a new MOSFET selector, electrical simulation, thermal simulation, and Build-It boards for prototyping.

Typical Application



Connection Diagram

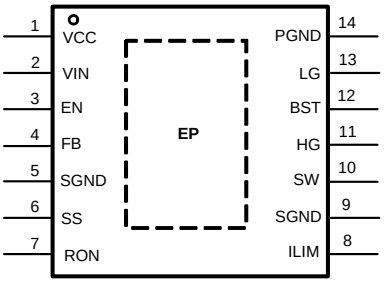


Figure 1. TSSOP-14

PIN DESCRIPTIONS

Pin	Name	Description	Function
1	VCC	Supply Voltage for FET Drivers	Nominally regulated to 5.95V. Connect a 1.0 µF to 4.7 µF decoupling capacitor from this pin to ground.
2	VIN	Input Supply Voltage	Supply pin to the device. Nominal input range is 6V to 42V.
3	EN	Enable	To enable the IC apply a logic high signal to this pin greater than 1.26V typical or leave floating. To disable the part, ground the EN pin.
4	FB	Feedback	Internally connected to the regulation, over-voltage, and short-circuit comparators. The regulation setting is 0.6V at this pin. Connect to feedback resistor divider between the output and ground to set the output voltage.
5,9	SGND	Signal Ground	Ground for all internal bias and reference circuitry. Should be connected to PGND at a single point.
6	SS	Soft-Start	An internal 7.7 µA current source charges an external capacitor to provide the soft-start function.
7	RON	On-time Control	An external resistor from VIN to this pin sets the high-side switch on-time.
8	ILIM	Current Limit	Monitors current through the low-side switch and triggers current limit operation if the inductor valley current exceeds a user defined value that is set by R_{LIM} and the Sense current, I_{LIM-TH}, sourced out of this pin during operation.
10	SW	Switch Node	Switch pin of controller and high-gate driver lower supply rail. A boost capacitor is also connected between this pin and BST pin
11	HG	High-Side Gate Drive	Gate drive signal to the high-side NMOS switch. The high-side gate driver voltage is supplied by the differential voltage between the BST pin and SW pin.
12	BST	Connection for Bootstrap Capacitor	High-gate driver upper supply rail. Connect a 0.33 µF-0.47 µF capacitor from SW pin to this pin. An internal diode charges the capacitor during the high-side switch off-time. Do not connect to an external supply rail.
13	LG	Low-Side Gate Drive	Gate drive signal to the low-side NMOS switch. The low-side gate driver voltage is supplied by VCC.
14	PGND	Power Ground	Synchronous rectifier MOSFET source connection. Tie to power ground plane. Should be tied to SGND at a single point.
EP	EP	Exposed Pad	Exposed die attach pad should be connected directly to SGND. Also used to help dissipate heat out of the IC.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VIN, RON to GND	-0.3V to 47V
SW to GND	-3V to 47V
BST to SW	-0.3V to 7V
BST to GND	-0.3V to 52V
All Other Inputs to GND	-0.3V to 7V
ESD Rating[3]	2 kV
Storage Temperature Range	-65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test Method is per JESD-22-A114.

Operating Ratings[1]

V_{IN}	6V to 42V
Junction Temperature Range (T_J)	−40°C to + 125°C
EN	0V to 5V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Start-Up Regulator, VCC						
VCC		C_{VCC} = 1 µF, 0 mA to 40 mA	**5.65**	5.95	**6.25**	V
VIN - VCC	VIN - VCC Dropout Voltage	I_{VCC} = 2 mA, V_{IN} = 5.5V		40		mV
		I_{VCC} = 30 mA, V_{IN} = 5.5V		330		
I_{VCCL}	VCC Current Limit[1]	VCC = 0V	**65**	100		mA
VCC_{UVLO}	VCC Under-Voltage Lockout Threshold (UVLO)	VCC Increasing	**4.75**	5.1	**5.40**	V
$VCC_{UVLO-HYS}$	VCC UVLO Hysteresis	VCC Decreasing		475		mV
$t_{CC-UVLO-D}$	VCC UVLO Filter Delay			3		µs
I_{IN}	Input Operating Current	No Switching, V_{FB} = 1V		3.5	**5**	mA
I_{IN-SD}	Input Operating Current, Device Shutdown	V_{EN} = 0V		32	**55**	µA
GATE Drive						
I_{Q-BST}	Boost Pin Leakage	$V_{BST} – V_{SW}$ = 6V		2		nA
$R_{DS-HG-Pull-Up}$	HG Drive Pull–Up On-Resistance	I_{HG} Source = 200 mA		5		Ω
$R_{DS-HG-Pull-Down}$	HG Drive Pull–Down On-Resistance	I_{HG} Sink = 200 mA		3.4		Ω
$R_{DS-LG-Pull-Up}$	LG Drive Pull–Up On-Resistance	I_{LG} Source = 200 mA		3.4		Ω
$R_{DS-LG-Pull-Down}$	LG Drive Pull–Down On-Resistance	I_{LG} Sink = 200 mA		2		Ω
Soft-Start						
I_{SS}	SS Pin Source Current	V_{SS} = 0V	**5.9**	7.7	**9.5**	µA
I_{SS-DIS}	SS Pin Discharge Current			200		µA
Current Limit						
I_{LIM-TH}	Current Limit Sense Pin Source Current		75	85	95	µA

(1) VCC provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

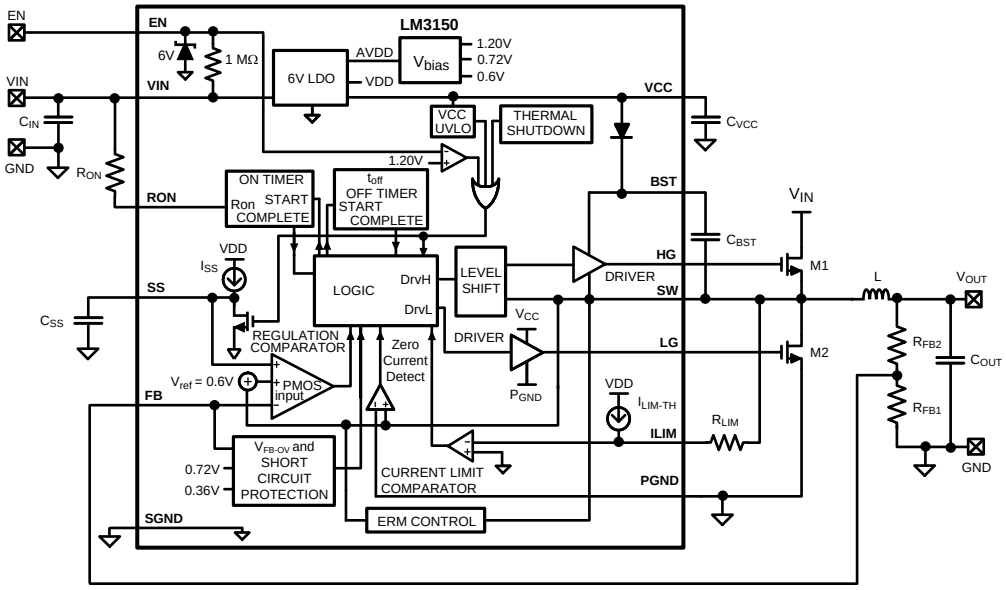
Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ON/OFF Timer						
t_{ON}	ON Timer Pulse Width	V_{IN} = 10V, R_{ON} = 100 kΩ, V_{FB} = 0.6V		1.02		µs
		V_{IN} = 18V, R_{ON} = 100 kΩ, V_{FB} = 0.6V		0.62		
		V_{IN} = 42V, R_{ON} = 100 kΩ, V_{FB} = 0.6V		0.36		
t_{ON-MIN}	ON Timer Minimum Pulse Width	See (2)		200		ns
t_{OFF}	OFF Timer Minimum Pulse Width			370	**525**	ns
Enable Input						
V_{EN}	EN Pin Input Threshold Trip Point	V_{EN} Rising	**1.14**	1.20	**1.26**	V
V_{EN-HYS}	EN Pin Threshold Hysteresis	V_{EN} Falling		120		mV
Regulation and Over-Voltage Comparator						
V_{FB}	In-Regulation Feedback Voltage	V_{SS} > 0.6V	**0.588**	0.600	**0.612**	V
V_{FB-OV}	Feedback Over-Voltage Threshold		**0.690**	0.720	**0.748**	V
I_{FB}	Feedback Bias Current			20		nA
Boost Diode						
V_f	Forward Voltage	I_{BST} = 2 mA		0.7		V
		I_{BST} = 30 mA		1		
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
	Thermal Shutdown Hysteresis	Falling		15		°C
θ_{JA}	Junction to Ambient	4 Layer JEDEC Printed Circuit Board, 9 Vias, No Air Flow		40		°C/W
		2 Layer JEDEC Printed Circuit Board. No Air Flow		140		
θ_{JC}	Junction to Case	No Air Flow		4		°C/W

(2) See Theory of Operation section for minimum on-time when using MOSFETs connected to gate drivers.

Simplified Block Diagram



Typical Performance Characteristics

Boost Diode Forward Voltage vs. Temperature

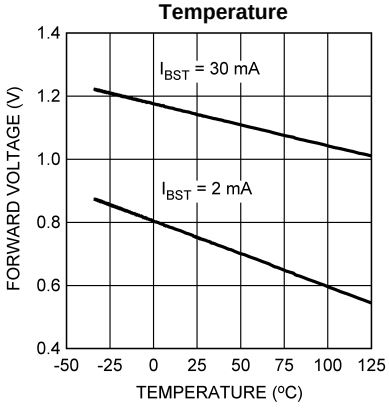


Figure 2.

I_{LIM-TH} vs. Temperature

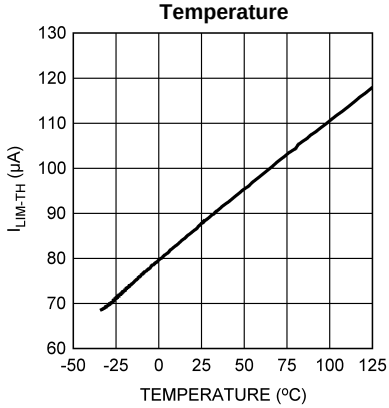


Figure 3.

Quiescent Current vs. Temperature

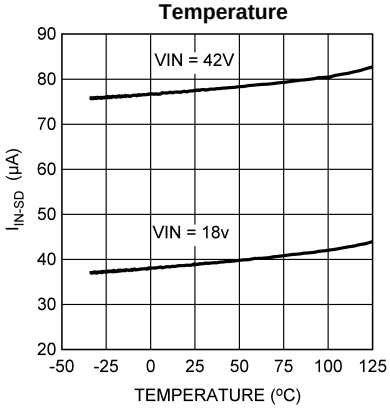


Figure 4.

Soft-Start Current vs. Temperature

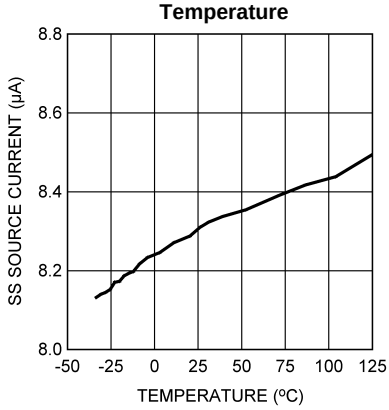


Figure 5.

t_{ON} vs. Temperature

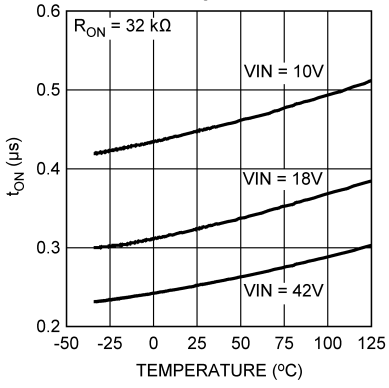


Figure 6.

t_{ON} vs. Temperature

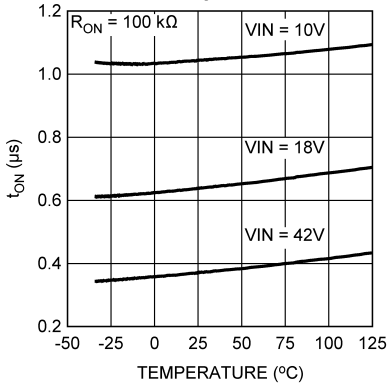


Figure 7.

Typical Performance Characteristics (continued)

t_{ON} vs. Temperature

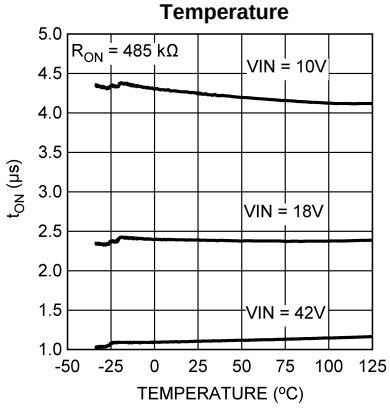


Figure 8.

VCC Current Limit vs. Temperature

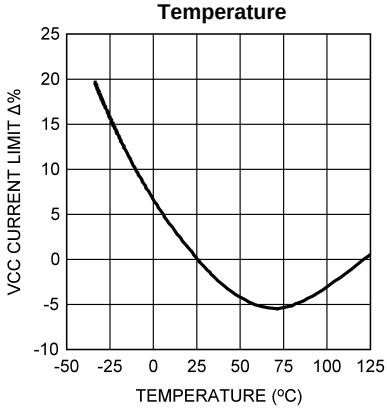


Figure 9.

VCC Dropout vs. Temperature

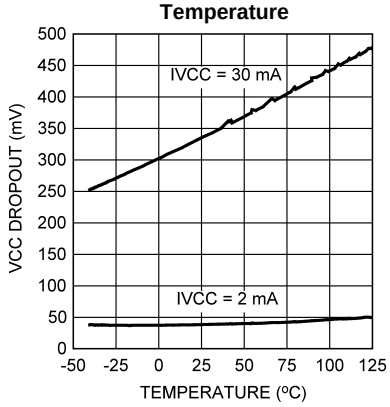


Figure 10.

VCC vs. Temperature

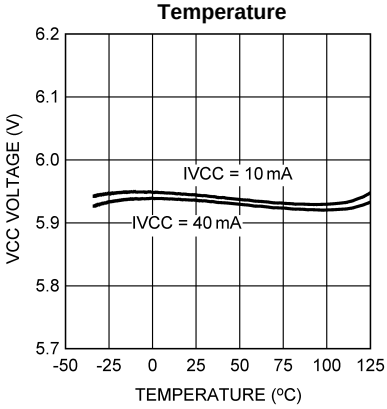


Figure 11.

THEORY OF OPERATION

The LM3150 synchronous step-down SIMPLE SWITCHER® Controller utilizes a Constant On-Time (COT) architecture which is a derivative of the hysteretic control scheme. COT relies on a fixed switch on-time to regulate the output. The on-time of the high-side switch can be set manually by adjusting the size of an external resistor (R_{ON}). To maintain a relatively constant switching frequency as V_{IN} varies, the LM3150 automatically adjusts the on-time inversely with the input voltage. Assuming an ideal system and V_{IN} is much greater than 1V, the following approximations can be made:

The on-time, t_{ON}:

$$t_{ON} = \frac{K \times R_{ON}}{V_{IN}}$$

where

- constant K = 100 pC (1)

The R_{ON} resistance value can be calculated as follows:

$$R_{ON} = \frac{V_{OUT}}{K \times f_S}$$

where

- f_s is the desired switching frequency (2)

Control is based on a comparator and the on-timer, with the output voltage feedback (FB) compared with an internal reference of 0.6V. If the FB level is below the reference, the high-side switch is turned on for a fixed time, t_{ON}, which is determined by the input voltage and the resistor R_{ON}. Following this on-time, the switch remains off for a minimum off-time, t_{OFF}, as specified in the Electrical Characteristics table or until the FB pin voltage is below the reference, then the switch turns on again for another on-time period. The switching will continue in this fashion to maintain regulation. During continuous conduction mode (CCM), the switching frequency ideally depends on duty-cycle and on-time only. In a practical application however, there is a small delay in the time that the HG goes low and the SW node goes low that also affects the switching frequency that is accounted for in the typical application curves. The duty-cycle and frequency can be approximated as:

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_S \approx \frac{V_{OUT}}{V_{IN}} \quad (3)$$

$$f_S = \frac{V_{OUT}}{K \times R_{ON}} \quad (4)$$

Typical COT hysteretic controllers need a significant amount of output capacitor ESR to maintain a minimum amount of ripple at the FB pin in order to switch properly and maintain efficient regulation. The LM3150 however, utilizes a proprietary Emulated Ripple Mode control scheme (ERM) that allows the use of low ESR output capacitors. Not only does this reduce the need for high output capacitor ESR, but also significantly reduces the amount of output voltage ripple seen in a typical hysteretic control scheme. The output ripple voltage can become so low that it is comparable to voltage-mode and current-mode control schemes.

Programming the Output Voltage

The output voltage is set by two external resistors (R_{FB1},R_{FB2}). The regulated output voltage is calculated as follows:

$$V_{OUT} = V_{FB} \times \frac{(R_{FB1} + R_{FB2})}{R_{FB1}}$$

where

- R_{FB2} is the top resistor connected between VOUT and FB
- R_{FB1} is the bottom resistor connected between FB and GND (5)

Regulation Comparator

The feedback voltage at FB is compared to the internal reference voltage of 0.6V. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 0.6V. The high-side switch stays on for the on-time, causing the FB voltage to rise above 0.6V. After the on-time period, the high-side switch stays off until the FB voltage falls below 0.6V.

Over-Voltage Comparator

The over-voltage comparator is provided to protect the output from over-voltage conditions due to sudden input line voltage changes or output loading changes. The over-voltage comparator continuously monitors the voltage at the FB pin and compares it to a 0.72V internal reference. If the voltage at FB rises above 0.72V, the on-time pulse is immediately terminated. This condition can occur if the input or the output load changes suddenly. Once the over-voltage protection is activated, the HG and LG signals remain off until the voltage at FB pin falls below 0.72V.

Current Limit

Current limit detection occurs during the off-time by monitoring the current through the low-side switch using an external resistor, R_{LIM}. If during the off-time the current in the low-side switch exceeds the user defined current limit value, the next on-time cycle is immediately terminated. Current sensing is achieved by comparing the voltage across the low side FET with the voltage across the current limit set resistor R_{LIM}. If the voltage across R_{LIM} and the voltage across the low-side FET are equal then the current limit comparator will terminate the next on-time cycle.

The R_{LIM} value can be approximated as follows:

$$I_{CL} = I_{OCL} - \frac{\Delta I_L}{2} \quad (6)$$

$$R_{LIM} = \frac{I_{CL} \times R_{DS(ON)max}}{I_{LIM-TH}}$$

where

- I_{OCL} is the user-defined average output current limit value
- $R_{DS(ON)max}$ is the resistance value of the low-side FETat the expected maximum FET junction temperature
- I_{LIM-TH} is an internal current supply of 85 µA typical (7)

Figure 12 illustrates the inductor current waveform. During normal operation, the output current ripple is dictated by the switching of the FETs. The current through the low-side switch, I_{valley}, is sampled at the end of each switching cycle and compared to the current limit, I_{CL}, current. The valley current can be calculated as follows:

$$I_{valley} = I_{OUT} - \frac{\Delta I_L}{2}$$

where

- I_{OUT} is the average output current
- ΔI_L is the peak-to-peak inductor ripple current (8)

If an overload condition occurs, the current through the low-side switch will increase which will cause the current limit comparator to trigger the logic to skip the next on-time cycle. The IC will then try to recover by checking the valley current during each off-time. If the valley current is greater than or equal to I_{CL}, then the IC will keep the low-side FET on and allow the inductor current to further decay.

Throughout the whole process, regardless of the load current, the on-time of the controller will stay constant and thereby the positive ripple current slope will remain constant. During each on-time the current ramps-up an amount equal to:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L} \quad (9)$$

The valley current limit feature prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any overload conditions.

Current sensing is achieved by either a low value sense resistor in series with the low-side FET or by utilizing the $R_{DS(ON)}$ of the low-side FET. The $R_{DS(ON)}$ sensing method is the preferred choice for a more simplified design and lower costs. The $R_{DS(ON)}$ value of a FET has a positive temperature coefficient and will increase in value as the FET's temperature increases. The LM3150 controller will maintain a more stable current limit that is closer to the original value that was set by the user, by positively adjusting the I_{LIM-TH} value as the IC temperature increases. This does not provide an exact temperature compensation but allows for a more tightly controlled current limit when compared to traditional $R_{DS(ON)}$ sensing methods when the $R_{DS(ON)}$ value can change typically 140% from room to maximum temperature and cause other components to be over-designed. The temperature compensated I_{LIM-TH} is shown below where T_J is the die temperature of the LM3150 in Celsius:

$$I_{LIM\text{-}TH}(T_J) = I_{LIM\text{-}TH} \times [1 + 3.3 \times 10^{-3} \times (T_J - 27)] \quad (10)$$

To calculate the R_{LIM} value with temperature compensation, substitute equation (10) into $I_{LIM\text{-}TH}$ in equation (7).

Short-Circuit Protection

The LM3150 will sense a short-circuit on the output by monitoring the output voltage. When the feedback voltage has fallen below 60% of the reference voltage, V_{ref} x 0.6 (≈ 0.36V), short-circuit mode of operation will start. During short-circuit operation, the SS pin is discharged and the output voltage will fall to 0V. The SS pin voltage, V_{SS}, is then ramped back up at the rate determined by the SS capacitor and I_{SS} until V_{SS} reaches 0.7V. During this re-ramp phase, if the short-circuit fault is still present the output current will be equal to the set current limit. Once the soft-start voltage reaches 0.7V the output voltage is sensed again and if the V_{FB} is still below V_{ref} x 0.6 then the SS pin is discharged again and the cycle repeats until the short-circuit fault is removed.

Soft-Start

The soft-start (SS) feature allows the regulator to gradually reach a steady-state operating point, which reduces start-up stresses and current surges. At turn-on, while VCC is below the under-voltage threshold, the SS pin is internally grounded and V_{OUT} is held at 0V. The SS capacitor is used to slowly ramp V_{FB} from 0V to 0.6V. By changing the capacitor value, the duration of start-up can be changed accordingly. The start-up time can be calculated using the following equation:

$$t_{SS} = \frac{V_{ref} \times C_{SS}}{I_{SS}}$$

where

- t_{SS} is measured in seconds
- V_{ref} = 0.6V
- I_{SS} is the soft-start pin source current, which is typically 7.7 µA (refer to Electrical Characteristics table) (11)

An internal switch grounds the SS pin if VCC is below the under-voltage lockout threshold, if a thermal shutdown occurs, or if the EN pin is grounded. By using an externally controlled switch, the output voltage can be shut off by grounding the SS pin.

During startup the LM3150 will operate in diode emulation mode, where the low-side gate LG will turn off and remain off when the inductor current falls to zero. Diode emulation mode will allow start-up into a pre-biased output voltage. When soft-start is greater than 0.7V, the LM3150 will remain in continuous conduction mode. During diode emulation mode at current limit the low-gate will remain off when the inductor current is off.

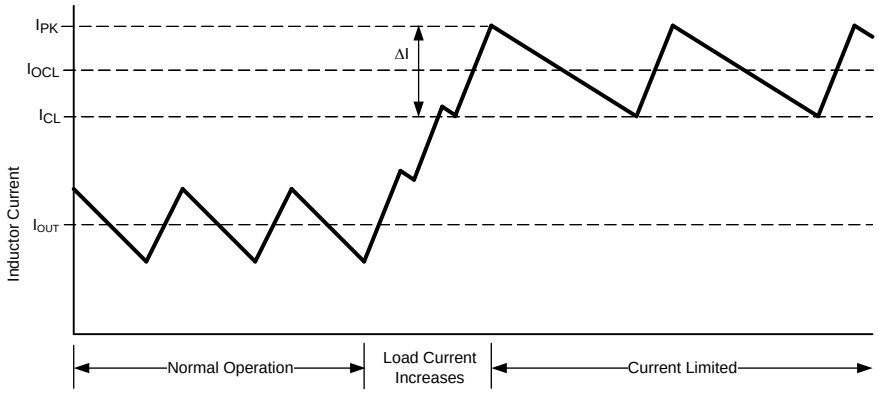


Figure 12. Inductor Current - Current Limit Operation

The soft-start time should be greater than the input voltage rise time and also satisfy the following equality to maintain a smooth transition of the output voltage to the programmed regulation voltage during startup.

$$t_{SS} \geq (V_{OUT} \times C_{OUT}) / (I_{OCL} - I_{OUT}) \quad (12)$$

Enable/Shutdown

The EN pin can be activated by either leaving the pin floating due to an internal pull up resistor to VIN or by applying a logic high signal to the EN pin of 1.26V or greater. The LM3150 can be remotely shut down by taking the EN pin below 1.02V. Low quiescent shutdown is achieved when V_{EN} is less than 0.4V. During low quiescent shutdown the internal bias circuitry is turned off.

The LM3150 has certain fault conditions that can trigger shutdown, such as over-voltage protection, current limit, under-voltage lockout, or thermal shutdown. During shutdown, the soft-start capacitor is discharged. Once the fault condition is removed, the soft-start capacitor begins charging, allowing the part to start-up in a controlled fashion. In conditions where there may be an open drain connection to the EN pin, it may be necessary to add a 1 nF bypass capacitor to this pin. This will help decouple noise from the EN pin and prevent false disabling.

Thermal Protection

The LM3150 should be operated such that the junction temperature does not exceed the maximum operating junction temperature. An internal thermal shutdown circuit, which activates at 165°C (typical), takes the controller to a low-power reset state by disabling the buck switch and the on-timer, and grounding the SS pin. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 150°C the SS pin is released and device operation resumes.

Design Guide

The design guide provides the equations required to design with the LM3150 SIMPLE SWITCHER® Controller. WEBENCH® design tool can be used with or in place of this section for a more complete and simplified design process.

1. Define Power Supply Operating Conditions

a. Required Output Voltage

b. Maximum and Minimum DC Input Voltage

c. Maximum Expected Load Current during Normal Operation

d. Soft-Start Time

2. Set Output Voltage With Feedback Resistors

$$V_{OUT} = V_{FB} \times \frac{(R_{FB1} + R_{FB2})}{R_{FB1}}$$

where

- R_{FB1} is the bottom resistor
- R_{FB2} is the top resistor (13)

3. Determine R_{ON} and f_s

The available frequency range for a given input voltage range, is determined by the duty-cycle, $D = V_{OUT}/V_{IN}$, and the minimum t_{ON} and t_{OFF} times as specified in the Electrical Characteristics table. The maximum frequency is thus, $f_{smax} = D_{min}/t_{ON\text{-}MIN}$. Where $D_{min}=V_{OUT}/V_{IN\text{-}MAX}$, is the minimum duty-cycle. The off-time will need to be less than the minimum off-time t_{OFF} as specified in the Electrical Characteristics table plus any turn off and turn on delays of the MOSFETs which can easily add another 200 ns. The minimum off-time will occur at maximum duty cycle D_{max} and will determine if the frequency chosen will allow for the minimum desired input voltage. The requirement for minimum off-time is $t_{OFF}= (1–D_{max})/f_s \geq (t_{OFF\text{-}MIN} + 200\ ns)$. If t_{OFF} does not meet this requirement it will be necessary to choose a smaller switching frequency f_S.

Choose R_{ON} so that the switching frequency at your typical input voltage matches your f_S chosen above using the following formula:

$$R_{ON} = [(V_{OUT} \times V_{IN}) - V_{OUT}] / (V_{IN} \times K \times f_S) + R_{OND} \quad (14)$$

$$R_{OND} = - [(V_{IN} - 1) \times (V_{IN} \times 16.5 + 100)] - 1000 \quad (15)$$

Use Figure 13 to determine if the calculated R_{ON} will allow for the minimum desired input voltage. If the minimum desired input voltage is not met, recalculate R_{ON} for a lower switching frequency.

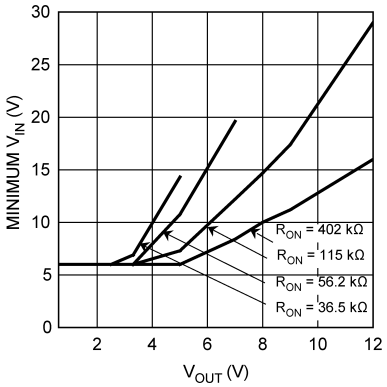


Figure 13. Minimum V_{IN} vs. V_{OUT} I_{OUT} = 10 A

4. Determine Inductor Required Using Figure 14

To use the nomograph in Figure 14, calculate the inductor volt-microsecond constant ET from the following formula:

$$ET = (Vinmax - V_{OUT}) \times \frac{V_{OUT}}{Vinmax} \times \frac{1000}{f_S} \ (V \times \mu s) \quad (16)$$

where

- f_s is in kHz units

The intersection of the Load Current and the Volt-microseconds lines on the chart below will determine which inductors are capable for use in the design. The chart shows a sample of parts that can be used. The offline calculator tools and WEBENCH® will fully calculate the requirements for the components needed for the design.

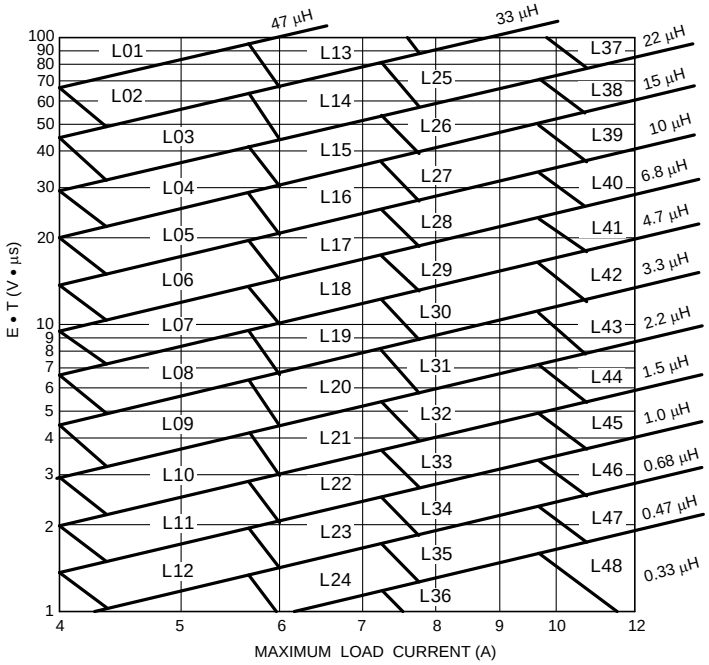


Figure 14. Inductor Nomograph

Table 1. Inductor Selection Table

Inductor Designator	Inductance (µH)	Current (A)	Part Name	Vendor
L01	47	7-9		
L02	33	7-9	SER2817H-333KL	COILCRAFT
L03	22	7-9	SER2814H-223KL	COILCRAFT
L04	15	7-9	7447709150	WURTH
L05	10	7-9	RLF12560T-100M7R5	TDK
L06	6.8	7-9	B82477-G4682-M	EPCOS
L07	4.7	7-9	B82477-G4472-M	EPCOS
L08	3.3	7-9	DR1050-3R3-R	COOPER
L09	2.2	7-9	MSS1048-222	COILCRAFT
L10	1.5	7-9	SRU1048-1R5Y	BOURNS
L11	1	7-9	DO3316P-102	COILCRAFT
L12	0.68	7-9	DO3316H-681	COILCRAFT
L13	33	9-12		
L14	22	9-12	SER2918H-223	COILCRAFT
L15	15	9-12	SER2814H-153KL	COILCRAFT
L16	10	9-12	7447709100	WURTH
L17	6.8	9-12	SPT50H-652	COILCRAFT
L18	4.7	9-12	SER1360-472	COILCRAFT
L19	3.3	9-12	MSS1260-332	COILCRAFT
L20	2.2	9-12	DR1050-2R2-R	COOPER
L21	1.5	9-12	DR1050-1R5-R	COOPER
L22	1	9-12	DO3316H-102	COILCRAFT
L23	0.68	9-12		
L24	0.47	9-12		
L25	22	12-15	SER2817H-223KL	COILCRAFT

Table 1. Inductor Selection Table (continued)

Inductor Designator	Inductance (µH)	Current (A)	Part Name	Vendor
L26	15	12-15		
L27	10	12-15	SER2814L-103KL	COILCRAFT
L28	6.8	12-15	7447709006	WURTH
L29	4.7	12-15	7447709004	WURTH
L30	3.3	12-15		
L31	2.2	12-15		
L32	1.5	12-15	MLC1245-152	COILCRAFT
L33	1	12-15		
L34	0.68	12-15	DO3316H-681	COILCRAFT
L35	0.47	12-15		
L36	0.33	12-15	DR73-R33-R	COOPER
L37	22	15-		
L38	15	15-	SER2817H-153KL	COILCRAFT
L39	10	15-	SER2814H-103KL	COILCRAFT
L40	6.8	15-		
L41	4.7	15-	SER2013-472ML	COILCRAFT
L42	3.3	15-	SER2013-362L	COILCRAFT
L43	2.2	15-		
L44	1.5	15-	HA3778–AL	COILCRAFT
L45	1	15-	B82477-G4102-M	EPCOS
L46	0.68	15-		
L47	0.47	15-		
L48	0.33	15-		

5. Determine Output Capacitance

Typical hysteretic COT converters similar to the LM3150 require a certain amount of ripple that is generated across the ESR of the output capacitor and fed back to the error comparator. Emulated Ripple Mode control built into the LM3150 will recreate a similar ripple signal and thus the requirement for output capacitor ESR will decrease compared to a typical Hysteretic COT converter. The emulated ripple is generated by sensing the voltage signal across the low-side FET and is then compared to the FB voltage at the error comparator input to determine when to initiate the next on-time period.

$$C_{Omin} = 70 / (f_s^2 \times L) \quad (17)$$

The maximum ESR allowed to prevent over-voltage protection during normal operation is:

$$ESR_{max} = (80\ mV \times L \times A_f) / ET_{min} \quad (18)$$

ET_{min} is calculated using V_{IN-MIN}

$A_f = V_{OUT} / 0.6$ if there is no feed-forward capacitor used

$A_f = 1$ if there is a feed-forward capacitor used

The minimum ESR must meet both of the following criteria:

$$ESR_{min} \geq (15\ mV \times L \times A_f) / ET_{max} \quad (19)$$

$$ESR_{min} \geq [\ ET_{max} / (V_{IN} - V_{OUT})\ ] \times (A_f / C_O) \quad (20)$$

ET_{max} is calculated using V_{IN-MAX}.

Any additional parallel capacitors should be chosen so that their effective impedance will not negatively attenuate the output ripple voltage.

6. Determine The Use of Feed-Forward Capacitor

Certain applications may require a feed-forward capacitor for improved stability and easier selection of available output capacitance. Use the following equation to calculate the value of C_{ff}.

$$Z_{FB} = (R_{FB1} \times R_{FB2})/(R_{FB1} + R_{FB2}) \quad (21)$$

$$C_{ff} = V_{OUT}/(V_{IN\text{-}MIN} \times f_S \times Z_{FB}) \quad (22)$$

7. MOSFET and R_{LIM} Selection

The high-side and low-side FETs must have a drain to source (V_{DS}) rating of at least 1.2 x V_{IN}.

Use the following equations to calculate the desired target value of the low-side FET $R_{DS(ON)}$ for current limit.

$$R_{LIM}(T_j) = \frac{I_{CL} \times R_{DS(ON)max}}{I_{LIM\text{-}TH}(T_j)} \quad (23)$$

$$I_{LIM\text{-}TH}(T_j) = I_{LIM\text{-}TH} \times [1 + 3.3 \times 10^{-3} \times (T_j - 27)] \quad (24)$$

The gate drive current from VCC must not exceed the minimum current limit of VCC. The drive current from VCC can be calculated with:

$$I_{VCCdrive} = Q_{gtotal} \times f_S$$

where

- Q_{gtotal} is the combined total gate charge of the high-side and low-side FETs (25)

The plateau voltage of the FET V_{GS} vs Q_g curve, as shown in Figure 15, must be less than VCC - 750 mV.

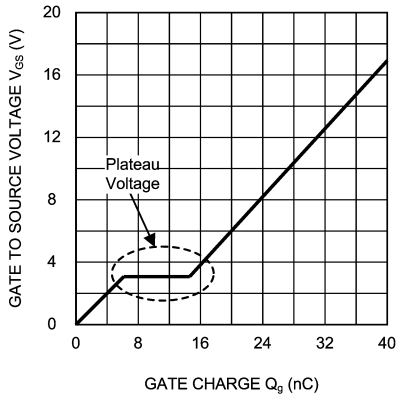


Figure 15. Typical MOSFET Gate Charge Curve

See following design example for estimated power dissipation calculation.

8. Calculate Input Capacitance

The main parameters for the input capacitor are the voltage rating, which must be greater than or equal to the maximum DC input voltage of the power supply, and its rms current rating. The maximum rms current is approximately 50% of the maximum load current.

$$C_{IN} = \frac{Iomax \times D \times (1\text{-}D)}{f_S \times \Delta V_{IN\text{-}MAX}}$$

where

- $\Delta V_{IN\text{-}MAX}$ is the maximum allowable input ripple voltage (26)

A good starting point for the input ripple voltage is 5% of V_{IN}.

When using low ESR ceramic capacitors on the input of the LM3150 a resonant circuit can be formed with the impedance of the input power supply and parasitic impedance of long leads/PCB traces to the LM3150 input capacitors. It is recommended to use a damping capacitor under these circumstances, such as aluminum electrolytic that will prevent ringing on the input. The damping capacitor should be chosen to be approximately 5 times greater than the parallel ceramic capacitors combination. The total input capacitance should be greater than 10 times the input inductance of the power supply leads/pcb trace. The damping capacitor should also be chosen to handle its share of the rms input current which is shared proportionately with the parallel impedance of the ceramic capacitors and aluminum electrolytic at the LM3150 switching frequency.

The C_{BYP} capacitor should be placed directly at the VIN pin. The recommended value is 0.1 µF.

9. Calculate Soft-Start Capacitor

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{ref}}$$

where

- t_{ss} is the soft-start time in seconds
- V_{ref} = 0.6V (27)

10. C_{VCC}, C_{BST} and C_{EN}

C_{VCC} should be placed directly at the VCC pin with a recommended value of 1 µF to 4.7 µF. C_{BST} creates a voltage used to drive the gate of the high-side FET. It is charged during the SW off-time. The recommended value for C_{BST} is 0.47 µF. The EN bypass capacitor, C_{EN}, recommended value is 1000 pF when driving the EN pin from open drain type of signal.

Design Example

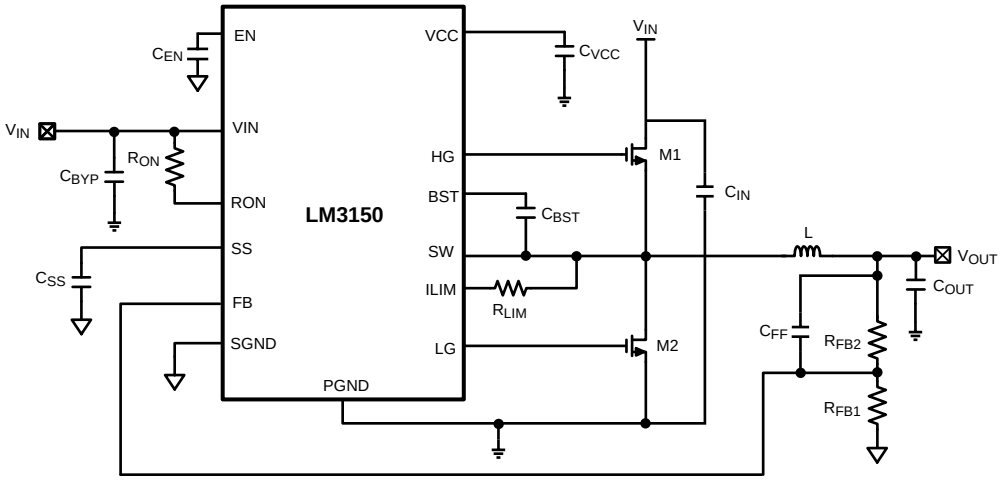


Figure 16. Design Example Schematic

1.Define Power Supply Operating Conditions

a. V_{OUT} = 3.3V

b. V_{IN-MIN} = 6V, V_{IN-TYP} = 12V, V_{IN-MAX} = 24V

c. Typical Load Current = 12A, Max Load Current = 15A

d. Soft-Start time t_{SS} = 5 ms

2. Set Output Voltage with Feedback Resistors

$$R_{FB2} = R_{FB1}\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

$$R_{FB2} = 4.99\ k\Omega\left(\frac{3.3V}{0.6V} - 1\right)$$

$$R_{FB2} = 22.455\ k\Omega$$

R_{FB2} = 22.6 kΩ, nearest 1% standard value.

3. Determine R_{ON} and f_S

$D_{min} = V_{OUT}/V_{IN-MAX}$

D_{min} = 3.3V/24V = 0.137

D_{max} = 3.3V / 6V = 0.55

f_{smax} = 0.137/ 200 ns = 687 kHz

$D_{max} = V_{OUT}/V_{IN-MIN}$

t_{OFF} = (1-0.55)/687 kHz = 654 ns

t_{OFF} should meet the following criteria:

$t_{OFF} > t_{OFF\text{-}MIN}$ + 200 ns

t_{OFF} > 725 ns

At the maximum switching frequency of 687 kHz, which is limited by the minimum on-time, the off-time of 654 ns is less than 725 ns. Therefore the switching frequency should be reduced and meet the following criteria:

$f_s < (1 - D)/725$ ns

$f_S < (1 - 0.55)/725$ ns = 620 kHz

A switching frequency is arbitrarily chosen at 500 kHz which should allow for reasonable size components and satisfies the requirements above.

f_S = 500 kHz

Using f_S = 500 kHz R_{ON} can be calculated as follows:

$R_{ON} = [(V_{OUT} \times V_{IN}) - V_{OUT}] / (V_{IN} \times K \times f_S) + R_{OND}$

$R_{OND} = - [(V_{IN} - 1) \times (V_{IN} \times 16.5 + 100)] - 1000$

$R_{OND} = - [(12 - 1) \times (12 \times 16.5 + 100)] -1000$

R_{OND} = -4.3 kΩ

$R_{ON} = [(3.3 \times 12) - 3.3] / (12 \times 100$ pC $\times 500$ kHz) - 4.3 kΩ

R_{ON} = 56.2 kΩ

Next, check the desired minimum input voltage for R_{ON} using Figure 13. This design will meet the desired minimum input voltage of 6V.

4. Determine Inductor Required

a. ET = (24-3.3) x (3.3/24) x (1000/500) = 5.7 V µs

b. From the inductor nomograph a 12A load and 5.7 V µs calculation corresponds to a L44 type of inductor.

c. Using the inductor designator L44 in Table 1 the Coilcraft HA3778–AL 1.65 µH inductor is chosen.

5. Determine Output Capacitance

The voltage rating on the output capacitor should be greater than or equal to the output voltage. As a rule of thumb most capacitor manufacturers suggests not to exceed 90% of the capacitor rated voltage. In the case of multilayer ceramics the capacitance will tend to decrease dramatically as the applied voltage is increased towards the capacitor rated voltage. The capacitance can decrease by as much as 50% when the applied voltage is only 30% of the rated voltage. The chosen capacitor should also be able to handle the rms current which is equal to:

$$Irmsco = I_{OUT} \times \frac{r}{\sqrt{12}}$$

For this design the chosen ripple current ratio, r = 0.3, represents the ratio of inductor peak-to-peak current to load current I_{OUT}. A good starting point for ripple ratio is 0.3 but it is acceptable to choose r between 0.25 to 0.5. The nomographs in this datasheet all use 0.3 as the ripple current ratio.

$$Irmsco = 12 \times \frac{0.3}{\sqrt{12}}$$

I_{rmsco} = 1A

t_{ON} = (3.3V/12V)/500 kHz = 550 ns

Minimum output capacitance is:

$C_{Omin} = 70 / (f_s^2 \times L)$

$C_{Omin} = 70 / (500$ kHz$^2 \times 1.65$ µH) = 169 µF

The maximum ESR allowed to prevent over-voltage protection during normal operation is:

$ESR_{max} = (80$ mV $\times L \times A_f) / ET$

$A_f = V_{OUT} / 0.6$ without a feed-forward capacitor

A_f = 1 with a feed-forward capacitor

For this design a feed-forward capacitor will be used to help minimize output ripple.

ESR_{max} = (80 mV x 1.65 µH x 1) / 5.7 V µs

ESR_{max} = 23 mΩ

The minimum ESR must meet both of the following criteria:

$ESR_{min} \geq$ (15 mV x L x A_f) / ET

$ESR_{min} \geq$ [ET / (V_{IN} - V_{OUT})] x (A_f / C_O)

$ESR_{min} \geq$ (15 mV x 1.65 µH x 1) / 5.7 V µs = 4.3 mΩ

$ESR_{min} \geq$ [5.7 V µs / (12 - 3.3)] x (1 / 169 µF) = 3.9 mΩ

Based on the above criteria two 150 µF polymer aluminum capacitors with a ESR = 12 mΩ each for a effective ESR in parallel of 6 mΩ was chosen from Panasonic. The part number is EEF-UE0J101P.

6. Determine Use of Feed-Forward Capacitor

From step 5 the capacitor chosen in ESR is small enough that we should use a feed-forward capacitor. This is calculated from:

$$C_{ff} = \frac{V_{OUT}}{V_{IN\text{-}MIN} \times f_s} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1} \times R_{FB2}}$$

$$C_{ff} = \frac{3.3V}{6V \times 500\ kHz} \times \frac{4.99\ k\Omega + 22.6\ k\Omega}{4.99\ k\Omega \times 22.6\ k\Omega} = 269\ pF$$

Let C_{ff} = 270 pF, which is the closest next standard value.

7. MOSFET and R_{LIM} Selection

The LM3150 is designed to drive N-channel MOSFETs. For a maximum input voltage of 24V we should choose N-channel MOSFETs with a maximum drain-source voltage, V_{DS}, greater than 1.2 x 24V = 28.8V. FETs with maximum V_{DS} of 30V will be the first option. The combined total gate charge Q_{gtotal} of the high-side and low-side FET should satisfy the following:

$Q_{gtotal} \leq I_{VCCL} / f_s$

$Q_{gtotal} \leq$ 65 mA / 500 kHz

$Q_{gtotal} \leq$ 130 nC

Where I_{VCCL} is the minimum current limit of VCC, over the temperature range, specified in the Electrical Characteristics table. The MOSFET gate charge Q_g is gathered from reading the V_{GS} vs Q_g curve of the MOSFET datasheet at the V_{GS} = 5V for the high-side, M1, MOSFET and V_{GS} = 6V for the low-side, M2, MOSFET.

The Renesas MOSFET RJK0305DPB has a gate charge of 10 nC at V_{GS} = 5V, and 12 nC at V_{GS} = 6V. This combined gate charge for a high-side, M1, and low-side, M2, MOSFET 12 nC + 10 nC = 22 nC is less than 130 nC calculated Q_{gtotal}.

The calculated MOSFET power dissipation must be less than the max allowed power dissipation, Pdmax, as specified in the MOSFET datasheet. An approximate calculation of the FET power dissipated Pd, of the high-side and low-side FET is given by:

High-Side MOSFET

$Pcond = I_{out}^2 \times R_{DS(ON)} \times D$

$$Psw = \frac{1}{2} \times V_{in} \times I_{out} \times Q_{gd} \times f_s \times \left(\frac{8.5}{Vcc - Vth} + \frac{6.8}{Vth} \right)$$

$Pdh = Pcond + Psw$

$Pcond = 12^2 \times 0.01 \times 0.275 = 0.396W$

$$Psw = \frac{1}{2} \times 12 \times 12 \times 1.5\ nC \times 500\ kHz \times \left(\frac{8.5}{6 - 2.5} + \frac{6.8}{2.5} \right) = 0.278W$$

$Pdh = 0.396 + 0.278 = 0.674W$

The max power dissipation of the RJK0305DPB is rated as 45W for a junction temperature that is 125°C higher than the case temperature and a thermal resistance from the FET junction to case, θ_{JC}, of 2.78°C/W. When the FET is mounted onto the PCB, the PCB will have some additional thermal resistance such that the total system thermal resistance of the FET package and the PCB, θ_{JA}, is typically in the range of 30°C/W for this type of FET package. The max power dissipation, Pdmax, with the FET mounted onto a PCB with a 125°C junction temperature rise above ambient temperature and θ_{JA} = 30°C/W, can be estimated by:

Pdmax = 125°C / 30°C/W = 4.1W

The system calculated Pdh of 0.674W is much less than the FET Pdmax of 4.1W and therefore the RJK0305DPB max allowable power dissipation criteria is met.

Low-Side MOSFET

Primary loss is conduction loss given by:

$P_{dl} = Iout^2 \times R_{DS(ON)} \times (1-D) = 12^2 \times 0.01 \times (1-0.275) = 1W$

Pdl is also less than the Pdmax specified on the RJK0305DPB MOSFET datasheet.

However, it is not always necessary to use the same MOSFET for both the high-side and low-side. For most applications it is necessary to choose the high-side MOSFET with the lowest gate charge and the low-side MOSFET is chosen for the lowest allowed $R_{DS(ON)}$. The plateau voltage of the FET V_{GS} vs Q_g curve must be less than VCC - 750 mV.

The current limit resistor, R_{LIM}, is calculated by estimating the $R_{DS(ON)}$ of the low-side FET at the maximum junction temperature of 100°C. By choosing to go into current limit when the average output load current is 20% higher than the output load current of 12A while the inductor ripple current ratio is 1/3 of the load current will make I_{CL}= 10.4A. Then the following calculation of R_{LIM} is:

$R_{LIM} = (10.4 \times 0.014) / (75 \times 10^{-6}) = 1.9\ k\Omega$

Let R_{LIM} = 1.91 kΩ which is the next standard value.

8. Calculate Input Capacitance

The input capacitor should be chosen so that the voltage rating is greater than the maximum input voltage which for this example is 24V. Similar to the output capacitor, the voltage rating needed will depend on the type of capacitor chosen. The input capacitor should also be able to handle the input rms current, which is a maximum of approximately 0.5 x I_{OUT}. For this example the rms input current is approximately 0.5 x 12A = 6A.

The minimum capacitance with a maximum 5% input ripple ΔV_{IN-MAX} = (0.05 x 12) = 0.6V:

$C_{IN} = [12 \times 0.275 \times (1-0.275)] / [500\ kHz \times 0.6] = 8\ \mu F$

To handle the large input rms current 2 ceramic capacitors are chosen at 10 µF each with a voltage rating of 50V and case size of 1210. Each ceramic capacitor is capable of handling 3A of rms current. A aluminum electrolytic of 5 times the combined input capacitance, 5 x 20 µF = 100 µF, is chosen to provide input voltage filter damping because of the low ESR ceramic input capacitors.

C_{BYP} = 0.1µF ceramic with a voltage rating greater than maximum V_{IN}

9. Calculate Soft-Start Capacitor

The soft start-time should be greater than the input voltage rise time and also satisfy the following equality to maintain a smooth transition of the output voltage to the programmed regulation voltage during startup. The desired soft-start time, tss, of 5 ms also needs to satisfy the equality in equation 12, by using the chosen component values through the previous steps as shown below:

5 ms > (3.3V x 300 µF) / (1.2 x 12A - 12A)

5 ms > 0.412 ms

Since the desired soft-start time satisfies the equality in equation 12, the soft start capacitor is calculated as:

$C_{SS} = (7.7\ \mu A \times 5\ ms) / 0.6V = 0.064\ \mu F$

Let C_{SS} = 0.068 µF, which is the next closest standard value. This should be a ceramic cap with a voltage rating greater than 10V.

10. C_{VCC}, C_{EN}, and C_{BST}

C_{VCC} = 4.7 µF ceramic with a voltage rating greater than 10V

C_{EN} = 1000 pF ceramic with a voltage rating greater than 10V

C_{BST} = 0.47 µF ceramic with a voltage rating greater than 10V

Bill of Materials

Designator	Value	Parameters	Manufacturer	Part Number
C_{BST}	0.47 µF	Ceramic, X7R, 16V, 10%	TDK	C2012X7R1C474K
C_{BYP}	0.1 µF	Ceramic, X7R, 50V, 10%	TDK	C2012X7R1H104K
C_{EN}	1000 pF	Ceramic, X7R, 50V, 10%	TDK	C1608X7R1H102K
C_{FF}	270 pF	Ceramic, C0G, 50V, 5%	Vishay-Bccomponents	VJ0805A271JXACW1BC
C_{IN1}, C_{IN2}	10 µF	Ceramic, X5R, 35V, 20%	Taiyo Yuden	GMK325BJ106KN-T
C_{OUT1}, C_{OUT2}	150 µF	Polymer Aluminum, , 6.3V, 20%	Panasonic	EEF-UE0J151R
C_{SS}	0.068 µF	Ceramic, 0805, 25V, 10%	Vishay	VJ0805Y683KXXA
C_{VCC}	4.7 µF	Ceramic, X7R, 16V, 10%	Murata	GRM21BR71C475KA73L
L1	1.65 µH	Shielded Drum Core, 2.53 mΩ	Coilcraft	HA3778–AL
M1, M2	30V	8 nC, $R_{DS(ON)}$ @4.5V=10 mΩ	Renesas	RJK0305DPB
R_{FB1}	4.99 kΩ	1%, 0.125W	Vishay-Dale	CRCW08054k99FKEA
R_{FB2}	22.6 kΩ	1%, 0.125W	Vishay-Dale	CRCW080522k6FKEA
R_{LIM}	1.91 kΩ	1%, 0.125W	Vishay-Dale	CRCW08051K91FKEA
R_{ON}	56.2 kΩ	1%, 0.125W	Vishay-Dale	CRCW080556K2FKEA
U1	LM3150		Texas Instruments	LM3150MH

PCB Layout Considerations

It is good practice to layout the power components first, such as the input and output capacitors, FETs, and inductor. The first priority is to make the loop between the input capacitors and the source of the low-side FET to be very small and tie the grounds of the low-side FET and input capacitor directly to each other and then to the ground plane through vias. As shown in Figure 17 when the input capacitor ground is tied directly to the source of the low-side FET, parasitic inductance in the power path, along with noise coupled into the ground plane, are reduced.

The switch node is the next item of importance. The switch node should be made only as large as required to handle the load current. There are fast voltage transitions occurring in the switch node at a high frequency, and if the switch node is made too large it may act as an antennae and couple switching noise into other parts of the circuit. For high power designs, it is recommended to use a multi-layer board. The FETs are going to be the largest heat generating devices in the design, and as such, care should be taken to remove the heat. On multi-layer boards using exposed-pad packages for the FETs such as the power-pak SO-8, vias should be used under the FETs to the same plane on the interior layers to help dissipate the heat and cool the FETs. For the typical single FET Power-Pak type FETs, the high-side FET DAP is V_{IN}. The V_{IN} plane should be copied to the other interior layers to the bottom layer for maximum heat dissipation. Likewise, the DAP of the low-side FET is connected to the SW node and the SW node shape should be duplicated to the other PCB layers for maximum heat dissipation.

See the Evaluation Board application note AN-1900 (SNVA371) for an example of a typical multi-layer board layout, and the Demonstration Board Reference Design Application Note for a typical 2 layer board layout. Each design allows for single sided component mounting.

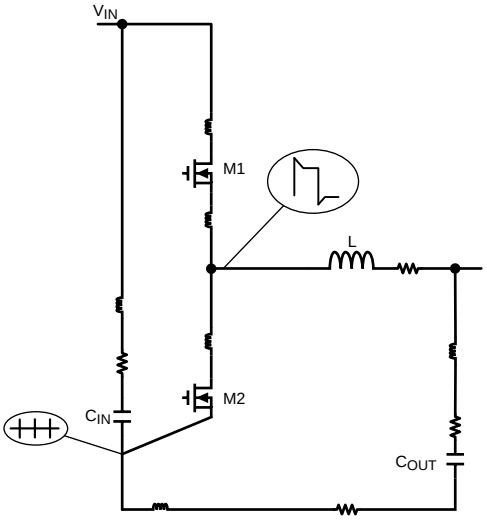


Figure 17. Schematic of Parasitics

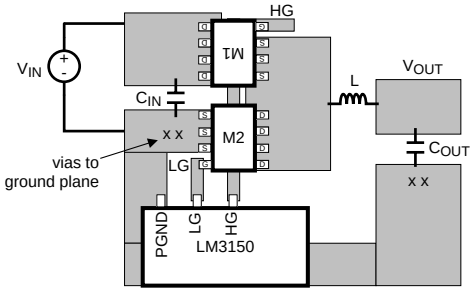


Figure 18. PCB Placement of Power Stage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3150MH/NOPB	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3150 MH	Samples
LM3150MHE/NOPB	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3150 MH	Samples
LM3150MHX/NOPB	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3150 MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

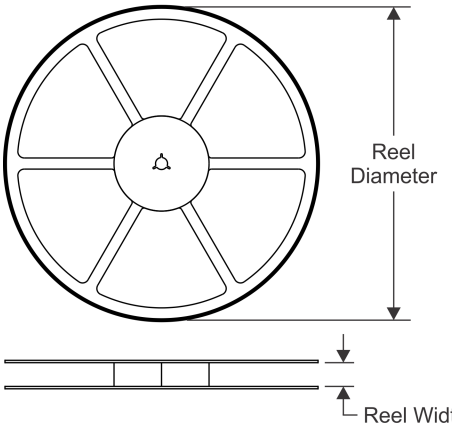
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

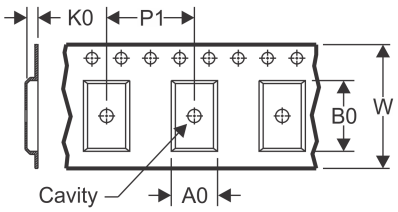
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

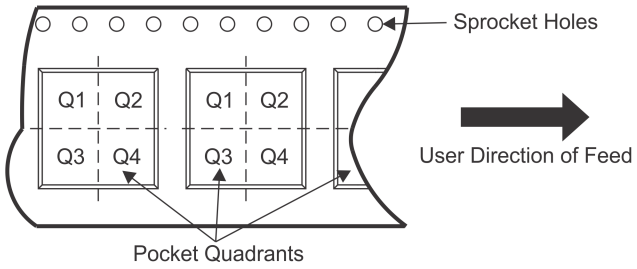


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

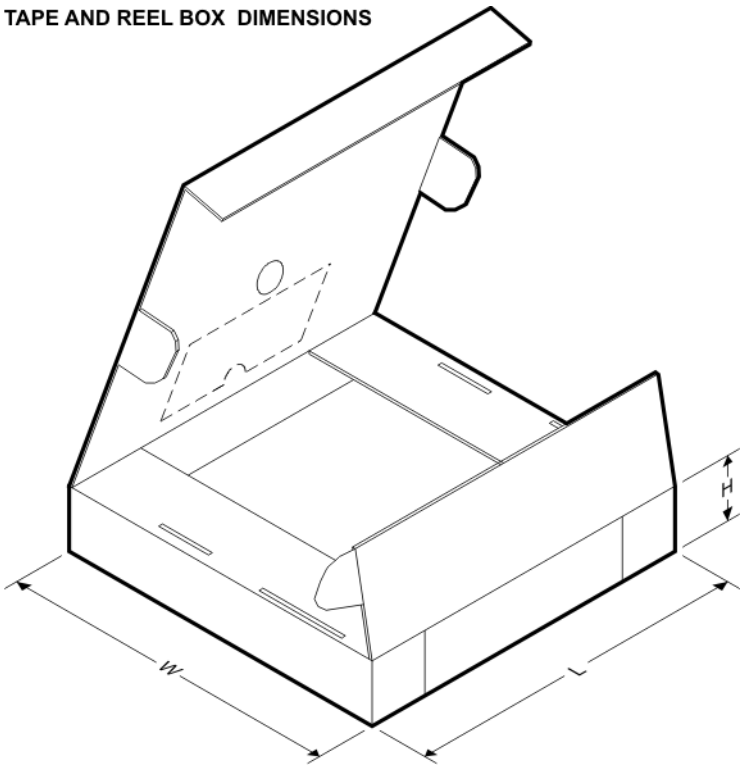
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3150MHE/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM3150MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

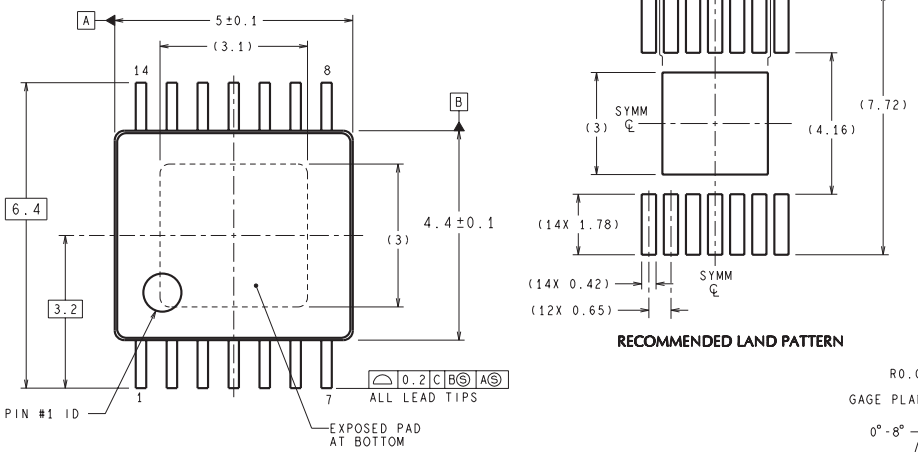
TAPE AND REEL BOX DIMENSIONS



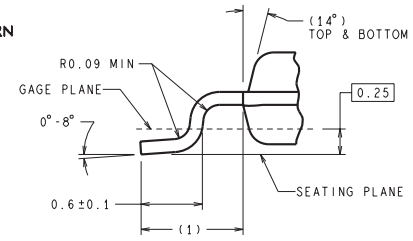
*All dimensions are nominal

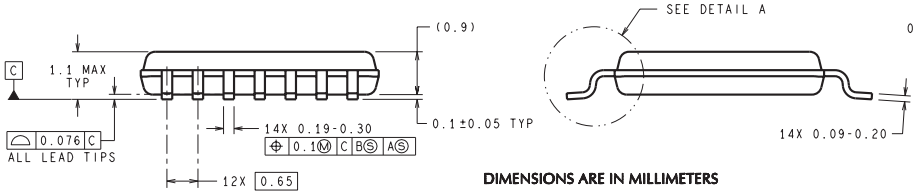
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3150MHE/NOPB	HTSSOP	PWP	14	250	210.0	185.0	35.0
LM3150MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0

PWP0014A



RECOMMENDED LAND PATTERN





DIMENSIONS ARE IN MILLIMETERS

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