Synchronous Buck Controller with Temperature-Compensated, Inductor-DCR-Based Overcurrent Protection and Programmable Thermal Shutdown

Check for Samples: LM27403

FEATURES

- **Up to 97% Efficiency and 93% Duty Cycle**
- **Wide Input Voltage Range of 3 V to 20 V**
- **Switching Frequency from 200 kHz to 1.2 MHz**
- **Inductor-DCR-Based Overcurrent Protection with Thermal Compensation**
- **0.6-V Reference with 1% Feedback Accuracy**
- **30-ns Min On-Time for Low VOUT**
- **Integrated High-Current MOSFET Drivers**
  - **Adaptive Deadtime Control**
- **Ultrafast Line and Load Transient Response**
  - **High GBW Error Amplifier**
  - **PWM Line Feedforward**
- **Integrated VDD Bias Supply LDO Subregulator**
- **Programmable System-Level OTP**
- **Precision Enable with Hysteresis**
- **Frequency Synchronization**
- **Monotonic Prebiased Startup with Soft-Start**
- **Open-Drain Power Good Indicator**
- **4 mm x 4 mm, WQFN-24 PowerPAD™ Package**

APPLICATIONS

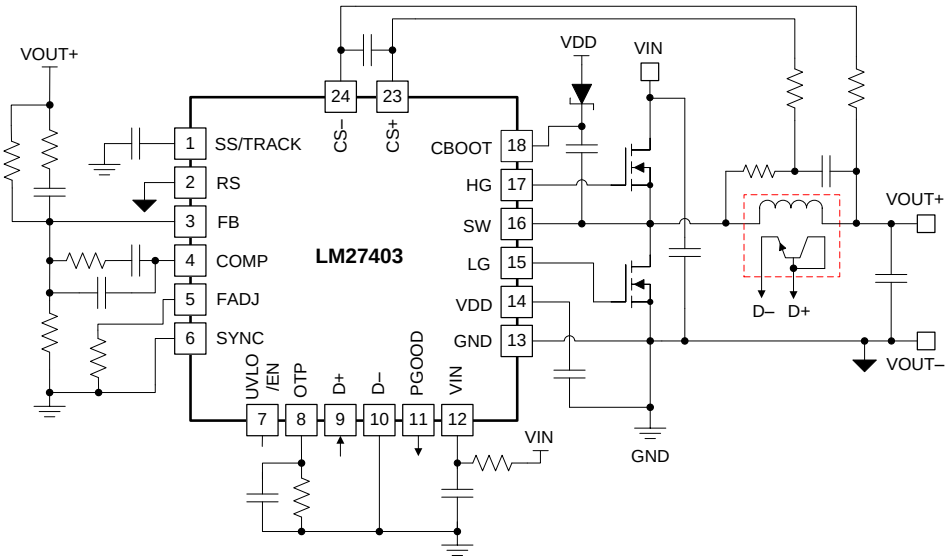
- **DC-DC Converters**
- **High Power Density POL Modules**
- **Telecommunications Infrastructure**
- **Embedded Computing, Servers, Storage**

DESCRIPTION

The LM27403 is a feature-rich, easy-to-use, synchronous buck controller offering exceptional levels of integration and performance for superior efficiency in high power density, point-of-load (POL) DC-DC regulator solutions. The resistor-programmable switching frequency from 200 kHz to 1.2 MHz and integrated, high-current MOSFET gate drivers with adaptive deadtime offer flexibility to optimize solution size and maximize conversion efficiency.

High precision and low output voltage are easily obtained with a 0.6-V, 1% accurate voltage reference together with a 30-ns high-side MOSFET minimum controllable on-time. Using lossless inductor dc resistance (DCR) current sensing and an inexpensive 2N3904 BJT to sense temperature remotely at the inductor, the LM27403 supports accurate and thermally-compensated overcurrent protection (OCP).

TYPICAL APPLICATION DIAGRAM



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DESCRIPTION (CONTINUED)

The LM27403 has a conventional voltage-mode control loop with high gain-bandwidth error amplifier and PWM input voltage feedforward to simplify compensation design and enable excellent transient response throughout the full line voltage and load current ranges. Forced-PWM (FPWM) operation eliminates frequency variation to minimize EMI in sensitive applications. An open-drain Power Good circuit provides power-rail sequencing and fault reporting. Other features include programmable system-level thermal shutdown with automatic recovery, output voltage remote sense, configurable soft-start, monotonic startup into prebiased loads, an integrated bias supply low-dropout (LDO) regulator, external power supply tracking, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), and synchronization capability for beat frequency sensitive and multiregulator applications. The LM27403 is offered in a 4-mm x 4-mm thermally-enhanced WQFN-24 package with 0.5-mm pitch.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VIN, CS+, CS–, SW(3)(4)	–0.3	22	V
	VDD, PGOOD	–0.3	6	V
	SS/TRACK, SYNC, FADJ, COMP, FB, RS	–0.3	V_{VDD} + 0.3	V
	UVLO/EN	–0.3	min (V_{VIN} + 0.3, 6)	V
	CBOOT(5)	–0.3	24	V
	CBOOT to SW	–0.3	6	V
	CS+ to CS–	–1	1	V
	OTP, D+, D–	–0.3	V_{VDD}	V
Thermal	Storage temperature, T_{stg}	–65	150	°C
	Operating junction temperature, T_J	–40	150	°C
Electrostatic discharge (ESD) (6)	Human body model (HBM) QSS 009-105 (JESSD22-A114A)		2	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to the network ground terminal unless otherwise noted.
(3) The SW pin can tolerate negative voltage spikes as low as –10 V and as high as 30 V for a duration up to 10 ns.
(4) Body diode of the low-side MOSFET notwithstanding, parasitic inductance in a real application may result in the SW voltage ringing negative.
(5) The CBOOT pin can tolerate positive voltage spikes as high as 35 V for a duration up to 10 ns.
(6) The human body model (HBM) is a 100-pF capacitor discharged through a 1.5-kΩ resistor to each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		LM27403 RTW (WQFN) 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	31.2	
θ_{JB}	Junction-to-board thermal resistance	11.2	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	11.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)(1).

			MIN	NOM	MAX	UNIT
VIN	Input voltage(2)	VIN tied to VDD	3.0		5.5	V
		VIN	3.0		20	V
SW	SW pin voltage(3)		–0.3		20	V
VDD	VDD pin voltage		2.6	4.7	5.5	V
PGOOD	PGOOD pin voltage		0		5.5	V
UVLO/EN	UVLO/EN pin voltage		0		min (V_{VIN}, 5.5)	V
SS/TRACK	SS/TRACK pin voltage		0		V_{VDD}	V
SYNC	SYNC pin voltage		0		5.5	V
RS	RS pin voltage		–0.1		0.1	V
T_J	Operating junction temperature		–40		+125	°C
T_A	Operating free-air temperature		–40		+125	°C

(1) Recommended Operating Conditions are conditions under which operation of the device is intended to be functional but does not guarantee performance limits.
(2) VDD is the output of the internal linear regulator bias supply. Under normal operating conditions, where VIN is greater than 5.5 V, VDD must not be tied to any external voltage source. In an application where VIN is between 3.0 V and 5.5 V, connecting VIN to VDD maximizes the bias supply rail voltage.
(3) Given the body diode of the low-side MOSFET and the parasitic inductance, the SW voltage should not exceed –3 V in a real application.

ELECTRICAL CHARACTERISTICS

At T_J = –40°C to +125°C and V_{VIN} = 12 V, all parameters at zero power dissipation (unless otherwise noted). Minimum and maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric normal specifications at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPERATIONAL SPECIFICATIONS							
I_Q	Quiescent current	V_{FB} = 0.6 V (not switching)			3.5	5.0	mA
I_{Q-SD}	Shutdown quiescent current	$V_{UVLO/EN}$ = 0 V			25	45	µA
REFERENCE							
V_{FB}	FB pin voltage accuracy			594	600	606	mV
I_{FB}	FB pin bias current	V_{FB} = 0.65 V		–165	0	165	nA
INTERNAL UVLO							
UVLO	Input undervoltage lockout	V_{VIN} rising, V_{VDD} rising		2.6	2.7	2.8	V
UVLO_hys	UVLO hysteresis	V_{VIN} falling, V_{VDD} falling			250		mV
SWITCHING							
F_{SW}	Switching frequency	R_{FADJ} = 4.12 kΩ		925	1050	1150	kHz
		R_{FADJ} = 20 kΩ		435	500	555	kHz
		R_{FADJ} = 95.3 kΩ		185	215	250	kHz
D_{MAX}	Maximum duty cycle	F_{SW} = 500 kHz		90%	93%		
$T_{OFF-MIN}$	Minimum off-time	V_{FB} = 0.5 V, F_{SW} = 500 kHz		110	150	190	ns
T_{ON-MIN}	Minimum controllable on-time	V_{FB} = 0.7 V, F_{SW} = 500 kHz			30		ns
VDD SUBREGULATOR AND BOOT							
V_{DD}	Subregulator output voltage	I_{VDD} = 25 mA		4.2	4.7	5.3	V
VDD_{VDO}	Dropout voltage	I_{VDD} = 15 mA, V_{VIN} = 3.0 V			150		mV
VDD_{CL}	VDD current limit	V_{VDD} = 4.0 V			106		mA
I_{QBOOT}	CBOOT pin leakage current	$V_{CBOOT} – V_{SW}$ = 4.5 V			0.5		nA
ERROR AMPLIFIER							
BW_{-3dB}	Error amplifier open-loop bandwidth				6		MHz
A_{VOL}	Error amplifier dc gain				70		dB
I_{SOURCE}	COMP source current	V_{FB} = 0.5 V			1		mA
I_{SINK}	COMP sink current	V_{FB} = 0.7 V			100		µA
$V_{COMP-MAX}$	Maximum COMP voltage	V_{FB} = 0.5 V			3.9		V
$V_{COMP-MIN}$	Minimum COMP voltage	V_{FB} = 0.7 V			0.5		V
OVERCURRENT PROTECTION							
V_{CS_OFFSET}	Current limit comparator offset voltage			–3.5	0	3.5	mV
I_{CS}	Current limit offset current	$V_{CS–}$ = 3 V, ΔV_{BE} = 59.4 mV(1), T_J = 25°C		9.3	9.9	10.5	µA
		$V_{CS–}$ = 3 V, D+ shorted to D–		3.4	5.0	6.6	µA
I_{CS-CV1}	I_{CS} compliance voltage	$V_{VIN} – V_{CS–}$, ΔI_{CS} < 5%	V_{VIN} = 12 V			800	mV
I_{CS-CV2}			V_{VIN} = 3 V			800	mV
I_{CS-TC}	I_{CS} temperature coefficient	Referenced to ΔV_{BE}(2)		160	187	212	nA/mV
$T_{CL-DELAY}$	Current limit hiccup delay				5		ms
GATE DRIVERS							
$R_{DS(ON)1}$	High-side MOSFET driver on-state resistance	$V_{CBOOT} – V_{SW}$ = 4.5 V	I_{HG} = 0.1 A (pullup)		1.5		Ω
$R_{DS(ON)2}$			I_{HG} = –0.1 A (pulldown)		1.0		Ω
$I_{DRV-HG-SRC}$	High-side MOSFET driver peak current	C_{LOAD} = 3 nF	Source current (pullup)		1.5		A
$I_{DRV-HG-SINK}$			Sink current (pulldown)		2.0		A

(1) The specified parameter is calculated based on a 2N3904 transistor at 25°C.
(2) Multiply by 19.9 to scale from nA/mV to ppm/°C (assumes 2N3904 BJT temperature sensor with ideality factor η =1.004).

ELECTRICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C and V_{VIN} = 12 V, all parameters at zero power dissipation (unless otherwise noted). Minimum and maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric normal specifications at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{DS(ON)3}$	Low-side MOSFET driver on-state resistance	V_{DD} = 4.5 V	I_{LG} = 0.1 A (pullup)		1.5		Ω
$R_{DS(ON)4}$			I_{LG} = –0.1 A (pulldown)		0.9		Ω
$I_{DRV-LG-SRC}$	Low-side MOSFET driver peak current	C_{LOAD} = 3 nF	Source current (pullup)		1.5		A
$I_{DRV-LG-SINK}$			Sink current (pulldown)		2.0		A
T_{DEAD}	Adaptive dead-time				15		ns
SOFT-START							
I_{SS}	Soft-start source current	$V_{SS/TRACK}$ = 0 V		1.0	3.0	5.0	µA
I_{SS-PD}	Soft-start pulldown resistance	$V_{SS/TRACK}$ = 0.6 V			330		Ω
T_{SS-INT}	Internal soft-start timeout				1.28		ms
POWER GOOD							
I_{PGS}	PGOOD low sink current	V_{PGOOD} = 0.2 V, V_{FB} = 0.75 V		70	100		µA
I_{PGL}	PGOOD leakage current	V_{PGOOD} = 5 V			1	10	µA
OVT	Overvoltage threshold	V_{FB} rising, RS tied to GND		111%	116.5%	123%	
OVT_{HYS}	OVT hysteresis	V_{FB} falling, RS tied to GND			3.5%		
UVT	Undervoltage threshold	V_{FB} rising, RS tied to GND		86%	91%	97%	
UVT_{HYS}	UVT hysteresis	V_{FB} falling, RS tied to GND			4%		
$t_{deglitch}$	Deglitch time	V_{PGOOD} rising and falling			20		µs
UVLO/ENABLE							
V_{UVLO1}	Logic low threshold	$V_{UVLO/EN}$ falling		0.94	0.985	1.03	V
V_{UVLO2}	Logic high threshold	$V_{UVLO/EN}$ rising		1.11	1.15	1.18	V
$V_{UVLO-HYS}$	UVLO/EN voltage hysteresis	$V_{UVLO/EN}$ falling		139	165	190	mV
I_{UVLO1}	UVLO/EN pullup current, disabled	$V_{UVLO/EN}$ = 0 V		0.8	1.8	2.7	µA
I_{UVLO2}	UVLO/EN pullup current, enabled	$V_{UVLO/EN}$ = 1.25 V		5.5	10.5	15.5	µA
CLOCK SYNCHRONIZATION							
$V_{IH-SYNC}$	SYNC pin V_{IH}			2			V
$V_{IL-SYNC}$	SYNC pin V_{IL}					0.8	V
$SYNC_{FSW-L}$	Minimum clock sync frequency			200			kHz
$SYNC_{FSW-H}$	Maximum clock sync frequency					1.2	MHz
$SYNC_I$	SYNC pin input current				1		µA
EXTERNAL TEMPERATURE SENSE AND THERMAL SHUTDOWN							
I_{D+1}	D+ pin state 1 current				10		µA
I_{D+2}	D+ pin state 2 current				100		µA
I_{OTP}	Remote thermal current	ΔV_{BE} = 79.3 mV(3)		13.5	14.6	15.5	µA
I_{OTP-TC}	I_{OTP} temperature coefficient	Referenced to ΔV_{BE}(4)		158	187	213	nA/mV
V_{TRIP}	Remote thermal trip point				1.15		V
$V_{TRIP-HYS}$	Remote thermal trip point hysteresis				80		mV
R_{OTP}	OTP resistance, thermal shutdown	$R_{OTP(nom)}$ = 80.7 kΩ, ΔV_{BE} = 79.3 mV(3), T_J = 125°C		–5%		5%	
T_{SHD}	Internal thermal shutdown threshold	Rising			150		°C
$T_{SHD-HYS}$	Internal thermal shutdown threshold hysteresis				20		°C

(3) The specified parameter is calculated based on a 2N3904 transistor at 125°C.
(4) Multiply by 19.9 to scale from nA/mV to ppm/°C (assumes 2N3904 BJT temperature sensor with ideality factor η =1.004).

DEVICE INFORMATION

4 mm × 4 mm × 0.75 mm, 0.5 mm Pitch
WQFN-24
(Top View)

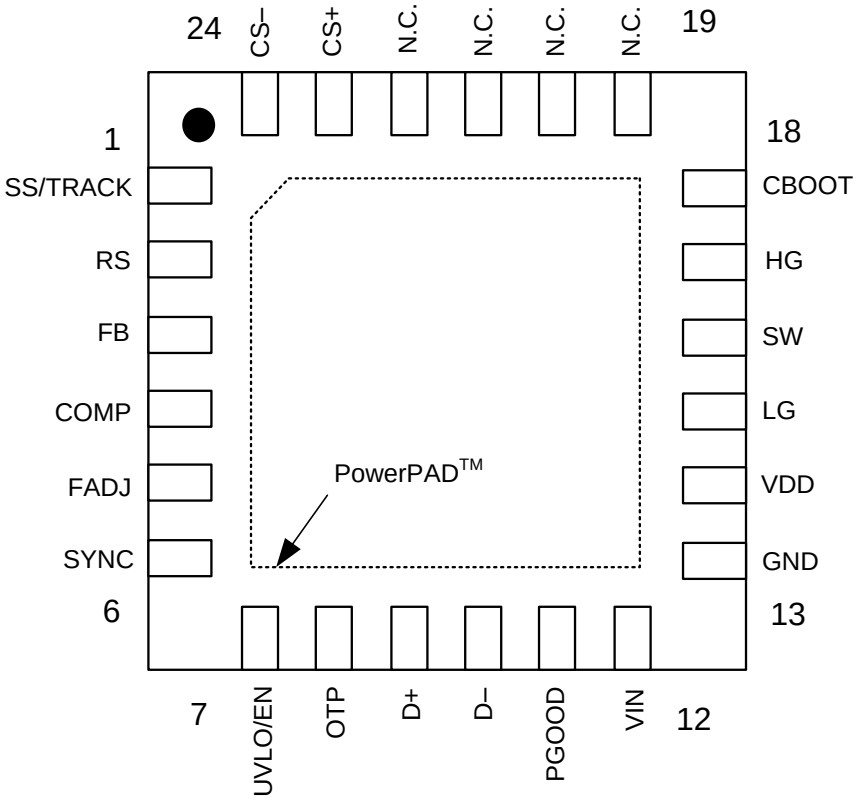


Table 1. PIN DESCRIPTIONS

PIN		I/O/P(1)	DESCRIPTION
NAME	NUMBER		
CBOOT	18	P	High-side bootstrap connection. This pin is the high-side N-FET gate driver power supply. Connect a 100-nF ceramic capacitor between CBOOT and SW.
COMP	4	O	Compensation node output. This pin is an output voltage control-loop error amplifier output. COMP is connected to the FB pin through a compensation network to ensure stability.
CS–	24	I	Current-sense negative input. This pin is the inverting input to the current-sense comparator. 9.9 µA of nominal offset current at room temperature is provided to adjust the current limit setpoint.
CS+	23	I	Current-sense positive input. This pin is the non-inverting input to the current-sense comparator.
D–	10	I	External temperature sense return. This pin is the return current path for the external NPN transistor configured as a thermal diode. This trace should be routed as a differential pair with the D+ trace back to the LM27403 to avoid excessive coupling from external noise sources. Connect D– to GND.
D+	9	I	External temperature sense. A 2N3904-type NPN transistor configured as a remote thermal diode with the base and collector shorted should be connected to this pin to sense the inductor temperature. The sensed temperature is used to compensate for the inductor DCR drift over temperature and to implement system-level thermal shutdown protection.
UVLO/EN	7	I	Precision UVLO/enable input. To implement a VIN UVLO function, connect UVLO/EN to the tap of a voltage divider between VIN and GND. UVLO/EN is initially pulled up by an internal 1.8-µA pullup current source. UVLO/EN has both a 165-mV voltage hysteresis and an 8.7-µA pullup current hysteresis. Thus, when a rising UVLO/EN voltage exceeds the 1.15-V enable threshold, the internal pullup current becomes 10.5 µA and the falling threshold voltage is 0.985 V. Therefore, the effective total hysteresis can be customized to suit the specific application.
EP	—	P	Exposed die attach pad. Connect this pad to the printed circuit board (PCB) ground plane using multiple thermal vias.
FADJ	5	I	Frequency adjust input. The switching frequency is programmable between 200 kHz and 1.2 MHz by virtue of the size of resistor connected to this pin and GND.
FB	3	I	Feedback input. This pin is a voltage-mode control-loop error amplifier inverting input to set the output voltage. In closed-loop (output in regulation) operation, FB is at 0.6 V ±1%.
GND	13	G	Common ground connection. This pin provides the power and signal return connections for analog functions, including low-side MOSFET gate return, soft-start capacitor, OTP resistor, and frequency adjust resistor.
HG	17	O	High-side MOSFET gate drive output. This pin is the high-side N-FET gate connection.
LG	15	O	Low-side MOSFET gate drive output. This pin is the low-side N-FET gate connection.
NC	19-22	G	No connection. Connect directly to GND.
OTP	8	I	Overtemperature protection (OTP) output. A resistor from this pin to GND sets the overtemperature protection setpoint for the DC-DC power supply solution using the temperature sensed at a remotely-connected thermal diode. Connect this pin to GND if the system level OTP function is not required.
PGOOD	11	O	Power Good monitor output. This open-drain output goes low during overcurrent, short-circuit, UVLO, output overvoltage and undervoltage, overtemperature, or when the output is not regulated (such as an output prebias). An external pullup resistor to VDD or to an external rail is required. Included is a 20-µs deglitch filter. The PGOOD voltage should not exceed 5.5 V.
RS	2	I	Negative remote sense input. This pin eliminates the voltage drop between GND and the local ground adjacent to the load. In particularly noisy environments, connect an RC filter between RS and GND. Connect RS to GND at the IC if not used.
SS/TRACK	1	I/O	Soft-start or tracking input. This pin allows a predetermined startup rate to be defined with the use of a capacitor to GND. A 3-µA current source charges the capacitor until the reference reaches 0.6 V. SS/TRACK can also be controlled with an external voltage source for tracking applications.
SW	16	P	Power stage switch-node connection. This pin is the high-side N-FET gate driver return.
SYNC	6	I	Synchronization input. This pin enables PLL synchronization to an external clock frequency. If a SYNC signal is not present, the switching frequency defaults to the frequency set by the FADJ pin. This pin should be tied to GND if not used.
VDD	14	P	Bias supply rail. This pin is a sub-regulated 4.7-V internal and gate drive bias supply rail. VDD also supplies the current to CBOOT to facilitate high-side switching. Decouple VDD to GND locally with a 10-µF ceramic capacitor. VDD should not be used to drive auxiliary system loads because of gate drive loading possibility.
VIN	12	P	Input voltage rail. This input is used to provide the feedforward modulation for output voltage control and for generating the internal bias supply voltage. Decouple VIN to GND locally with a 1-µF ceramic capacitor. For better noise rejection, connect to the power stage input rail with an RC filter.

(1) I=Input, O=Output, P=Power, G=Ground

FUNCTIONAL BLOCK DIAGRAM

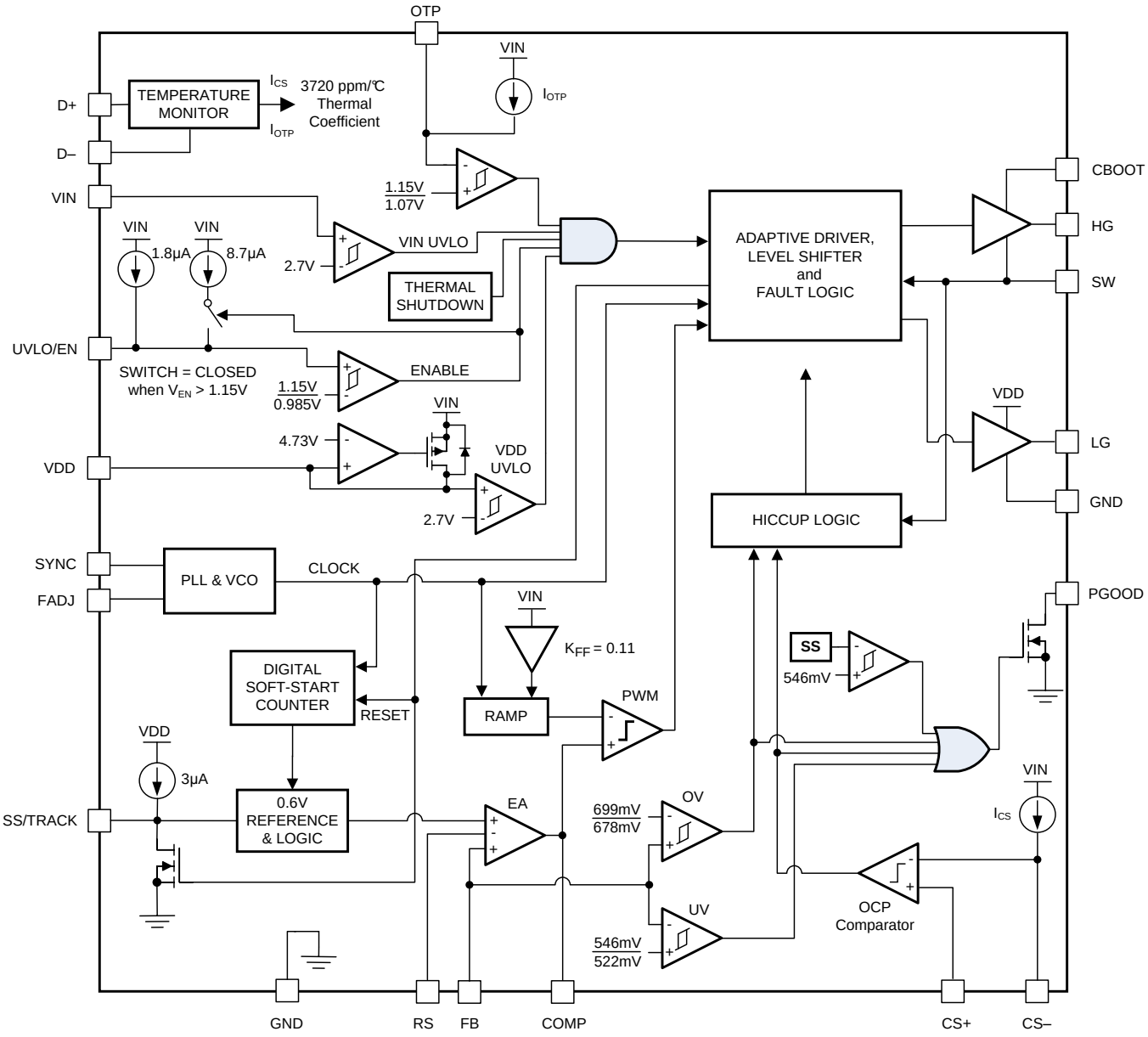


Figure 1. Block Diagram

TYPICAL CHARACTERISTICS

Unless otherwise stated, all datasheet curves were recorded using the circuit and powertrain designated *Design 1* in the DESIGN EXAMPLES section with input and output voltages of 12 V and 1.2 V, respectively.

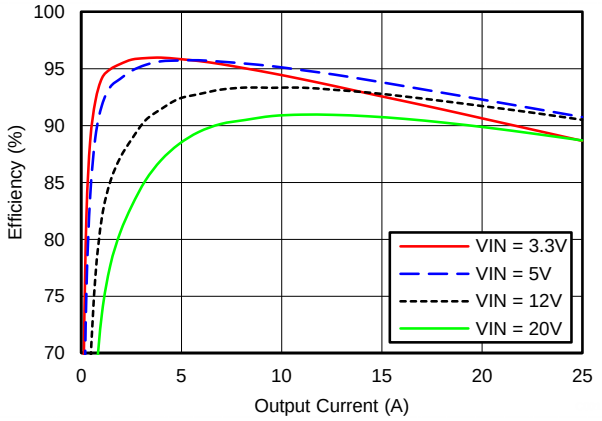


Figure 2. Efficiency Plot, V_{OUT} = 1.2 V

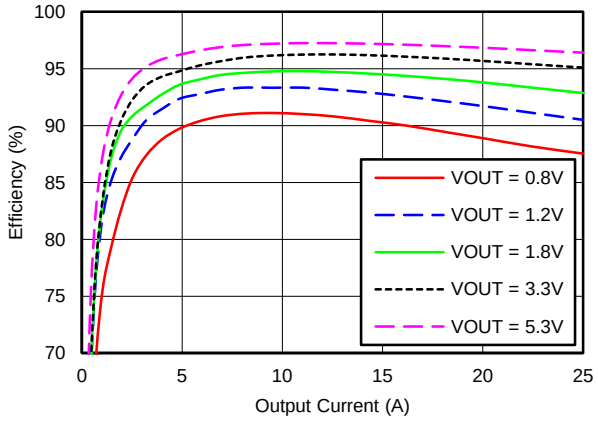


Figure 3. Efficiency Plot, V_{IN} = 12 V

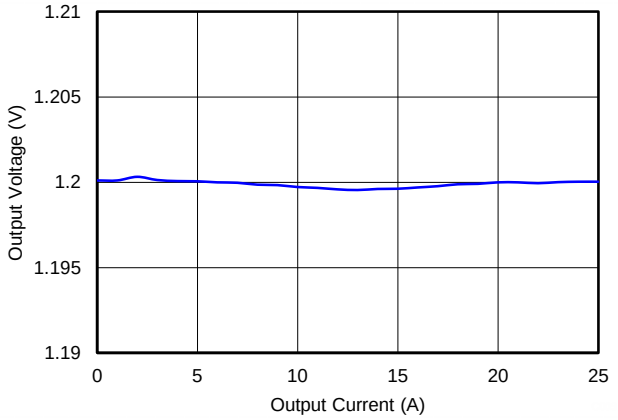


Figure 4. Load Regulation

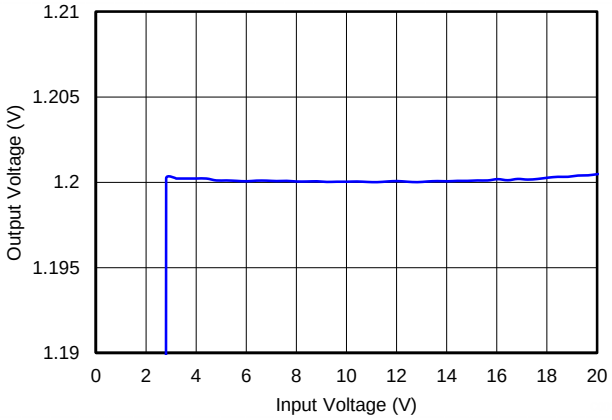


Figure 5. Line Regulation

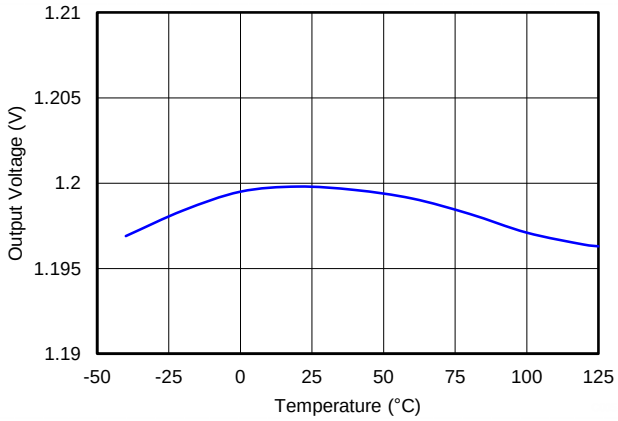


Figure 6. Temperature Regulation

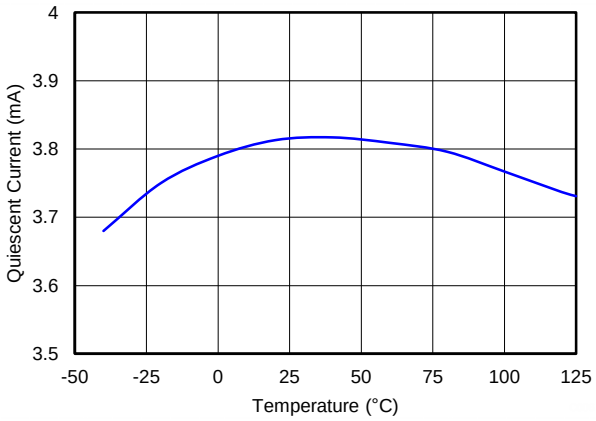


Figure 7. Quiescent Current vs. Temperature, non switching

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, all datasheet curves were recorded using the circuit and powertrain designated *Design 1* in the DESIGN EXAMPLES section with input and output voltages of 12 V and 1.2 V, respectively.

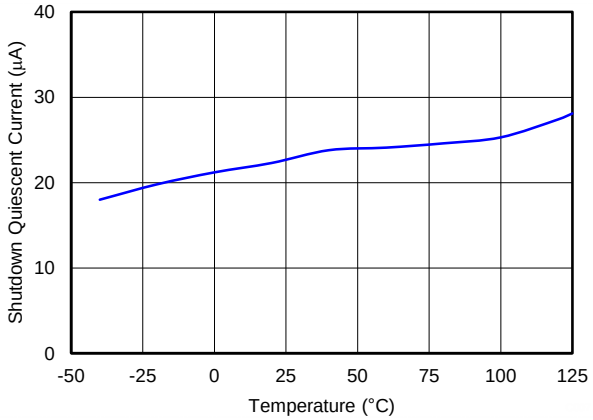


Figure 8. Shutdown Quiescent Current vs. Temperature

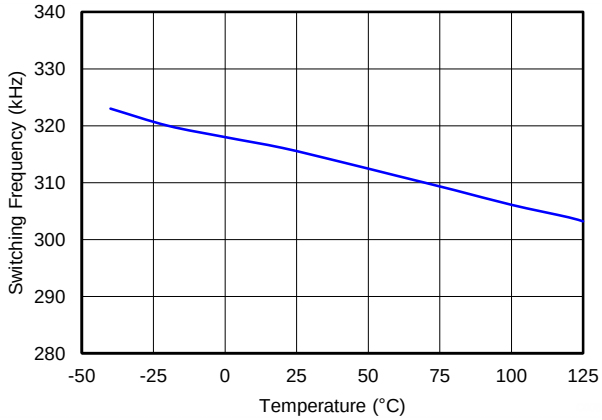


Figure 9. Switching Frequency vs. Temperature

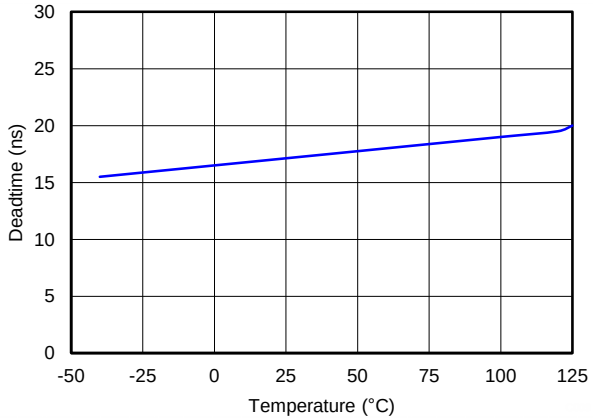


Figure 10. Deadtime vs. Temperature

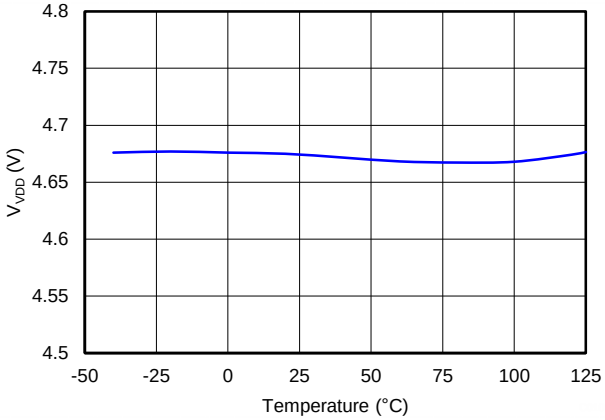


Figure 11. VDD Voltage vs. Temperature

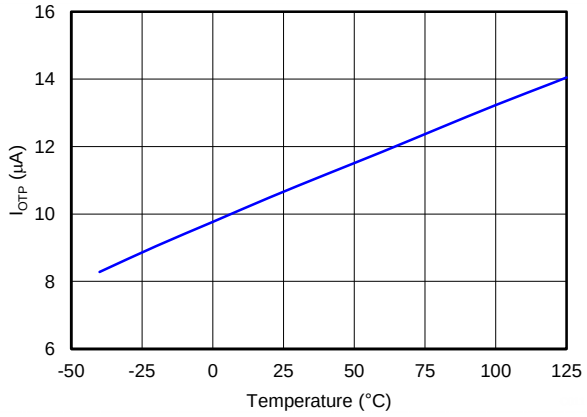


Figure 12. OTP Current vs. Temperature

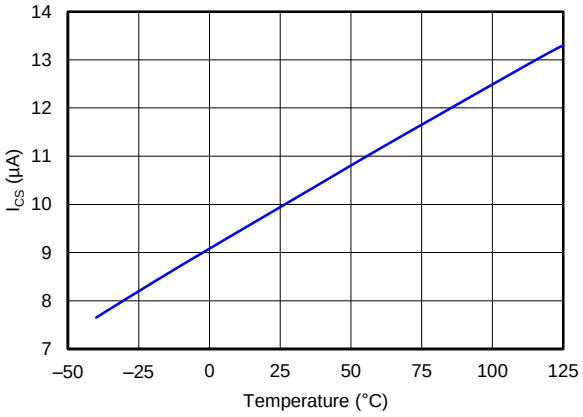


Figure 13. CS– Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, all datasheet curves were recorded using the circuit and powertrain designated *Design 1* in the DESIGN EXAMPLES section with input and output voltages of 12 V and 1.2 V, respectively.

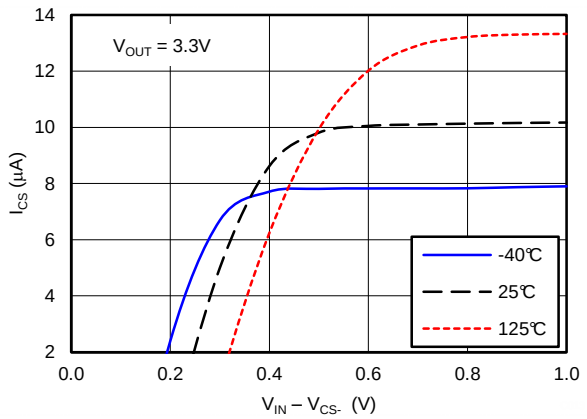


Figure 14. CS– Current Source Compliance Voltage

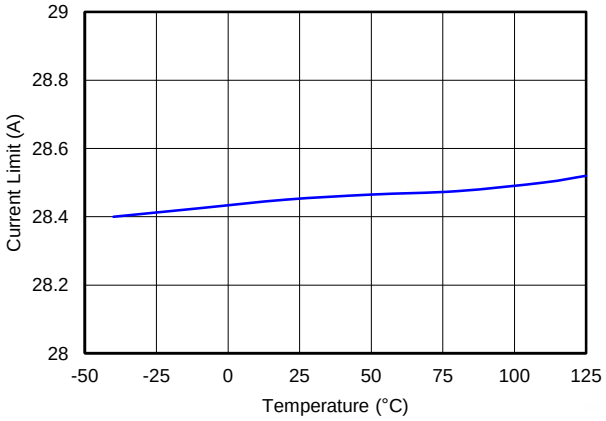


Figure 15. Current Limit Inception vs. Temperature

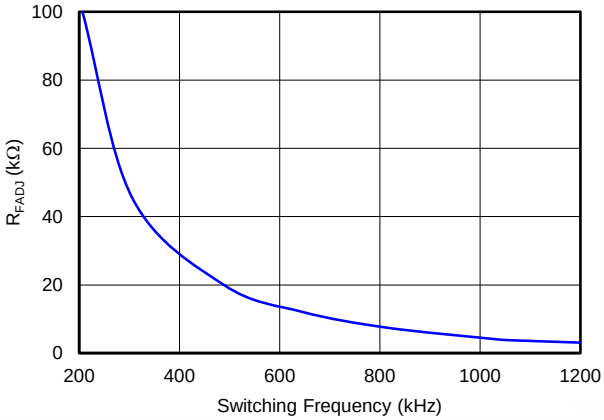


Figure 16. Switching Frequency vs. Frequency Adjust Resistance

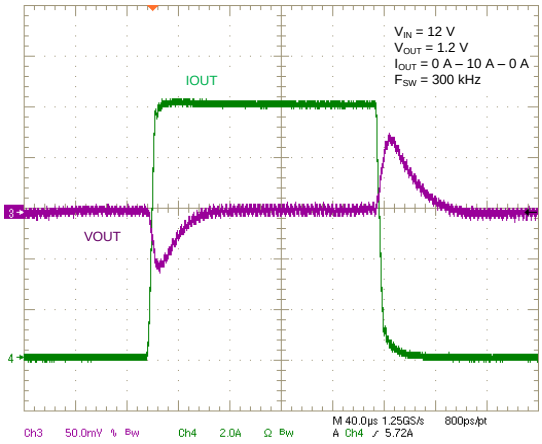


Figure 17. 10-A Step Load Transient Response, 2.5-A/µs Slew Rate

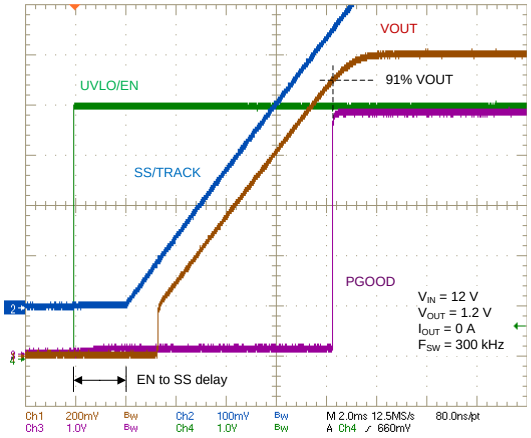


Figure 18. Startup Characteristic

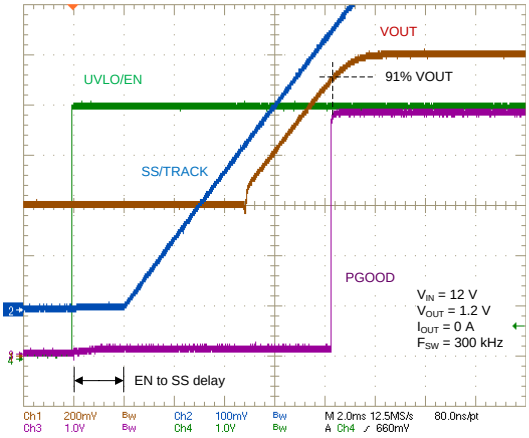


Figure 19. Prebias Startup Characteristic

TYPICAL CHARACTERISTICS (continued)

Unless otherwise stated, all datasheet curves were recorded using the circuit and powertrain designated *Design 1* in the DESIGN EXAMPLES section with input and output voltages of 12 V and 1.2 V, respectively.

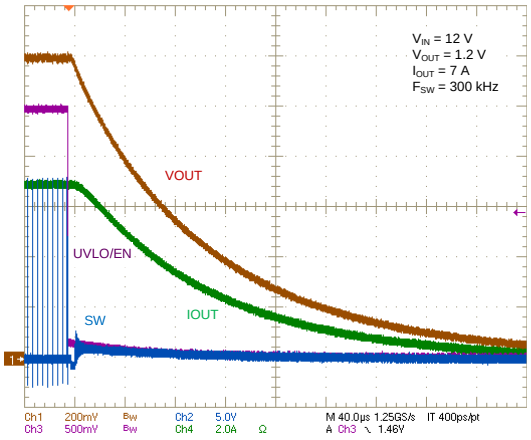


Figure 20. Shutdown Characteristic

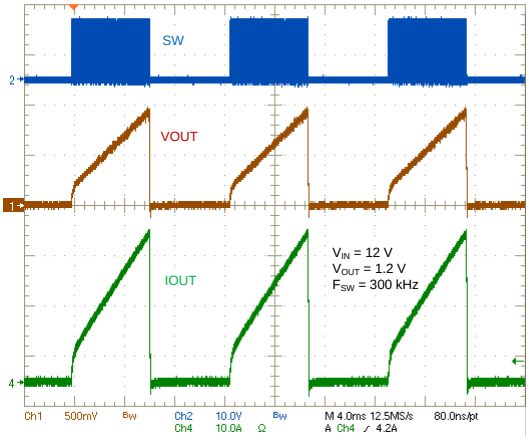


Figure 21. Current Limit Hiccup Mode

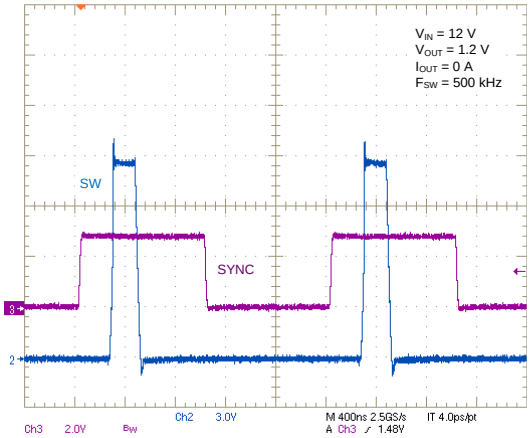


Figure 22. SYNC Waveform

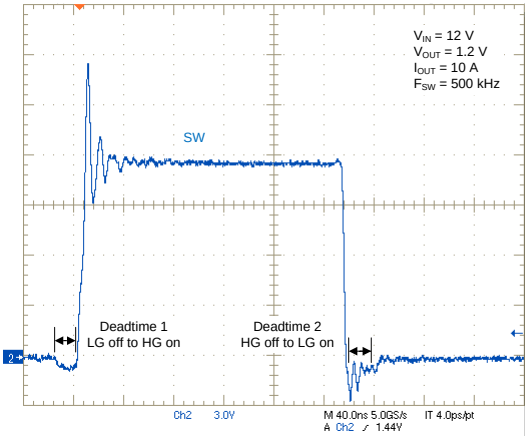


Figure 23. Switch Node Waveform

OVERVIEW

APPLICATION AND ARCHITECTURE

The distributed power supply architecture, pervasive in myriad applications including communications infrastructure equipment and computing systems, uses an intermediate bus and multiple downstream DC-DC regulators dedicated and proximate to each “point-of-load.” The ASICs, FPGAs, and microprocessors that comprise these loads have supply voltage requirements whose levels are decreasing on an absolute basis and whose tolerance bands are decreasing on a percentage basis. The hallmarks of point-of-load (POL) DC-DC regulators are efficiency, size, load transient response, and cost.

To this end, the LM27403 is a feature-rich, easy-to-use, synchronous PWM DC-DC step-down controller capable of providing an ultrahigh current output for demanding, high power density POL applications. An input voltage range of 3 V to 20 V is compatible with a wide range of intermediate bus system rails and battery chemistries; especially 3.3-V, 5-V, and 12-V inputs. The output voltage is adjustable from 0.6 V to as high as 93% of the input voltage, with better than ±1% feedback system regulation accuracy over the full junction temperature range. With an accurate, adjustable and thermally-compensated inductor DCR based current limit setpoint, ferrite and composite core inductors with low DCR and small footprint can be specified to maximize efficiency and reduce power loss. High-current gate drivers with adaptive deadtime are used for the high-side and low-side MOSFETs to provide further efficiency gains.

The LM27403 employs a voltage-mode control loop with output voltage remote sense, input voltage feedforward modulation, and a high gain-bandwidth error amplifier to accurately regulate the output voltage over substantial load, line, and temperature ranges. The switching frequency is programmable between 200 kHz and 1.2 MHz via a resistor or an external synchronization signal. The LM27403 is available in a 4-mm × 4-mm, thermally-enhanced, 24-lead WQFN PowerPad™ package. This device offers high levels of integration by including MOSFET gate drivers, a low dropout (LDO) bias supply linear regulator, and comprehensive fault protection features to enable highly-flexible, reliable, energy-efficient, and high power density regulator solutions.

Multiple fault conditions are accommodated, including overvoltage, undervoltage, overcurrent, and overtemperature. To improve overcurrent setpoint accuracy and enable easier filter inductor selection, the LM27403 thermally compensates for the temperature coefficient (TC) of the inductor's winding resistance by sensing the inductor temperature with an external NPN transistor configured as a thermal diode. The same thermal diode also monitors the PCB temperature to initiate a thermal shutdown in the event that the sensed temperature exceeds the programmed thermal shutdown setpoint.

DESIGN AND IMPLEMENTATION

To expedite and streamline the process of designing of a LM27403-based regulator for a given application, a comprehensive *LM27403 design tool* is available for download. This is complimented by the availability of two LM27403 evaluation modules (EVMs) as well as numerous LM27403 designs populated in TI's PowerLab™ reference design library. In addition, five designs are provided in the DESIGN EXAMPLES section of this datasheet. The LM27403 is also Webench®-enabled.

THEORY OF OPERATION

INPUT RANGE: VIN

The LM27403 operational input voltage range is from 3 V to 20 V. The device is intended for POL conversions from 3.3-V, 5-V, and 12-V unregulated, semiregulated and fully-regulated supply rails. It is also suitable for connection to intermediate bus converters with output rails centered at 12 V and 9.6 V (derived from 4:1 and 5:1 primary-secondary transformer step-downs in non-regulated full-bridge converter topologies) and voltage levels intrinsic to a wide variety of battery chemistries.

The LM27403 uses an internal LDO subregulator to provide a 4.7-V bias rail for the gate drive and control circuits (assuming the input voltage is higher than 4.7 V plus the necessary subregulator dropout specification). Naturally, it can be more favorable to connect VDD directly to the input during low input voltage operation (V_{VIN} < 5.5 V). In summary, connecting VDD to VIN during low input voltage operation provides a greater gate drive voltage level and thus an inherent efficiency benefit. However, by virtue of the low subregulator dropout voltage, this VDD to VIN connection is not mandatory, thus enabling input ranges from 3 V up to 20 V. The application circuits shown below detail LM27403 configuration options suitable for several input rails.

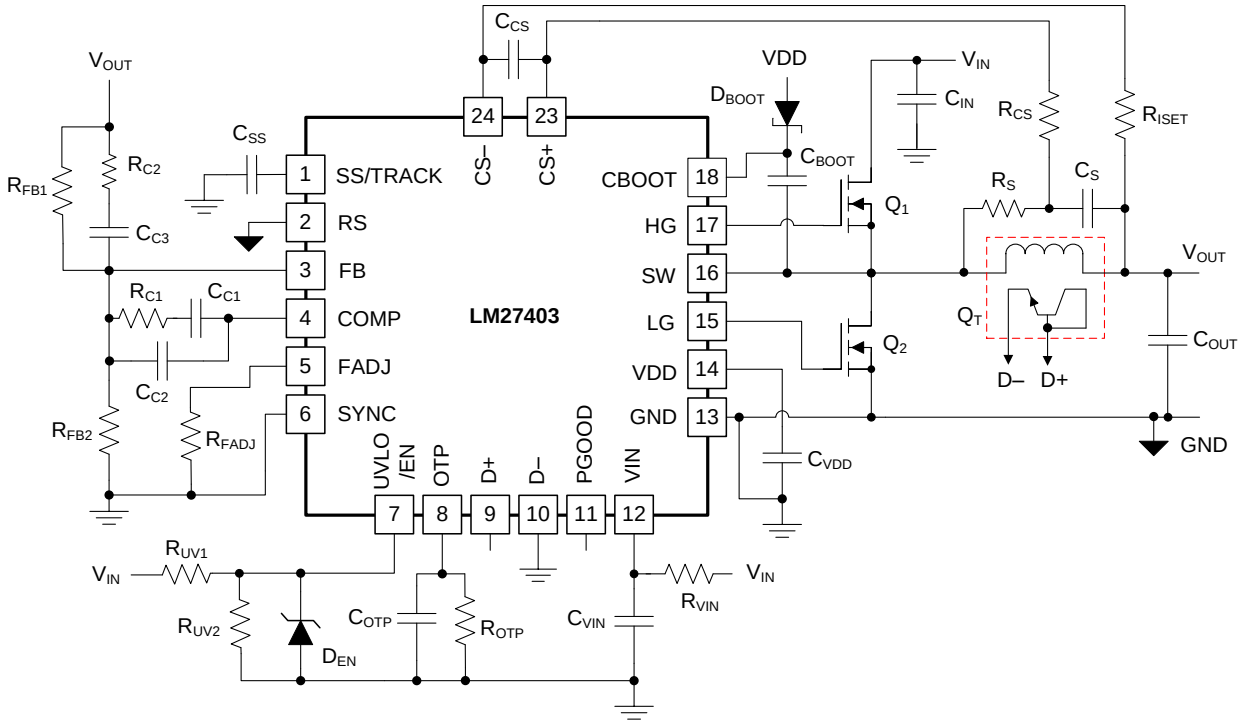


Figure 24. Schematic Diagram for VIN Operating Range of 3 V to 20 V

Figure 24 shows the schematic diagram for an input voltage ranging from 3 V to 20 V. Note that a finite subregulator dropout voltage exists and is manifested to a larger extent when driving high gate charge (Q_G) power MOSFETs at elevated switching frequencies. For example, at V_{VIN} = 3 V, the VDD rail voltage is 2.8 V with a dc operating current, I_{VDD}, of 40 mA. Such a low gate drive rail may be insufficient to fully enhance the power MOSFET gates. At the very least, MOSFET on-state resistance, $R_{DS(ON)}$, increases at such low gate drive levels. Here are the main concerns when operating at a low input voltage:

- Increase of conduction losses (higher $R_{DS(on)}$ at lower V_{GS}).
- Increase of switching losses associated with sluggish switching times when operating at low V_{GS} levels.
- Deadtime may be larger as a result of the lower gate drive level and associated slower gate voltage slew rate. This may become evident, for example, when using two high-side MOSFETs in a 3.3-V to 2.5-V converter design.
- Dramatic reduction in the range of suitable MOSFETs that a designer can choose from (MOSFETs with $R_{DS(on)}$ rated at V_{GS} = 2.5 V become mandatory).

Note that the increased on-state resistance is compounded by an increase in MOSFET junction temperature, bearing in mind the negative temperature coefficient of the MOSFET threshold voltage.

In general, the subregulator is rated to drive the two internal gate driver stages in addition to the quiescent current associated with LM27403 operation. Figure 25 shows the schematic diagram for lower input voltages such as 3.0 V to 5.5 V. The LM27403's VDD and VIN pins can be tied together if the input voltage is guaranteed not to exceed 5.5 V (absolute maximum 6 V). This short bypasses the internal LDO bias regulator and eliminates the LDO dropout voltage and power dissipation. An RC filter from the input rail to the VIN pin, for example 2.2 Ω and 1 µF, presents supplementary filtering at the VIN pin. Low gate threshold voltage MOSFETs are recommended for this configuration.

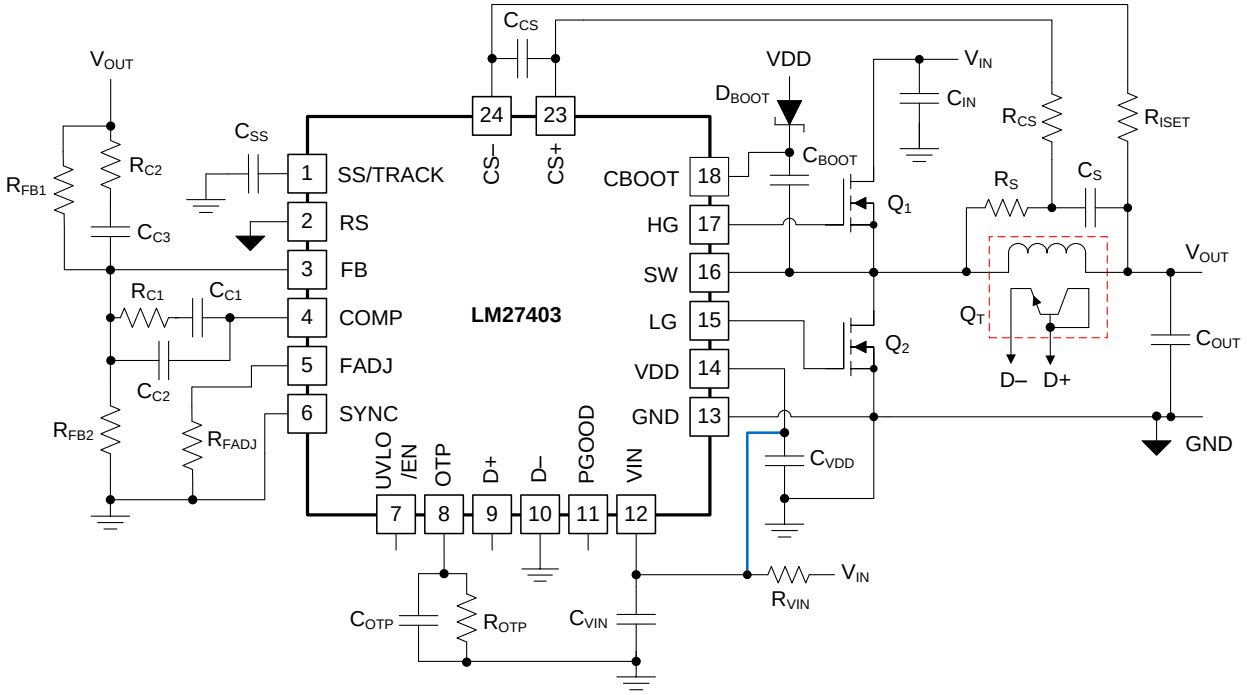


Figure 25. Schematic Diagram for VIN Operating Range of 3.0 V to 5.5 V

OUTPUT VOLTAGE: FB VOLTAGE AND ACCURACY

The reference voltage seen at the FB pin is set at 0.6 V, and a feedback system accuracy of ±1% over the full junction temperature range is met. Junction temperature range for the device is –40°C to +125°C. While somewhat dependent on frequency and load current levels, the LM27403 is generally capable of providing output voltages in the range of 0.6 V to a maximum of greater than 90% VIN. The dc output voltage during normal operation is set by the feedback resistor network, R_{FB1} and R_{FB2}, connected to VOUT.

INPUT AND BIAS RAIL VOLTAGES: VIN and VDD

The LM27403 internal UVLOs ensure that the input rail (VIN) and bias supply rail (VDD) are charged and stable at 2.7 V before switching begins. VDD and VIN have independent UVLO comparators, each with 250 mV of hysteresis. There is a definite delay between UVLO power-on and switching power-on. This delay is related to the fact that the LM27403 does not begin switching until the internal temperature sense circuitry is ready and stabilized. The delay is four measurement cycles on D+, equivalent to 512 clock cycles.

The VDD bias supply LDO has a nominal current limit of 106 mA during normal operation. However, a lower current limit is engaged at startup to control the rate of rise of the VDD voltage. Figure 26 shows the typical scope waveforms of VDD and VOUT when the input voltage is instantaneously applied. Here, the VDD voltage ramps in approximately 1.4 ms based on a 10-µF VDD decoupling capacitor and current-limited VDD feature. For more details, please see the LM27403 EVM User's Guide.

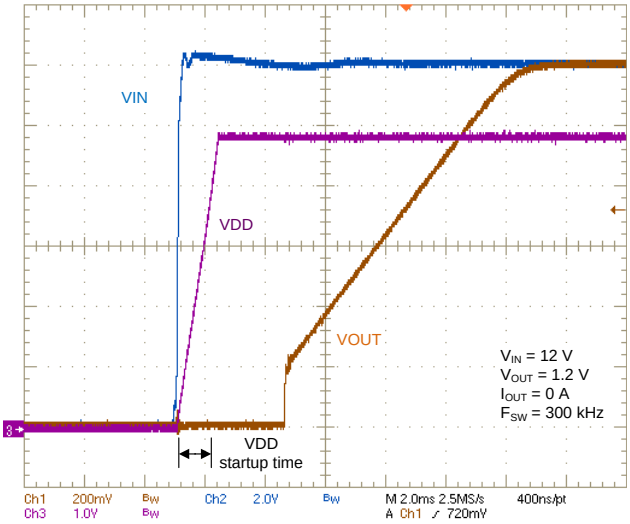


Figure 26. Typical Startup Waveforms of VDD and VOUT with Controlled Ramp Rates

PRECISION ENABLE: UVLO/EN

The UVLO/EN pin represents a precision analog enable function for user-defined UVLO power-on input voltage levels and to toggle the output on and off. The UVLO/EN pin is essentially a comparator-based input referenced to a flat bandgap voltage with a fixed hysteresis of 165 mV.

The UVLO/EN pin has an internal pullup current of 1.8 µA, as shown in Figure 27. There is also a low I_Q shutdown mode when UVLO/EN is effectively pulled below a base-emitter voltage drop (approximately 0.7 V at room temperature). This mode shuts down the bias currents of the LM27403, but the UVLO/EN pullup current source is still available. If UVLO/EN is pulled below this hard shutdown threshold, the internal LDO regulator powers off and the VDD rail collapses.

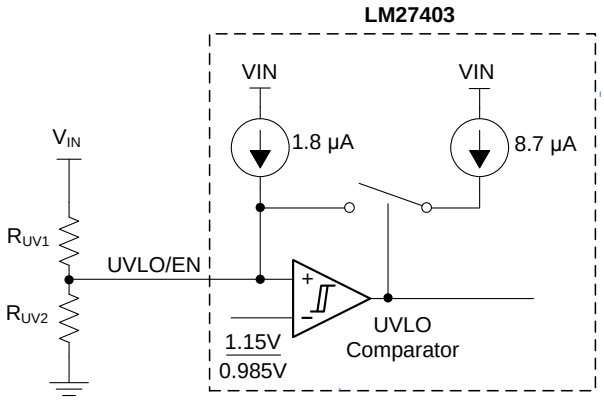


Figure 27. Precision UVLO/Enable Circuit with Hysteretic Comparator and Pullup Current Sources

When the precision enable threshold of 1.15 V is exceeded, the UVLO/EN pullup current source increases from 1.8 µA to 10.5 µA (that is, an 8.7-µA hysteresis current). Use this feature to create a customizable UVLO hysteresis (above the standard 165-mV fixed voltage hysteresis) based on the resistor divider from VIN to turn on and off the LM27403 at the required input voltage levels. Also, use a capacitor from the UVLO/EN pin to GND to implement a fixed time delay in power systems with timed sequencing requirements.

Figure 28 shows an example using the circuit in Figure 24 where the input voltage is ramping from 0 V to 10 V in 100 ms. Here, the UVLO resistors, R_{UV1} and R_{UV2}, are respectively set to 47.5 kΩ and 10 kΩ. Given these resistances, the typical input UVLO turn-on and turn-off levels are 6.5 V and 5.2 V, respectively. The UVLO/EN pin voltage steps at the rising and falling thresholds are defined by the UVLO/EN pin current hysteresis.

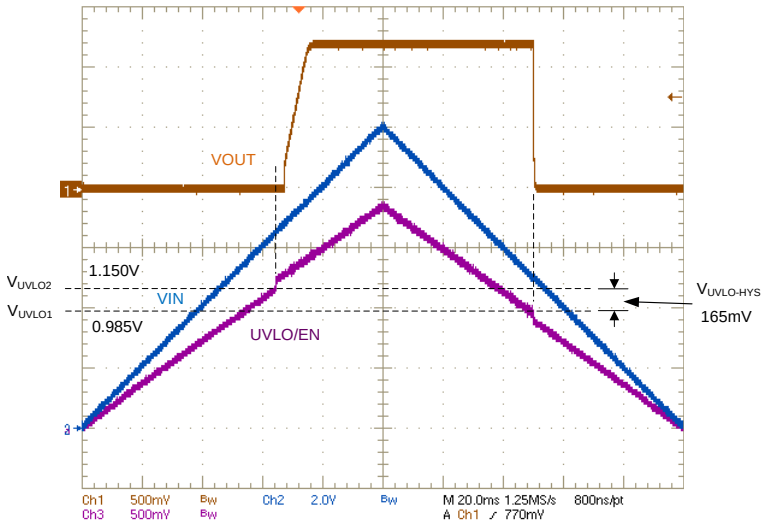


Figure 28. Typical Input Voltage UVLO Turn On and Off Behavior

Given $V_{IN(on)}$ and $V_{IN(off)}$ as the input voltage turn-on and turn-off thresholds, respectively, select the UVLO resistors using the following expressions:

$$R_{UV1} = \frac{V_{IN(on)} \frac{V_{UVLO1}}{V_{UVLO2}} - V_{IN(off)}}{I_{UVLO2} - I_{UVLO1} \frac{V_{UVLO1}}{V_{UVLO2}}} \quad (1)$$

$$R_{UV2} = R_{UV1} \frac{V_{UVLO2}}{V_{IN(on)} - V_{UVLO2} + R_{UV1} I_{UVLO1}} \quad (2)$$

The UVLO/EN pin has a maximum operating voltage rating equal to the input voltage or 5.5V, whichever is lower. Do not exceed this rating. If the input UVLO level is set at low input voltage, it is possible that this maximum UVLO/EN pin voltage could be exceeded at the higher end of the input voltage operating range. In this case, use a small 4.7-V zener diode clamp, designated D_{EN} in Figure 24, from UVLO/EN to GND, such that the maximum operating level is never exceeded.

SWITCHING FREQUENCY

There are two options for setting the switching frequency of the LM27403, thus providing a power supply designer a level of flexibility when choosing external components for multiple applications. To adjust the frequency, use a resistor from the FADJ pin to GND, or synchronize the LM27403 to an external clock signal through the SYNC pin.

FREQUENCY ADJUST: FADJ

Adjust the LM27403 free-running switching frequency by using a resistor from the FADJ pin to GND. The switching frequency range of the device is from 200 kHz to 1.2 MHz. An open circuit at the FADJ pin forces the frequency to the minimum value. FADJ shorted moves the frequency to its maximum value. The frequency set resistance, R_{FADJ}, is governed by Equation 3.

$$R_{FADJ}\left[k\Omega\right] = \frac{10000}{F_{sw}\left[kHz\right]^{0.99} - 100} - 7 \quad (3)$$

E96 resistors for common switching frequencies are given in Table 2.

Table 2. Frequency Set Resistors

SWITCHING FREQUENCY (kHz)	FREQUENCY SET RESISTANCE (kΩ)
215	95.3
250	68.1
300	47.5
500	20
600	15
800	7.5
1050	4.12
1200	2.87

CLOCK SYNCHRONIZATION: SYNC

Apply an external clock synchronization signal to the LM27403 to synchronize switching in both frequency and phase. Requirements for the clock SYNC signal are:

- Clock SYNC range: 200 kHz to 1.2 MHz
- SYNC frequency range from the FADJ frequency: up to 400 kHz (up only)

In applications where the external clock is not applied to the LM27403, use the external FADJ resistor to set the minimum switching frequency. When the external clock is applied, it takes precedence only if the switching frequency is greater than that set by the FADJ resistor. When the external clock is disconnected, the LM27403 switching frequency does not decrease below the minimum frequency set by the resistor. Setting a minimum frequency in this way prevents the inductor ripple current from increasing dramatically. Externally tie SYNC to GND if synchronization functionality is not required. The SYNC logic thresholds are based on an NMOS threshold referenced to GND and, as such, are effectively independent of the VDD operating voltage.

Figure 29 shows a SYNC TTL signal at 600 kHz and the corresponding SW node waveform (V_{IN} = 12 V, V_{OUT} = 1.2 V, free-running frequency = 250 kHz). The synchronization is with respect to the rising edge of SYNC. The rising edge of the SW voltage is phase delayed relative to SYNC by approximately 250 ns.

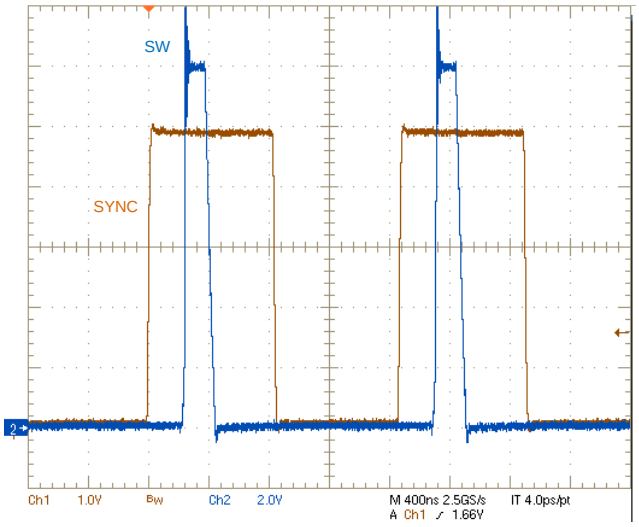


Figure 29. Typical 600-kHz SYNC Waveform

TEMPERATURE SENSING: D+ and D–

The LM27403 PWM controller offers low-cost programmable thermal protection by using remote thermal diode temperature measurements based on the change in forward bias voltage of a diode when operated at two different currents. The thermal diode is a discrete small-signal 2N3904 type silicon NPN BJT located (in good thermal contact) adjacent the filter inductor.

The ideality factor is a parameter in the diode I-V relationship that approaches 1.0 or 2.0 as carrier diffusion or recombination current dominate current flow, respectively. The ideality factor for 2N3904 type diode-connected BJTs available from several manufacturers is typically 1.004. Note that 3-terminal BJTs such as the 2N3904 are vastly preferred over true 2-terminal diodes in this application. Discrete 2-terminal diodes with current largely dictated by recombination have a much higher ideality factor (η = 1.2 to 1.5) than BJTs and, to such an extent, would cause unacceptable temperature measurement error.

Switched capacitor technology is integrated in the LM27403 to sample and measure the base-emitter voltages created by respective 10-µA and 100-µA bias currents flowing from the D+ to D– pins. The difference in these voltages, termed ΔV_{BE}, is readily extracted and the sensed temperature is calculated noting that ΔV_{BE} is directly proportional to temperature as follows:

$$V_{BE(high)} - V_{BE(low)} = \frac{\eta k T}{q} \ln\left(\frac{I_{high}}{I_{low}}\right) \quad (4)$$

where

- k = Boltzmann's constant, 1.3806488 × 10^{-23}J/K (Joules/Kelvin)
- T = absolute temperature in Kelvin (K)
- q = electron charge = 1.602176 x 10^{-19} C (Coulombs)
- η = diode ideality factor = 1.004
- I_{low} = bias current in state 1 = 10 µA
- I_{high} = bias current in state 2 = 100 µA

The source currents from the D+ pin during state 1 and state 2 are 10 µA and 100 µA, respectively. The sensed temperature in Kelvin becomes:

$$T = \frac{q\Delta V_{BE}}{\eta k \ln(10)} \quad (5)$$

Figure 30 shows the 2N3904 V_{BE} voltage at ambient temperatures of –40°C, 25°C and 125°C. The low and high states in V_{BE} voltage correspond to the 10-µA and 100-µA currents sourced from D+, each of 64 clock cycle duration. The voltage level is sampled at the end of each state. While the dc level of the V_{BE} voltage decreases logarithmically with increasing temperature, the ΔV_{BE} amplitude increases with and is directly proportional to temperature according to Equation 5.

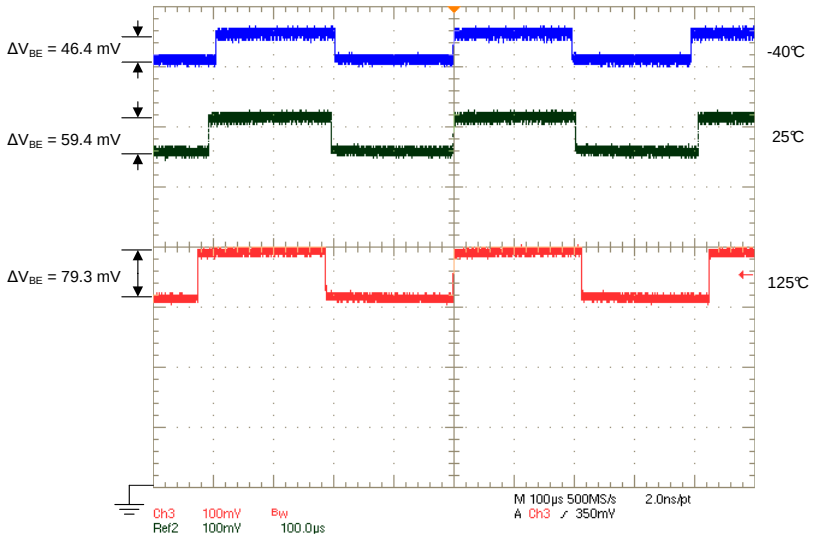


Figure 30. Typical 2N3904 Base-Emitter Voltage at -40°C, 25°C and 125°C

Note that D– is essentially a kelvin connection to the remote thermal diode. As such, the D– pin needs to be tied to GND at the LM27403; the D– trace should not connect to any of the PCB's current-carrying ground planes.

THERMAL SHUTDOWN: OTP

A current proportional to the sensed temperature is sourced from the OTP pin. The resultant voltage at the OTP pin (set by a resistor connected from OTP to GND) is compared to an internal shutdown threshold of 1.15 V with 80-mV hysteresis. When the threshold is exceeded, the device stops switching until the sensed temperature drops to a level where the OTP pin voltage falls to the restart threshold. The external thermal protection is disabled by grounding the OTP pin. The thermal shutdown setpoint is governed by Equation 6:

$$R_{OTP} = R_{OTP(125℃)} \frac{398}{T_{OTP}(℃) + 273}$$

where

- R_{OTP} is the required resistance at the OTP pin for the desired thermal shutdown temperature
- $R_{OTP(125°C)}$ is the nominal resistance at the OTP pin , 80.7 kΩ, for 125°C thermal shutdown, and
- T_{OTP} is the desired thermal shutdown temperature. (6)

For example, the OTP resistor required for a thermal shutdown setpoint of 105°C is calculated as shown in Equation 7:

$$R_{OTP} = 80.7\ k\Omega \frac{398}{105 + 273} = 85\ k\Omega \quad (7)$$

A 100-nF capacitor connected in parallel with R_{OTP} is recommended. When the IC detects an overtemperature event, it responds with the normal hiccup-mode sequence of events when going into shutdown. More specifically, the following steps occur when an internal or external OTP event is detected:

1. The high-side MOSFET immediately turns off.
2. An internal zero-cross circuit is enabled to detect whether the inductor current is positive or negative:
   (a) If the current is negative, the low-side MOSFET immediately turns off.
   (b) If the current is positive, the low-side MOSFET turns off when the inductor current ramps down to zero.

Note that it is important to prevent water-soluble flux residues from contaminating the PCB during the manufacturing process. Contaminants such as these can result in unexpected leakage currents and consequent temperature-measurement errors.

INDUCTOR DCR BASED OVERCURRENT PROTECTION

The LM27403 exploits the filter inductor DCR to detect overcurrent events. This technique enables lossless and continuous monitoring of the output current using an RC sense network in parallel with the inductor. DCR current sensing allows the system designer to use inductors specified with low tolerance DCRs to improve the current limit setpoint accuracy. A dc current limit setpoint accuracy within the range of 10% to 15% is easily achieved using inductors with low DCR tolerances.

CURRENT SENSING: CS+ and CS–

As mentioned, the LM27403 implements an inductor DCR lossless current sense scheme designed to provide both accurate overload (current limit) and short-circuit protection. Figure 31 shows the popular inductor DCR current sense method. Figure 32 shows an implementation with current shunt resistor, R_{ISNS}.

Components R_S and C_S in Figure 31 create a low-pass filter across the inductor to enable differential sensing of the inductor DCR voltage drop. When R_SC_S is equal to L/R_{dcr}, the voltage developed across the sense capacitor, C_S, is a replica of the inductor DCR's voltage waveform. Choose the capacitance of C_S greater than 0.1 µF to maintain low impedance of the sense network, thus reducing the susceptibility of noise pickup from the switch node.

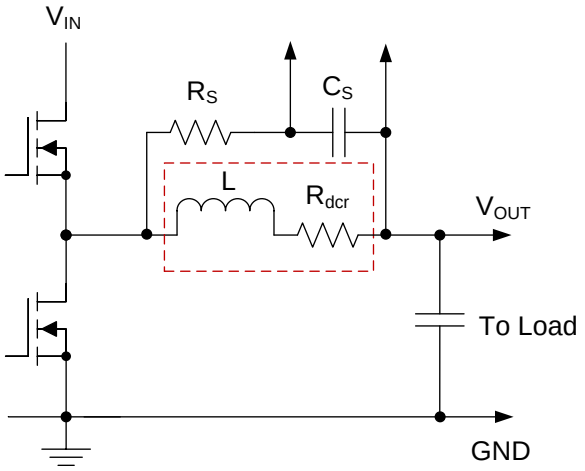


Figure 31. Current Sensing using Inductor DCR

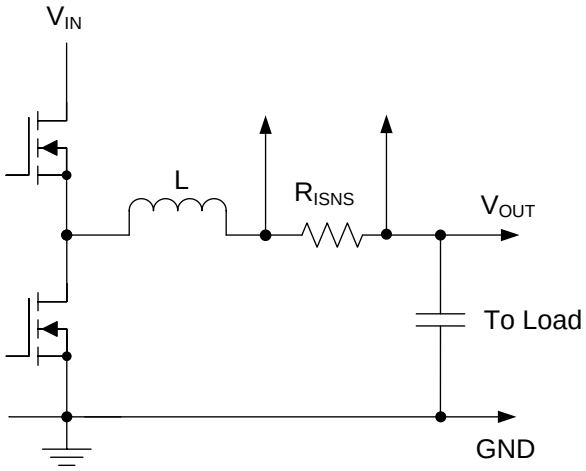


Figure 32. Current Sensing using Shunt Resistor

The current limit circuit arrangement is portrayed in Figure 33. The current limit setpoint is set by a single external resistor, R_{ISET}, connected from the CS– pin to the output voltage terminal. The current sourced from CS– in combination with this series resistance sets the reference voltage to the current limit comparator, as governed by Equation 8.

$$R_{ISET} = \frac{R_{dcr}\left(I_{OCP} + \frac{\Delta i_L}{2}\right)}{I_{CS}} \quad (8)$$

where

- I_{CS} is the CS– pin current, 9.9 µA typically at 25°C
- I_{OCP} is the dc overcurrent protection setpoint, and
- Δi_L is the peak-to-peak inductor ripple current.

Inductor DCR temperature compensation is automatically provided using the remote-diode sensed temperature. The temperature coefficient (TC) of the inductor winding resistance is typically 3720 ppm/°C. The current-limit setpoint is maintained essentially constant over temperature by the slope of CS– pin current over temperature. An increase in sensed DCR voltage associated with an increase of inductor winding temperature is matched by a concomitant increase in current limit comparator reference voltage. The inductor temperature is measured by placing an external diode-connected 2N3904 discrete NPN transistor, designated Q_T in Figure 33, in close proximity to the inductor (see the TEMPERATURE SENSING: D+ and D– section for more details).

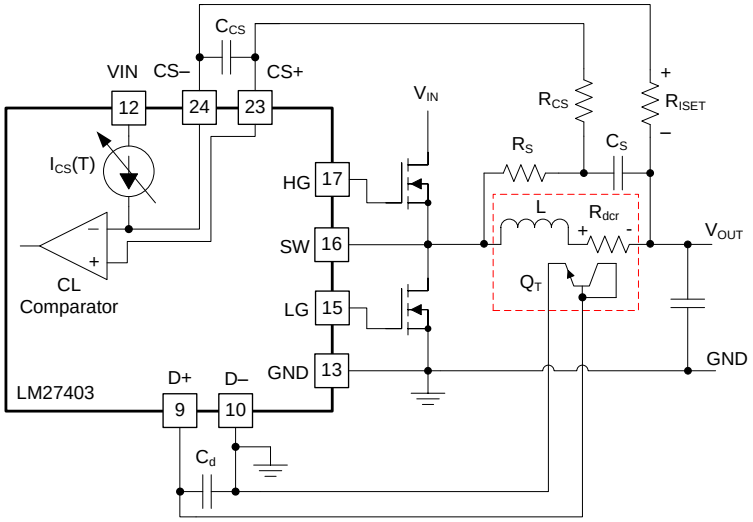


Figure 33. Current-Limit Setpoint Defined by Current Source I_{CS} and Resistor R_{ISET}

Note that the inductor DCR is shown schematically as a discrete element in Figure 31 and Figure 33. The current-sense comparator inputs operate at common mode up to the input rail voltage. The comparator incorporates a very low input-referred offset to reduce the SNR of the voltage detected across the inductor DCR. The CS– pin current is specified down to a headroom compliance voltage of less than 0.8 V (that is, $V_{VIN} – V_{CS–}$) and over the full operating temperature range (see the ELECTRICAL CHARACTERISTICS Table and Figure 14). The current source is powered from the input to allow the current limit circuit to work in high duty cycle applications.

With power inductors selected to provide lowest possible DCR to minimize power losses, the typical DCR ranges from 0.4 mΩ to 4 mΩ. Then, given a load current of 25 A, the voltage presented across the CS+ and CS– pins ranges between 10 mV and 100 mV. Note that this small differential signal is superimposed on a large common-mode signal that is the dc output voltage, which makes the current sense signal challenging to process. To aid in rejection of high frequency common-mode noise, a series resistor, R_{CS}, of same resistance as R_{ISET}, is added to the CS+ signal path as shown in Figure 33. A small capacitor, C_{CS}, added across CS+ and CS– provides differential filtering.

A current sense (or current shunt) resistor in series with the inductor can also be implemented at lower output current levels to provide accurate overcurrent protection, see Figure 32. Burdened by the unavoidable efficiency penalty and/or additional cost implications, this configuration is not usually implemented in high-current applications (except where OCP setpoint accuracy and stability over the operating temperature range are critical specifications). However, if a shunt resistor is used, temperature compensation is not required. In this case, short the D+ to D– pins to disable this function. The current sourced from CS– in this case becomes 5 µA (typical) and is independent of temperature.

In the PCB layout, component pads are recommended to install a small capacitor, designated C_d in Figure 33, between the D+ and D– pins as close to the LM27403 as possible. This capacitor should not exceed 1 nF for 2N3904-type devices. Locate an additional capacitor, typically 100 pF, at the BJT, when operating in noisy environments (for example, where leakage flux from the airgap of a ferrite inductor may couple into the adjacent circuit board traces).

CURRENT LIMIT HANDLING

The LM27403 implements a *hiccup* mode to allow the device to cool down during overcurrent events. If five overcurrent events are detected during any 32 clock cycle interval, the LM27403 shuts down and stops switching for a period of 5 ms. During this time, negative inductor current is not allowed, and the output cannot swing negative. After 5 ms, the LM27403 starts up in the normal startup routine at an output voltage ramp rate determined by the internal soft-start function or the external soft-start capacitor (if one is used). With each detected current limit event, the high-side MOSFET is turned off and the low-side MOSFET is turned on.

SOFT-START: SS/TRACK

After the UVLO/EN pin exceeds the rising threshold of 1.15 V, the LM27403 begins charging the output to the dc level dictated by the feedback resistor network. The LM27403 features an adjustable soft-start (set by a capacitor from the SS/TRACK pin to GND) that determines the charging time of the output. A 3-µA current source charges this soft-start capacitor. Soft-start limits inrush current as a result of high output capacitance and avoids an overcurrent condition. Stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by Equation 9:

$$t_{SS} = \frac{C_{SS} \; V_{REF}}{I_{SS}} \tag{9}$$

where

- C_{SS} is the soft-start capacitance
- V_{REF} is the 0.6-V reference, and
- I_{SS} is the 3-µA current sourced from the SS/TRACK pin.

If a soft-start capacitor is not used, then the LM27403 defaults to a minimum internal soft-start time of 1.28 ms and provides a resolution of 128 steps. Thus, the internal soft-start dictates the fastest startup time for the circuit.

When the SS/TRACK voltage exceeds 91% of the reference voltage, the Power Good flag transitions high. Conversely, the Power Good flag goes low when the SS/TRACK voltage goes below 87% of the reference.

TRACKING

The SS/TRACK pin also doubles as a tracking pin when master-slave power-supply tracking is required. This tracking is achieved by simply dividing down the master's output voltage with a simple resistor network. Coincident, ratiometric, and offset tracking modes are possible.

If an external voltage source is connected to the SS/TRACK pin, the external soft-start capability of the LM27403 is effectively disabled (the internal soft-start is still enabled). The regulated output voltage level is reached when the SS/TRACK pin reaches the 0.6-V reference voltage level. It is the responsibility of the system designer to determine if an external soft-start capacitor is required to keep the device from entering current limit during a startup event. Likewise, the system designer must also be aware of how fast the input supply ramps if the tracking feature is enabled.

Figure 34 shows a triangular voltage signal directly driving SS/TRACK and the corresponding output voltage tracking response. Nominal output voltage here is 1.2 V, with channel scales chosen such that the waveforms overlap during tracking. As expected, the PGOOD flag transitions at thresholds of 91% (rising) and 87% (falling) of the nominal output voltage setpoint.

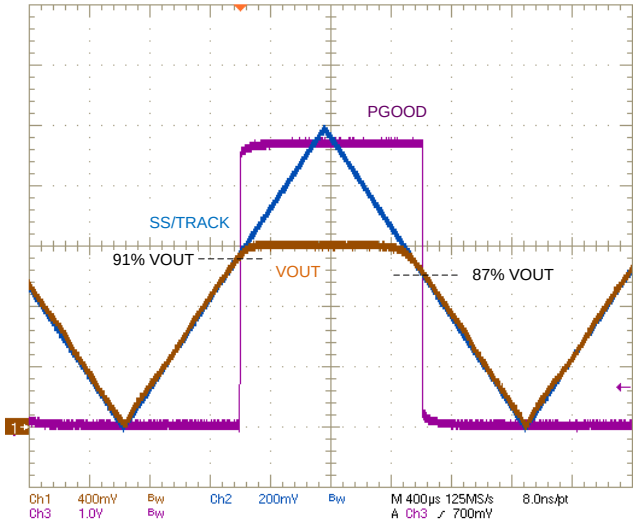


Figure 34. Typical Output Voltage Tracking Waveforms and PGOOD Flag

Two practical tracking configurations, ratiometric and coincident, are shown in Figure 35. The most common application is coincident tracking, used in core vs. I/O voltage tracking in DSP and FPGA implementations. Coincident tracking forces the master and slave channels to have the same output voltage ramp rate until the slave output reaches its regulated setpoint. Conversely, ratiometric tracking sets the slave's output voltage to a fraction of the master's output voltage during startup.

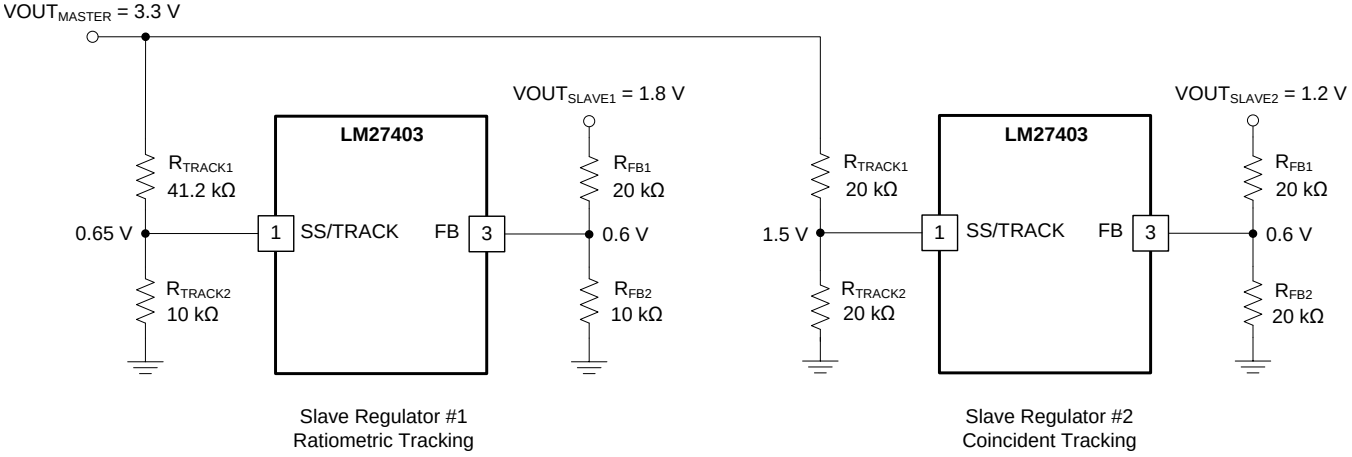


Figure 35. Tracking Implementation with Master, Ratiometric Slave and Coincident Slave Rails

For coincident tracking, connect the slave regulator's SS/TRACK input to a resistor divider from the master's output voltage that is the same as the divider used on the slave's FB pin. In other words, simply select R_{TRACK1} = R_{FB1} and R_{TRACK2} = R_{FB2} as shown in Figure 35. As the master voltage rises, the slave voltage rises identically. Eventually, the slave voltage reaches its regulation voltage, at which point the internal reference takes over the regulation while the SS/TRACK input continues to increase, thus removing itself from changing the output voltage.

In all cases, to ensure that the output voltage accuracy is not compromised by the SS/TRACK voltage being too close to the 0.6-V reference voltage, the final value of the slave's SS/TRACK voltage should be at least 20 mV above FB.

MONOTONIC STARTUP

The LM27403 has monotonic startup capability with no dips or flat spots in the output voltage waveform during startup (including prebiased startup) and fault recovery. During the soft-start interval, FB follows SS/TRACK, and the output voltage linearly increases to the nominal output setpoint. Figure 36 illustrates the output voltage behavior during a monotonic startup to a nominal level of 1.2V. The UVLO/EN pin is driven high by a TTL logic signal. As mentioned previously, the startup time is determined by the use of an external soft-start capacitor at the SS/TRACK pin charged by an internally generated 3-µA constant current source. If a soft-start capacitor is not used, the device automatically enables the internal 7-bit (128 step) digital soft-start. The PGOOD flag transitions high when FB reaches its 91% threshold. As described previously, there is a calibration interval based on four cycles on the D+ pin (i.e. 512 clock cycles) that creates a delay from UVLO/EN crossing its precision threshold to SS/TRACK being released.

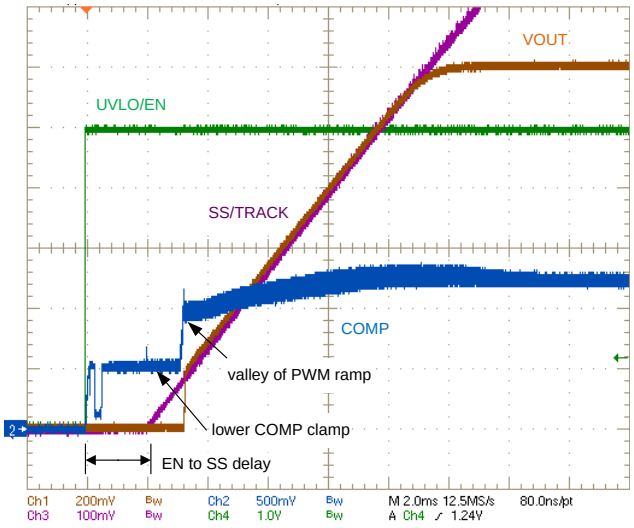


Figure 36. Typical Monotonic Output Voltage Startup Waveforms, 1.2-V Output

PREBIAS STARTUP

In certain applications, the output voltage may have an initial voltage prebias before the LM27403 is powered on or enabled. The LM27403 is able to startup into a prebiased load while maintaining a monotonic output voltage startup characteristic.

The LM27403 does not allow switching until the SS/TRACK pin voltage has reached the feedback (FB) voltage level. Once this level is reached, the controller begins to regulate and switch synchronously, allowing a certain amount of negative current during PWM switching operation. Thereafter, the feedback voltage follows the soft-start voltage up to 0.6 V. This is illustrated in Figure 37 where nominal output voltage is 1.2 V and the output voltage waveform represents twice the FB level. The output is not pulled low during a prebiased startup condition. Note that if the output is prebiased to a higher voltage than the nominal level (as set by the feedback resistor divider), the LM27403 does not pull the output low, hence eliminating current flow through parasitic paths in the system.

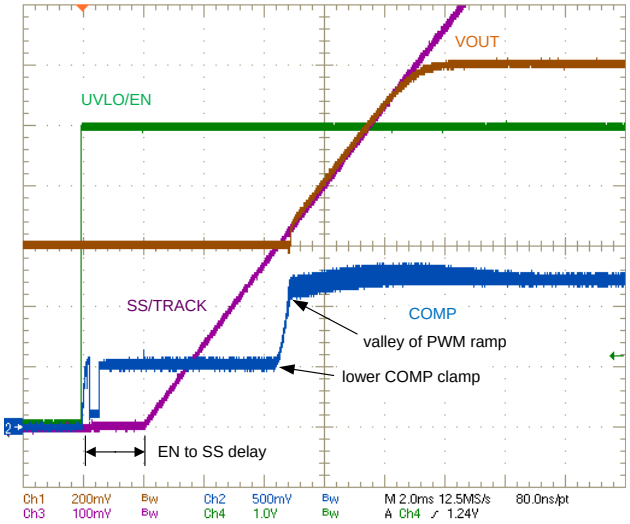


Figure 37. Typical Startup Waveforms with 0.6-V Prebiased Output, 1.2-V Nominal Output

The LM27403 automatically pulls down the SS/TRACK pin to GND before the onset of switching and during a restart from a fault condition. When SS/TRACK is initially released, subsequent to the temperature sense calibration delay, the COMP voltage is released to the lower COMP clamp level and no switching occurs. Both the LG and HG pins are held low while the SS/TRACK voltage stays below the FB voltage level. This action ensures that a prebiased load is not pulled down by a negative dc output current component. When the SS/TRACK pin voltage crosses above either FB or VREF, the COMP voltage slews up to the valley of the PWM ramp and switching begins.

VOLTAGE-MODE CONTROL

The LM27403 incorporates a voltage-mode control loop implementation with input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies feedback loop design because loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, k_{FF}, is 1/9, equivalent to the ramp amplitude divided by the input voltage, V_{RAMP}/V_{IN}. See the CONTROL LOOP COMPENSATION section for more detail.

OUTPUT VOLTAGE REMOTE SENSE: RS

High-current switching power supplies typically use output voltage remote sensing to achieve the greatest accuracy at the point of load. There are usually some finite bus structure resistances between the power supply and load, denoted by lumped elements R_{BUS+} and R_{BUS-} in Figure 38, that cause unwanted voltage drops or load regulation errors, particularly at high output currents.

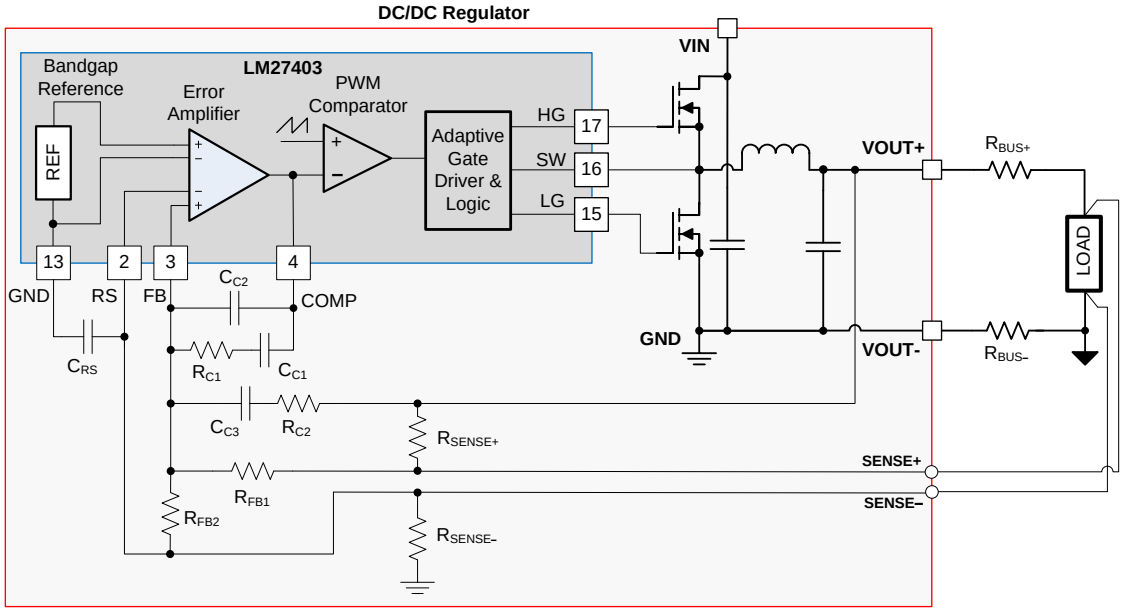


Figure 38. LM27403 Output Remote Sense and Voltage Control Loop

Remote ground sensing is implemented in the LM27403 by bringing another amplifier input, designated RS, outside of the device package to act as a kelvin ground sense. This circuit is created by replacing the standard error amplifier used in the PWM loop with a new amplifier that has two pairs of differential inputs. One of the differential input pairs is used to sense the internal reference voltage relative to the IC ground potential. The other differential input is used to remotely sense the feedback (FB) voltage relative to RS connected to the negative load terminal (at the output point of load). The output of the new error amplifier is the difference between the two pairs of inputs multiplied by some gain factor, and in all other respects works the same as the classic op-amp type error amplifier.

For accurate remote sensing of the output at the load, make sure to tie upper feedback resistor R_{FB1} directly to the load at the point where output regulation is required. However, in order to minimize injected noise into the high-impedance FB node, connect the RC lead network, R_{C2} and C_{C3}, typically found across R_{FB1} in voltage-mode control loop compensation networks, to the local VOUT connection, as shown in Figure 38. Similarly, connect the negative sense line locally at the negative load terminal and route both sense lines as a differential pair to minimize pickup and injected noise. Sense resistors, R_{SENSE+} and $R_{SENSE–}$, typically 10 Ω each, are used to maintain regulation when the remote sense lines are not connected or as a fail-safe measure if the lines become disconnected. In particularly noisy environments, capacitor C_{RS} shown in Figure 38 (typically 0.1 µF) is supplemented by a series resistor (for example, 10 Ω). If remote sense is not required, RS is simply shorted to GND.

The configuration in Figure 38 avoids the use of a separate unity-gain differential amplifier, a solution commonly used to perform remote sensing. The offset and gain error of this differential amplifier configuration compound any inaccuracy associated with the reference and error amplifier input offset voltage. The accuracy of the feedback system is not compromised when using the method shown in Figure 38. The LM27403 specified feedback accuracy of ±1% is preserved over the full operating temperature range.

POWER GOOD: PGOOD

To implement an open-drain power-good function for sequencing and fault detection, use the PGOOD pin of the LM27403. The PGOOD open-drain MOSFET is pulled low during current limit, UVLO, output undervoltage and overvoltage, or if the output is not regulated.

More specifically, this function can be triggered by multiple events, including the output voltage either exceeding the overvoltage threshold (117% VREF) or decreasing below the undervoltage threshold (91% VREF), heavy overcurrent, soft-start voltage (both internal and external) below 91% VREF, UVLO, thermal shutdown, enable delay, or disabled state.

To prevent momentary glitches to the PGOOD pin, a 20-µs deglitch filter is built into the LM27403 to prevent multiple triggerings of the flag. Note that the primary objective of PGOOD is to signal to the system that the soft-start period has expired and the output voltage is in regulation for loads within the rated limit. This can be used for sequencing downstream regulators, an example of which is shown schematically in Figure 43.

During soft-start operation, the PGOOD flag is effectively a logic AND of two signals:

1. The internal soft-start counter (signals the internal soft-start-done flag when the count reaches 128).
2. The UVT comparator output. Note that the UVT comparator monitors SS/TRACK voltage until the first PWM pulse, and then monitors the FB voltage.

The reason for multiplexing the UVT comparator is to support prebias loads and tracking. The PGOOD voltage waveform is shown in Figure 34 with a 100-kΩ pullup resistor to VDD. As described previously, VDD disappears when UVLO/EN is pulled lower than an effective diode drop (~0.7 V). This does not represent a system-level issue because PGOOD is already pulled low in that scenario.

GATE DRIVERS: LG and HG

The LM27403 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{VDD} = 4.5 V, the LM27403's low-side driver has a low impedance pull-down path of 0.9 Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.5-Ω and 1.0-Ω pull-up and pull-down impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

Furthermore, there is a proprietary adaptive deadtime control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery related losses. The LM27403 is fully compatible with discrete and Power Block NexFET™ MOSFETs from TI.

SINK AND SOURCE CAPABILITY

Even though an LM27403-based dc/dc regulator is capable of sinking and sourcing current (as it operates in CCM), the inductor DCR-based overcurrent protection operates only with positive currents. Negative currents are detected through the low-side MOSFET only when the device is in an overvoltage condition (refer to Zero Cross and NEGATIVE CURRENT LIMIT sections). Note that prebias startup still operates normally (refer to PREBIAS STARTUP section).

FAULT CONDITIONS

Overcurrent, overtemperature, output undervoltage and overvoltage protection features are included in the LM27403.

THERMAL SHUTDOWN

The LM27403 includes an internal junction temperature monitor. If the temperature exceeds 150°C (typ), thermal shutdown occurs. When entering thermal shutdown, the device:

1. turns off the low-side and high-side MOSFETs;
2. flushes the external soft-start capacitor;
3. initiates a soft-start sequence when the die temperature decreases by the OTP hysteresis, 20°C (typ).

This is a non-latching protection, and, as such, the device will cycle into and out of thermal shutdown if the fault persists.

CURRENT LIMIT AND SHORT CIRCUIT OPERATION (POSITIVE OVERCURRENT)

When detecting a current-limit (CL) event, one of the following actions occur:

1. *Light CL*: When a current limit event is detected, the high-side on-pulse is immediately terminated (HG off, LG on) and the system continues regulating on the next system clock event;
2. *Heavy CL*: If five current limit events occur in any 32 clock cycles, the pulse is terminated (HG off, LG off) and hiccup mode is entered.

The following actions occur in hiccup mode:

1. HG off, LG off;

2. Re-enable soft-start clock to count 5-ms timeout for hiccup delay;
3. At the end of the hiccup delay, re-enter the startup sequence, including the internal enable delay.

Every time a current limit event is detected, the current limit event counter is incremented on the next clock edge. If the current limit event counter reaches its threshold of five, then the hiccup mode is entered.

NEGATIVE CURRENT LIMIT

Negative current limit detection is in effect only after an overvoltage (OV) condition is met. The OV flag is deglitched by 10 µs. By the time OV is signaled, the loop has most likely moved into a low- or zero-percent duty cycle that poses the threat of excessive negative current. Thus, the negative current limit is in effect as soon as the OV condition is detected rather than waiting for the deglitched version. If the negative current limit is exceeded, the low-side MOSFET gate (LG pin) is pulled low and the LM27403 enters *Negative Current Limit* hiccup mode for 5 ms.

Negative Current Limit hiccup mode (subsequent to OVP) is different from Current Limit hiccup mode in that zero-cross current detection is active in the latter and the LG output is high. However, as with Current Limit hiccup mode, the system attempts to restart after the 5-ms timeout, as described in the CURRENT LIMIT HANDLING section. The LM27403 detects a negative current limit by monitoring the switch-node (SW) voltage while the low-side MOSFET is on. If the switch-node voltage (that is, the low-side MOSFET drain-source voltage) rises 100 mV above ground during the low-side MOSFET conduction interval, the comparator trips, signaling that the negative current limit threshold has been reached. The low-side MOSFET is turned off, thus protecting it from excess current.

The negative current comparator is valid only when the LG is high. Blanking time lasts 20 ns to 50 ns after LG has been asserted. Blanking recurs as soon as PWM goes high.

UNDERVOLTAGE THRESHOLD (UVT)

The FB pin is also monitored for an output voltage excursion below the nominal level. However, if the UVT comparator is tripped, no action occurs on the normal switching cycles. The UVT signal is used solely as a valid condition for the Power Good flag to transition low. When the FB voltage exceeds 91% of the reference voltage, the Power Good flag transitions high. Conversely, the Power Good flag transitions low when the FB voltage is less than 87% of the reference.

OVERVOLTAGE THRESHOLD (OVT)

When the FB voltage exceeds 116.5% of the reference voltage, the Power Good flag transitions low after a 10-µs deglitch. The control loop attempts to bring the output voltage back to the nominal setpoint. Conversely, when the FB voltage goes below 113% of the reference, the Power Good flag is allowed to transition high. Negative current-limit detection is activated when the regulator is in an OV condition. See the NEGATIVE CURRENT LIMIT section for more details.

APPLICATION INFORMATION

POWER TRAIN COMPONENTS

Comprehensive knowledge and understanding of the power train components are key to successfully completing a buck regulator design. The LM27403 design tool and Webench™ are available to assist the designer with selection of these components for a given application.

FILTER INDUCTOR

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 20% and 40% of the maximum dc output current. Choose the inductance using the following equation:

$$L = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{\Delta I_L F_{sw}} \right) \quad (10)$$

Check the inductor datasheet to ensure that the inductor's saturation current is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic – the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that an inductor's saturation current generally deceases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

OUTPUT CAPACITORS

Ordinarily, the regulator's output capacitor energy store combined with the control loop response are prescribed to maintain the integrity of the output voltage within both the static and dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics – equivalent series resistance (ESR) and equivalent series inductance (ESL) – take increasing precedence in shaping the regulator's load transient response as the output current ramp amplitude and slew rate increase.

So, the output capacitor, C_{OUT}, exists to filter the inductor ripple current and provide a reservoir of charge for step load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_O, choose an output capacitance that is larger than

$$C_{OUT} \geq \frac{\Delta I_L}{8 F_{sw} \sqrt{\Delta V_O^2 - (R_{ESR} \Delta I_L)^2}} \quad (11)$$

Figure 39 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load-on transient. Similarly, during and after a load-off transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that needs to be depleted as quickly as possible.

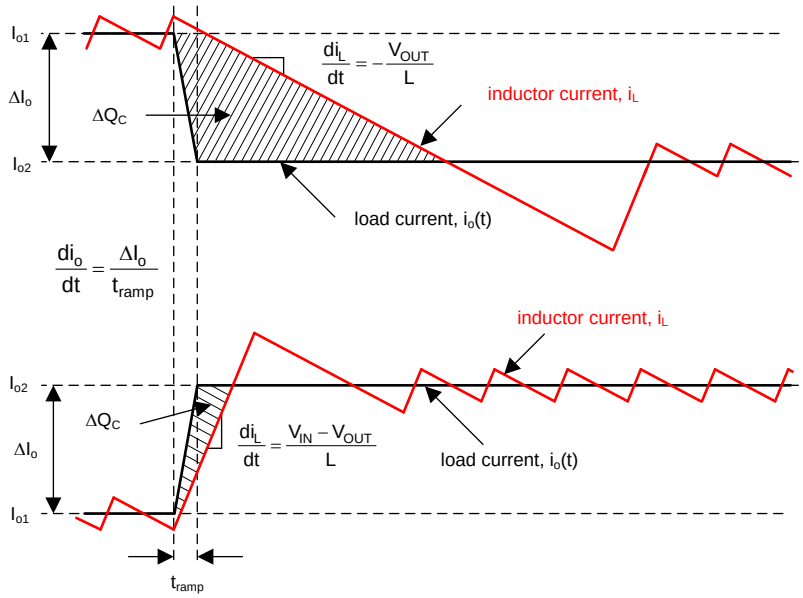


Figure 39. Load Transient Response Representation Showing C_{OUT} Charge Surplus Or Deficit.

In a typical regulator application of 12-V input to low output voltage (say 1.2 V), it should be recognized that the load-off transient represents worst-case. In that case, the steady-state duty cycle is approximately 10% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and rein in the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{overshoot}$ with step reduction in output current given by ΔI_o), the output capacitance should be larger than

$$C_{OUT} \geq \frac{\Delta I_o^2 L}{(V_{OUT} + \Delta V_{overshoot})^2 - V_{OUT}^2} \quad (12)$$

The ESR of a capacitor is provided in the manufacturer's datasheet either explicitly as a specification or implicitly in the impedance vs. frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some ESR and ESL as well. Ceramic output capacitors, on the other hand, are such that the impedances related to the ESR and ESL are small at the switching frequency, and the capacitive impedance dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied voltage and operating temperature.

Ignoring the ESR term in Equation 11 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. One to four 100-µF, 6.3-V, X5R capacitors in 1206 or 1210 footprint is a common choice. Use Equation 12 to quantify if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale of paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range of interest. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load-transient demands.

INPUT CAPACITORS

Input capacitors are necessary to limit the input ripple voltage while switching-frequency ac current to the buck power stage. It is generally recommended to use X5R or X7R dielectric ceramic capacitors, thus providing low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET.

The input capacitors' RMS current is given by Equation 13.

$$I_{CIN,rms} = \sqrt{D\left(I_O^2(1-D) + \frac{\Delta I_L^2}{12}\right)} \quad (13)$$

The highest requirement for input capacitor RMS current rating occurs at D = 0.5, at which point the RMS current rating should be greater than half the output current.

Ideally, the dc component of input current is provided by the input voltage source and the ac component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude $I_o - I_{IN}$ during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of ac ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by Equation 14.

$$\Delta V_{IN} = \frac{I_O D(1-D)}{F_{sw} C_{IN}} + D I_O R_{ESR} \quad (14)$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 15.

$$C_{IN} \geq \frac{D(1-D) I_O}{F_{sw}(\Delta V_{IN} - D R_{ESR} I_O} \quad (15)$$

Low ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and one or two 10-µF 25-V X7R ceramic decoupling capacitors are usually sufficient. Select the input bulk capacitor based on its ripple current rating and operating temperature.

POWER MOSFETs

The choice of MOSFET has significant impact on DC-DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge, Q_G, and vice versa. As a result, the product $R_{DS(on)}$*Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting MOSFET selection in an LM27403 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 4.5 V;
- Drain-source voltage rating, BV_{DSS}, typically 25 V or 30 V;
- Gate charge parameters at V_{GS} = 4.5 V;
- Body diode reverse recovery charge, Q_{RR};
- Gate threshold voltage, $V_{GS(th)}$, derived from the plateau in the Q_G vs. V_{GS} curve in the MOSFET's datasheet. $V_{GS(th)}$ should be in the range 2 V to 3 V such that the MOSFET is adequately enhanced when on and margin against Cdv/dt shoot-through exists when off.

The MOSFET-related power losses are summarized by the equations presented in Table 3. While the affect of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances, are not discussed. Consult the *LM27403 design tool* to assist with loss calculations.

Table 3. Buck Regulator MOSFET Power Losses

Power Loss Mode	High-Side MOSFET	Low-Side MOSFET
Conduction (1)	$P_{cond_{high-side}} = D\left(I_o^2 + \frac{\Delta I_L^2}{12}\right)R_{DS(on)_{high-side}}$	$P_{cond_{low-side}} = D'\left(I_o^2 + \frac{\Delta I_L^2}{12}\right)R_{DS(on)_{low-side}}$ (2)
Switching	$P_{sw_{high-side}} = V_{IN}F_{sw}\left[\left(I_o - \frac{\Delta I_L}{2}\right)t_R + \left(I_o + \frac{\Delta I_L}{2}\right)t_F\right]$	Negligible
Gate Drive (3)	$P_{Gate_{high-side}} = V_{DD}F_{sw}Q_{G_{high-side}}$	$P_{Gate_{low-side}} = V_{DD}F_{sw}Q_{G_{low-side}}$
Body Diode Conduction	N/A	$P_{cond_{body\ diode}} = V_F F_{sw}\left[\left(I_o + \frac{\Delta I_L}{2}\right)t_{dt1} + \left(I_o - \frac{\Delta I_L}{2}\right)t_{dt2}\right]$
Body Diode Reverse Recovery	$P_{RR} = V_{IN}F_{sw}Q_{RR_{low-side}}$	

(1) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4000 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance.
(2) D' = 1–D is the duty cycle complement.
(3) Gate drive loss is not dissipated in the MOSFET but rather in the LM27403's integrated drivers.

The high-side (control) MOSFET carries the inductor current during the PWM on time (or D interval) and typically incurs most of the switching losses. It is therefore imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the deadtime. The LM27403, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high input voltage and low output voltage applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery.

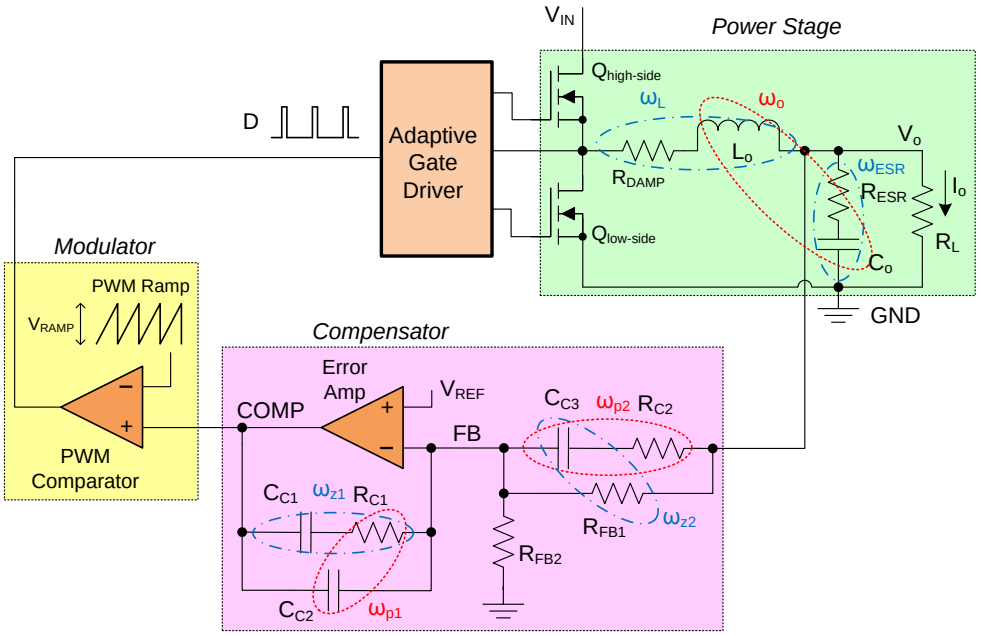
The LM27403 is well matched to TI's comprehensive portfolio of 25-V and 30-V NexFET™ family of power MOSFETs. In fact, the LM27403 is ideally suited to driving the Power Block NexFET™ modules with integrated high-side and low-side MOSFETs. Excellent efficiency is obtained by virtue of reduced parasitics and exemplary thermal performance of the Power Block MOSFET implementation. See the DESIGN EXAMPLES section for more details.

CONTROL LOOP COMPENSATION

The poles and zeros inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in Table 4.

The compensation network typically employed with voltage-mode control is a type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy then is to use two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. Finally, a resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, R_{FB2}, has no impact on the control loop from an ac standpoint since the FB node is the input to an error amplifier and is effectively at ac ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.

Table 4. Regulator Poles and Zeros



Power Stage Poles	Power Stage Zeros	Compensator Poles	Compensator Zeros
$\omega_o = \frac{1}{\sqrt{L_o C_o \left(\frac{1+R_{ESR}/R_L}{1+R_{ESR}/R_{DAMP}}\right)}} \cong \frac{1}{\sqrt{L_o C_o}}$	$\omega_{ESR} = \frac{1}{R_{ESR} C_o}$ (1)	$\omega_{p1} = \frac{1}{R_{C2} C_{C3}}$	$\omega_{z1} = \frac{1}{R_{C1} C_{C1}}$
	$\omega_L = \frac{L_o}{R_{DAMP}}$ (2)	$\omega_{p2} = \frac{1}{R_{C1}(C_{C1} \parallel C_{C2})} \cong \frac{1}{R_{C1} C_{C2}}$	$\omega_{z2} = \frac{1}{(R_{FB2} + R_{C2}) C_{C3}}$

(1) R_{ESR} represents the ESR of output capacitor C_o.
(2) $R_{DAMP} = D*R_{DS(on)high\text{-}side} + (1–D)*R_{DS(on)low\text{-}side} + R_{dcr}$, shown as a lumped element in the schematic, represents the effective series damping resistance.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the output capacitor's ESR. The dc (and low frequency) gain of the modulator and power stage is V_{IN}/V_{RAMP}. Representing the gain from COMP to the average voltage at the input of the LC filter, this is held essentially constant by the LM27403's PWM line feedforward feature at 9 V/V or 19 dB.

Complete expressions for small-signal frequency analysis are presented in Table 5. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified directly by its loop gain but by its performance related characteristics, namely closed-loop output impedance and audio susceptibility.

Table 5. Buck Regulator Small-Signal Analysis

PARAMETER	EXPRESSION
Open-loop transfer function	$T_v(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)} \cdot \frac{\hat{v}_o(s)}{\hat{d}(s)} \cdot \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = G_c(s)G_{vd}(s)F_M$
Duty-cycle-to-output transfer function	$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Big\|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_o(s)=0}} = V_{IN} \frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^2}}$
Compensator transfer function(1)	$G_c(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)} = K_{mid} \frac{\left(1+\frac{\omega_{z1}}{s}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$
Modulator transfer function	$F_M = \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = \frac{1}{V_{RAMP}}$

(1) $K_{mid} = R_{C1}/R_{FB1}$ is the compensator's mid-band gain. By expressing one of the compensator zeros in inverted zero format, the mid-band gain is denoted explicitly.

An illustration of the open-loop response gain and phase is given in Figure 40. The poles and zeros of the system are marked with x and o symbols, respectively, and a + symbol indicates the crossover frequency. When plotted on a log (dB) scale, the open-loop gain is effectively the sum of the individual gain components from the modulator, power stage and compensator – this is clear from Figure 41. The open-loop response of the system is measured experimentally by breaking the loop, injecting a variable-frequency oscillator signal and recording the ensuing frequency response using a network analyzer setup.

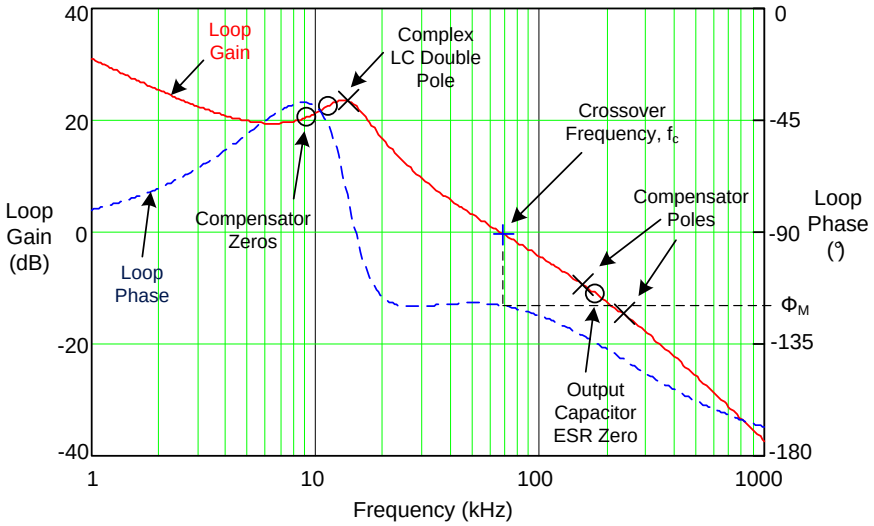


Figure 40. Typical Buck Regulator Loop Gain and Phase with Voltage-Mode Control

If the pole located at ω_{p1} cancels the zero located at ω_{ESR} and the pole at ω_{p2} is located well above crossover, the expression for the loop gain, $T_v(s)$ in Table 5, can be manipulated to yield the simplified expression given as follows.

$$T_v(s) = \frac{R_{C1}C_{C3}}{s}\omega_o^2 \frac{V_{IN}}{V_{RAMP}} \quad (16)$$

Essentially, a multi-order system is reduced to a single order approximation by judicious choice of compensator components. A simple solution for the crossover frequency, denoted as f_c in Figure 40, with type-III voltage-mode control is derived as follows.

$$\omega_c = 2\pi f_c = K_{mid} \frac{V_{IN}}{V_{RAMP}} \omega_o \quad (17)$$

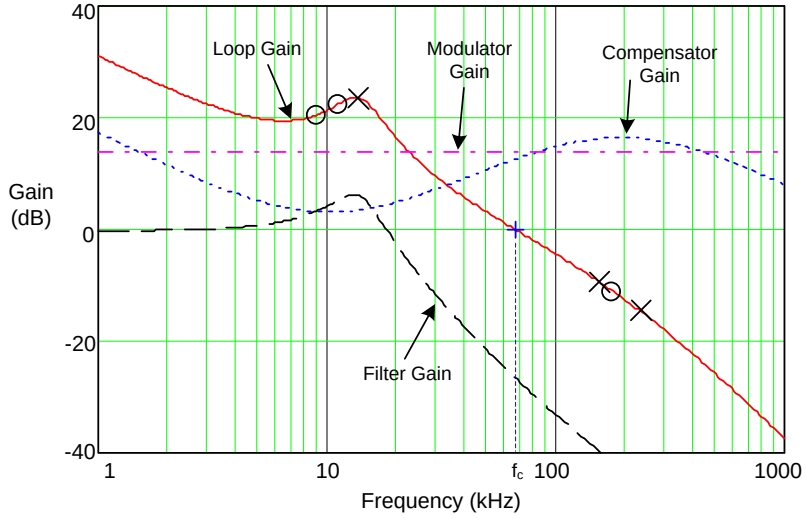


Figure 41. Buck Regulator Constituent Gain Components

The loop crossover frequency is usually selected between one-tenth to one-fifth of switching frequency. Inserting an appropriate crossover frequency into Equation 17 gives a target for the compensator's mid-band gain, K_{mid}. Given an initial value for R_{FB1}, R_{FB2} is then selected based on the desired output voltage. Values for R_{C1}, R_{C2}, C_{C1}, C_{C2} and C_{C3} are calculated from the design-oriented expressions listed in Table 6, with the premise that the compensator poles and zeros are set as follows: $\omega_{z1} = 0.5\omega_o$, $\omega_{z2} = \omega_o$, $\omega_{p1} = \omega_{ESR}$, $\omega_{p2} = \omega_{sw}/2$.

Table 6. Compensation Component Selection

RESISTORS	CAPACITORS
$R_{FB2} = \frac{R_{FB1}}{(V_o/V_{REF}) - 1}$	$C_{C1} = \frac{2}{\omega_{z1} R_{C1}}$
$R_{C1} = K_{mid} R_{FB1}$	$C_{C2} = \frac{1}{\omega_{p2} R_{C1}}$
$R_{C2} = \frac{1}{\omega_{p1} C_{C3}}$	$C_{C3} = \frac{1}{\omega_{z2} R_{FB1}}$

Referring to the bode plot in Figure 40, the phase margin, indicated as φ_M, is the difference between the loop phase and –180° at crossover. A target of 50° to 70° for this parameter is considered ideal. Additional phase boost is dialed in by locating the compensator zeros at a frequency lower than the LC double pole (hence why C_{C1} is scaled by a factor of 2 above). This helps to mitigate the phase dip associated with the LC filter, particularly at light loads when the Q-factor is higher and the phase dip becomes especially prominent. The ramification of low phase in the frequency domain is an under-damped transient response in the time domain.

The power supply designer now has all the tools at his/her disposal to optimally position the loop crossover frequency while maintaining adequate phase margin over the power supply's required line, load and temperature operating ranges.

DESIGN EXAMPLES

DESIGN 1 - High-Efficiency Synchronous Buck Regulator for Telecom Power

The schematic diagram of a 25-A regulator is given in Figure 42. The full-load efficiency is 91% and 97% at 1.2-V and 5.3-V output voltages, respectively. Output voltage is adjusted simply by changing R_{FB2}.The powertrain components are cited in Table 7, and many of the components are available from multiple vendors. The switching frequency is set by a synchronization signal at 300 kHz. Free-running switching frequency (in the event that the synchronization signal disappears) is set to 250 kHz by resistor R_{FADJ}. The current limit setpoint is 28.5 A based on resistor R_{ISET} and the inductor DCR (1.1 mΩ typ at 25°C). This design is quite similar to the LM27403 EVM circuit; refer to the *LM27403EVM User's Guide* for more detail.

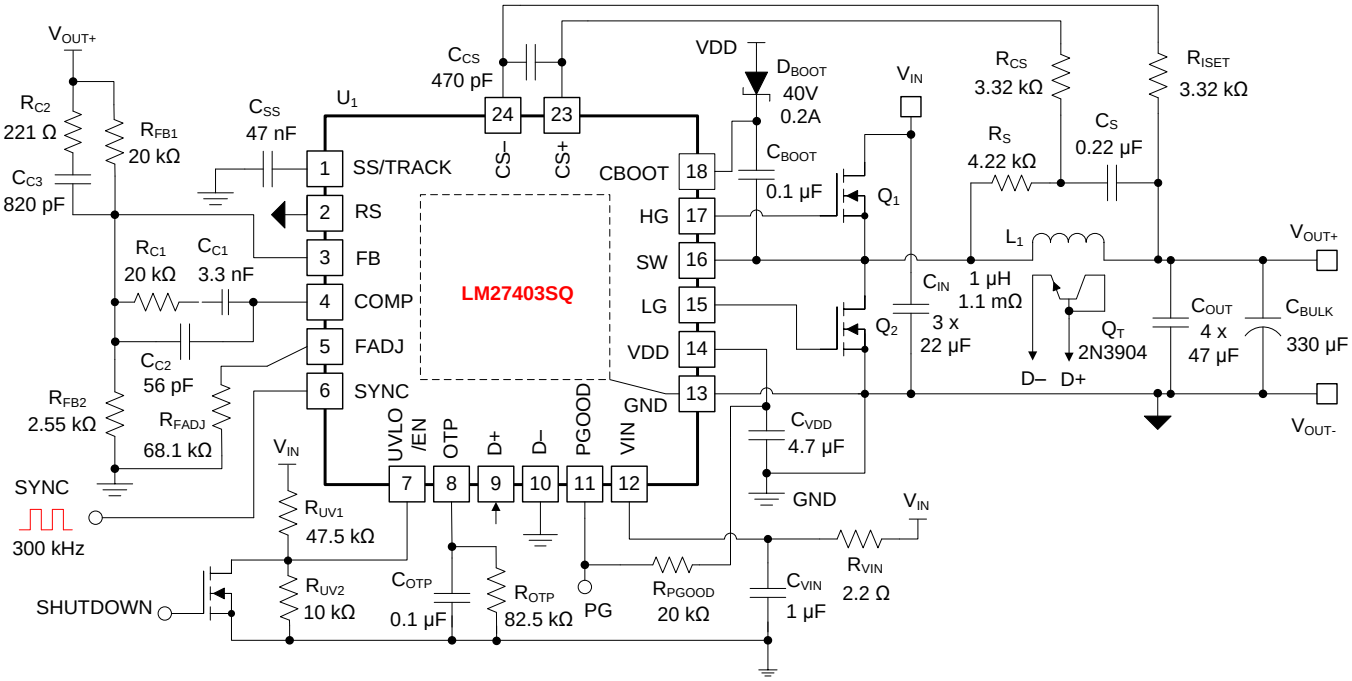


Figure 42. Application Circuit 1 with V_{IN} = 6.5 V to 20 V ($V_{IN(nom)}$ = 12 V), V_{OUT} = 0.6 V to 5.3 V, $I_{OUT(max)}$ = 25 A, F_{SW} = 300 kHz (using external synchronization signal)

Table 7. List of Materials for Design 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	3	22 µF, 25 V, X7R, 1210 ceramic	Kemet	C1210C226M3RACTU
			Taiyo Yuden	TMK325B7226MM-TR
			Murata	GRM32ER71E226KE15L
C_{OUT}	4	47 µF, 10 V, X7R, 1210 ceramic	Taiyo Yuden	LMK325B7476MM-TR
			Murata	GRM32ER71A476KE15L
C_{BULK}	1	330 µF, 6.3 V, 9 mΩ, D3L POSCAP	Sanyo	6TPF330M9L
L_1	1	1.0 µH, 30 A, 1.08 mΩ ±10%, ferrite	Delta	HMP1360-1R0-63
Q_1	1	25 V, high-side MOSFET	Infineon	BSC032NE2LS
			Texas Instruments	CSD16322Q5
Q_2	1	25 V, low-side MOSFET	Infineon	BSC010NE2LS
			Texas Instruments	CSD16415Q5

DESIGN 2 - Powering Multicore DSPs

The schematic diagram of a 450-kHz, 12-V nominal input, 15-A regulator powering a KeyStone™ DSP is given in Figure 43. The important components are listed in Table 8. The regulator output current requirements are dependent upon the baseline and activity power consumptions of the DSP in a real-use case. While baseline power is highly dependent on voltage, temperature and DSP frequency, activity power relates to dynamic core utilization, DDR3 memory access, peripherals, and so on. To this end, the IDAC_OUT pin of the LM10011 connects to the LM27403 FB pin to allow continuous optimization of the core voltage. The SmartReflex-enabled DSP provides 6-bit information using the VCNTL open-drain IOs(1) to command the output voltage setpoint with 6.4-mV step resolution. This design uses a TI NexFET™ Power Block module CSD87330Q3D (dual asymmetric MOSFETs in SON 3.3-mm x 3.3-mm package) together with low-DCR, metal-powder inductor and composite ceramic–polymer electrolytic output capacitor implementation.

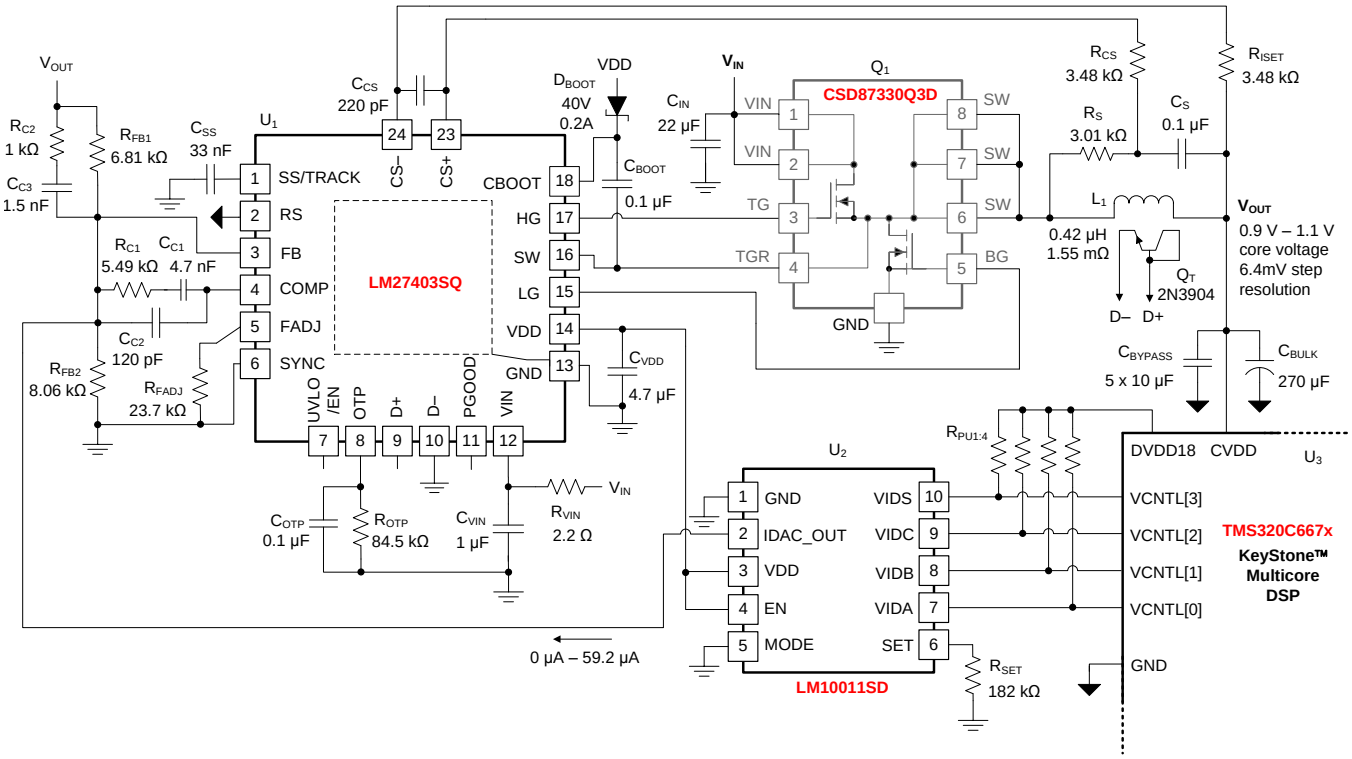


Figure 43. Application Circuit 2 with V_{IN} = 3 V to 20 V, V_{OUT} = 0.9 V to 1.1 V, $I_{OUT(max)}$ = 15 A, F_{SW} = 450 kHz

Table 8. List of Materials for Design 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	1	22 µF, 25 V, X5R, 1210 ceramic	Taiyo Yuden	TMK325BJ226MM-T
C_{BYPASS}	5	10 µF, 4 V, X5R, 0402 ceramic	Taiyo Yuden	AMK105BJ106MV-F
C_{BULK}	1	270 µF, 2 V, 6 mΩ, 3.2 Arms, 3.5 mm x 2.8 mm, POSCAP	Panasonic	2TPSF270M6E
L_1	1	0.42 µH, 22 A, 1.55 mΩ ±7%, molded, 6.9 mm x 6.6 mm	Cyntec	PIME064T-R42MS1R557
Q_1	1	30 V Power Block Q3D MOSFET Module, 3.3 mm x 3.3 mm	Texas Instruments	CSD87330Q3D
Q_T	1	2N3904 type NPN transistor, 40 V, 0.2 A, SOT-523	Diodes, Inc.	MMBT3904T
U_2	1	6- or 4-bit VID Programmable Current DAC, WSON-10	Texas Instruments	LM10011SD
U_3	1	KeyStone™ DSP	Texas Instruments	TMS320C667x

(1) See TI Application Report entitled *Hardware Design Guide for Keystone I Devices* for further detail.

DESIGN 3 - Powering FPGAs using Flexible 30A Regulator with Small Footprint

The schematic diagram of a 600-kHz, 30-A regulator is given in Figure 44. A high power density, high efficiency solution is feasible by using TI NexFET™ Power Block module CSD87350Q5D (dual asymmetric MOSFETs in a SON 5-mm x 6-mm package) together with and low-DCR ferrite inductor and all-ceramic capacitor design. The design occupies 20 mm x 15 mm on a single-sided PCB. Knowing the cumulative resistance of the inductor DCR and Power Block MOSFET SW clip (approximately 1 mΩ at 25°C), resistor R_{ISET} positions the current limit setpoint at 28A. The output voltage is adjusted by choosing the resistance of R_{FB2} appropriately. Resistors R_{TRK1} and R_{TRK2} connected to the SS/TRACK pin define a coincidental tracking startup sequence from a master power supply, V_{TRACK}.

The powertrain components are listed in Table 9. Additional input and/or output capacitance can be added if needed, but adjust the compensation if C_{OUT} changes. The T_{GR} pin of the Power Block MOSFET serves as a kelvin connection to the high-side MOSFET's source and represents the return path for the high-side gate drive. Along with bootstrap capacitor, C_{BOOT}, T_{GR} is connected to the LM27403's SW pin.

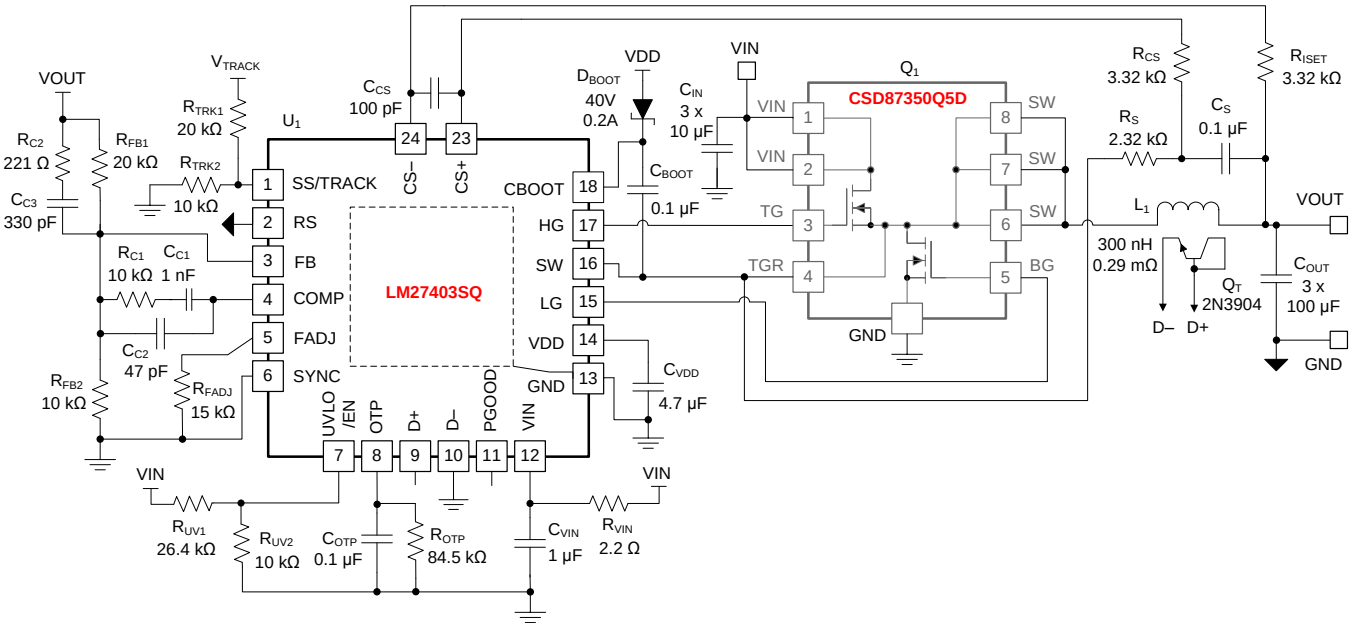


Figure 44. Application Circuit 3 with V_{IN} = 4.5 V to 15 V ($V_{IN(nom)}$ = 12 V), V_{OUT} = 1.8 V, $I_{OUT(max)}$ = 30 A, F_{SW} = 600 kHz

Table 9. List of Materials for Design 3

REFERENCE DESIGNATOR	QTY	SPECIFICATION		MANUFACTURER	PART NUMBER
C_{IN}	3	10 µF, 25 V, X5R, 0805 ceramic		Taiyo Yuden	TMK212BBJ106KG-T
				Murata	GRM21BR61E106KA73L
				TDK	C2012X5R1E106M
C_{OUT}	1	100 µF, 6.3 V, X5R, 1206 ceramic		Taiyo Yuden	JMK316BJ107ML-T
				Murarta	GRM31CR60J107ME39L
				TDK	C3216X5R0J107M
				Kemet	C1206C107M9PACTU
L_1	1	300 nH, ferrite	35 A, 0.29 mΩ ±8%	Coiltronics	FP1107R1-R30-R
			34 A, 0.29 mΩ ±7%	Cyntec	PCDC1107-R30EMO
		270 nH, ferrite	37 A, 0.24 mΩ ±5%	Coilcraft	SLC1175-271MEC
		250 nH, ferrite	44 A, 0.37 mΩ ±7%	Wurth	744308025
Q_1	1	30 V Power Block Q5D MOSFET Module, 5 mm x 6 mm		Texas Instruments	CSD87350Q5D

DESIGN 4 - Regulated 12-V Rail with LDO Low-Noise Auxiliary Output for RF Power

The schematic diagram of a 280-kHz, 12-V output, 10-A buck regulator for RF power applications is given in Figure 45(1). A 10-Ω resistor in series with C_{BOOT} is used to slow the turn-on transition of the high-side MOSFET, reducing the spike amplitude and ringing of the SW node waveform and minimizing the possibility of Cdv/dt-induced shoot-through of the low-side MOSFET. If needed, place an RC snubber (for example, 2.2 Ω and 1 nF) close to the SW node and GND(2). An auxiliary 10-V, 800-mA rail to power noise-sensitive circuits is available using the LP38798 ultra-low noise LDO as a post-regulator. The internal pullup of the LP38798's EN pin facilitates direct connection to the LM27403's PGOOD for sequential startup control.

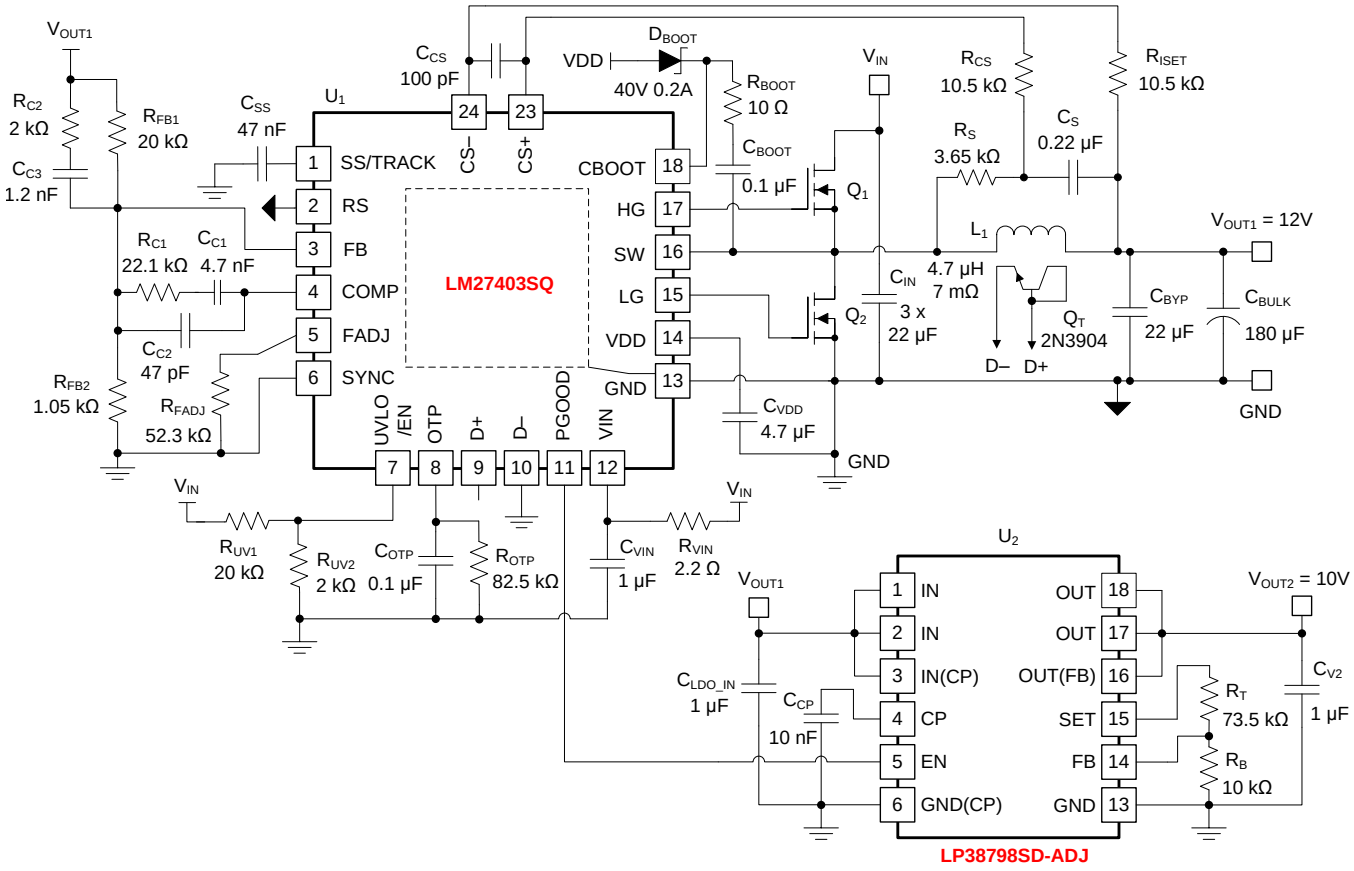


Figure 45. Application Circuit 4 with V_{IN} = 13 V to 20 V ($V_{IN(nom)}$ = 18 V), V_{OUT1} = 12 V, $I_{OUT1(max)}$ = 10 A, F_{SW} = 280 kHz, V_{OUT2} = 10 V, $I_{OUT2(max)}$ = 0.8 A

Table 10. List of Materials for Design 4

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	3	22 µF, 25 V, X5R, 1210 ceramic	Taiyo Yuden	TMK325BJ226MM-T
C_{BYP}	1	22 µF, 16 V, X7R, 1210 ceramic	Taiyo Yuden	EMK325B7226MM-T
C_{BULK}	1	180 µF, 16 V, 22 mΩ, 3.3 Arms, C6, OSCON	Panasonic	16SVPF180M
L_1	1	4.7 µH, 15 A, 7 mΩ, flat wire high current	Wurth	7443551470
Q_1	1	30 V, high-side MOSFET	Texas Instruments	CSD17309Q3
Q_2	1	30 V, low-side MOSFET	Infineon	BSC011NE3LS
U_2	1	Ultra-Low Noise, High PSRR LDO for RF/Analog Circuits, 4-mm x 4-mm WSON-12	Texas Instruments	LP38798SD-ADJ

(1) These design examples are provided to showcase the LM27403 in numerous applications. Depending on the impedance of the input bus, an electrolytic capacitor may be required at the input to ensure stability.
(2) Kam, K. W. et. al., "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis," IEEE International Symposium on Electromagnetic Compatibility, 2008.

DESIGN 5 - High Power Density Implementation from 3.3-V or 5-V Supply Rail

The schematic diagram of a 250-kHz, 25-A regulator is given in Figure 46. A high power density, ultra-high efficiency solution is possible using two paralleled TI CSD87353Q5D NexFET™ Power Block modules (dual MOSFETs in a SON 5-mm x 6-mm package) and low-DCR ferrite inductor. The design occupies 25 mm x 15 mm on a two-sided PCB. Knowing the cumulative resistance of the inductor DCR and Power Block MOSFET SW clip (approximately 0.8 mΩ at 25°C), resistor R_{ISET} positions the current limit setpoint at 30A. VDD is tied to VIN to maximize the gate drive voltage for the MOSFETs. Capacitor C_{DLY} defines a 3-ms startup delay based on the current sourced from the UVLO/EN pin.

The powertrain components are listed in Table 11, and the filter components are available from multiple vendors. The T_{GR} pin of the Power Block MOSFET serves as a kelvin connection to the high-side MOSFET's source and represents the return path for the high-side gate drive. Along with bootstrap capacitor, C_{BOOT}, T_{GR} is connected to the LM27403's SW pin.

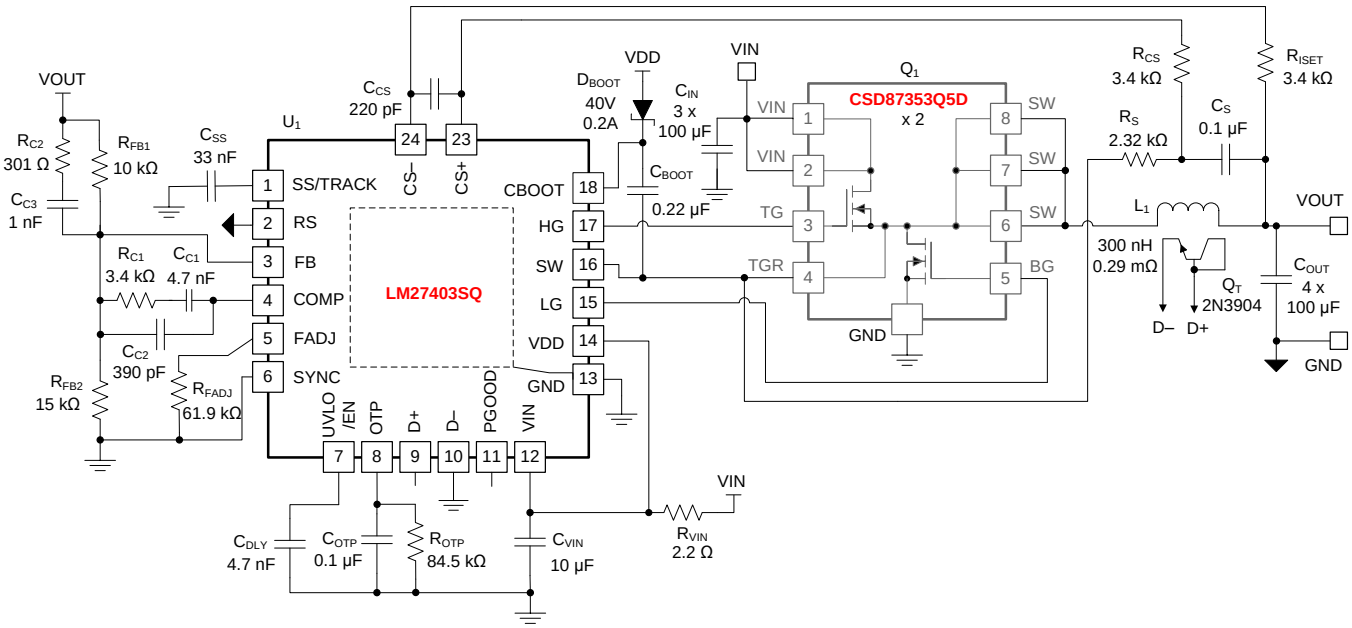


Figure 46. Application Circuit 5 with V_{IN} = 3.3 V to 5.5 V, V_{OUT} = 1 V, $I_{OUT(max)}$ = 25 A, F_{SW} = 250 kHz

Table 11. List of Materials for Design 5

REFERENCE DESIGNATOR	QTY	SPECIFICATION		MANUFACTURER	PART NUMBER
C_{IN}	3	100 µF, 6.3 V, X5R, 1210 ceramic		Kemet	C1210C107M9PACTU
				TDK	C3225X5R0J107M
				Murata	GRM32ER60J107ME20K
C_{OUT}	4	100 µF, 6.3 V, X5R, 1206 ceramic		Taiyo Yuden	JMK316BJ107ML-T
				Murarta	GRM31CR60J107ME39L
				TDK	C3216X5R0J107M
				Kemet	C1206C107M9PACTU
L_1	1	300 nH, ferrite	35 A, 0.29 mΩ ±8%	Coiltronics	FP1107R1-R30-R
		330 nH, ferrite	46 A, 0.32 mΩ ±7%	Wurth Electronik	744301033
Q_1	2	30 V Power Block Q5D MOSFET Module, 5 mm x 6 mm		Texas Instruments	CSD87353Q5D

PC BOARD LAYOUT CONSIDERATIONS

Proper PCB design and layout is important in a high current, fast switching circuit (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the LM27403. The main switching loop of the power stage is denoted by #1 in Figure 47. The topological architecture of a buck converter means that particularly high di/dt current will flow in loop #1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. For loop #2 however, the di/dt through inductor L_1 and capacitor C_{OUT} is naturally limited by the inductor. Keeping the area of loop #2 small is not nearly as important as that of loop #1. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by #3 and #4, respectively, in Figure 47.

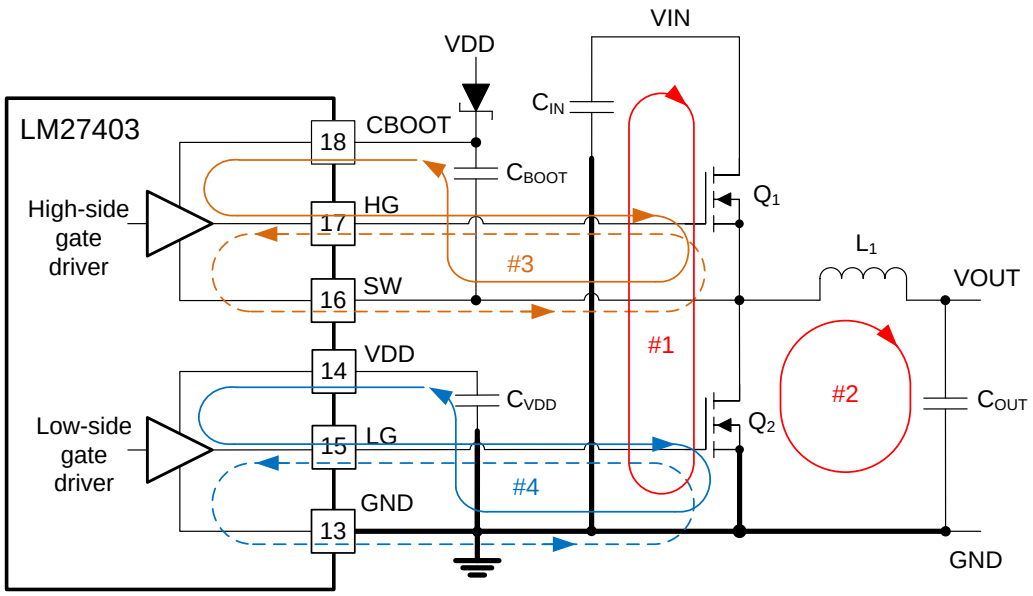


Figure 47. DC-DC Regulator Ground System with Power Stage and Gate Drive Circuit Switching Loops

POWER STAGE LAYOUT

1. Input capacitor(s), output capacitor(s) and MOSFETs are the constituent components in the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). Leveraging any system-level airflow, the benefits of convective heat transfer are thus maximized. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC/DC converter has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and parasitic loop inductance and optimize switching performance.
   - Loop #1: The most important loop to minimize the area of is the path from the input capacitor(s) through the high- and low-side MOSFETs, and back to the capacitor(s) through the ground connection. Connect the input capacitor(s) negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor(s) positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop #1 of Figure 47.
   - Loop #2. The second important loop is the path from the low-side MOSFET through inductor and output capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative terminal of the output capacitor(s) at ground as close as possible. Refer to loop #2 of Figure 47.
3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, should be short and wide. However, the SW connection is a source of injected EMI and thus should not be too large.
4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.

5. The SW pin connects to the switch node of the power conversion stage, and it acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop #1 in Figure 47 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (>100 MHz) ringing on the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the printed circuit board layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components.

GATE DRIVE LAYOUT

The LM27403 high- and low-side gate drivers incorporate short propagation delays, adaptive deadtime control and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray/parasitic loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop #3: high-side MOSFET, Q_1. During the high-side MOSFET turn on, high current flows from the boot capacitor through the gate driver and high-side MOSFET, and back to negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from gate of the high-side MOSFET through the gate driver and SW, and back to source of the high-side MOSFET through the SW trace. Refer to loop #3 of Figure 47.
- Loop #4: low-side MOSFET, Q_2. During the low-side MOSFET turn on, high current flows from VDD decoupling capacitor through the gate driver and low-side MOSFET, and back to negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and GND, and back to source of the low-side MOSFET through ground. Refer to loop #4 of Figure 47.

The following circuit layout guidelines are strongly recommended when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HG and LG, to the respective gate of the high-side or low-side MOSFET should be as short as possible to reduce series parasitic inductance. Use 0.65 mm (25 mils) or wider traces. Use via(s), if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HG and SW gate traces as a differential pair from the LM27403 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VDD and CBOOT pins through their respective capacitors as these provide the high instantaneous current to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BOOT}, close to the LM27403's CBOOT and SW pins to minimize the area of loop #3 associated with the high-side driver. Similarly, locate the VDD capacitor, C_{VDD}, close to the LM27403's VDD and GND pins to minimize the area of loop #4 associated with the low-side driver.
3. Placing a 2-Ω to 10-Ω BOOT resistor in series with the BOOT capacitor, as shown in Figure 45, slows down the high-side MOSFET turn-on transition, serving to reduce the voltage ringing and peak amplitude at the SW node at the expense of increased MOSFET turn-on power loss.

CONTROLLER LAYOUT

Components related to the analog and feedback signals, current limit setting and temperature sense are considered in the following:

1. In general, separate power and signal traces, and use a ground plane to provide noise shielding.
2. Place all sensitive analog traces and components such as COMP, FB, RS, FADJ, OTP, D+ and SS/TRACK away from high-voltage switching nodes such as SW, HG, LG or CBOOT avoid coupling. Use internal layer(s) as ground plane(s). Pay particular attention to shielding the feedback (FB) trace from power traces and components.
3. The upper feedback resistor can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side. Connect RS to the ground return point at the load device or the

general ground plane/layer. These connections can be used for the purpose of remote sensing across the downstream load; however, care must be taken to minimize the routing trace to prevent noise injection into the sense lines. The remote sense lines (SENSE+ and SENSE- in Figure 38) are typically routed as a differential pair, either side-by-side on the same PCB layer or overlapping each other on adjacent layers.

4. Connect the OCP setting resistor from CS+ pin to VOUT and make the connections as close as possible to the LM27403. The trace from the CS+ pin to the resistor should avoid coupling to a high-voltage switching node. Similar precautions apply if a resistor is tied to the CS– pin (as shown in Figure 33).
5. Minimize the current loop from the VDD and VIN pins through their respective decoupling capacitors to the GND pin. In other words, locate these capacitors as close as possible to the LM27403.
6. The layout of the temperature sense circuit is particularly important. Locate the thermal diode (2N3904-type BJT) adjacent the inductor on the same side of the PCB if possible. Close thermal coupling to the inductor is imperative to match the inductor winding's temperature coefficient.
   (a) Keep D+ and D– traces close together to minimize pickup. 10-mil trace width with 10-mil spacing is adequate. Keep D+ and D– traces short and surround with ground guard copper in especially noisy environments.
   (b) Route traces away from inductor, particularly with ferrite cores that have wide airgap and large fringing/leakage flux fields. Run a separate trace from the 2N3904 emitter back to LM27403 D– pin. Then connect D– to GND at the LM27403's DAP. Do not use a ground plane that carries high currents to make a return connection.

THERMAL DESIGN AND LAYOUT

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by:

- average gate drive current requirements of the power MOSFETs;
- switching frequency;
- operating input voltage (affecting LDO voltage drop and hence its power dissipation);
- thermal characteristics of the package and operating environment.

In order for a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM27403 controller is available in a small 4-mm x 4-mm WQFN-24 (RSW) PowerPAD™ package to cover a range of application requirements. The thermal metrics of this package are summarized in the Thermal Information section of this datasheet. For detailed information regarding the thermal information table, please refer to *IC Package Thermal Metrics* application report.

The WQFN-24 package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the LM27403's package is not directly connected to any leads of the package, it is thermally connected to the substrate of the device (ground). This allows a significant improvement in heat-sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The LM27403's exposed pad is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value. Wide traces of the copper tying in the LM27403's no-connect pins (pins 19–23) and connection to this thermal land helps to dissipate heat.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The high-side MOSFET's drain pad is normally connected to a VIN plane for heat-sinking. The low-side MOSFET's drain pad is tied to the SW plane, but the SW plane area is purposely kept relatively small to mitigate EMI concerns.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM27403SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L27403	Samples
LM27403SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L27403	Samples
LM27403SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L27403	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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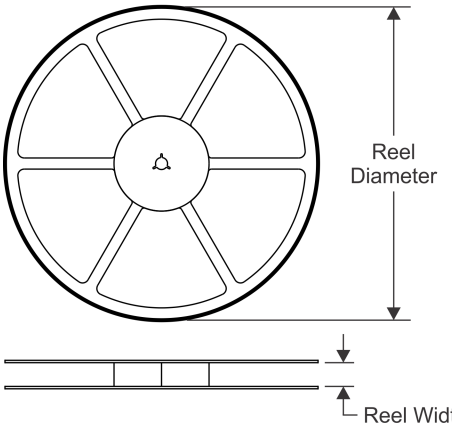
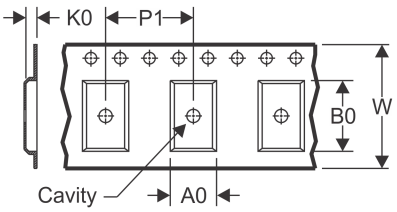
REEL DIMENSIONS

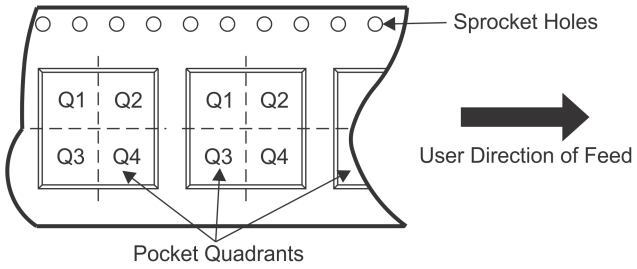


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

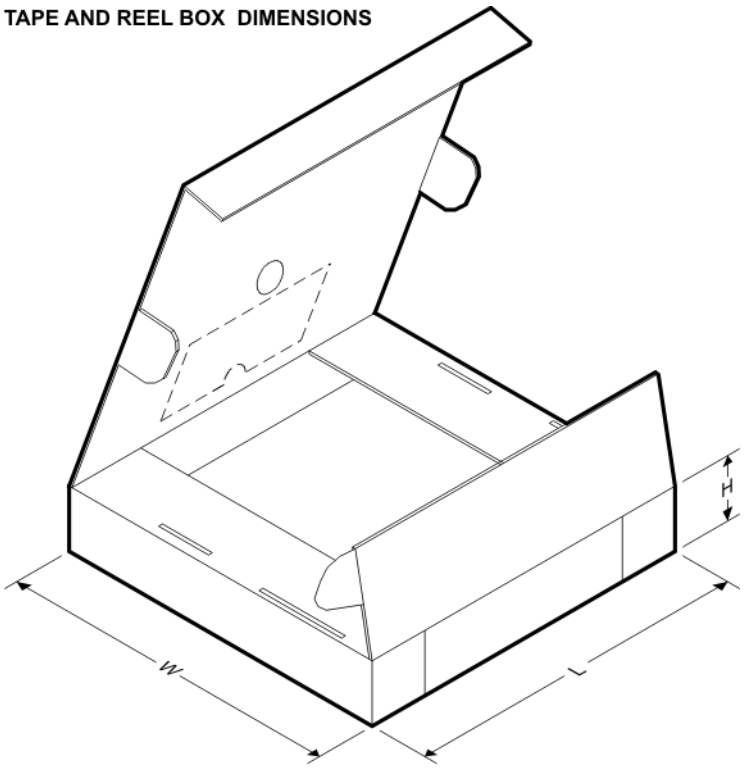
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27403SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM27403SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM27403SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

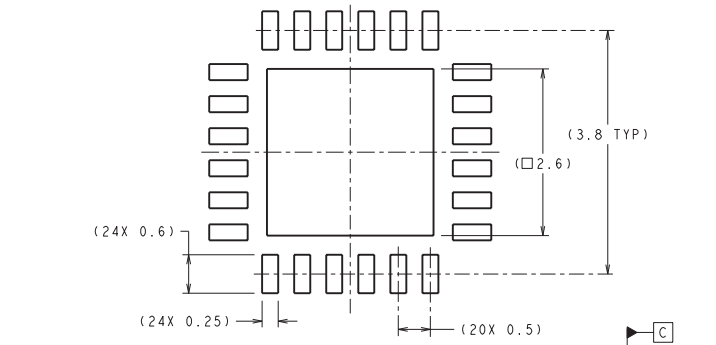
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

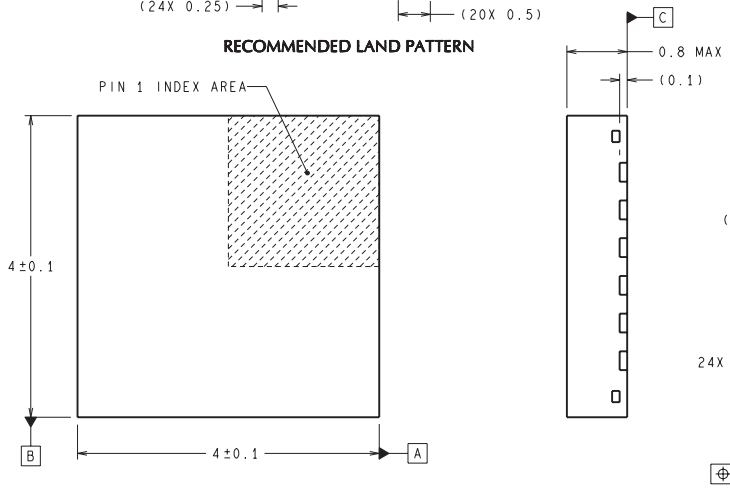
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27403SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LM27403SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LM27403SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

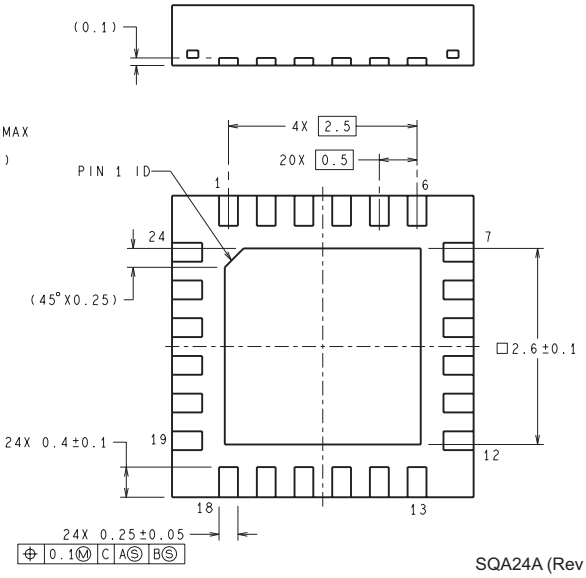
RTW0024A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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