5A Adjustable Frequency Synchronous Buck Regulator

Check for Samples: LM21305

FEATURES

- **High Efficiency Switcher Core With Integrated Low R_{DSon} Power MOSFETs**
- **Resistor Programmable Switching Frequency With Frequency Synchronization**
- **Internal Soft-Start With Monotonic and Pre-Biased Startup**
- **Low Shutdown Quiescent Current**
- **Precision Enable With Hysteresis**
- **PGOOD Indicator Function**
- **Input Under-Voltage Lock-Out (UVLO)**
- **Output Over-Voltage Protection (OVP)**
- **High-Bandwidth Load Transient Response With Peak Current-Mode Control**
- **Cycle-by-Cycle Current Limiting**
- **Thermal Shutdown**

KEY SPECIFICATIONS

- **3V to 18V Single-Rail Input Voltage**
- **0.598V Feedback Voltage Reference**
- **300 kHz to 1.5 MHz Switching Frequency**
- **WQFN-28 Package (5 x 5 x 0.8 mm, 0.5 mm Pitch)**

APPLICATIONS

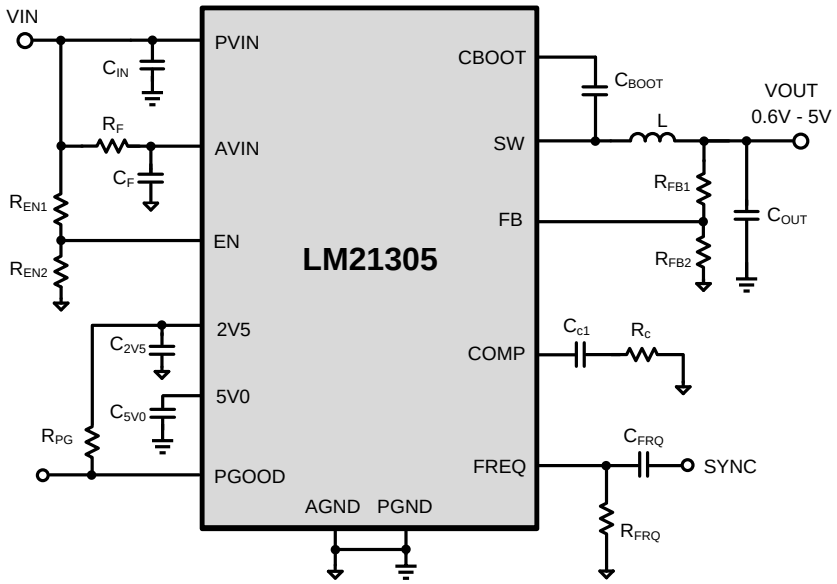
- **POL Regulation From 3.3V, 5V, and 12V Supply Rails**
- **High Efficiency Supply for DSPs, FPGAs, ASICs and Processors**
- **Broadband, Networking and Optical Communications Infrastructure**

DESCRIPTION

The LM21305 is a full-featured 5A synchronous buck POL regulator optimized for solution size, flexibilty, and high conversion efficiency. High power density LM21305 designs are achieved via monolithic integration of the high-side and low-side power MOSFETs, high switching frequency, current-mode control, and optimized thermal design. The efficiency of the LM21305 is elevated at light loads with diode emulation mode operation and at heavy loads by optimal design of the MOSFET gate drivers to minimize switch dead-times and body-diode conduction losses.

The LM21305 accepts a wide input voltage range of 3V to 18V, facilitating interface to all intermediate bus voltages, including 3.3V, 5V and 12V rails. An output voltage as low as 0.598V is supported with excellent setpoint accuracy and low ripple and RMS noise.

Typical Application Circuit



DESCRIPTION (CONTINUED)

The LM21305 offers flexible system configuration with programmable switching frequency from 300 kHz to 1.5 MHz using one resistor or via external clock synchronization. On-chip bias supply sub-regulators alleviate the need for external bias power and simplify PCB layout. The device also offers internal soft-start to limit inrush current, pre-biased and monotonic startup capability, cycle-by-cycle current limiting, and thermal shutdown. Peak current-mode control with a high-gain error amplifier maintains stability throughout the entire input voltage and load current ranges and enables excellent line and load transient response.

Offered in a thermally enhanced WQFN-28 package, the LM21305 features internal output over-voltage and over-current protection circuits for increased system reliability. A precision enable pin and integrated input UVLO allow the turn-on of the device to be tightly controlled and sequenced. An integrated open-drain power good indicator provides power rail sequencing capability and fault indication.

Connection Diagram

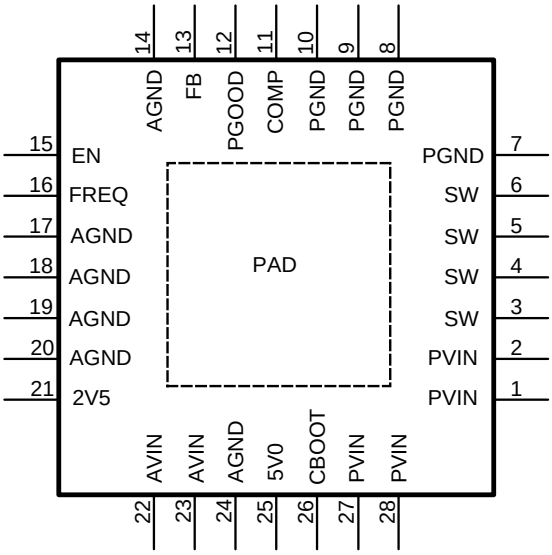


Figure 1. WQFN-28 Package, Exposed Pad
Package Number RSG

PIN DESCRIPTIONS

Number	Name	Type(1)	Pad Description
1,2,27,28	PVIN	P	Input voltage to the power switches inside the device.
3,4,5,6	SW	P	Switch node output of the power switches. Voltage swings from PVIN to GND on this pin. SW also delivers current to the external inductor.
7,8,9,10	PGND	G	Power ground for the internal power switches.
11	COMP	A	Compensation pin to connect to external compensation network.
12	PGOOD	OD	Power Good, open-drain output. If high, indicates the output voltage is regulated within tolerance. A pull-up resistor (10 kΩ to 100 kΩ) is recommended for most applications.
13	FB	A	Voltage Feedback pin. This pin can be connected to the output voltage directly or through a resistor divider to set the output voltage range.
14,17,18,19,20,24	AGND	G	Analog ground for the internal bias circuitry.
15	EN	I	Precision enable pin. An external divider can be used to set the device turn-on threshold. If not used, the EN pin should be connected to AVIN.
16	FREQ	A	Frequency setting pin. This pin can be connected to a resistor to AGND to set the internal oscillator frequency. It also can be connected to an external clock source via a capacitor such that the switching frequency of the device is synchronized to the external clock.
21	2V5	P	2.5V output of internal regulator. This pin is only for bypassing the internal LDO. Loading this pin is not recommended.
22,23	AVIN	P	Analog power input. AVIN powers the internal 2.5V and 5.0V LDOs which provide bias current and internal driver power. It can be connected to PVIN through a low pass RC filter or can be supplied by a separate rail.
25	5V0	P	5.0V output of internal regulator. This pin is only for bypassing the internal LDO. Loading this pin is not recommended.
26	CBOOT	A	Bootstrap pin to drive the high-side switch. A bootstrap capacitor should be connected between this pin and the SW pin.
PAD	PAD		Exposed pad at the back of the device. The PAD should be connected to PGND, but cannot be used as primary ground connection. Use multiple vias under the PAD for optimal thermal performance.

(1) P: Power, A: Analog, I: Digital Input, OD: Open Drain, G: Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

PVIN, AVIN, SW, EN, PGOOD to AGND	−0.3V to +20V
CBOOT to AGND	−0.3V to +25V
CBOOT to SW	−0.3V to +5.5V
5V0, FB, COMP, FREQ to AGND	−0.3V to +6V
2V5 to AGND	−0.3V to +3V
AGND to PGND	−0.3V to +0.3V
Junction Temperature ($T_{J\text{-}MAX}$)	150°C
Storage Temperature Range	−65°C to 150°C
Maximum Continuous Power Dissipation $P_{D\text{-}MAX}$ (3)	Internally limited
Maximum Lead Temperature Lead-free Compatible (4)	260°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The amount of Absolute Maximum power dissipation allowed in the device depends on the ambient temperature and can be calculated using the formula $P = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high power dissipation exists, special care must be paid to thermal dissipation issues in PC board design. Internal thermal shutdown circuitry protects the device from permanent damage.
(4) For detailed soldering specifications, please refer to Application Note AN-1187: Leadless Leadframe Package (LLP) (literature number SNOA401).

ESD Ratings

All pins, Human Body Model (1)	±2kV

(1) The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin (MIL-STD-883 3015.7).

Operating Ratings

PVIN to PGND, AGND	3V to 18V
AVIN to PGND, AGND	3V to 18V
Junction Temperature	−40°C to 125°C
Ambient Temperature (1)	−40°C to 85°C
Junction-to-Ambient Thermal Resistance θ_{JA} (2)	32.4°C/W

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

(2) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer standard JEDEC thermal test board or 4LJEDEC, 4" x 3" in size, with a 3 by 3 array of thermal vias. The board has two embedded copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one, is 2 oz./1oz./1oz./2 oz. For WQFN, thermal vias are placed between the die attach pad in the 1st. copper layer and 2nd. copper layer. Detailed description of the board can be found in JESD 51-7. Ambient temperature in the simulation is 22°C, still air. Power dissipation is 1W. The value of θ_{JA} of this product can vary significantly depending on PCB material, layout, and environmental conditions. In applications with high power dissipation (e.g. high V_{OUT}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to Application Note AN-1187: Leadless Leadframe Package (LLP) (literature number SNOA401).

Electrical Characteristics (1) (2)(2)

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to +125°C). Unless otherwise specified, $V_{IN} = V_{PVIN} = V_{AVIN}$ = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A.

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
$V_{FB-default}$	Feedback pin factory-default voltage		**0.588**	0.598	**0.608**	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.1A to 5A		0.02		%/A
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{PVIN} = 3V to 18V		0.01		%/V
R_{DSonHS}	High-Side Switch On Resistance	I_{DS} = 5A		44		mΩ
R_{DSonLS}	Low-Side Switch On Resistance	I_{DS} = 5A		22		mΩ
I_{CL-HS}	High-Side Switch Current Limit	High-side FET	**5.9**	7.0	**7.87**	A
I_{CL-LS}	Low-Side Switch Current Limit	Low-side FET (3)	**5.9**	8.0	**10.2**	A
$I_{NEG-CL-LS}$	Low-Side Switch Negative Current Limit	Low-side FET	**-7.0**	-4.1	**-1.64**	A
I_{SD}	Quiescent Current, disabled	$V_{AVIN} = V_{PVIN}$ = 5V		0.1	**2**	µA
		$V_{AVIN} = V_{PVIN}$ = 18V		1	**4.1**	
I_Q	Quiescent Current, enabled, not switching	$V_{AVIN} = V_{PVIN}$ = 18V		9	**9.7**	mA
I_{FB}	Feedback Pin Input Bias Current	V_{FB} = 0.598V		1		nA
G_M	Error Amplifier Transconductance			2400		µS
A_{VOL}	Error Amplifier Voltage Gain			65		dB
V_{IH-OVP}	OVP Tripping Threshold	Output voltage rising threshold, percentage of V_{OUT}	**103.5**	109.5	**115**	%
$V_{HYST-OVP}$	OVP Hysteresis Window	Percentage of V_{OUT}		-4.3		%

(1) All limits are specified by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) Capacitors: low ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.

(3) The low-side switch current limit is ensured to be higher than the high-side current limit.

Electrical Characteristics [1] [2][2] (continued)

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to +125°C). Unless otherwise specified, V_{IN} = V_{PVIN} = V_{AVIN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A.

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
$V_{UVLO-HI-AVIN}$	AVIN UVLO Rising Threshold		**2.84**	2.93	**2.987**	V
$V_{UVLO-LO-AVIN}$	AVIN UVLO Falling Threshold		**2.66**	2.73	**2.83**	V
$V_{UVLO-HYS-AVIN}$	AVIN UVLO Hysteresis Window			195		mV
V_{5V0}	Internal LDO1 Output Voltage	Measured at 5V0 pin, 1kΩ load		4.88		V
$C_{OUT-CAP-5V0}$	Recommended Capacitance connected to 5V0 pin	Ceramic capacitor		1		µF
$I_{SHORT-5V0}$	Short Circuit Current of 5V0 pin			31		mA
V_{2V5}	Internal LDO2 output voltage	Measured at 2V5 pin, 1kΩ load		2.47		V
$C_{OUT-CAP-2V5}$	Recommended Capacitance connected to 2V5 pin	Ceramic capacitor		100		nF
$I_{SHORT-2V5}$	Short Circuit Current of 2V5 pin			47		mA
$VF_{CBOOT-D}$	CBOOT Diode Forward Voltage	Measured between 5V0 and CBOOT @ 10 mA		0.76		V
I_{CBOOT}	CBOOT Leakage Current	V_{CBOOT} = 5.5V, not switching		0.65		µA
$T_{STARTUP-DELAY}$	Startup Time from EN high to the beginning of internal soft-start			160		µs
SS	Internal Soft-Start	10% to 90% V_{FB}	**1.41**	2.7	**4.15**	ms
OSCILLATOR						
$F_{OSC-NOM}$	Oscillator Frequency, nominal measured at SW pin	R_{FRQ} = 61.9 kΩ, 0.025%	**695**	750	**795**	kHz
$F_{OSC-MAX}$	Maximum Oscillator Frequency measured at SW pin	R_{FRQ} = 28.4 kΩ		1500		kHz
$F_{OSC-MIN}$	Minimum Oscillator Frequency measured at SW pin	R_{FRQ} = 167.5 kΩ		300		kHz
$T_{OFF-MIN}$	Minimum Off-Time measured at SW pin	f_S = 1.5 MHz, V_{IN} = 3.3V, V_{FB} = 1V, voltage divider ratio = 3.3		50		ns
T_{ON-MIN}	Minimum On-Time measured at SW pin	f_S = 1.5 MHz, voltage divider ratio = 1		70		ns
LOGIC						
V_{IH-EN}	EN Pin Rising Threshold		**1.1**	1.2	**1.3**	V
$V_{HYST-EN}$	EN Pin Hysteresis Window		**130**	200	**302**	mV
I_{EN-IN}	EN Pin Input Current	V_{EN} = 12V		18	**23**	µA
$V_{IH-UV-PGOOD}$	PGOOD UV Rising Threshold	Percentage of V_{OUT}	**87.5**	93	**97.5**	%
$V_{HYST-UV-PGOOD}$	PGOOD UV Hysteresis Threshold	Percentage of V_{OUT}		-4.2		%
$I_{OL-\ PGOOD}$	PGOOD Sink Current	V_{OL} = 0.2V		3		mA
$I_{OH-\ PGOOD}$	PGOOD Leakage Current	V_{OH} = 18V			**460**	nA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown [4]			160		°C
T_{SD-HYS}	Thermal Shutdown Hysteresis [4]			10		°C

(4) Specified by design.

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 12V, V_{OUT} = 3.3V, f_S = 500 kHz, T_A = 25°C, L = 3.3 µH, C_{OUT} = 100 µF ceramic.

Efficiency with PVIN = AVIN = 5V, f_S = 300 kHz

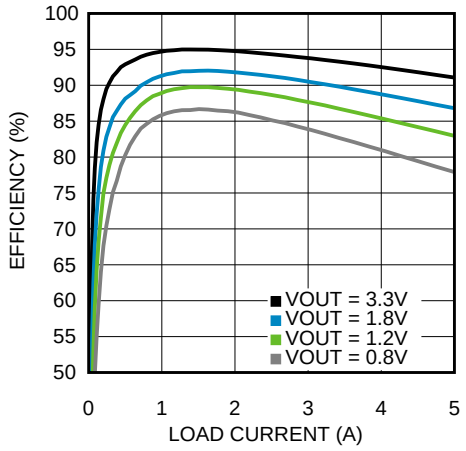


Figure 2.

Efficiency with PVIN = AVIN = 12V, f_S = 300 kHz

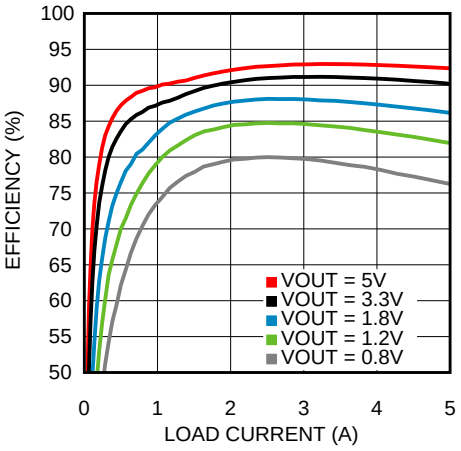


Figure 3.

Efficiency with PVIN = AVIN = 5V, f_S = 500 kHz

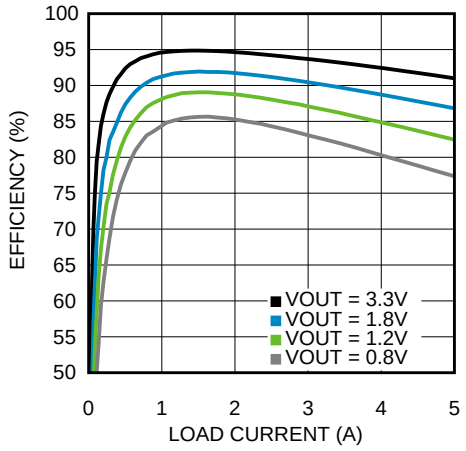


Figure 4.

Efficiency with PVIN = AVIN = 12V, f_S = 500 kHz

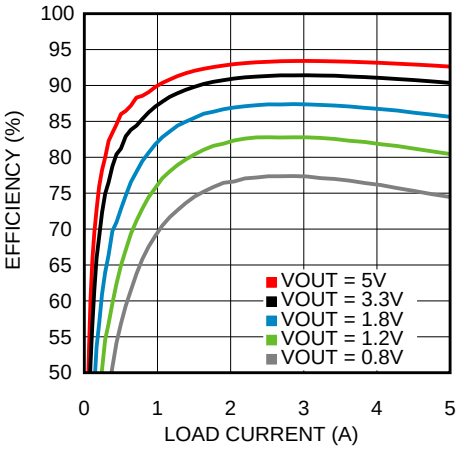


Figure 5.

Efficiency with PVIN = AVIN = 5V, f_S = 1 MHz

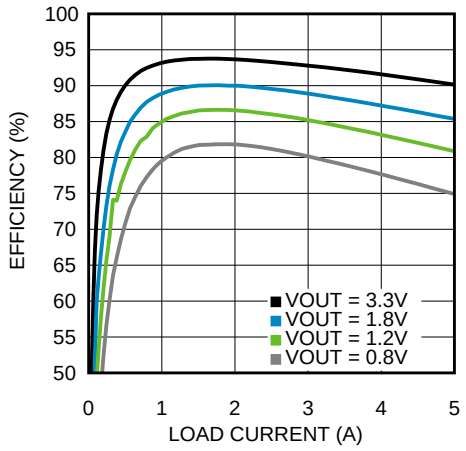


Figure 6.

Efficiency with PVIN = AVIN = 12V, f_S = 1 MHz

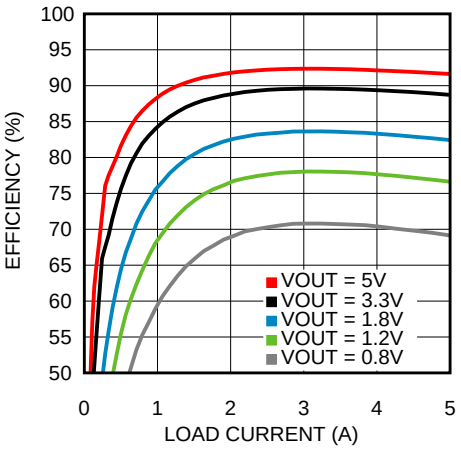


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 12V, V_{OUT} = 3.3V, f_S = 500 kHz, T_A = 25°C, L = 3.3 µH, C_{OUT} = 100 µF ceramic.

Load Regulation (%)

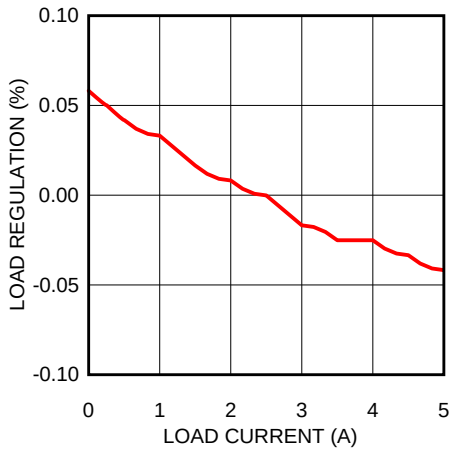


Figure 8.

Line Regulation (%)

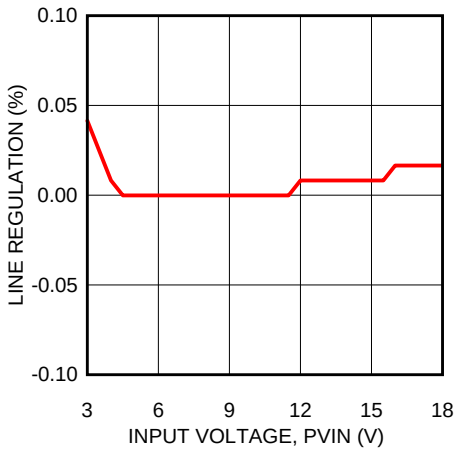


Figure 9.

V_{OUT} Regulation (%) vs. Temperature

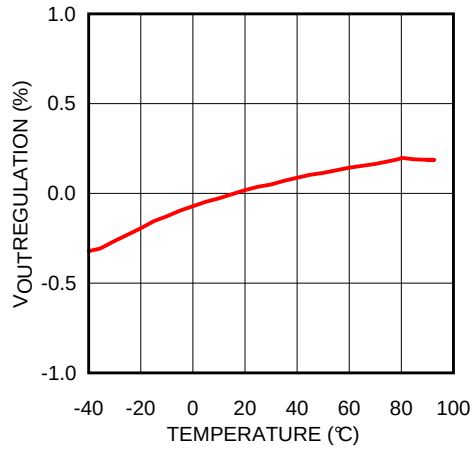


Figure 10.

Quiescent Current, Not Switching

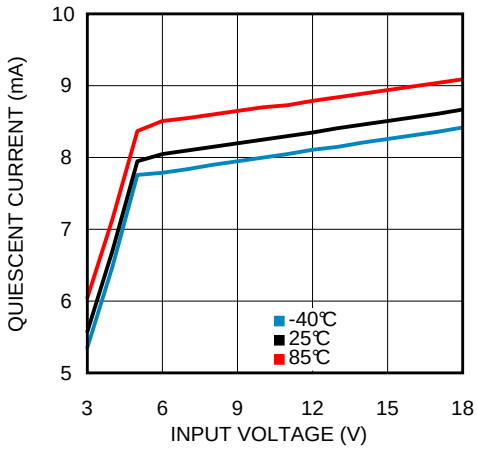


Figure 11.

High-Side and Low-Side MOSFET R_{DSon} vs. Temperature

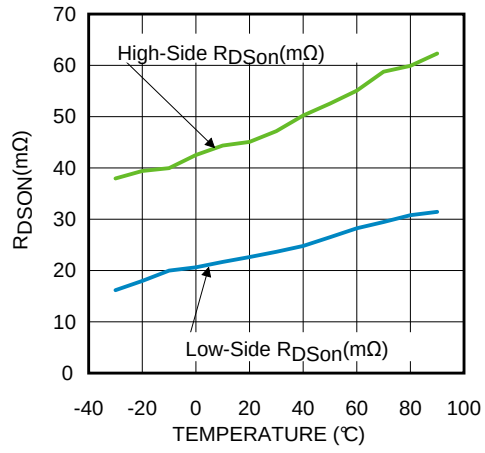


Figure 12.

Switching Frequency vs. R_{FRQ}

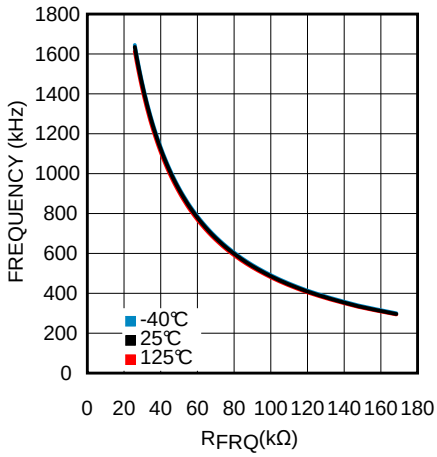


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 12V, V_{OUT} = 3.3V, f_S = 500 kHz, T_A = 25°C, L = 3.3 µH, C_{OUT} = 100 µF ceramic.

Soft-Start, No Load

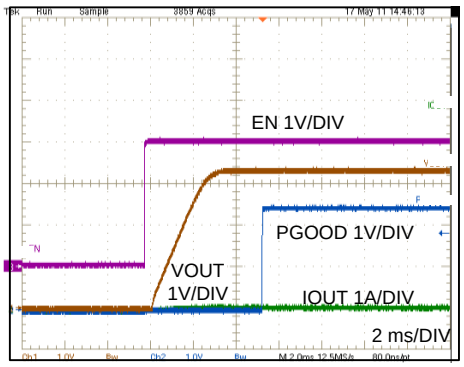


Figure 14.

Soft-Start with Resistive Load

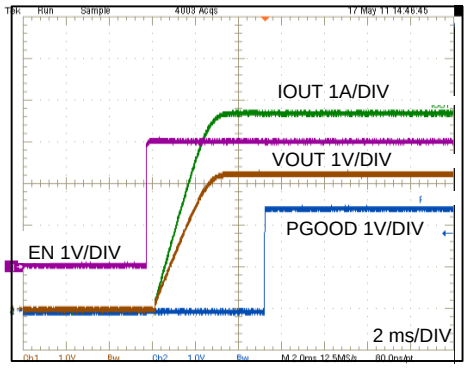


Figure 15.

Soft-Start with 2V Pre-Bias Voltage, No Load

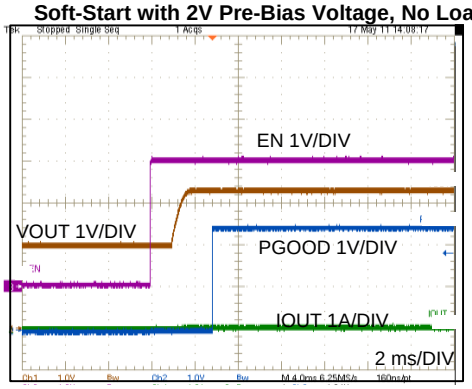


Figure 16.

Switching Waveform with 0A Load (DCM Operation)

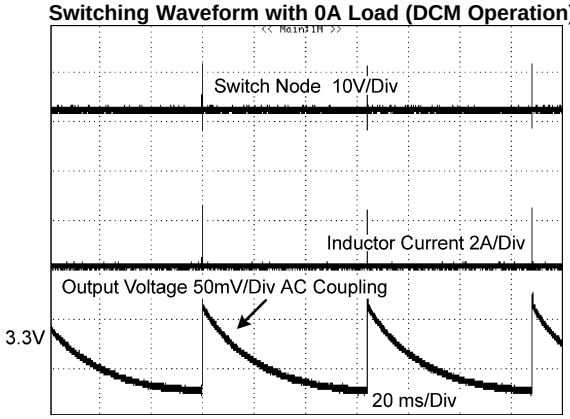


Figure 17.

Switching Waveform with 5A Load

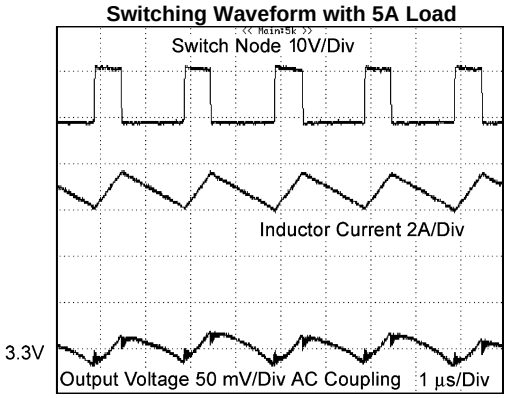


Figure 18.

Load Transient 0.1A to 5A

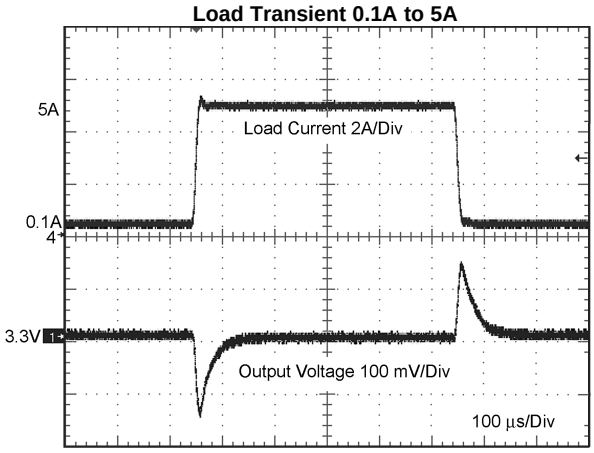
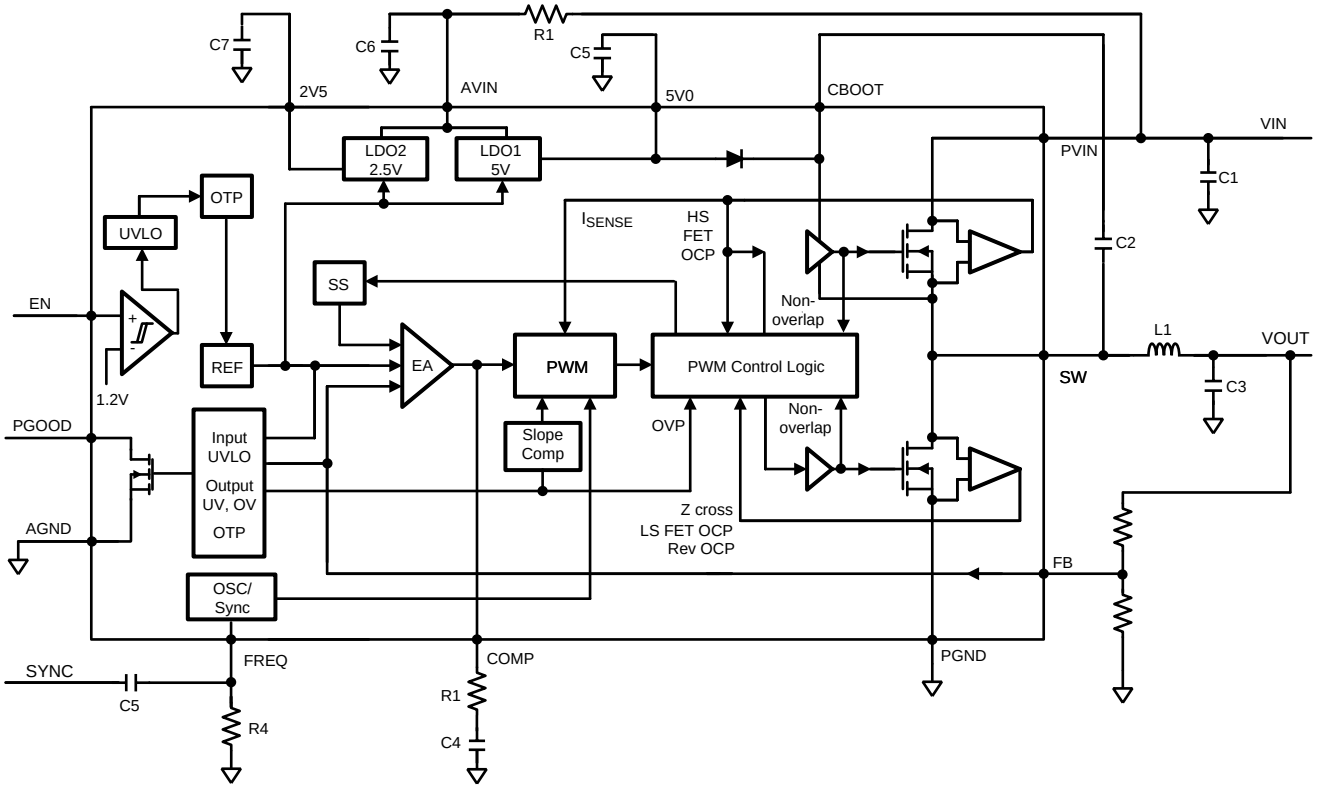


Figure 19.

BLOCK DIAGRAM



OPERATION DESCRIPTION

The LM21305 employs peak current-mode control. The 0.598V reference is compared to the feedback signal at the error amplifier (EA). The PWM modulator block compares the on-time current sense information with the summation of the EA output (control voltage) and slope compensation. The PWM modulator outputs on/off signals to the high-side and low-side MOSFET drivers. Adaptive dead-time control is applied to the PWM output such that shoot through current is avoided. The drivers then amplify the PWM signals to control the integrated high-side and low-side MOSFETs.

SWITCHING REGULATOR

The LM21305 employs a buck type (step-down) converter architecture. It utilizes many advanced features to achieve excellent voltage regulation and efficiency. This easy-to-use regulator features two integrated switches and is capable of supplying up to 5A of continuous output current. The regulator utilizes peak current-mode control with slope compensation scaled with switching frequency to optimize stability and transient response over the entire output voltage and switching frequency ranges. Peak current-mode control also provides inherent line feed-forward, cycle-by-cycle current limiting, and easy loop compensation. The switching frequency can be adjusted between 300 kHz and 1.5 MHz. The device can operate with a small external L-C filter and still provide very low output voltage ripple. The precision internal voltage reference allows the output to be set as low as 0.598V. Using an external compensation circuit, the regulator bandwidth can be selected based on the switching frequency to provide fast load transient response. The switching regulator is specially designed for high efficiency operation throughout the load range. Synchronous rectification yields high efficiency for low voltage and heavy load current situations, while discontinuous conduction and diode emulation modes enable high efficiency conversion at lighter load currents. Fault protection features include: high-side and low-side switch current limiting, negative current limiting on the low-side switch, over-voltage protection and thermal shutdown. The device is available in the WQFN-28 package featuring an exposed pad to aid thermal dissipation. The LM21305 can be used in numerous applications to efficiently step-down from a wide range of input rails: 3V to 18V.

PEAK CURRENT-MODE CONTROL

In most applications, the peak current-mode control architecture used in the LM21305 only requires two external components to achieve a stable design. External compensation allows the user to set the crossover frequency and phase margin, thus optimizing the transient performance of the device. For duty cycles above 50%, all peak current-mode control buck converters require the addition of an artificial ramp to avoid sub-harmonic oscillation. This linear ramp is commonly referred to as slope compensation. The amount of slope compensation in the LM21305 will automatically change depending on the switching frequency: the higher the switching frequency, the larger the slope compensation. This allows smaller inductors to be used with high switching frequency to increase the power density.

SWITCHING FREQUENCY SETTING AND SYNCHRONIZATION

The LM21305 switching regulator can operate at a frequency ranging from 300 kHz to 1.5 MHz. The switching frequency can be set / controlled in two ways. One is by selecting the external resistor attached to the FREQ pin to set the internal oscillator frequency which controls the switching frequency. An external 100 pF capacitor, C_{FRQ}, should also be connected from the FREQ pin to analog ground as a noise filter, as shown in Figure 20.

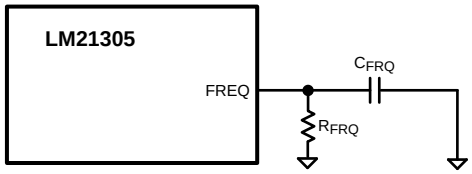


Figure 20. Switching Frequency set by External Resistor

The other way is to synchronize the switching frequency to an external clock in the range of 300 kHz to 1.5 MHz. The external clock should be applied through a 100 pF coupling capacitor, C_{FRQ}, as shown in Figure 21.

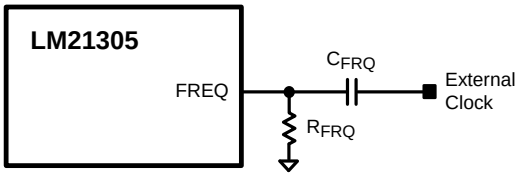


Figure 21. Switching Frequency Synchronized to External Clock

The recommendations for the external clock include peak-to-peak voltage above 1.5V, duty cycle between 20% and 80%, and the edge rate faster than 100 ns. Circuits that use an external clock should still have a resistor connected from the FREQ pin to analog ground. The external clock frequency should be within -10% to +50% of the frequency set by R_{FRQ}. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails and the coupling capacitor on the clock side is grounded or pulled to logic high.

If the external clock fails low, timeout circuits will prevent the high-side FET from staying off for longer than 1.5 times the switching period (switching period $T_s = 1/f_s$). At the end of this timeout period, the regulator will begin to switch at the frequency set by R_{FRQ}.

If the external clock fails high, timeout circuits will again prevent the high-side FET from staying off longer than 1.5 times the switching period. After this timeout period, the internal oscillator takes over and switches at a fixed 1 MHz until the voltage on the FREQ pin has decayed to approximately 0.6V. This decay follows the time constant of C_{FRQ} and R_{FRQ}, and once it is complete the regulator will switch at the frequency set by R_{FRQ}.

LIGHT-LOAD OPERATION

The LM21305 offers increased efficiency at light loads by allowing Discontinuous Conduction Mode (DCM). When the load current is less than half of the inductor ripple current, the device will enter DCM thus preventing negative inductor current. The current at which this occurs is the critical conduction boundary and can be calculated according to the following equation:

$$I_{BOUNDARY} = \frac{V_{OUT}(1 - D)}{2Lf_S} \quad (1)$$

where D is the duty cycle of the high-side switch, equal to the high-side switch on-time divided by the switching period. For more details, please refer to the CALCULATING THE DUTY CYCLE section in the Design Guide provided later. Several diagrams are shown in Figure 22 illustrating continuous conduction mode (CCM), Discontinuous Conduction Mode (DCM), and the boundary condition. It can be seen that in DCM, whenever the inductor current reaches zero, the SW node will become high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the effective parasitic capacitance at the switch node. At very light loads, usually below 100 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

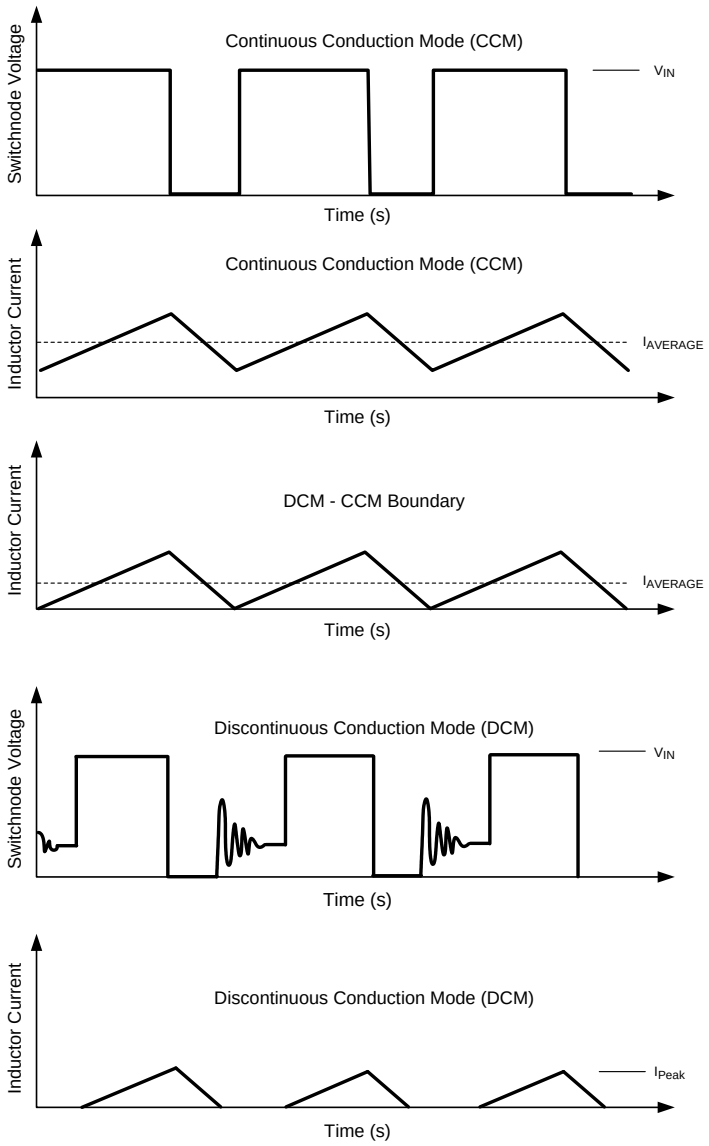


Figure 22. CCM And DCM Operation

PRECISION ENABLE

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.2V (typical). The EN pin has 200 mV (typical) of hysteresis and will disable the output when the enable voltage falls below 1.0V (typical). If the EN pin is not used, it should be pulled up to AVIN via a 10 kΩ to 100 kΩ resistor. Since the enable pin has a precise turn-on threshold, it can be used along with an external resistor divider network from an external voltage to configure the device to turn on at a precise voltage. The precision enable circuitry will remain active even when the device is disabled. The turn-on voltage with a divider can be found by

$$V_{EN\text{-}EXT} = 1.2 \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \quad (2)$$

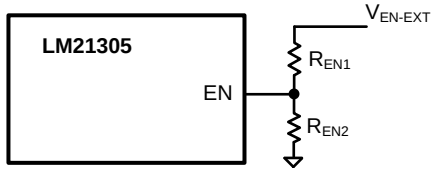


Figure 23. Use External Resistor To Set The EN Threshold

DEVICE ENABLE, SOFT-START AND PRE-BIAS STARTUP CAPABILITY

The device output can be turned off by removing AVIN or pulling the EN pin low. To enable the device, EN pin must be high with the presence of AVIN and PVIN. Once enabled, the device engages the internal soft-start. The soft-start feature allows the regulator output to gradually reach the steady state operating point, thus reducing stresses on the input supply and controlling startup current. Soft-start begins at the rising edge of EN with AVIN above UVLO level. It is important to make sure PVIN is high when soft-start begins. The LM21305 allows AVIN to be higher than PVIN, or PVIN higher than AVIN, as long as both of them are within their operating voltage ranges.

Soft-start of the LM21305 is controlled internally. It typically takes 2.7 ms to finish the soft-start sequence. PGOOD will be high after soft-start is finished.

The LM21305 is in a pre-biased state when the device initiates startup with an output voltage greater than zero. This often occurs in many multi-rail applications such as when powering an FPGA, ASIC, or DSP. In these applications, the output can be pre-biased through parasitic conduction paths from one supply rail to another. Even though the LM21305 is a synchronous converter, it will not pull the output low when a pre-bias condition exists. During startup, the LM21305 will be in diode emulation mode with low-side switch turned off when zero crossing of the inductor current is detected.

PEAK CURRENT PROTECTION AND NEGATIVE CURRENT LIMITING

The LM21305 switching regulator detects the peak inductor current and limits it to a value of 7A typical. To determine the average current from the peak current, the inductor size, input and output voltage, and switching frequency must be known. The average current limit can be found by :

$$I_{ave(limit)} = I_{peak(limit)} - \frac{V_{OUT}(1-D)}{2Lf_s} \quad (3)$$

When the peak inductor current sensed from the high-side switch reaches the current limit threshold, an over-current event is triggered and the internal high-side FET turns off and the low-side FET turns on allowing the inductor current to ramp down until the next switching cycle. When the high-side over-current condition persists, the output voltage will be reduced by the reduced high-side switch on-time.

In cases such as output short circuit or when high-side switch minimum on-time conditions are reached, the high-side switch current limiting may not be sufficient to limit the inductor current. The LM21305 features an additional low-side switch current limit to prevent the inductor current from running away. The low-side switch current limit is set higher than the high-side current limit, 8A typical. When the low-side switch current is higher than the limit level, PWM pulses will be skipped until the low-side over-current event is not detected during the entire low-side switch conduction time. Normal PWM switching subsequently occurs when the condition is removed. High-side and low-side current protections result in a current limit that does not aggressively foldback for brief over-current

events, while at the same time providing frequency and voltage foldback protection during hard short circuit conditions. The low-side switch also has negative current limit (-4.1A typical) for secondary protection, and this can engage duing response to over-voltage events. If the negative current limit is triggered, the low-side switch will be turned off. The negative current will be forced to go through the high-side switch body diode and will quickly reduce.

PGOOD AND OVER- / UNDER-VOLTAGE HANDLING

PGOOD should be pulled high with an external resistor (10kΩ to 100kΩ recommended). When the FB voltage is typically within -7% to +9.5% of the reference voltage, PGOOD will be high. Otherwise, an internal open-drain pull-down device will pull PGOOD low. PGOOD should be tied to ground if the function is not required.

The LM21305 has built-in under- and over-voltage comparators that control the power switches. Whenever there is an excursion in output voltage above the set OVP threshold, the device will terminate the present on-pulse, turn on the low-side FET, and pull PGOOD low. The low-side FET will remain on until either the FB voltage falls back into regulation or the inductor current zero-cross is detected which in turn tri-states the FETs. If the output reaches the UVP threshold, the part will continue switching and PGOOD will be asserted and go low. To avoid false tripping during transient glitches, PGOOD has 16 µs of built-in deglitch time to both rising and falling edges. OVP is disabled during soft-start to prevent false triggering.

UVLO

The LM21305 has a built-in under-voltage lockout (UVLO) protection circuit that prevents the device from switching until the AVIN voltage reaches 2.93V (typical). The UVLO threshold has typically 190 mV of hysteresis that keeps the device from responding to power-on glitches during startup.

INTERNAL REGULATORS

The LM21305 contains two internal low dropout (LDO) regulators to produce internal driving and bias voltage rails from AVIN. One LDO produces 5V to power the internal MOSFET drivers, the other produces 2.5V to power the internal bias circuitry. Both the 5V0 or 2V5 LDOs should be bypassed to analog ground (AGND) with an external ceramic capacitor (1 µF and 0.1 µF recommended, respectively). Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation within the LDOs. Connecting a load to the 5V0 or 2V5 pins is not recommended since it will degrade their driving capability to internal circuitry, further pushing the LDOs into their RMS current ratings and increasing power dissipation and die temperature.

The LM21305 allows AVIN to be as low as 3V which makes the voltage at the 5V0 LDO lower than 5V. Low supply voltage at the MOSFET drivers can increase on-time resistance of the high-side and low-side MOSFETs and reduce efficiency of the regulator. When AVIN is between 3V and 5.5V, the best practice is to short the 5V0 pin to AVIN to avoid the voltage drop on the internal LDO. However, the device can be damaged if the 5V0 pin is pulled to a voltage higher than 5.5V. For efficiency considerations, it is best to use AVIN = 5V if possible. When AVIN is above 5V, reduced efficiency can be observed at light load due to the power loss of the LDOs. When AVIN is close to 3V, increased MOSFET on-state resistance can reduce efficiency at high load current levels.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, T_{ON-MIN}, is the smallest duration of time that the high-side MOSFET can be on. This time is typically 70 ns in the LM21305. In CCM operation, the minimum on-time limit imposes a minimum duty cycle of

$$D_{MIN} = f_S \times T_{ON-MIN} \quad (4)$$

For a given output voltage, minimum on-time imposes limits on the switching regulator when operating simultaneously at high input voltage and high switching frequency. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. With a given switching frequency and desired output voltage, the maximum allowed PVIN can be approximated by

$$V_{PVIN\text{-}max} = \frac{V_{OUT}}{f_S} \times \frac{1}{T_{ON\text{-}MIN}} \quad (5)$$

Similarly, if the PVIN input rail is fixed, the maximum switching frequency without imposing minimum on-time can be found by:

$$f_{s\text{-}max} = \frac{V_{OUT}}{V_{PVIN\text{-}max}} \times \frac{1}{T_{ON\text{-}MIN}} \quad (6)$$

In rare cases where steady-state operation at minimum duty cycle is unavoidable, the regulator will automatically skip cycles to keep V_{OUT} regulated, similar to light-load DCM operation.

THERMAL PROTECTION

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the LM21305 tri-states the power MOSFETs and resets soft-start. After the junction temperature cools to approximately 150°C, the LM21305 starts up using the normal startup routine. This feature is provided to prevent catastrophic failures from due to device overheating.

DESIGN GUIDE

This section walks the designer through the steps necessary to select the external components to build a fully functional efficient step-down power supply. As with any DC-DC converter, numerous tradeoffs are possible to optimize the design for efficiency, size, and performance. These will be taken into account and highlighted throughout this discussion. To facilitate component selection discussions, the typical application circuit shown below may be used as a reference. Unless otherwise indicated, all formulae assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance, Volts (V) for voltages and Hertz (Hz) for frequencies.

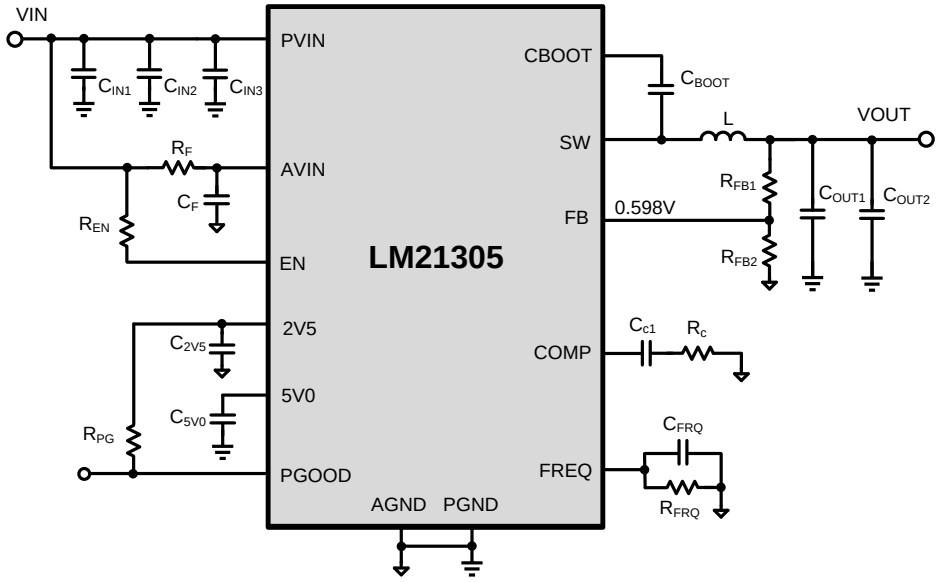


Figure 24. LM21305 Typical Application Circuit

SETTING THE OUTPUT VOLTAGE

The FB pin of the LM21305 can be connected to V_{OUT} directly or through a resistor divider. With an external resistor divider, the output voltage can be scaled up from the 0.598V feedback voltage. Figure 25 shows the connection of the divider and the FB pin.

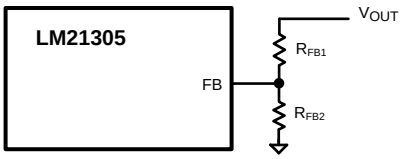


Figure 25. Setting the Output Voltage by Resistor Divider

The output voltage can be found by:

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) 0.598V \quad (7)$$

For example, if the desired output voltage is 1.2V, R_{FB1} = 10 kΩ and R_{FB2} = 10 kΩ can be used.

CALCULATING THE DUTY CYCLE

The first equation to calculate for any buck converter is duty cycle. In an ideal (no loss) buck converter, the duty cycle can be found by:

$$D_{ideal} = \left(\frac{V_{OUT}}{V_{PVIN}}\right) \quad (8)$$

In applications with low output voltage (<1.2V) and high load current (> 3A), the losses should not be ignored when calculation the duty cycle. Considering the effect of conduction losses associated with the MOSFETs and inductor, the duty cycle can be approximated by:

$$D = \frac{V_{OUT} + I_{OUT} \times \left(R_{DSon_{LS}} + R_{dcr}\right)}{V_{IN} + I_{OUT} \times \left(R_{DSon_{LS}} - R_{DSon_{HS}}\right)} \quad (9)$$

R_{DSonHS} and R_{DSonLS} are the on-state parasitic resistances of the high-side and low-side MOSFETs, respectively. R_{dcr} is the equivalent DC resistance of the inductor used in the output filter. Other parasitics, such as PCB trace resistance, can be included if desired. I_{OUT} is the load current. It is also equal to the average inductor current. The duty cycle will increase slightly with increase of load current.

SUPPLY POWER AND INPUT CAPACITORS

PVIN is the supply voltage for the switcher power stage. It is the input source that delivers the output power to the load. The input capacitors on the PVIN rail supply the large AC switching current drawn by the switching action of the internal power MOSFETs. The input current of a buck converter is discontinuous and the ripple current supplied by the input capacitor can be quite large. The input capacitor must be rated to handle this current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT}\,(V_{PVIN} - V_{OUT})}}{V_{PVIN}} \text{ (A)} \quad (10)$$

The power dissipation of the input capacitor is given by: $P_{D\_CIN} = I^2_{RMS\_CIN}\, R_{ESR\_CIN}$(W) where R_{ESR_CIN} is the ESR of the input capacitor. This equation has a maximum at PVIN = $2V_{OUT}$, where $I_{RMS\_CIN} \cong I_{OUT}/2$ and D ≅ 50%. This simple worst-case condition is commonly used for design purposes because even significant deviations from the worst case duty cycle operating point do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load current changes. A 1 µF ceramic bypass capacitor is also recommended directly adjacent the IC between the PVIN and PGND pins.

Please refer to Figure 33 and the PCB LAYOUT CONSIDERATIONS section provided later in this document.

AVIN FILTER

An RC filter should be added to prevent any switching noise on PVIN from interfering with the internal analog circuitry connected to AVIN. These can be seen on the schematic as components R_F and C_F. There is a practical limit to the size of resistor R_F as the AVIN pin will draw a short 60 mA burst of current during startup and if R_F is too large the resulting voltage drop can trigger the UVLO comparator. A recommended 1 µF capacitor coupled with a 1Ω resistor provides approximately 10 dB of attenuation at 500 kHz switching frequency.

SWITCHING FREQUENCY SELECTION

The LM21305 supports a wide range of switching frequencies: 300 kHz to 1.5 MHz. The choice of switching frequency is usually a compromise between conversion efficiency and the size of the circuit. Lower switching frequency implies reduced switching losses (including gate charge losses, switch transition losses, etc.) and usually results in higher overall efficiency. But higher switching frequency allows use of smaller LC output filters and hence a more compact design. Lower inductance also helps transient response (higher large-signal slew

rate of inductor current) and reduces the DCR losses. The optimal switching frequency is usually a tradeoff in a given application and thus needs to be determined on a case-by-case basis. It is related to the input voltage, output voltage, most common load current level, external component choices, and circuit size requirements. The choice of switching frequency may also be limited if an operating condition triggers T_{ON-MIN} or $T_{OFF-MIN}$. Please refer to the aforementioned MINIMUM ON-TIME CONSIDERATIONS section.

The following equation or Figure 26 can be used to calculate the resistance to obtain a desired frequency of operation:

$$f_s\,[kHz] = 31000 \times R_{FRQ}^{-0.9}[k\Omega] \quad (11)$$

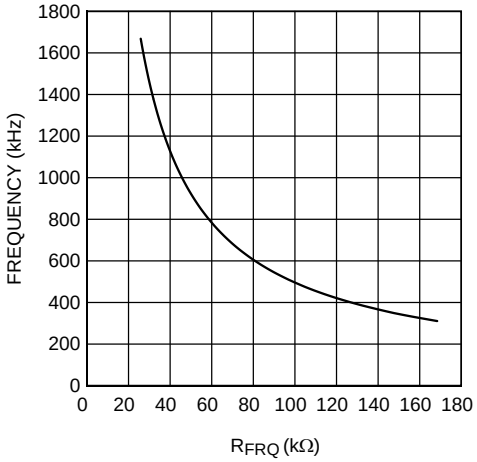


Figure 26. External Resistor Selection to Set the Switching Frequency

INDUCTOR

A general recommendation for the filter inductor in an LM21305 application is to keep a peak-to-peak ripple current between 20% and 40% of the maximum DC load current of 5A. It also should have a sufficiently high saturation current rating and a DCR as low as possible.

The peak-to-peak current ripple can be calculated by:

$$\Delta i_{Lp\text{-}p} = \frac{(1 - D) \times V_{OUT}}{f_S \times L} \approx \frac{V_{OUT}}{f_S \times L}\left(1 - \frac{V_{OUT}}{V_{PVIN}}\right) \quad (12)$$

It is recommended to choose L such that:

$$\frac{(1 - D) \times V_{OUT}}{f_S \times 0.4 \times I_{L(MAX)}} \le L \le \frac{(1 - D) \times V_{OUT}}{f_S \times 0.2 \times I_{L(MAX)}} \quad (13)$$

The inductor should be rated to handle the maximum load current plus the ripple current:

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta i_{L(MAX)}/2 \quad (14)$$

An inductor with saturation current higher than the over-current protection limit is a safe choice. In general, it is desirable to have lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor ripple current such that over-current protection at the full load could be falsely triggered. It also generates more conduction loss, since the RMS inductor current is slightly higher relative to that with lower current ripple at the same DC current. Larger inductor ripple current also implies larger output voltage ripple with the same output capacitors. With peak current-mode control, it is recommended to not have too small of an inductor current ripple so that the peak current comparator has enough signal-to-noise ratio.

Once the inductance is determined, the type of inductor must be selected. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the saturation current is exceeded. The 'hard' saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

OUTPUT CAPACITOR

The device is designed to be used with a wide variety of LC filters. It is generally desirable to use as little output capacitance as possible to keep cost and size down. The output capacitor(s), C_{OUT}, should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during a load current transient.

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors: $\Delta V_{OUT\text{-}ESR} = \Delta i_{Lp\text{-}p} * ESR$.

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\text{-}C} = \frac{\Delta i_{Lp\text{-}p}}{8 f_S C_{OUT}} \tag{15}$$

Figure 27 shows an illustration of the two ripple components. Since the two ripple components are not in phase, the actual peak-to-peak ripple is smaller than the sum of the two peaks:

$$\Delta V_{OUT} < \Delta i_{Lp\text{-}p} \times \left(\frac{1}{8 f_S C_{OUT}} + ESR \right) \tag{16}$$

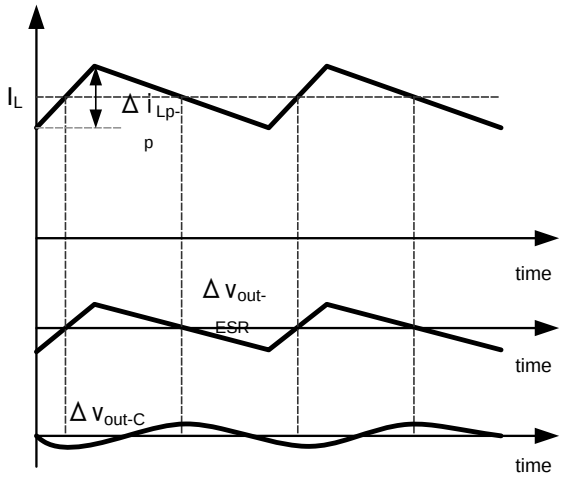


Figure 27. Two Components of V_{OUT} Ripple

Output capacitance is usually limited by system transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a fast large load transient occurs, output capacitors provide the required charge before the inductor current can slew to the appropriate level. The initial output voltage step is equal to the load current step multiplied by the ESR. V_{OUT} continues to droop until the control loop response increases or decreases the inductor current to supply the load. To maintain a small over- or undershoot during a transient, small ESR and large capacitance are desired. But these also come with the penalty of higher cost and size. Thus, the motivation is to seek a fast control loop response to reduce the output voltage deviation.

One or more ceramic capacitors are generally recommended because they have very low ESR and remain capacitive up to high frequencies. The capacitor dielectric should be X5R or X7R to maintain proper tolerance. Other types of capacitors also can be used, particularly if large bulk capacitance is needed (such as tantalum, POSCAP and OSCON). Such electrolytic capacitors have lower ESR zero {1/(2π*ESR* *C_{OUT}} frequency than ceramic capacitors. The lower ESR zero frequency can influence the control loop, particularly if it occurs close to the desired crossover frequency. If high switching frequency and high loop crossover frequency are warranted, an all ceramic design can be more appropriate.

EFFICIENCY CONSIDERATIONS

The efficiency of a switching regulator is defined as the output power divided by the input power times 100%. Efficiency also can be found by:

$$\eta = 1 - \frac{\text{Total Power Loss}}{\text{Input Power}} \quad (17)$$

It is often useful to analyze individual losses to determine what is limiting the efficiency and what change would produce the most improvement. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LM21305-based converters: 1) conduction losses; 2) switching and gate drive losses; 3) bias losses. Conduction losses are the I^2R losses in parasitic resistances including on-state resistances of the internal switches R_{DSon}, equivalent inductor DC resistance R_{dcr}, and PC board trace resistances R_{trace}. The conduction loss can be approximated by:

$$W_{cond\text{-}loss} = I_{OUT}^2 \times \left(D \times R_{DSon_{HS}} + (1-D) \times R_{DSon_{LS}} + R_{dcr} + R_{trace}\right) \quad (18)$$

The total conduction loss can be reduced by reducing these parasitic resistances. For example, the LM21305 is designed to have low R_{DSon} internal MOSFET switches. The inductor DCR should be small. The traces that conduct the current should be wide, thick and as short as possible. Obviously, the conduction losses affect the efficiency more at heavier load.

Switching losses include all the losses generated by the switching action of the two power MOSFETs. Each time the switch node swings from low to high or vice versa, charges are applied or removed from the parasitic capacitance from the SW node to GND. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge moves from 5V0 to ground. Furthermore, each time a power MOSFET is turned on or off, a transition loss is generated related to the overlap of voltage and current. MOSFET parasitic diodes generate reverse recovery loss and dead time conduction loss. RMS currents through the input and output capacitor ESR also generate loss. All of these losses should be evaluated and carefully considered to design a high efficiency switching power converter. Since these losses only occur during 'switching', reducing the switching frequency always helps to reduce the switching loss and the resultant improvement in efficiency is more pronounced at lighter load.

Since the 5V0 rail is an LDO output from AVIN, the current drawn from AVIN is the same as i_{Drive} and the associated power loss is V_{AVIN} * i_{Drive}. The other portion of AVIN power loss is the bias current through the 2V5 rail which equals V_{AVIN}* i_{bias}. Powering AVIN from a 5V system rail provides an optimal tradeoff between bias power loss and switching loss.

LOAD CURRENT DERATING WHEH DUTY CYCLE EXCEEDS 50%

The LM21305 is optimized for lower duty cycle operation, e.g. high input to output voltage ratio. The high-side MOSFET is designed to be half the size of the low-side MOSFET thus optimizing the relative levels of switching loss in the high-side switch and the conduction loss in the low-side switch. The continuous current rating of the low-side switch is the maximum load current of 5A, while the high-side MOSFET is rated at 2.5A. If the LM21305 is operating with duty cycles higher than 50%, the maximum output current should be derated.

$$I_{OUT\text{-}max} = 5 \times \min\left[(1.5-D), 1\right] \quad (19)$$

Derating of maximum load current when D > 50% is also illustrated in Figure 28.

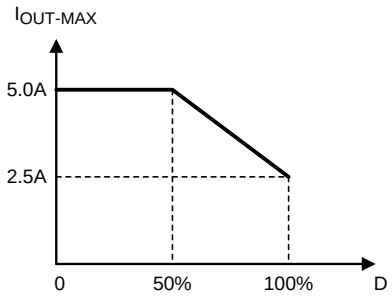


Figure 28. LM21305 Maximum Load Current Derating when D > 50%

CONTROL LOOP COMPENSATION

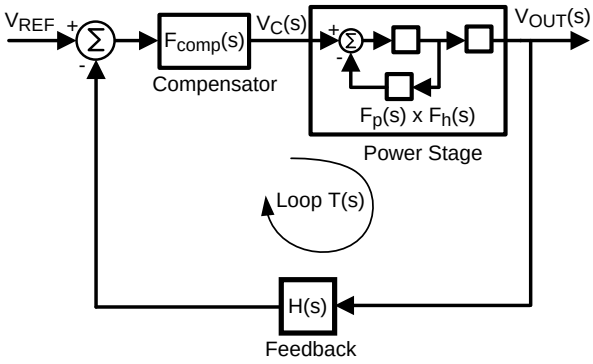


Figure 29. Control Block Diagram of a Peak Current-Mode Controlled Buck Converter

This section will not provide a rigorous analysis of current-mode control, but rather a simplified yet relatively accurate method to determine the control loop compensation network. The LM21305 employs a peak current-mode controller and therefore the control loop block diagram representation involves two feedback loops (see Figure 29). The inner feedback loop derives its feedback from the sensed inductor current while the outer loop monitors the output voltage. The LM21305 compensation components from COMP to AGND are shown in Figure 30. The purpose of the compensator block is to stabilize the control loop and achieve high performance in terms of the load transient response, audio susceptibility and output impedance. The LM21305 will typically require only a single resistor R_c and capacitor C_{c1} for compensation. However, depending on the location of the power stage ESR zero, a second (small) capacitor, C_{c2}, may be required to create a high frequency pole.

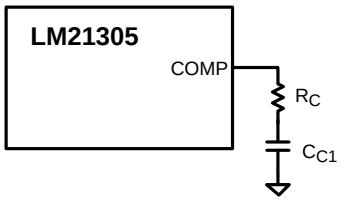


Figure 30. LM21305 Compensation Network

The overall loop transfer function is a product of the power stage transfer function, internal amplifier gains and the feedback network transfer function and can be expressed by:

$$T(s) = Gain_0 F_p(s) F_h(s) F_{comp}(s)$$

where $Gain_0$ includes all the DC gains in the loop, $F_p(s)$ represents the power stage pole and zero (including the inner current loop), $F_h(s)$ represents the sampling effect in such a current-mode converter and $F_{comp}(s)$ is the transfer function of the external compensator. Figure 31 shows an asymptotic approximation plot of the loop gain.

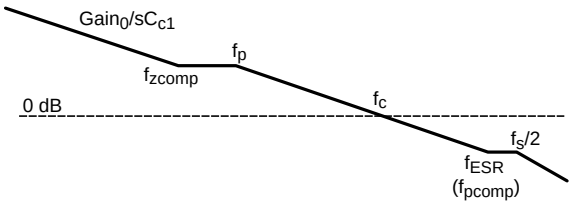


Figure 31. LM21305 Loop Gain Asymptotic Approximation

The loop gain determines both static and dynamic performance of the converter. The power stage response is fixed by the selection of the power components and the compensator is therefore designed around the power stage response to achieve the desired loop response. The goal is to design a control loop characteristic with high crossover frequency (or loop bandwidth) and adequate gain and phase margins under all operation conditions.

COMPENSATION COMPONENTS SELECTION

To select the compensation components, a desired crossover frequency needs to be selected. It is recommended to select f_c equal to or lower than 1/6 of the switching frequency. The effect of $F_h(s)$ can be ignored to simplify the design. The capacitor ESR zero is also assumed to be at least 3 times higher than f_c. The compensation resistor can be found by:

$$R_c = \frac{1}{Gain_0} \times \frac{f_c}{f_p} = \frac{V_{OUT}}{V_{FB}} \times 302 \times f_c \times C_{OUT} \quad (20)$$

C_{c1} does not affect the crossover frequency f_c, but it sets the compensator zero f_{Zcomp} and affects the phase margin of the loop. For a fast design, C_{c1} = 4.7 nF gives adequate performance in most LM21305 applications. Larger C_{c1} capacitance gives higher phase margin but at the expense of longer transient response settling time. It is recommended to set the compensation zero no higher than $f_c/3$ to ensure enough phase margin, implying:

$$C_{c1} \geq \frac{3}{2\pi R_c f_c} \quad (21)$$

PLOTTING THE LOOP GAIN

To include the effect of $F_h(s)$ and the ESR zero, the complete loop gain can be plotted using a software tool such as MATLAB, Mathcad, or Excel. The components in the loop gain can be determined as follows. The DC gain of the power stage can be found by:

$$Gain_0 = \frac{V_{FB}}{V_{OUT}} \times \frac{R_{OUT}}{1 + \frac{R_{OUT}}{f_s L}(m_c D' - 0.5)} \times 0.021 \quad (22)$$

where f_s is the switching frequency,

$$m_c = 1 + \frac{4 \times f_S \times L}{V_{IN} - V_{OUT}} \quad (23)$$

and D' = 1 − D.

Minimum R_{OUT} should be used in the calculation $R_{OUT} = V_{OUT}/I_{OUT}$. $F_p(s)$ can be expressed by:

$$F_p(s) = \frac{1 + s C_{OUT} ESR}{1 + \frac{s}{2\pi f_p}} \quad (24)$$

where the power stage pole considering the slope compensation effect is:

$$f_p = \frac{1}{2\pi C_{OUT}} \left(\frac{1}{R_{OUT}} + \frac{1}{f_s L} (m_c D' - 0.5) \right) \quad (25)$$

The high frequency behavior $F_h(s)$ can be expressed by:

$$F_h(s) = \frac{1}{1 + \frac{s}{w_n Q_p} + \frac{s^2}{w_n^2}} \quad (26)$$

where:

$$w_n = \pi f_s \text{ and } Q_p = \frac{1}{\pi(m_c D' - 0.5)} \quad (27)$$

The compensator network transfer function is:

$$F_{comp}(s) = R_c + \frac{1}{sC_{c1}} \quad (28)$$

With the above equations, the loop gain T(s) can be plotted and more accurate loop performance metrics (crossover frequency and phase margin) can be determined.

HIGH FREQUENCY CONSIDERATIONS

$F_h(s)$ represents the additional magnitude and phase drop around $f_s/2$ caused by the switching behavior of the current-mode converter. $F_h(s)$ contains a pair of double poles with quality factor Q_p at half of the switching frequency. It is a good idea to check that Q_p is between 0.15 and 2, ideally around 0.6. If Q_p is too high, the resonant peaking at $f_s/2$ could become severe and coincide with subharmonic oscillations in the duty cycle and inductor current. If Q_p is too low, the two complex poles split, the converter begins to act like a voltage-mode controlled converter and the compensation scheme used above should be changed.

$F_p(s)$ also contains the ESR zero of the output capacitors:

$$f_{ESR} = \frac{1}{2\pi C_{OUT} ESR} \quad (29)$$

In a typical ceramic capacitor design, f_{ESR} is at least three times higher than the desired crossover frequency f_c. If f_{ESR} is lower than $f_s/2$, an additional capacitor C_{c2} can be added between the COMP pin and AGND to give a high-frequency pole:

$$C_{c2} = \frac{1}{2\pi R_c f_{ESR}} \quad (30)$$

C_{c2} should be much smaller than C_{c1} to avoid affecting the compensation zero.

BOOTSTRAP CAPACITOR

A capacitor is needed between the CBOOT pin and the SW node to supply the gate drive charge when the high-side switch is turning ON. The capacitor should be large enough to supply the charge without significant voltage drop. A 0.1 µF ceramic bootstrap capacitor is recommended in LM21305 applications.

5V0 AND 2V5 CAPACITORS

5V0 and 2V5 pins are internal LDO outputs. As previously mentioned, the two LDOs are used for internal circuits only and should not be substantially loaded. Output capacitors are needed to stabilize the LDOs. Ceramic capacitors within a specified range should be used to meet stability requirements. The dielectric should be X5R, X7R, or better and rated for the required operating temperature range. Use the following table to choose a suitable LDO output capacitor:

	Output Voltage NOMINAL	Capacitance (Recommended Value and Minimum Voltage Rating)
5V0	4.88V	1 µF ± 20% 16V
2V5	2.47V	0.1 µF ± 20% 10V

PCB LAYOUT CONSIDERATIONS

PC board layout is an important and critical part of any DC-DC converter design. Poor PC board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, resistive voltage loss in the traces, and thermal problems. Erroneous signals can reach the DC-DC converter, possibly resulting in poor regulation or instability.

Good PCB layout with an LM21305-based converter can be implemented by following a few simple design rules.

1. Provide adequate device heat sinking by utilizing the PCB ground planes as the primary thermal path. As such, the use of thermal vias facilitates the transfer of heat from the LM21305 into the system board. Use at least a 4-layer PCB with the copper thickness for the four layers, starting from the top layer, of 2 oz/1oz/1oz/2 oz. Use a 3 by 3 array of 10mil thermal vias to connect the DAP to the system ground plane heat sink. The vias should be evenly distributed under the DAP. The system ground planes should predominately be PGND planes (representing input and output capacitor return paths, input and output DC current return paths, etc.).
2. It is imperative that the input capacitors are located as close as possible to the PVIN and PGND pins; the inductor should be placed as close as possible to the SW pins and output capacitors. This is to minimize the area of switching current loops and reduce the resistive loss of the high current path. Based the LM21305 pinout, a 1 µF to 10 µF ceramic capacitor can be placed right by pins 1, 2 and pin 7, across the SW node trace, as an addition to the bulk input capacitors. Using a size 1206 or 1210 capacitor allows enough copper width for the switch node to be routed underneath the capacitor for good conduction (see LM21305 evaluation board layout detailed in Application Note AN-2042 (literature number SNVA432)).
3. The copper area of the switch node should be thick and short to both provide a good conduction path for the switch node current to the inductor and to minimize radiated EMI. This also requires the inductor be placed as close as possible to the SW pins.
4. The feedback trace from VOUT to the feedback divider resistors should be routed away from the SW pin and inductor to avoid contaminating this feedback signal with switch noise. This is most important when high resistances are used to set the output voltage. It is recommended to route the feedback trace on a different layer than the inductor and SW node trace such that a ground plane exists between the feedback trace and inductor/SW node polygon. This provides further cancellation of EMI on the feedback trace.
5. If voltage accuracy at the load is important, make sure feedback voltage sense is made directly at the load terminals. Doing so will correct for voltage drops in the PCB planes and traces and provide optimal output voltage setpoint accuracy and load regulation. It is always better to place the resistor divider closer to the FB node, rather than close to the load, as the FB node is the input to the error amplifier and is thus noise sensitive. COMP is also a noise sensitive node and the compensation components should be located as close as possible to the IC.
6. Make input and output power bus connections as wide and short as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Use copper plates/planes on top to connect the multiple PVIN pins and PGND pins together.
7. The 0.1 µF boot capacitor connected between the CBOOT pin and SW node should be placed as close as possible to the CBOOT and SW pins.
8. The frequency set resistor and its associated capacitor should be placed as close as possible to the FREQ pin.

Thermal Considerations

The thermal characteristics of the LM21305 are specified using the parameter θ_{JA}, which relates junction temperature to ambient temperature in a particular LM21305 application. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship: $T_J = P_D\theta_{JA} + T_A$ where

P_D =	P_{IN} x (1 − Efficiency) − 1.1 x I_{OUT}^2x R_{dcr}
T_J =	Junction temperature of the LM21305 in °C
P_{IN} =	Input power in Watts ($P_{IN} = V_{IN}$ x I_{IN})
θ_{JA} =	Junction-to-ambient thermal resistance of the LM21305 in °C/W
T_A =	Ambient temperature in °C

I_{OUT} = Output (load) current

R_{dcr} = Inductor parasitic DC resistance

It is important to always keep the LM21305 operating junction temperature (T_J) below 125°C to assure reliable operation. If the junction temperature exceeds 160°C, the device will cycle in and out of thermal shutdown. If thermal shutdown occurs, it is a sign of inadequate heat-sinking and/or excessive power dissipation in the device. PC board heat-sinking can be improved by using more thermal vias, a larger board, or more heat-spreading layers within that board.

Application Circuit Example

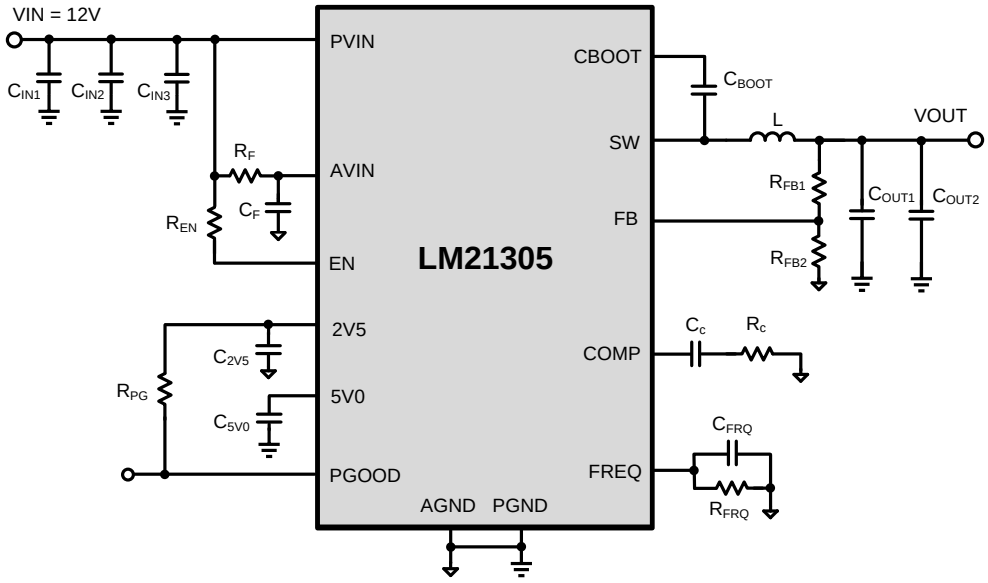


Figure 32. LM21305 Application Circuit Example

Table 1. Bill Of Materials (500kHz Switching Frequency)

V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V	Package
C_{IN1}	TANT 47 µF 25V	TANT 47 µF 25V	TANT 47 µF 25V	TANT 47 µF 25V	TANT 47 µF 25V	CASE D
C_{IN2}	10 µF 25V	10 µF 25V	10 µF 25V	10 µF 25V	10 µF 25V	1210
C_{IN3}	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1206
C_F	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	1.0 µF 25V	0603
C_{2V5}, C_{BOOT}	0.1 µF 16V	0.1 µF 16V	0.1 µF 16V	0.1 µF 16V	0.1 µF 16V	0603
C_{5V0}	1.0 µF 16V	1.0 µF 16V	1.0 µF 16V	1.0 µF 16V	1.0 µF 16V	0603
C_{FRQ}	100 pF 50V	100 pF 50V	100 pF 50V	100 pF 50V	100 pF 50V	0603
C_c	3300 pF 25V	3300 pF 25V	4700 pF 25V	4700 pF 25V	4700 pF 25V	0603
C_{OUT1}, C_{OUT2}	47 µF 6.3V X5R	47 µF 6.3V X5R	47 µF 6.3V X5R	47 µF 10V X5R	47 µF 10V X5R	1210
L	1.5 µH 10A	2.2 µH 10A	2.2 µH 10A	3.3 µH 10A	3.3 µH 10A	SMD
R_F	1Ω 1%	1Ω 1%	1Ω 1%	1Ω 1%	1Ω 1%	0603
R_{FRQ}, R_{PG}	100 kΩ 1%	100 kΩ 1%	100 kΩ 1%	100 kΩ 1%	100 kΩ 1%	0603
R_{FB2}, R_{EN}	10 kΩ 1%	10 kΩ 1%	10 kΩ 1%	10 kΩ 1%	10 kΩ 1%	0603
R_c	3.32 kΩ 1%	4.22 kΩ 1%	5.10 kΩ 1%	7.15 kΩ 1%	8.2 kΩ 1%	0603
R_{FB1}	10 kΩ 1%	20 kΩ 1%	31.6 kΩ 1%	45.3 kΩ 1%	73.2 kΩ 1%	0603

PCB Layout

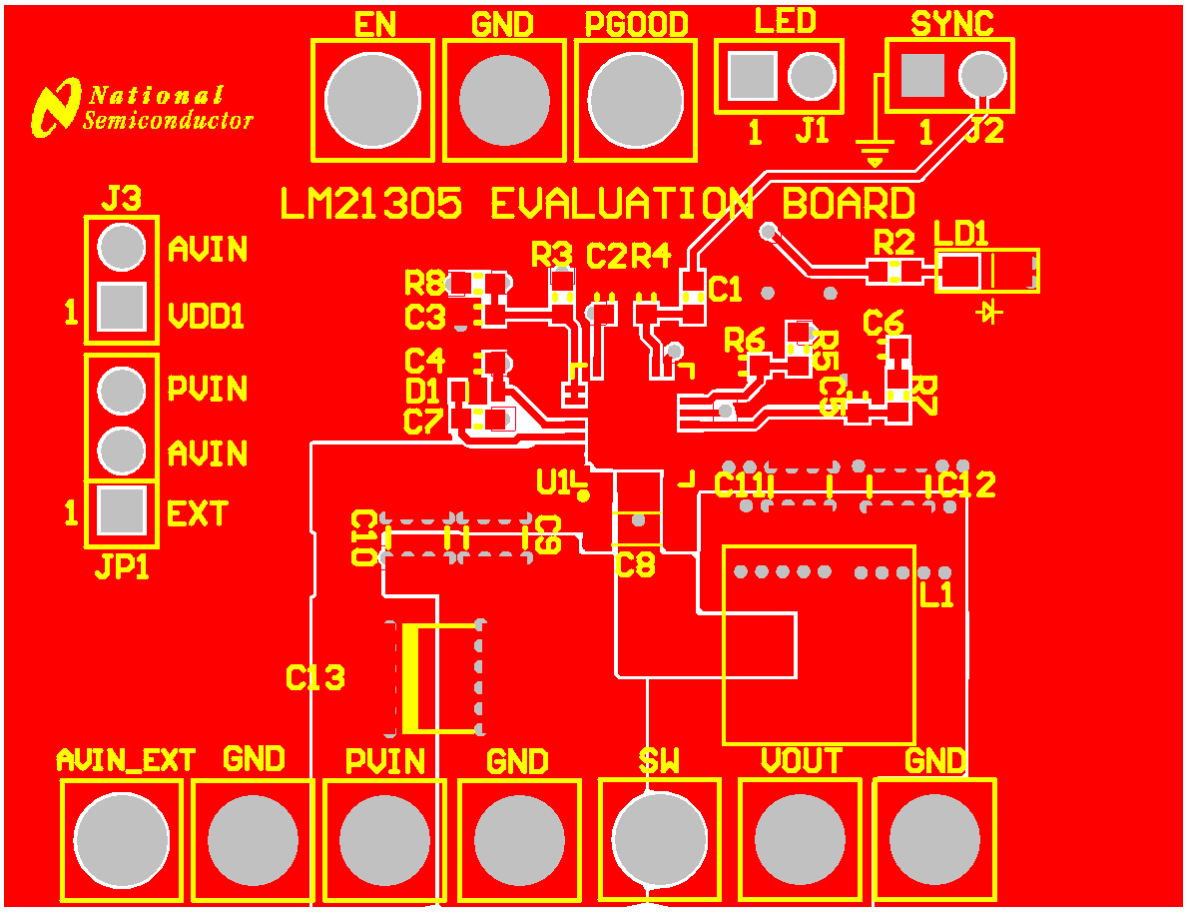


Figure 33. PCB Top Layer Copper and Silkscreen

An example of an LM21305 PCB layout is shown in Figure 33. Only the top layer copper and top silkscreen are shown. For more details, please refer to Application Note AN-2042 (literature number SNVA432).

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	26

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM21305SQ/NOPB	ACTIVE	WQFN	RSG	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	21305SQ	Samples
LM21305SQE/NOPB	ACTIVE	WQFN	RSG	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	21305SQ	Samples
LM21305SQX/NOPB	ACTIVE	WQFN	RSG	28	4500	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	21305SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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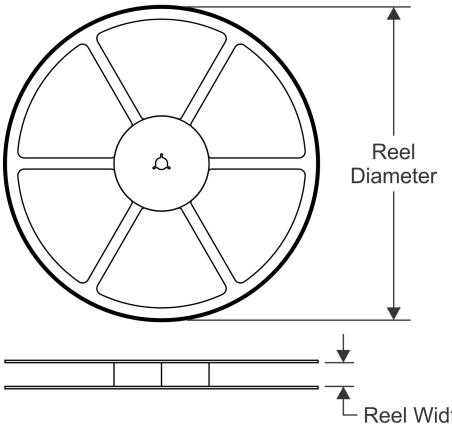
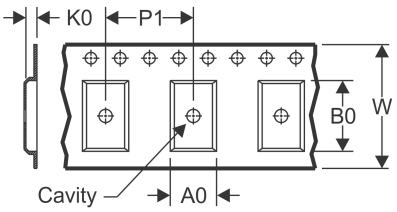
REEL DIMENSIONS

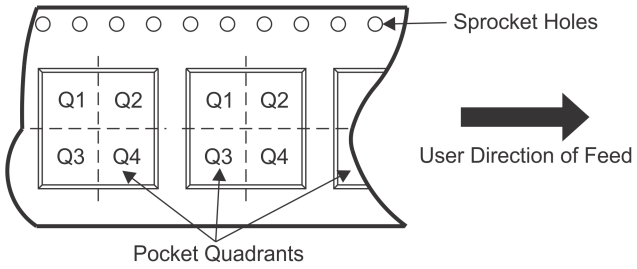


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

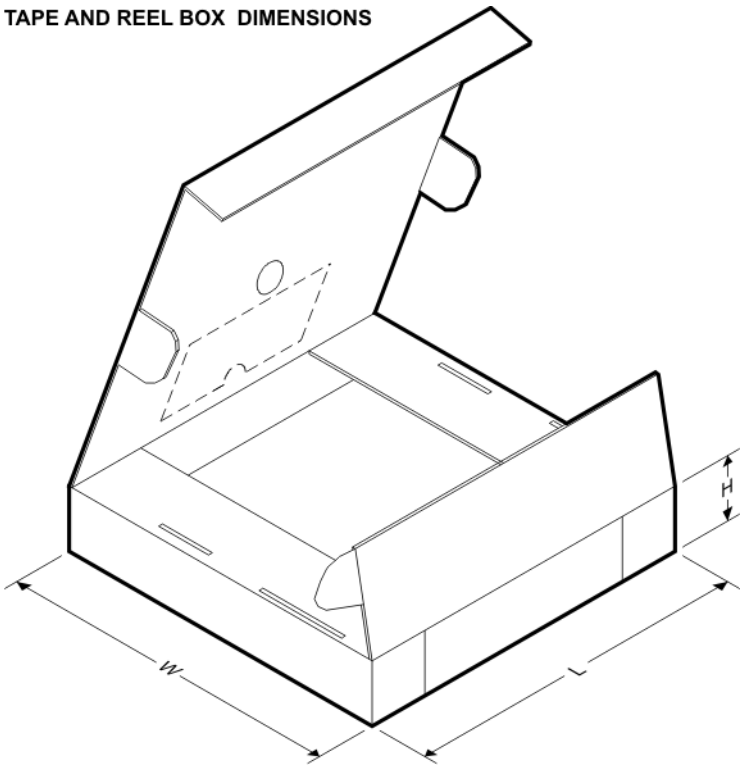
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM21305SQ/NOPB	WQFN	RSG	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM21305SQE/NOPB	WQFN	RSG	28	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM21305SQX/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM21305SQ/NOPB	WQFN	RSG	28	1000	213.0	191.0	55.0
LM21305SQE/NOPB	WQFN	RSG	28	250	213.0	191.0	55.0
LM21305SQX/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0

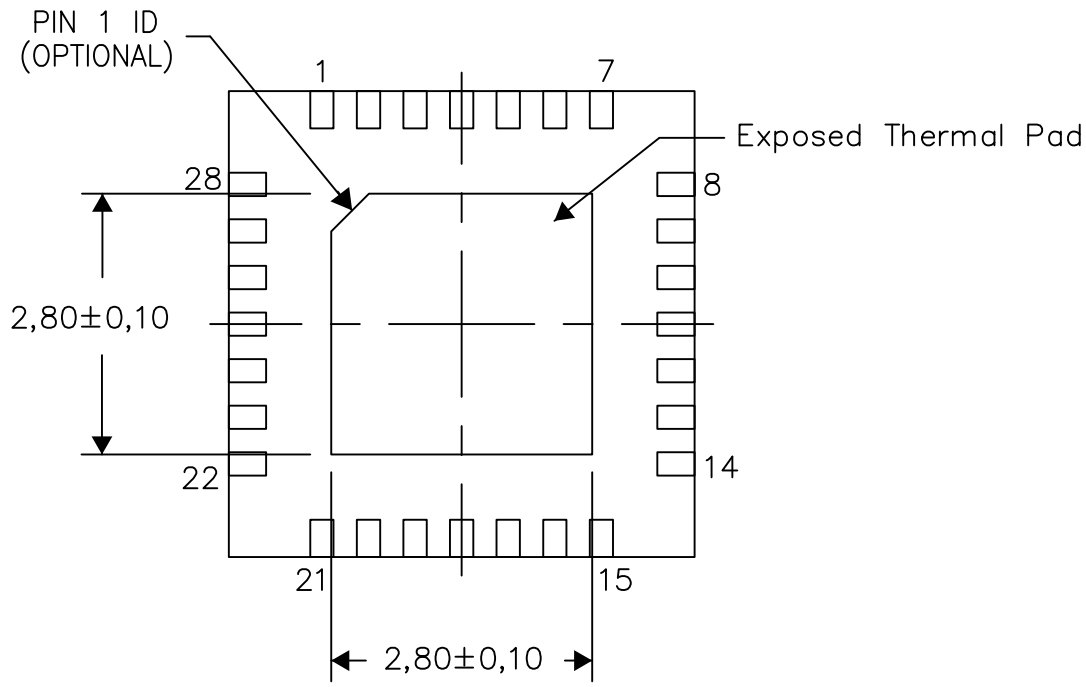
RSG (S–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4221534–3/A 05/14

NOTE: All linear dimensions are in millimeters

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