

±15kV ESD Protected MII/RMII Fast-Ethernet PHY with HP Auto-MDIX and SMSC flexPWR[™]

PRODUCT FEATURES

Datasheet

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- ESD Protection levels of ±8kV HBM without external protection devices
- ESD protection levels of IEC61000-4-2, ±8kV contact mode, and ±15kV for air discharge mode per independent test facility
- Comprehensive SMSC flexPWR[™] Technology
 - Flexible Power Management Architecture
- LVCMOS Variable I/O voltage range: +1.6V to +3.6V
- Integrated 3.3V to 1.8V regulator for optional single supply operation.
 - Regulator can be disabled if 1.8V system supply is available.
- Performs HP Auto-MDIX in accordance with IEEE 802.3ab specification
- Automatic Polarity Correction
- Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
- Energy Detect power-down mode
- Low Current consumption power down mode
- Low operating current consumption:
 - 39mA typical in 10BASE-T and
 - 79mA typical in 100BASE-TX mode
- Supports Auto-negotiation and Parallel Detection
- Supports the Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
- Compliant with IEEE 802.3-2005 standards
 - MII Pins tolerant to 3.6V
- IEEE 802.3-2005 compliant register functions
- Integrated DSP with Adaptive Equalizer
- Baseline Wander (BLW) Correction
- Vendor Specific register functions
- Low profile 64-pin TQFP lead-free RoHS compliant package (10 x 10 x 1.4mm)
- 4 LED status indicators
- Commercial Operating Temperature 0° C to 70° C
- Industrial Operating Temperature -40° C to 85° C version available (LAN8187I)

Applications

- Set Top Boxes
- Network Printers and Servers
- LAN on Motherboard
- 10/100 PCMCIA/CardBus Applications
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- Personal Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- POS Terminals
- Automotive Networking
- Gaming Consoles
- Security Systems
- Access Control

Order Number(S):

LAN8187-JT for 64-pin, TQFP Lead-Free RoHS Compliant Package

LAN8187I-JT for (Industrial Temp) 64-pin, TQFP Lead-Free RoHS Compliant Package



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Chapter 1 General Description

The SMSC LAN8187/LAN8187I is a low-power, industrial temperature (LAN8187I), variable I/O voltage, analog interface IC with HP Auto-MDIX for high-performance embedded Ethernet applications. The LAN8187/LAN8187I can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.8V linear regulator. An option is available to disable the linear regulator to optimize system designs that have a 1.8V power plane available.

1.1 Architectural Overview

The LAN8187/LAN8187I consists of an encoder/decoder, scrambler/descrambler, wave-shaping transmitter, output driver, twisted-pair receiver with adaptive equalizer and baseline wander (BLW) correction, and clock and data recovery functions. The LAN8187/LAN8187I can be configured to support either the Media Independent Interface (MII) or the Reduced Media Independent Interface (RMII).

The LAN8187/LAN8187I is compliant with IEEE 802.3-2005 standards (MII Pins tolerant to 3.6V) and supports both IEEE 802.3-2005 -compliant and vendor-specific register functions. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

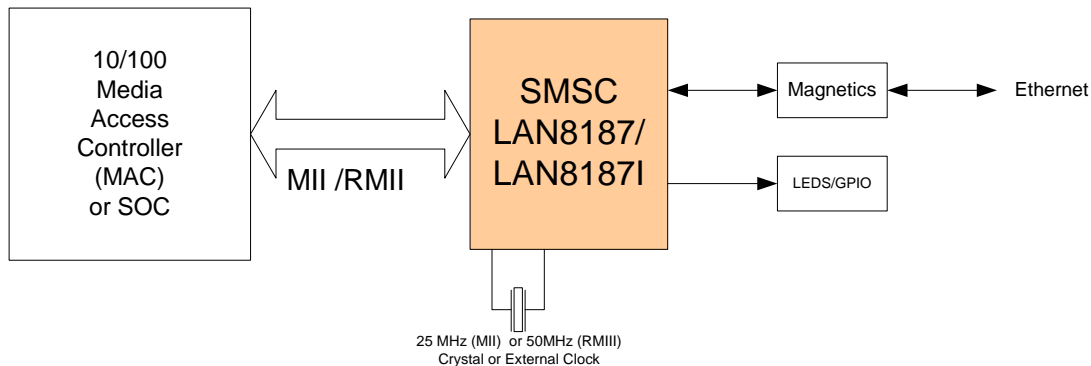


Figure 1.1 LAN8187/LAN8187I System Block Diagram

Hubs and switches with multiple integrated MACs and external PHYs can have a large pin count due to the high number of pins needed for each MII interface. An increasing pin count causes increasing cost.

The RMII interface is intended for use on Switch based ASICs or other embedded solutions requiring minimal pincount for ethernet connectivity. RMII requires only 6 pins for each MAC to PHY interface plus one common reference clock. The MII requires 16 pins for each MAC to PHY interface.

The SMSC LAN8187/LAN8187I is capable of running in RMII mode. Please refer to the RMII consortium for more information on the RMII standard <http://www.rmii-consort.com>.

The LAN8187/LAN8187I referenced throughout this document applies to both the commercial temperature and industrial temperature components. The LAN8187I refers to only the industrial temperature component.

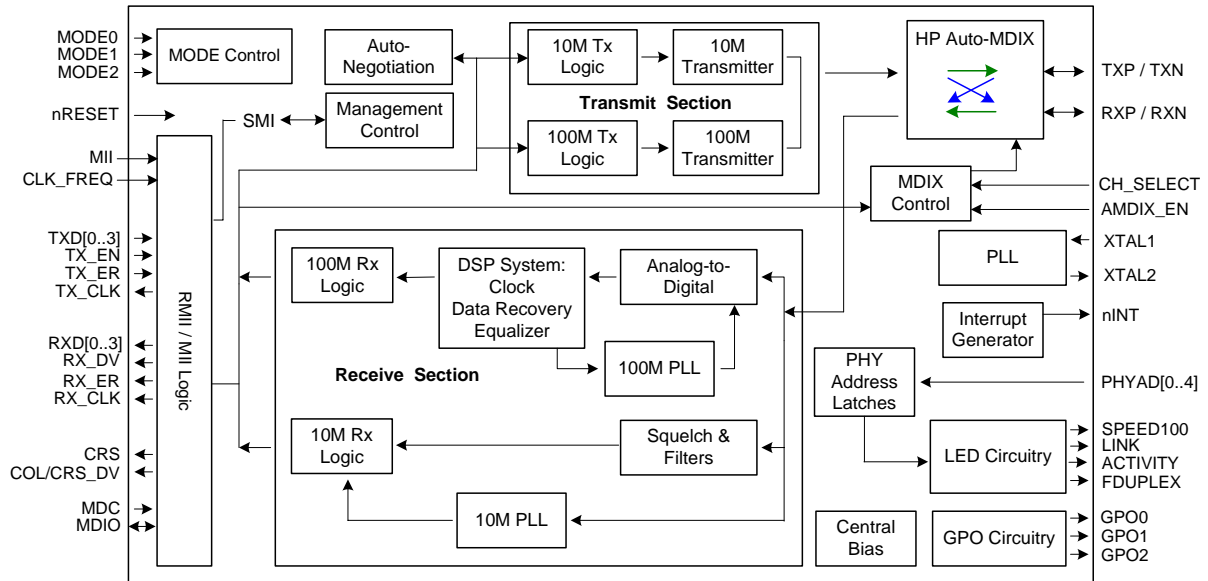


Figure 1.2 LAN8187/LAN8187I Architectural Overview

Chapter 2 Pin Configuration

2.1 Package Pin-out Diagram and Signal Table

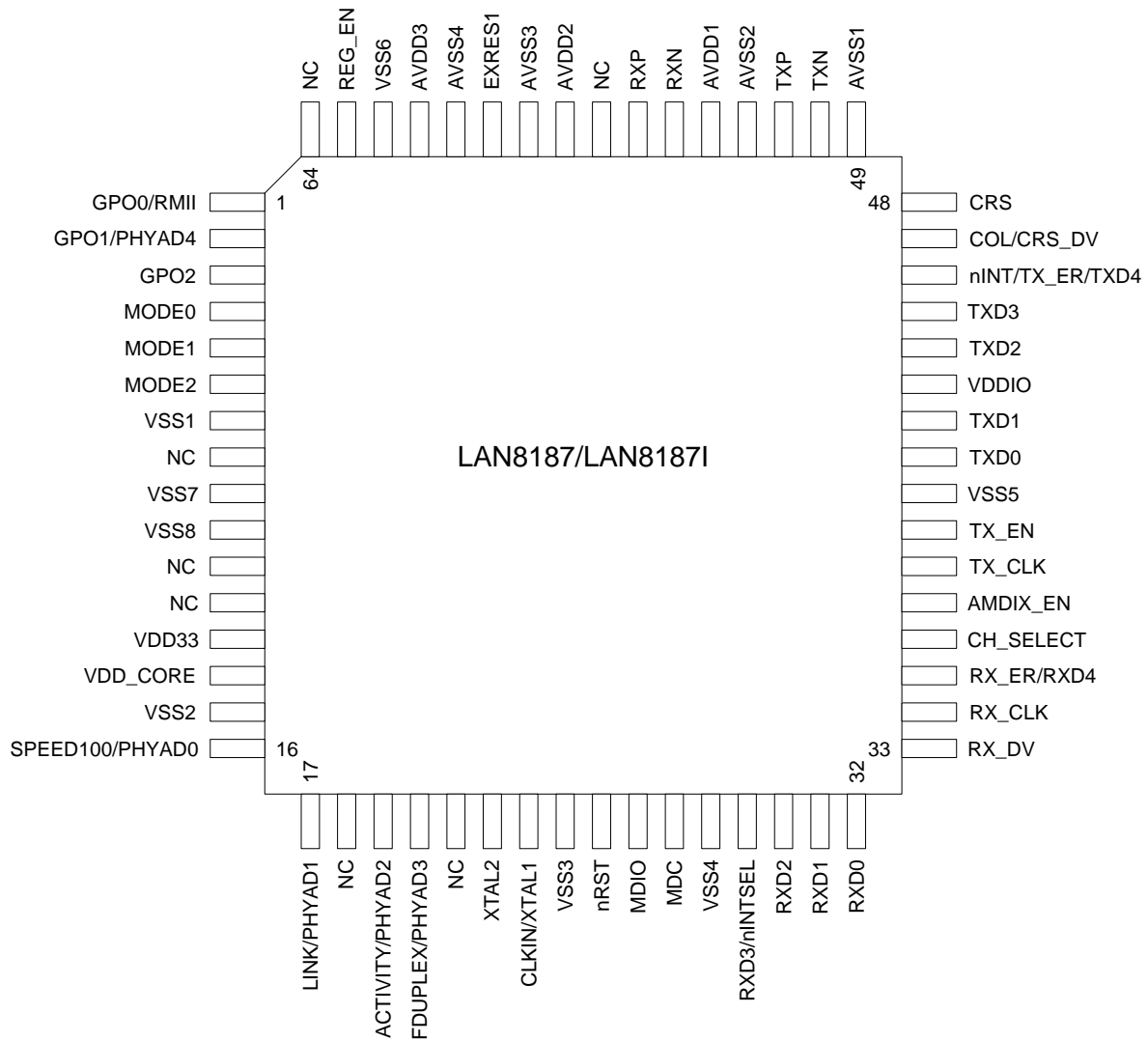


Figure 2.1 Package Pinout (Top View)

Table 2.1 LAN8187/LAN8187I 64-PIN TQFP Pinout

| PIN NO. | PIN NAME | PIN NO. | PIN NAME |
|---------|-----------------|---------|-----------------|
| 1 | GPO0/RMII | 33 | RX_DV |
| 2 | GPO1/PHYAD4 | 34 | RX_CLK |
| 3 | GPO2 | 35 | RX_ER/RXD4 |
| 4 | MODE0 | 36 | CH_SELECT |
| 5 | MODE1 | 37 | AMDIX_EN |
| 6 | MODE2 | 38 | TX_CLK |
| 7 | VSS1 | 39 | TX_EN |
| 8 | NC | 40 | VSS5 |
| 9 | VSS7 | 41 | TXD0 |
| 10 | VSS8 | 42 | TXD1 |
| 11 | NC | 43 | VDDIO |
| 12 | NC | 44 | TXD2 |
| 13 | VDD33 | 45 | TXD3 |
| 14 | VDD_CORE | 46 | nINT/TX_ER/TXD4 |
| 15 | VSS2 | 47 | COL/CRS_DV |
| 16 | SPEED100/PHYAD0 | 48 | CRS |
| 17 | LINK/PHYAD1 | 49 | AVSS1 |
| 18 | NC | 50 | TXN |
| 19 | ACTIVITY/PHYAD2 | 51 | TXP |
| 20 | FDUPLEX/PHYAD3 | 52 | AVSS2 |
| 21 | NC | 53 | AVDD1 |
| 22 | XTAL2 | 54 | RXN |
| 23 | CLKIN/XTAL1 | 55 | RXP |
| 24 | VSS3 | 56 | NC |
| 25 | nRST | 57 | AVDD2 |
| 26 | MDIO | 58 | AVSS3 |
| 27 | MDC | 59 | EXRES1 |
| 28 | VSS4 | 60 | AVSS4 |
| 29 | RXD3/nINTSEL | 61 | AVDD3 |
| 30 | RXD2 | 62 | VSS6 |
| 31 | RXD1 | 63 | REG_EN |
| 32 | RXD0 | 64 | NC |



Chapter 3 Pin Description

This chapter describes the signals on each pin. When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

3.1 I/O Signals

I Input. Digital LVCMOS levels.

O Output. Digital LVCMOS levels.

I/O Input or Output. Digital LVCMOS levels.

Note: The digital signals are not 5V tolerant. They are variable voltage from +1.6V to +3.6V.

AI Input. Analog levels.

AO Output. Analog levels.

Table 3.1 MII Signals

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------------------|------|---|
| TXD0 | I | Transmit Data 0: Bit 0 of the 4 data bits that are accepted by the PHY for transmission. |
| TXD1 | I | Transmit Data 1: Bit 1 of the 4 data bits that are accepted by the PHY for transmission. |
| TXD2 | I | Transmit Data 2: Bit 2 of the 4 data bits that are accepted by the PHY for transmission Note: This signal should be grounded in RMII Mode. |
| TXD3 | I | Transmit Data 3: Bit 3 of the 4 data bits that are accepted by the PHY for transmission. Note: This signal should be grounded in RMII Mode |
| nINT/ TX_ER/ TXD4 | I/O | MIl Transmit Error: When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in 10Base-T operation. MIl Transmit Data 4: In Symbol Interface (5B Decoding) mode, this signal becomes the MIl Transmit Data 4 line, the MSB of the 5-bit symbol code-group. Notes: <ul style="list-style-type: none"> ■ This signal is not used in RMII Mode. ■ This signal is mux'd with nINT ■ See Section 4.10, "(TX_ER/TXD4)/nINT Strapping," on page 31 for additional information on configuration/strapping options. |
| TX_EN | I | Transmit Enable: Indicates that valid data is presented on the TXD[3:0] signals, for transmission. In RMII Mode, only TXD[1:0] have valid data. |
| TX_CLK | O | Transmit Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. Note: This signal is not used in RMII Mode |

Table 3.1 MII Signals (continued)

| SIGNAL NAME | TYPE | DESCRIPTION |
|------------------|------|--|
| RXD0 | O | Receive Data 0: Bit 0 of the 4 data bits that are sent by the PHY in the receive path. |
| RXD1 | O | Receive Data 1: Bit 1 of the 4 data bits that are sent by the PHY in the receive path. |
| RXD2 | O | Receive Data 2: Bit 2 of the 4 data bits that sent by the PHY in the receive path. Note: This signal is not used in RMII Mode. |
| RXD3/ nINTSEL | O | Receive Data 3: Bit 3 of the 4 data bits that sent by the PHY in the receive path. nINTSEL: On power-up or external reset, the mode of the nINT/TXER/TXD4 pin is selected. <ul style="list-style-type: none"> ■ When floated or pulled to VDDIO, nINT is selected (default). ■ When pulled low to VSS through a Pull-down resistor (see Table 4.4, "Boot Strapping Configuration Resistors," on page 32), TXER/TXD4 is selected. Notes: <ul style="list-style-type: none"> ■ RXD3 is not used in RMII Mode ■ If the nINT/TXER/TXD4 pin is configured for nINT mode, it needs a pull-up resistor to VDDIO. ■ See Section 4.10, "(TX_ER/TXD4)/nINT Strapping," on page 31 for additional information on configuration/strapping options. |
| RX_ER/ RXD4 | I/O | Receive Error: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY. MII Receive Data 4: In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. Notes: <ul style="list-style-type: none"> ■ The RX_ER signal is optional in RMII Mode. |
| RX_CLK | O | Receive Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. Notes: <ul style="list-style-type: none"> ■ This signal is not used in RMII Mode |
| COL/CRS_DV | O | MII Collision Detect: Asserted to indicate detection of collision condition. RMII CRS_DV (Carrier Sense/Receive Data Valid) Asserted to indicate when the receive medium is non-idle. When a 10BT packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. In 10BT, half-duplex mode, transmitted data is not looped back onto the receive data pins, per the RMII standard. Note: See Section 4.6.3, "MII vs. RMII Configuration," on page 26 for more details. |



Table 3.2 LED Signals

| SIGNAL NAME | TYPE | DESCRIPTION |
|---------------------|------|--|
| CRS | O | Carrier Sense: Indicates detection of carrier. |
| RX_DV | O | Receive Data Valid: Indicates that recovered and decoded data nibbles are being presented on RXD[3:0]. Note: This signal is not used in RMII Mode. |
| SPEED100/ PHYAD0 | I/O | LED1 – SPEED100 indication. Active indicates that the selected speed is 100Mbps. Inactive indicates that the selected speed is 10Mbps. Note: This signal is mux'd with PHYAD0 |
| LINK/ PHYAD1 | I/O | LED2 – LINK ON indication. Active indicates that the Link (100Base-TX or 10Base-T) is on. Note: This signal is mux'd with PHYAD1 |
| ACTIVITY/ PHYAD2 | I/O | LED3 – ACTIVITY indication. Active indicates that there is Carrier sense (CRS) from the active PMD. Note: This signal is mux'd with PHYAD2 |
| FDUPLEX/ PHYAD3 | I/O | LED4 – DUPLEX indication. Active indicates that the PHY is in full-duplex mode. Note: This signal is mux'd with PHYAD3 |

Table 3.3 Management Signals

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|---|
| MDIO | I/O | Management Data Input/OUTPUT: Serial management data input/output. |
| MDC | I | Management Clock: Serial management clock. |

Table 3.4 Boot Strap Configuration Inputs^a

| SIGNAL NAME | TYPE | DESCRIPTION |
|---------------------|------|--|
| GPO1/ PHYAD4 | I/O | PHY Address Bit 4: set the default address of the PHY. This signal is mux'd with GPO1 |
| FDUPLEX/ PHYAD3 | I/O | PHY Address Bit 3: set the default address of the PHY. Note: This signal is mux'd with FDUPLEX |
| ACTIVITY/ PHYAD2 | I/O | PHY Address Bit 2: set the default address of the PHY. Note: This signal is mux'd with ACTIVITY |
| LINK/ PHYAD1 | I/O | PHY Address Bit 1: set the default address of the PHY. Note: This signal is mux'd with LINK |
| SPEED100/ PHYAD0 | I/O | PHY Address Bit 0: set the default address of the PHY. Note: This signal is mux'd with SPEED100 |

Table 3.4 Boot Strap Configuration Inputs^a

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|--|
| MODE2 | I | PHY Operating Mode Bit 2: set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 53, for the MODE options. |
| MODE1 | I | PHY Operating Mode Bit 1: set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 53, for the MODE options. |
| MODE0 | I | PHY Operating Mode Bit 0: set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 53, for the MODE options. |
| REG_EN | I | Regulator Enable: Internal +1.8V regulator enable: VDDIO – Enables internal regulator. VSS– Disables internal regulator. |
| AMDIX_EN | I | HP Auto-MDIX Enable: This pin is used to manually disable the HP Auto-MDIX function. This can be bypassed using the internal register 27 bit 15. Please see Table 4.3, "Auto-MDIX Control," on page 30 for more information. (VDDIO or Floating) – Enables HP Auto-MDIX. VSS – Disables HP Auto-MDIX |
| CH_SELECT | I | Channel Select: This pin is used in conjunction with the AMDIX_EN pin above to manually select the channel to transmit and receive on. For more information please see Table 4.3, "Auto-MDIX Control," on page 30 (VDDIO or Floating) – MDIX - TX pair receives RX pair transmits. 0V – MDI -TX pair transmits RX pair receives. |
| GPO0/RMII | I/O | General Purpose Output 0 – General Purpose Output signal. Driven by bits in registers 27 and 31. RMII – MII/RMII mode selection is latched on the rising edge of the internal reset (nreset) based on the following strapping: Float the GPO0 pin for MII mode or pull-high with an external Pull-up resistor (see Table 4.4, "Boot Strapping Configuration Resistors," on page 32) to VDDIO to set the device in RMII mode. Note: See Section 4.6.3, "MII vs. RMII Configuration," on page 26 for more details. |

a. On nRST transition high, the PHY latches the state of the configuration pins in this table.

Table 3.5 General Signals

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|---|
| nINT | I/O | LAN Interrupt – Active Low output. Place a pull-up external resistor (see Table 4.4, "Boot Strapping Configuration Resistors," on page 32) to VCC 3.3V. Notes: <ul style="list-style-type: none"> ■ This signal is mux'd with TX_ER/TXD4 ■ See Section 4.10, "(TX_ER/TXD4)/nINT Strapping," on page 31 for additional details on Strapping options. |
| nRST | I | External Reset – input of the system reset. This signal is active LOW. |

**Table 3.5 General Signals (continued)**

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|--|
| CLKIN/XTAL1 | I | <p>Clock Input – 25 Mhz or 50 MHz external clock or crystal input.</p> <p>In MII mode, this signal is the 25 MHz reference input clock</p> <p>In RMII mode, this signal is the 50 MHz reference input clock which is typically also driven to the RMII compliant Ethernet MAC clock input.</p> <p>Note: See Section 4.10, "(TX_ER/TXD4)/nINT Strapping," on page 31 for additional details on Strapping options.</p> |
| XTAL2 | O | <p>Clock Output – 25 MHz crystal output.</p> <p>Note: See Section 4.10, "(TX_ER/TXD4)/nINT Strapping," on page 31 for additional details on Strapping options. Also, float this pin if using an external clock being driven through CLKIN/XTAL1</p> |
| GPO2 | O | <p>General Purpose Output 2 – General Purpose Output signal Driven by bits in registers 27 and 31.</p> |
| GPO1 | O | <p>General Purpose Output 1 – General Purpose Output signal Driven by bits in registers 27 and 31. This signal is mux'd with PHYAD4.</p> |
| GPO0/RMII | I/O | <p>General Purpose Output 0 – General Purpose Output signal. Driven by bits in registers 27 and 31.</p> <p>RMII – MII/RMII mode selection is latched on the rising edge of nRST based on the following strapping:</p> <p>Float the GPO0 pin for MII mode or pull-high with an external resistor to VDDIO to set the device in RMII mode. See Table 4.4, "Boot Strapping Configuration Resistors," on page 32</p> <p>Note: See Section 4.6.3, "MII vs. RMII Configuration," on page 26 for more details.</p> |

Table 3.6 10/100 Line Interface

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|--|
| TXP | AO | Transmit Data: 100Base-TX or 10Base-T differential transmit outputs to magnetics. |
| TXN | AO | Transmit Data: 100Base-TX or 10Base-T differential transmit outputs to magnetics. |
| RXP | AI | Receive Data: 100Base-TX or 10Base-T differential receive inputs from magnetics. |
| RXN | AI | Receive Data: 100Base-TX or 10Base-T differential receive inputs from magnetics. |

Table 3.7 Analog References

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|-------------|
|-------------|------|-------------|

Table 3.7 Analog References

| | | |
|--------|----|---|
| EXRES1 | AI | Connects to reference resistor of value 12.4K-Ohm, 1% connected as described in the Analog Layout Guidelines. |
|--------|----|---|

Table 3.8 No Connect Signals

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|------|-------------|
| NC | | No Connect |

Table 3.9 Power Signals

| SIGNAL NAME | TYPE | DESCRIPTION |
|-------------|-------|---|
| AVDD[1-3] | POWER | +3.3V Analog Power |
| AVSS[1-4] | POWER | Analog Ground |
| VDD_CORE | POWER | +1.8V (Core voltage) - 1.8V regulator output for digital circuitry on chip. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. In parallel, place a 4.7uF +/- 20% low ESR capacitor near this pin and connect the capacitor from this pin to ground. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower than 0.1ohm at frequencies greater than 10kHz. |
| VDD33 | POWER | +3.3V Digital Power |
| VDDIO | POWER | +1.6V to +3.6V Variable I/O Pad Power |
| VSS[1-8] | POWER | Digital Ground (GND) |

Chapter 4 Architecture Details

4.1 Top Level Functional Architecture

Functionally, the PHY can be divided into the following sections:

- 100Base-TX transmit and receive
- 10Base-T transmit and receive
- MII or RMII interface to the controller
- Auto-negotiation to automatically determine the best speed and duplex possible
- Management Control to read status registers and write control registers

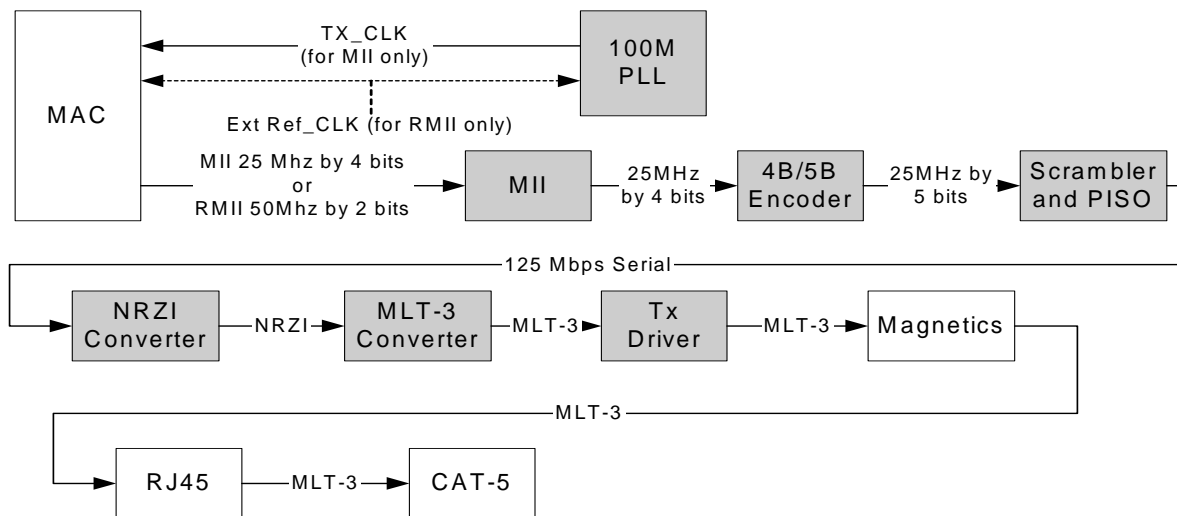


Figure 4.1 100Base-TX Data Path

4.2 100Base-TX Transmit

The data path of the 100Base-TX is shown in [Figure 4.1](#). Each major block is explained below.

4.2.1 100M Transmit Data Across the MII/RMII

For MII, the MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 25MHz data.

The MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of REF_CLK. The data is in the form of 2-bit wide 50MHz data.

4.2.2 4B/5B Encoding

The transmit data passes from the MII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to [Table 4.1](#). Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

The encoding process may be bypassed by clearing bit 6 of register 31. When the encoding is bypassed the 5th transmit data bit is equivalent to TX_ER.

Note that encoding can be bypassed only when the MAC interface is configured to operate in MII mode.

Table 4.1 4B/5B Code Table

| CODE GROUP | SYM | RECEIVER INTERPRETATION | | | TRANSMITTER INTERPRETATION | | |
|------------|-----|---|------|------|-----------------------------|------|------|
| | | | | | | | |
| 11110 | 0 | 0 | 0000 | DATA | 0 | 0000 | DATA |
| 01001 | 1 | 1 | 0001 | | 1 | 0001 | |
| 10100 | 2 | 2 | 0010 | | 2 | 0010 | |
| 10101 | 3 | 3 | 0011 | | 3 | 0011 | |
| 01010 | 4 | 4 | 0100 | | 4 | 0100 | |
| 01011 | 5 | 5 | 0101 | | 5 | 0101 | |
| 01110 | 6 | 6 | 0110 | | 6 | 0110 | |
| 01111 | 7 | 7 | 0111 | | 7 | 0111 | |
| 10010 | 8 | 8 | 1000 | | 8 | 1000 | |
| 10011 | 9 | 9 | 1001 | | 9 | 1001 | |
| 10110 | A | A | 1010 | | A | 1010 | |
| 10111 | B | B | 1011 | | B | 1011 | |
| 11010 | C | C | 1100 | | C | 1100 | |
| 11011 | D | D | 1101 | | D | 1101 | |
| 11100 | E | E | 1110 | | E | 1110 | |
| 11101 | F | F | 1111 | | F | 1111 | |
| 11111 | I | IDLE | | | Sent after /T/R until TX_EN | | |
| 11000 | J | First nibble of SSD, translated to "0101" following IDLE, else RX_ER | | | Sent for rising TX_EN | | |
| 10001 | K | Second nibble of SSD, translated to "0101" following J, else RX_ER | | | Sent for rising TX_EN | | |
| 01101 | T | First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RX_ER | | | Sent for falling TX_EN | | |
| 00111 | R | Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RX_ER | | | Sent for falling TX_EN | | |
| 00100 | H | Transmit Error Symbol | | | Sent for rising TX_ER | | |
| 00110 | V | INVALID, RX_ER if during RX_DV | | | INVALID | | |
| 11001 | V | INVALID, RX_ER if during RX_DV | | | INVALID | | |
| 00000 | V | INVALID, RX_ER if during RX_DV | | | INVALID | | |
| 00001 | V | INVALID, RX_ER if during RX_DV | | | INVALID | | |

**Table 4.1 4B/5B Code Table (continued)**

| CODE GROUP | SYM | RECEIVER INTERPRETATION | TRANSMITTER INTERPRETATION |
|------------|-----|--------------------------------|----------------------------|
| 00010 | V | INVALID, RX_ER if during RX_DV | INVALID |
| 00011 | V | INVALID, RX_ER if during RX_DV | INVALID |
| 00101 | V | INVALID, RX_ER if during RX_DV | INVALID |
| 01000 | V | INVALID, RX_ER if during RX_DV | INVALID |
| 01100 | V | INVALID, RX_ER if during RX_DV | INVALID |
| 10000 | V | INVALID, RX_ER if during RX_DV | INVALID |

4.2.3 Scrambling

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the PHY address, PHYAD[4:0], ensuring that in multiple-PHY applications, such as repeaters or switches, each PHY will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

4.2.4 NRZI and MLT3 Encoding

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

4.2.5 100M Transmit Driver

The MLT3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media across a 1:1 ratio isolation transformer. The 10Base-T and 100Base-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

4.2.6 100M Phase Lock Loop (PLL)

The 100M PLL locks onto reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100Base-Tx Transmitter.

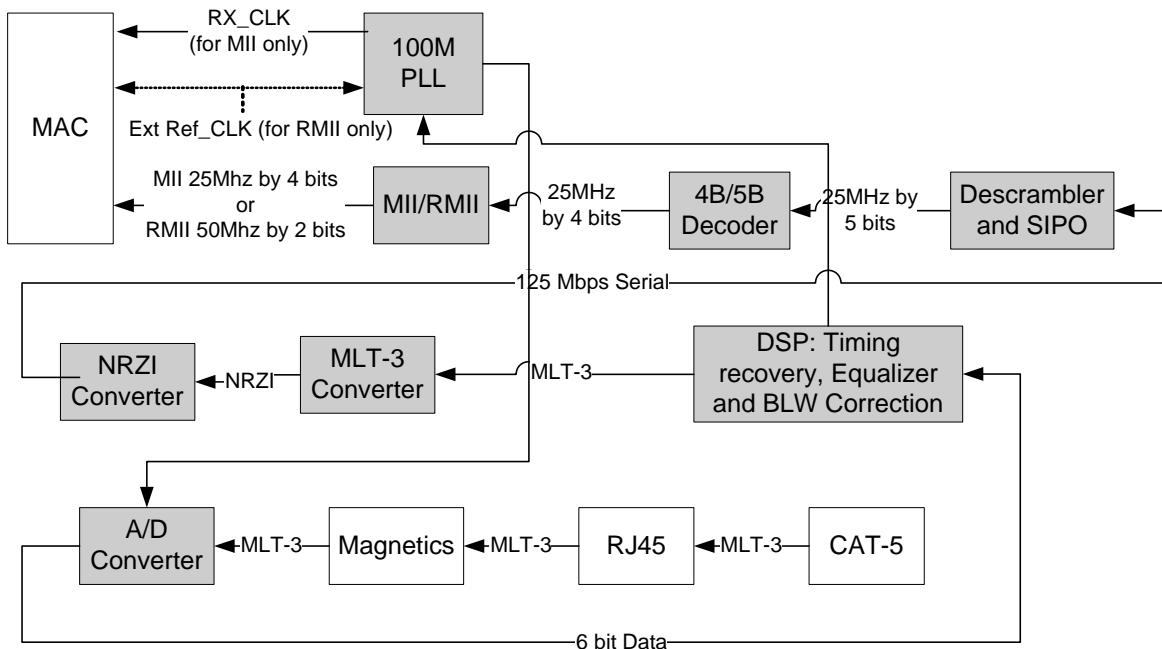


Figure 4.2 Receive Data Path

4.3 100Base-TX Receive

The receive data path is shown in [Figure 4.2](#). Detailed descriptions are given below.

4.3.1 100M Receive Input

The MLT-3 from the cable is fed into the PHY (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quantizer it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

4.3.2 Equalizer, Baseline Wander Correction and Clock and Data Recovery

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT-5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

4.3.3 NRZI and MLT-3 Decoding

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

4.3.4 Descrambling

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols, the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote PHY by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

The descrambler can be bypassed by setting bit 0 of register 31.

4.3.5 Alignment

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

4.3.6 5B/4B Decoding

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[3:0] signal lines. The SSD, /J/K/, is translated to "0101 0101" as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the PHY to assert the RX_DV signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the PHY to de-assert carrier sense and RX_DV.

These symbols are not translated into data.

The decoding process may be bypassed by clearing bit 6 of register 31. When the decoding is bypassed the 5th receive data bit is driven out on RX_ER/RXD4. Decoding may be bypassed only when the MAC interface is in MII mode.

4.3.7 Receive Data Valid Signal

The Receive Data Valid signal (RX_DV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RX_CLK. RX_DV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RX_DV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII).

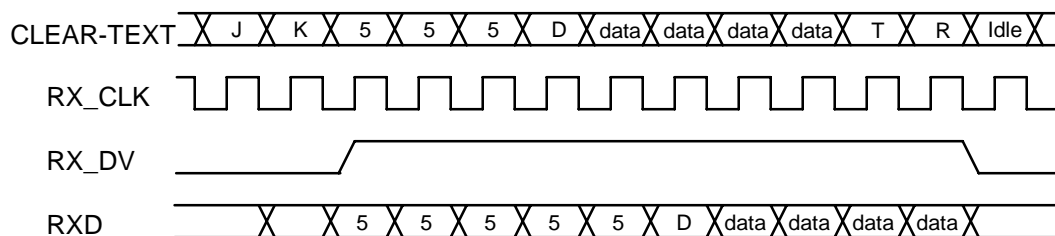


Figure 4.3 Relationship Between Received Data and specific MII Signals

4.3.8 Receiver Errors

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RX_ER signal is asserted and arbitrary data is driven onto the RXD[3:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RX_ER is asserted true and the value '1110' is driven onto the RXD[3:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

4.3.9 100M Receive Data Across the MII/RMII Interface

In MII mode, the 4-bit data nibbles are sent to the MII block. These data nibbles are clocked to the controller at a rate of 25MHz. The controller samples the data on the rising edge of RX_CLK. To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of RX_CLK. RX_CLK is the 25MHz output clock for the MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock (CLKIN).

When tracking the received data, RX_CLK has a maximum jitter of 0.8ns (provided that the jitter of the input clock, CLKIN, is below 100ps).

In RMII mode, the 2-bit data nibbles are sent to the RMII block. These data nibbles are clocked to the controller at a rate of 50MHz. The controller samples the data on the rising edge of CLKIN/XTAL1 (REF_CLK). To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of CLKIN/XTAL1 (REF_CLK).

4.4 10Base-T Transmit

Data to be transmitted comes from the MAC layer controller. The 10Base-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

4.4.1 10M Transmit Data Across the MII/RMII Interface

The MAC controller drives the transmit data onto the TXD BUS. For MII, when the controller has driven TX_EN high to indicate valid data, the data is latched by the MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 2.5MHz data.

In order to comply with legacy 10Base-T MAC/Controllers, in Half-duplex mode the PHY loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The PHY also supports the SQE (Heartbeat) signal. See [Section 5.4.2, "Collision Detect," on page 51](#), for more details.

For RMII, TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the LAN8187/LAN8187I. TXD[1:0] shall be "00" to indicate idle when TX_EN is deasserted. Values of TXD[1:0] other than "00" when TX_EN is deasserted are reserved for out-of-band signalling (to be defined). Values other than "00" on TXD[1:0] while TX_EN is deasserted shall be ignored by the LAN8187/LAN8187I. TXD[1:0] shall provide valid data for each REF_CLK period while TX_EN is asserted.

4.4.2 Manchester Encoding

The 4-bit wide data is sent to the TX10M block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TX_EN is low), the TX10M block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner.

4.4.3 10M Transmit Drivers

The Manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXP and TXN outputs.

4.5 10Base-T Receive

The 10Base-T receiver gets the Manchester- encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller across the MII at a rate of 2.5MHz.

This 10M receiver uses the following blocks:

- Filter and SQUELCH (analog)
- 10M PLL (analog)
- RX 10M (digital)
- MII (digital)

4.5.1 10M Receive Input and Squelch

The Manchester signal from the cable is fed into the PHY (on inputs RXP and RXN) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

4.5.2 Manchester Decoding

The output of the SQUELCH goes to the RX10M block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), then this is identified and corrected. The reversed condition is indicated by the flag "XPOL", bit 4 in register 27. The 10M PLL is locked onto the received Manchester signal and from this, generates the received 20MHz clock. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The RX10M block also detects valid 10Base-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

4.5.3 10M Receive Data Across the MII/RMII Interface

For MII, the 4 bit data nibbles are sent to the MII block. In MII mode, these data nibbles are valid on the rising edge of the 2.5 MHz RX_CLK.

For RMII, the 2bit data nibbles are sent to the RMII block. In RMII mode, these data nibbles are valid on the rising edge of the RMII REF_CLK.

4.5.4 Jabber Detection

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, that results in holding the TX_EN input for a long period. Special logic is used to detect the jabber state and abort the transmission to the line, within 45ms. Once TX_EN is deasserted, the logic resets the jabber condition.

As shown in [Table 5.31](#), bit 1.1 indicates that a jabber condition was detected.

4.6 MAC Interface

The MII/RMII block is responsible for the communication with the controller. Special sets of hand-shake signals are used to indicate that valid received/transmitted data is present on the 4 bit receive/transmit bus.

The device must be configured in MII or RMII mode. This is done by specific pin strapping configurations.

See section [Section 4.6.3, "MII vs. RMII Configuration,"](#) on page 26 for information on pin strapping and how the pins are mapped differently.

4.6.1 MII

The MII includes 16 interface signals:

- transmit data - TXD[3:0]
- transmit strobe - TX_EN
- transmit clock - TX_CLK
- transmit error - TX_ER/TXD4
- receive data - RXD[3:0]
- receive strobe - RX_DV
- receive clock - RX_CLK
- receive error - RX_ER/RXD4
- collision indication - COL
- carrier sense - CRS

In MII mode, on the transmit path, the PHY drives the transmit clock, TX_CLK, to the controller. The controller synchronizes the transmit data to the rising edge of TX_CLK. The controller drives TX_EN high to indicate valid transmit data. The controller drives TX_ER high when a transmit error is detected.

On the receive path, the PHY drives both the receive data, RXD[3:0], and the RX_CLK signal. The controller clocks in the receive data on the rising edge of RX_CLK when the PHY drives RX_DV high. The PHY drives RX_ER high when a receive error is detected.

4.6.2 RMII

The SMSC LAN8187/LAN8187I supports the low pin count Reduced Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch ASICs. Under IEEE 802.3, an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or PHY interfaces such as switches, the number of pins can add significant cost as the port counts increase. The management interface (MDIO/MDC) is identical to MII. The RMII interface has the following characteristics:

- It is capable of supporting 10Mb/s and 100Mb/s data rates
- A single clock reference is sourced from the MAC to PHY (or from an external source)
- It provides independent 2 bit wide (di-bit) transmit and receive data paths



- It uses LVCMOS signal levels, compatible with common digital CMOS ASIC processes

The RMII includes 6 interface signals with one of the signals being optional:

- transmit data - TXD[1:0]
- transmit strobe - TX_EN
- receive data - RXD[1:0]
- receive error - RX_ER (Optional)
- carrier sense - CRS_DV
- Reference Clock - CLKIN/XTAL1 (RMII references usually define this signal as REF_CLK)

4.6.2.1 Reference Clock

The Reference Clock - CLKIN, is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. The Reference Clock is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device.

The “Reference Clock” frequency must be 50 MHz +/- 50 ppm with a duty cycle between 35% and 65% inclusive. The SMSC LAN8187/LAN8187I uses the “Reference Clock” as the network clock such that no buffering is required on the transmit data path. The SMSC LAN8187/LAN8187I will recover the clock from the incoming data stream, the receiver will account for differences between the local REF_CLK and the recovered clock through use of sufficient elasticity buffering. The elasticity buffer does not affect the Inter-Packet Gap (IPG) for received IPGs of 36 bits or greater. To tolerate the clock variations specified here for Ethernet MTUs, the elasticity buffer shall tolerate a minimum of +/-10 bits.

4.6.2.2 CRS_DV - Carrier Sense/Receive Data Valid

The CRS_DV is asserted by the LAN8187/LAN8187I when the receive medium is non-idle. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected, carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (i.e. CRS_DV is deasserted only on nibble boundaries). If the LAN8187/LAN8187I has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the LAN8187/LAN8187I shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and de-assert CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. The result is: Starting on nibble boundaries CRS_DV toggles at 25 MHz in 100Mb/s mode and 2.5 MHz in 10Mb/s mode when CRS ends before RX_DV (i.e. the FIFO still has bits to transfer when the carrier event ends.) Therefore, the MAC can accurately recover RX_DV and CRS.

During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place.

4.6.3 MII vs. RMII Configuration

The LAN8187/LAN8187I must be configured to support the MII or RMII bus for connectivity to the MAC. This configuration is done through the GPO0/RMII pin.

MII or RMII mode selection is latched on the rising edge of the internal reset (nreset) based on the strapping of the GPO0/RMII pin. To select MII mode, float the GPO0/RMII pin. To select RMII mode, pull-high with an external resistor (see [Table 4.4, “Boot Strapping Configuration Resistors,” on page 32](#)) to VDD33.

Most of the MII and RMII pins are multiplexed. [Table 4.2, "MII/RMII Signal Mapping"](#), shown below, describes the relationship of the related device pins to what pins are used in MII and RMII mode.

Table 4.2 MII/RMII Signal Mapping

| SIGNAL NAME | MII MODE | RMII MODE |
|----------------|-----------------|-----------------------------------|
| TXD0 | TXD0 | TXD0 |
| TXD1 | TXD1 | TXD1 |
| TX_EN | TX_EN | TX_EN |
| RX_ER/ RXD4 | RX_ER/ RXD4/ | RX_ER Note 4.2 |
| COL/CRS_DV | COL | CRS_DV |
| RXD0 | RXD0 | RXD0 |
| RXD1 | RXD1 | RXD1 |
| TXD2 | TXD2 | Note 4.1 |
| TXD3 | TXD3 | Note 4.1 |
| TX_ER/ TXD4 | TX_ER/ TXD4 | |
| CRS | CRS | |
| RX_DV | RX_DV | |
| RXD2 | RXD2 | |
| RXD3 | RXD3 | |
| TX_CLK | TX_CLK | |
| RX_CLK | RX_CLK | |
| CLKIN/XTAL1 | CLKIN/XTAL1 | REF_CLK |

Note 4.1 In RMII mode, this pin needs to tied to VSS.

Note 4.2 The RX_ER signal is optional on the RMII bus. This signal is required by the PHY, but it is optional for the MAC. The MAC can choose to ignore or not use this signal.

4.7 Auto-negotiation

The purpose of the Auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication bits in register 31, as well as the Link Partner Ability Register (Register 5).

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.



The advertised capabilities of the PHY are stored in register 4 of the SMI registers. The default advertised by the PHY is determined by user-defined on-chip signal options.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)
- 10M PLL (analog)
- 10M Transmitter (analog)

When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset
- Power-down reset
- Link status down
- Setting register 0, bit 9 high (auto-negotiation restart)

On detection of one of these events, the PHY begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). These are bursts of link pulses from the 10M transmitter. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a "1", while absence represents a "0".

The data transmitted by an FLP burst is known as a "Link Code Word." These are defined fully in IEEE 802.3 clause 28. In summary, the PHY advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in register 4 of the SMI registers.

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (Highest priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex

If the full capabilities of the PHY are advertised (100M, Full Duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of Half and Full duplex modes, then auto-negotiation selects Full Duplex as the highest performance operation.

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if not all of the required FLP bursts are received.

The capabilities advertised during auto-negotiation by the PHY are initially determined by the logic levels latched on the MODE[2:0] bus after reset completes. This bus can also be used to disable auto-negotiation on power-up.

Writing register 4 bits [8:5] allows software control of the capabilities advertised by the PHY. Writing register 4 does not automatically re-start auto-negotiation. Register 0, bit 9 must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing register 0, bit 12.

The LAN8187/LAN8187I does not support "Next Page" capability.

4.7.1 Parallel Detection

If the LAN8187/LAN81871 is connected to a device lacking the ability to auto-negotiate (i.e. no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be Half Duplex per the IEEE standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then bit 0 in register 6 is cleared to indicate that the Link Partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, bit 4 of register 6 is set.

Register 5 is used to store the Link Partner Ability information, which is coded in the received FLPs. If the Link Partner is not auto-negotiation capable, then register 5 is updated after completion of parallel detection to reflect the speed capability of the Link Partner.

4.7.2 Re-starting Auto-negotiation

Auto-negotiation can be re-started at any time by setting register 0, bit 9. Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts Auto-negotiation by writing to bit 9 of the control register, the LAN8187/LAN81871 will respond by stopping all transmission/receiving operations. Once the break_link_timer is done, in the Auto-negotiation state-machine (approximately 1200ms) the auto-negotiation will re-start. The Link Partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

4.7.3 Disabling Auto-negotiation

Auto-negotiation can be disabled by setting register 0, bit 12 to zero. The device will then force its speed of operation to reflect the information in register 0, bit 13 (speed) and register 0, bit 8 (duplex). The speed and duplex bits in register 0 should be ignored when auto-negotiation is enabled.

4.7.4 Half vs. Full Duplex

Half Duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. In this mode, If data is received while the PHY is transmitting, a collision results.

In Full Duplex mode, the PHY is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.







4.8 HP Auto-MDIX

HP Auto-MDIX facilitates the use of CAT-3 (10 Base-T) or CAT-5 (100 Base-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable, or a cross-over patch cable, as shown in [Figure 4.4 on page 31](#), the SMSC LAN8187/LAN81871 Auto-MDIX PHY is capable of configuring the TXP/TXN and RXP/RXN pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled through an internal register 27, or the external control pins AMDIX_EN. When disabled the TX and RX pins can be configured with the Channel Select (CH_SELECT) pin as desired. The table below shows how the control pins and the register are used to configure the Auto-MDIX function.

Table 4.3 Auto-MDIX Control

| Register 27 bits | | | External Pins | | Status |
|------------------|----|----|---------------|-----------|---|
| 15 | 14 | 13 | AMDIXEN | CH_SELECT | TX and RX output Pins |
| 0 | X | X | 1 | X | Auto-MDIX  |
| 0 | X | X | 0 | 0 | Normal MDI  |
| 0 | X | X | 0 | 1 | Crossed MDIX  |
| 1 | 1 | X | X | X | Auto-MDIX  |
| 1 | 0 | 0 | X | X | Normal MDI  |
| 1 | 0 | 1 | X | X | Crossed MDIX  |

Note: X = either 1 or 0.

Note: X = Dont Care.

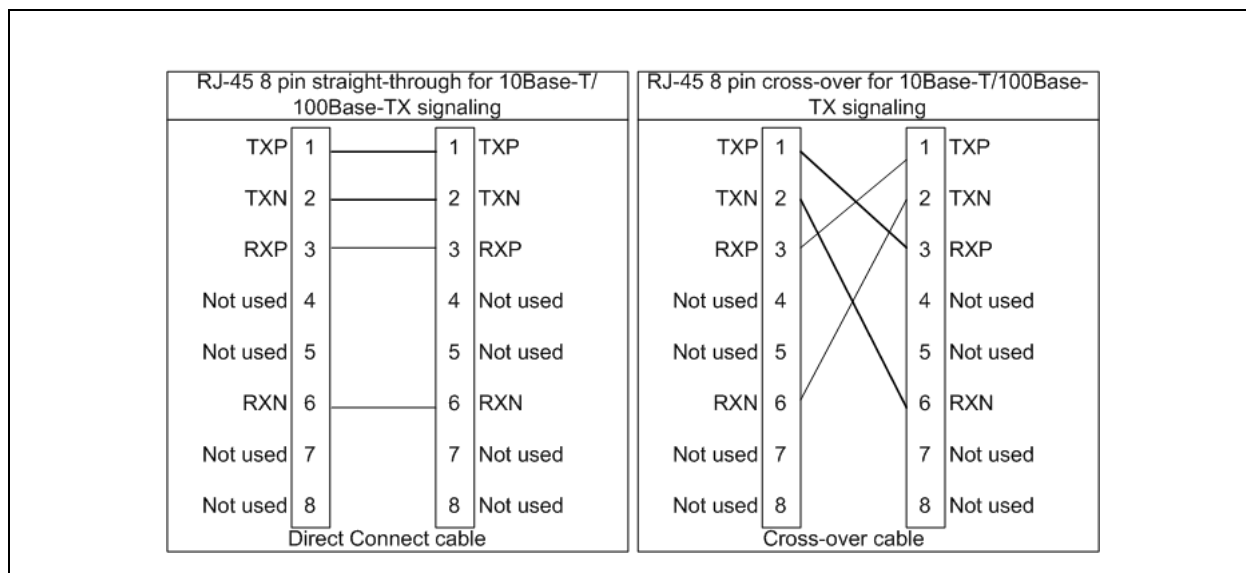


Figure 4.4 Direct cable connection vs. Cross-over cable connection.

4.9 Internal +1.8V Regulator Disable

Part of the LAN8187/LAN8187I SMSC flexPWR™ technology is the ability to disable the internal +1.8v regulator. This further increases the power savings as a more efficient external switching regulator can provide the necessary +1.8v to the internal PHY circuitry.

4.9.1 Disable the Internal +1.8V Regulator

To disable the +1.8v internal regulator, a pull-down strapping resistor (see [Table 4.4, "Boot Strapping Configuration Resistors," on page 32](#)) is attached from REG_EN to VDDIO. When both VDDIO and VDDA are within specification, the PHY will sample the REG_EN pin to determine if the internal regulator should turn on. If the pin is grounded to VSS, then the internal regulator is off, and the system needs to supply +1.8v +/- 10% to the VDD_CORE pin.

A 4.7uF low ESR and 0.1uF capacitor must be added to VDD_CORE and placed close to the PHY. This capacitance provides decoupling of the external power supply noise and ensures stability of the internal regulator.

4.9.2 Enable the Internal +1.8V Regulator

To enable the internal regulator, a pull-up resistor (see [Table 4.4, "Boot Strapping Configuration Resistors," on page 32](#)) to VDDIO needs to be added to the REG_EN pin.

A 4.7uF low ESR and 0.1uF capacitor must be added to VDD_CORE and placed close to the PHY. This capacitance provides decoupling of the external power supply noise and ensures stability of the internal regulator.

4.10 (TX_ER/TXD4)/nINT Strapping

The TX_ER, TXD4 and nINT functions share a common pin. There are two functional modes for this pin, the TX_ER/TXD4 mode and nINT (interrupt) mode. The RXD3 pin is used to select one of these two functional modes.

The RXD3 pin is latched on the rising edge of the internal reset (nreset) to select the mode. The system designer must float the RXD3 pin for nINT mode or pull-low with an external resistor (see

Table 4.4, “Boot Strapping Configuration Resistors,” on page 32) to VSS to set the device in TX_ER/TXD4 mode. The default setting is high (nINT mode).

4.11 PHY Address Strapping and LED Output Polarity Selection

The PHY ADDRESS bits are latched on the rising edge of the internal reset (nreset). The 5-bit address word[0:4] is input on the LED1, LED2, LED3, LED4, GPO1 output pins. The default setting is all high 5'b1_1111.

The address lines are strapped as defined in the diagram below. The LED outputs will automatically change polarity based on the presence of an external pull-down resistor. If the LED pin is pulled high (by an internal 100K pull-up resistor) to select a logical high PHY address, then the LED output will be active low. If the LED pin is pulled low (by an external pull-down resistor (see Table 4.4, “Boot Strapping Configuration Resistors,” on page 32) to select a logical low PHY address, the LED output will then be an active high output.

To set the PHY address on the LED pins without LEDs or on the GPO1 or CRS pin, float the pin to set the address high or pull-down the pin with an external resistor (see Table 4.4, “Boot Strapping Configuration Resistors,” on page 32) to GND to set the address low. See the figure below:

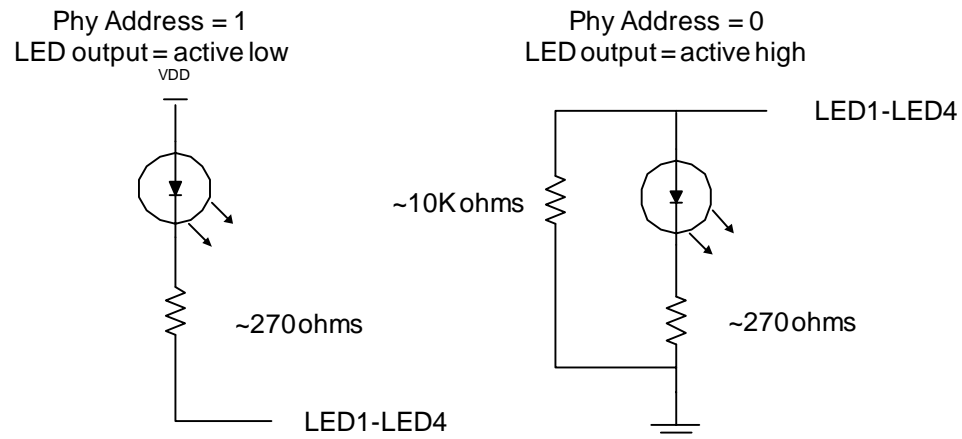


Figure 4.5 PHY Address Strapping on LED's

4.12 Variable Voltage I/O

The Digital I/O pins on the LAN8187/LAN8187I are variable voltage to take advantage of low power savings from shrinking technologies. These pins can operate from a low I/O voltage of +1.6V up to +3.6V. Due to this low voltage feature addition, the system designer needs to take consideration as for two aspects of their design. Boot strapping configuration and I/O voltage stability.

4.12.1 Boot Strapping Configuration.

Due to a lower I/O voltage, a lower strapping resistor needs to be used to ensure the strapped configuration is latched into the PHY device at power-on reset.

Table 4.4 Boot Strapping Configuration Resistors

| I/O voltage | Pull-up/Pull-down Resistor |
|-------------|----------------------------|
| 3.0 to 3.6 | 10k ohm resistor |
| 2.0 to 3.0 | 7.5k ohm resistor |

Table 4.4 Boot Strapping Configuration Resistors

| I/O voltage | Pull-up/Pull-down Resistor |
|-------------|----------------------------|
| 1.6 to 2.0 | 5k ohm resistor |

4.12.2 I/O Voltage Stability

The I/O voltage the System Designer applies on VDDIO needs to maintain its value with a tolerance of +/- 10%. Varying the voltage up or down, after the PHY has completed power-on reset can cause errors in the PHY operation.

4.13 PHY Management Control

The Management Control module includes 3 blocks:

- Serial Management Interface (SMI)
- Management Registers Set
- Interrupt

4.13.1 Serial Management Interface (SMI)

The Serial Management Interface is used to control the LAN8187/LAN8187I and obtain its status. This interface supports registers 0 through 6 as required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers 16 to 31 allowed by the specification. Non-supported registers (7 to 15) will be read as hexadecimal “FFFF”.

At the system level there are 2 signals, MDIO and MDC where MDIO is bi-directional open-drain and MDC is the clock.

A special feature (enabled by register 17 bit 3) forces the PHY to disregard the PHY-Address in the SMI packet causing the PHY to respond to any address. This feature is useful in multi-PHY applications and in production testing, where the same register can be written in all the PHYs using a single write transaction.

The MDC signal is an aperiodic clock provided by the station management controller (SMC). The MDIO signal receives serial data (commands) from the controller SMC, and sends serial data (status) to the SMC. The minimum time between edges of the MDC is 160 ns. There is no maximum time between edges.

The minimum cycle time (time between two consecutive rising or two consecutive falling edges) is 400 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the MDIO line is latched on the rising edge of the MDC. The frame structure and timing of the data is shown in [Figure 4.6](#) and [Figure 4.7](#).

The timing relationships of the MDIO signals are further described in [Section 6.1, "Serial Management Interface \(SMI\) Timing,"](#) on page 55.



Read Cycle

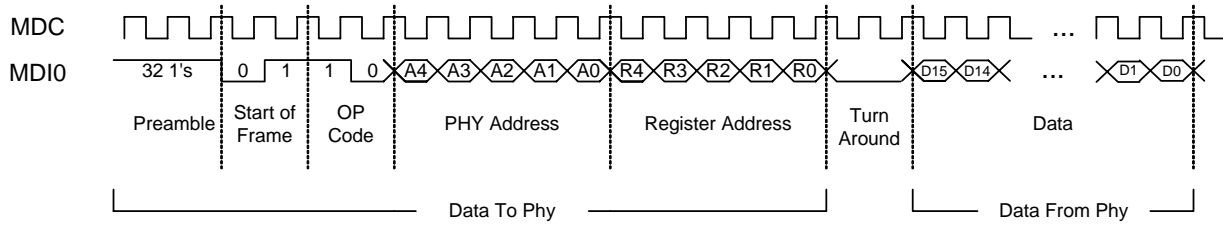


Figure 4.6 MDIO Timing and Frame Structure - READ Cycle

Write Cycle

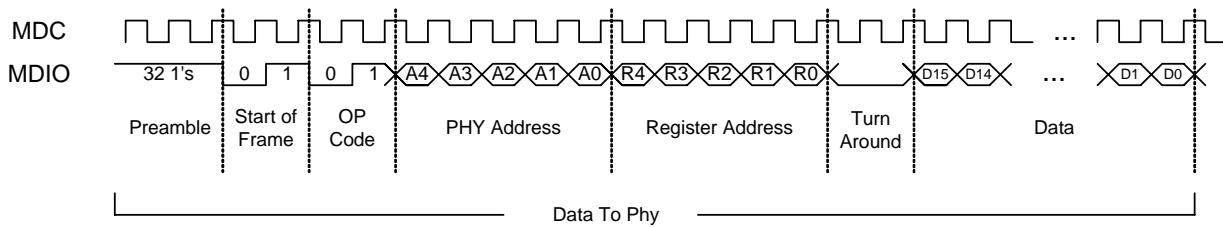


Figure 4.7 MDIO Timing and Frame Structure - WRITE Cycle

Chapter 5 Registers

Revision 1.0 (12-14-06)

±15kV ESD Protected MII/RMII Fast-Ethernet PHY with HP Auto-MDIX and SMSC flexPWR™
Datasheet

Table 5.1 Control Register: Register 0 (Basic)

| | | | | | | | | | | | | | | | |
|-------|----------|--------------|------------|------------|---------|-------------|-------------|----------------|----------|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset | Loopback | Speed Select | A/N Enable | Power Down | Isolate | Restart A/N | Duplex Mode | Collision Test | Reserved | | | | | | |

Table 5.2 Status Register: Register 1 (Basic)

| | | | | | | | | | | | | | | | |
|------------|------------------------|------------------------|----------------------|----------------------|----------|---|---|---|---|--------------|--------------|-------------|-------------|---------------|---------------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 100Base-T4 | 100Base-TX Full Duplex | 100Base-TX Half Duplex | 10Base-T Full Duplex | 10Base-T Half Duplex | Reserved | | | | | A/N Complete | Remote Fault | A/N Ability | Link Status | Jabber Detect | Extended Capability |

Table 5.3 PHY ID 1 Register: Register 2 (Extended)

| | | | | | | | | | | | | | | | |
|---|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY ID Number (Bits 3-18 of the Organizationally Unique Identifier - OUI) | | | | | | | | | | | | | | | |

Table 5.4 PHY ID 2 Register: Register 3 (Extended)

| | | | | | | | | | | | | | | | |
|--|----|----|----|----|----|---------------------------|---|---|---|---|---|------------------------------|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY ID Number (Bits 19-24 of the Organizationally Unique Identifier - OUI) | | | | | | Manufacturer Model Number | | | | | | Manufacturer Revision Number | | | |

Table 5.5 Auto-Negotiation Advertisement: Register 4 (Extended)

| | | | | | | | | | | | | | | | |
|-----------|----------|--------------|----------|-----------------|----|------------|------------------------|------------|----------------------|----------|---------------------------|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Next Page | Reserved | Remote Fault | Reserved | Pause Operation | | 100Base-T4 | 100Base-TX Full Duplex | 100Base-TX | 10Base-T Full Duplex | 10Base-T | IEEE 802.3 Selector Field | | | | |

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 DATASHEET

SMSC LAN8187/LAN8187I

Table 5.6 Auto-Negotiation Link Partner Base Page Ability Register: Register 5 (Extended)

| | | | | | | | | | | | | | | | |
|-----------|-------------|--------------|----------|----|-------|------------|------------------------|------------|----------------------|----------|---------------------------|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Next Page | Acknowledge | Remote Fault | Reserved | | Pause | 100Base-T4 | 100Base-TX Full Duplex | 100Base-TX | 10Base-T Full Duplex | 10Base-T | IEEE 802.3 Selector Field | | | | |

Table 5.7 Auto-Negotiation Expansion Register: Register 6 (Extended)

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|-----------------------|-----------------------------|----------------|---------------|-----------------------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | Parallel Detect Fault | Link Partner Next Page Able | Next Page Able | Page Received | Link Partner A/N Able |

Table 5.8 Auto-Negotiation Link Partner Next Page Transmit Register: Register 7 (Extended)

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | | | | | |

Note: Next Page capability is not supported.

Table 5.9 Register 8 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.10 Register 9 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.11 Register 10 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.12 Register 11 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.13 Register 12 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.14 Register 13 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.15 Register 14 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.16 Register 15 (Extended)

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IEEE Reserved | | | | | | | | | | | | | | | |

Table 5.17 Silicon Revision Register 16: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|------------------|---|---|---|---|----------|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | Silicon Revision | | | | | Reserved | | | | |

Table 5.18 Mode Control/ Status Register 17: Vendor-Specific

| | | | | | | | | | | | | | | | |
|------|-----------|------|---------|---------|-------------|------|--------|------|---------|------------------------|----------|----------|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RSVD | EDPWRDOWN | RSVD | LOWSQEN | MDPREBP | FARLOOPBACK | RSVD | ALTINT | RSVD | PHYADBP | Force Good Link Status | ENERGYON | Reserved | | | |

RSVD = Reserved

Table 5.19 Special Modes Register 18: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|---------|----------|----|----|----|---|---|------|---|---|-------|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | MIIMODE | Reserved | | | | | | MODE | | | PHYAD | | | | |

Table 5.20 Reserved Register 19: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | | | | | |

Table 5.21 Register 24: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | | | | | |

Table 5.22 Register 25: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | | | | | |

Table 5.23 Register 26: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | | | | | |

Table 5.24 Special Control/Status Indications Register 27: Vendor-Specific

| | | | | | | | | | | | | | | | |
|-----------|----------|-----------|----------|--------|----------|---|---|---|---|---|------|----------|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AMDIXCTRL | Reserved | CH_SELECT | Reserved | SQEOFF | Reserved | | | | | | XPOL | Reserved | | | |

Table 5.25 Special Internal Testability Control Register 28: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | | | | | | | |

Table 5.26 Interrupt Source Flags Register 29: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|------|------|------|------|------|------|------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | Reserved |

Table 5.27 Interrupt Mask Register 30: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | Mask Bits | | | | | | | Reserved |

Table 5.28 PHY Special Control/Status Register 31: Vendor-Specific

| | | | | | | | | | | | | | | | |
|----------|----|----|----------|----------|----|------|------|------|-------------|----------|------------------|---|----------|------------------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | Autodone | Reserved | | GPO2 | GPO1 | GPO0 | Enable 4B5B | Reserved | Speed Indication | | Reserved | Scramble Disable | |

5.1 SMI Register Mapping

The following registers are supported (register numbers are in decimal):

Table 5.29 SMI Register Mapping

| REGISTER # | DESCRIPTION | Group |
|------------|--|-----------------|
| 0 | Basic Control Register | Basic |
| 1 | Basic Status Register | Basic |
| 2 | PHY Identifier 1 | Extended |
| 3 | PHY Identifier 2 | Extended |
| 4 | Auto-Negotiation Advertisement Register | Extended |
| 5 | Auto-Negotiation Link Partner Ability Register | Extended |
| 6 | Auto-Negotiation Expansion Register | Extended |
| 16 | Silicon Revision Register | Vendor-specific |
| 17 | Mode Control/Status Register | Vendor-specific |
| 18 | Special Modes | Vendor-specific |
| 20 | Reserved | Vendor-specific |
| 21 | Reserved | Vendor-specific |
| 22 | Reserved | Vendor-specific |
| 23 | Reserved | Vendor-specific |
| 27 | Control / Status Indication Register | Vendor-specific |
| 28 | Reserved | Vendor-specific |
| 29 | Interrupt Source Register | Vendor-specific |
| 30 | Interrupt Mask Register | Vendor-specific |
| 31 | PHY Special Control/Status Register | Vendor-specific |

5.2 SMI Register Format

The mode key is as follows:

- RW = Read/write,
- SC = Self clearing,
- WO = Write only,
- RO = Read only,
- LH = Latch high, clear on read of register,
- LL = Latch low, clear on read of register,
- NASR = Not Affected by Software Reset
- X = Either a 1 or 0.

Table 5.30 Register 0 - Basic Control

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|-------------------------|---|-------|----------------------|
| 0.15 | Reset | 1 = software reset. Bit is self-clearing. For best results, when setting this bit do not set other bits in this register. | RW/SC | 0 |
| 0.14 | Loopback | 1 = loopback mode, 0 = normal operation | RW | 0 |
| 0.13 | Speed Select | 1 = 100Mbps, 0 = 10Mbps. Ignored if Auto Negotiation is enabled (0.12 = 1). | RW | Set by MODE[2:0] bus |
| 0.12 | Auto-Negotiation Enable | 1 = enable auto-negotiate process (overrides 0.13 and 0.8) 0 = disable auto-negotiate process | RW | Set by MODE[2:0] bus |
| 0.11 | Power Down | 1 = General power down mode, 0 = normal operation | RW | 0 |
| 0.10 | Isolate | 1 = electrical isolation of PHY from MII 0 = normal operation | RW | Set by MODE[2:0] bus |
| 0.9 | Restart Auto-Negotiate | 1 = restart auto-negotiate process 0 = normal operation. Bit is self-clearing. | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full duplex, 0 = Half duplex. Ignored if Auto Negotiation is enabled (0.12 = 1). | RW | Set by MODE[2:0] bus |
| 0.7 | Collision Test | 1 = enable COL test, 0 = disable COL test | RW | 0 |
| 0.6:0 | Reserved | | RO | 0 |

Table 5.31 Register 1 - Basic Status

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|-------------------------|--|-------|---------|
| 1.15 | 100Base-T4 | 1 = T4 able, 0 = no T4 ability | RO | 0 |
| 1.14 | 100Base-TX Full Duplex | 1 = TX with full duplex, 0 = no TX full duplex ability | RO | 1 |
| 1.13 | 100Base-TX Half Duplex | 1 = TX with half duplex, 0 = no TX half duplex ability | RO | 1 |
| 1.12 | 10Base-T Full Duplex | 1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability | RO | 1 |
| 1.11 | 10Base-T Half Duplex | 1 = 10Mbps with half duplex 0 = no 10Mbps with half duplex ability | RO | 1 |
| 1.10:6 | Reserved | | | |
| 1.5 | Auto-Negotiate Complete | 1 = auto-negotiate process completed 0 = auto-negotiate process not completed | RO | 0 |
| 1.4 | Remote Fault | 1 = remote fault condition detected 0 = no remote fault | RO/LH | 0 |

**Table 5.31 Register 1 - Basic Status (continued)**

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|------------------------|--|-----------|---------|
| 1.3 | Auto-Negotiate Ability | 1 = able to perform auto-negotiation function 0 = unable to perform auto-negotiation function | RO | 1 |
| 1.2 | Link Status | 1 = link is up, 0 = link is down | RO/ LL | 0 |
| 1.1 | Jabber Detect | 1 = jabber condition detected 0 = no jabber condition detected | RO/ LH | 0 |
| 1.0 | Extended Capabilities | 1 = supports extended capabilities registers 0 = does not support extended capabilities registers | RO | 1 |

Table 5.32 Register 2 - PHY Identifier 1

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|---------------|--|------|---------|
| 2.15:0 | PHY ID Number | Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively. OUI=00800Fh | RW | 0007h |

Table 5.33 Register 3 - PHY Identifier 2

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|-----------------|--|------|---------|
| 3.15:10 | PHY ID Number | Assigned to the 19 th through 24 th bits of the OUI. | RW | C0h |
| 3.9:4 | Model Number | Six-bit manufacturer's model number. | RW | 0Ch |
| 3.3:0 | Revision Number | Four-bit manufacturer's revision number. | RW | 3h |

Table 5.34 Register 4 - Auto Negotiation Advertisement

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|-----------------|--|------|---------|
| 4.15 | Next Page | 1 = next page capable, 0 = no next page ability This Phy does not support next page ability. | RO | 0 |
| 4.14 | Reserved | | RO | 0 |
| 4.13 | Remote Fault | 1 = remote fault detected, 0 = no remote fault | RW | 0 |
| 4.12 | Reserved | | | |
| 4.11:10 | Pause Operation | 00 = No PAUSE 01 = Asymmetric PAUSE toward link partner 10 = Symmetric PAUSE 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device | R/W | 00 |
| 4.9 | 100Base-T4 | 1 = T4 able, 0 = no T4 ability This Phy does not support 100Base-T4. | RO | 0 |

Table 5.34 Register 4 - Auto Negotiation Advertisement (continued)

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|------------------------|---|------|----------------------------|
| 4.8 | 100Base-TX Full Duplex | 1 = TX with full duplex, 0 = no TX full duplex ability | RW | Set by MODE[2:0] bus |
| 4.7 | 100Base-TX | 1 = TX able, 0 = no TX ability | RW | 1 |
| 4.6 | 10Base-T Full Duplex | 1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability | RW | Set by MODE[2:0] bus |
| 4.5 | 10Base-T | 1 = 10Mbps able, 0 = no 10Mbps ability | RW | Set by MODE[2:0] bus |
| 4.4:0 | Selector Field | [00001] = IEEE 802.3 | RW | 00001 |

Table 5.35 Register 5 - Auto Negotiation Link Partner Ability

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|------------------------|--|------|---------|
| 5.15 | Next Page | 1 = "Next Page" capable, 0 = no "Next Page" ability This Phy does not support next page ability. | RO | 0 |
| 5.14 | Acknowledge | 1 = link code word received from partner 0 = link code word not yet received | RO | 0 |
| 5.13 | Remote Fault | 1 = remote fault detected, 0 = no remote fault | RO | 0 |
| 5.12:11 | Reserved | | RO | 0 |
| 5.10 | Pause Operation | 1 = Pause Operation is supported by remote MAC, 0 = Pause Operation is not supported by remote MAC | RO | 0 |
| 5.9 | 100Base-T4 | 1 = T4 able, 0 = no T4 ability. This Phy does not support T4 ability. | RO | 0 |
| 5.8 | 100Base-TX Full Duplex | 1 = TX with full duplex, 0 = no TX full duplex ability | RO | 0 |
| 5.7 | 100Base-TX | 1 = TX able, 0 = no TX ability | RO | 0 |
| 5.6 | 10Base-T Full Duplex | 1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability | RO | 0 |
| 5.5 | 10Base-T | 1 = 10Mbps able, 0 = no 10Mbps ability | RO | 0 |
| 5.4:0 | Selector Field | [00001] = IEEE 802.3 | RO | 00001 |

**Table 5.36 Register 6 - Auto Negotiation Expansion**

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|------------------------------------|--|-----------|---------|
| 6.15:5 | Reserved | | RO | 0 |
| 6.4 | Parallel Detection Fault | 1 = fault detected by parallel detection logic 0 = no fault detected by parallel detection logic | RO/ LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = link partner has next page ability 0 = link partner does not have next page ability | RO | 0 |
| 6.2 | Next Page Able | 1 = local device has next page ability 0 = local device does not have next page ability | RO | 0 |
| 6.1 | Page Received | 1 = new page received 0 = new page not yet received | RO/ LH | 0 |
| 6.0 | Link Partner Auto-Negotiation Able | 1 = link partner has auto-negotiation ability 0 = link partner does not have auto-negotiation ability | RO | 0 |

Table 5.37 Register 16 - Silicon Revision

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|----------|------------------|---------------------------------------|------|---------|
| 16.15:10 | Reserved | | RO | 0 |
| 16.9:6 | Silicon Revision | Four-bit silicon revision identifier. | RO | 0001 |
| 16.5:0 | Reserved | | RO | 0 |

Table 5.38 Register 17 - Mode Control/Status

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|----------|-------------|---|------|---------|
| 17.15:14 | Reserved | Write as 0; ignore on read. | RW | 0 |
| 17.13 | EDPWRDOWN | Enable the Energy Detect Power-Down mode: 0 = Energy Detect Power-Down is disabled 1 = Energy Detect Power-Down is enabled | RW | 0 |
| 17.12 | Reserved | Write as 0, ignore on read | RW | 0 |
| 17.11 | LOWSQEN | The Low_Squelch signal is equal to LOWSQEN AND EDPWRDOWN. Low_Squelch = 1 implies a lower threshold (more sensitive). Low_Squelch = 0 implies a higher threshold (less sensitive). | RW | 0 |
| 17.10 | MDPREBP | Management Data Preamble Bypass: 0 – detect SMI packets with Preamble 1 – detect SMI packets without preamble | RW | 0 |
| 17.9 | FARLOOPBACK | Force the module to the FAR Loop Back mode, i.e. all the received packets are sent back simultaneously (in 100Base-TX only). This bit is only active in RMII mode. In this mode the user needs to supply a 50MHz clock to the PHY. This mode works even if MII Isolate (0.10) is set. | RW | 0 |
| 17.8:7 | Reserved | Write as 0, ignore on read. | RW | 00 |

Table 5.38 Register 17 - Mode Control/Status (continued)

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|------------------------|---|------|---------|
| 17.6 | ALTINT | Alternat Interrupt Mode. 0 = Primary interrupt system enabled (Default). 1 = Alternate interrupt system enabled. See Section 5.3, "Interrupt Management," on page 49. | RW | 0 |
| 17.5:4 | Reserved | Write as 0, ignore on read. | RW | 00 |
| 17.3 | PHYADBP | 1 = PHY disregards PHY address in SMI access write. | RW | 0 |
| 17.2 | Force Good Link Status | 0 = normal operation; 1 = force 100TX- link active; Note: This bit should be set only during lab testing | RW | 0 |
| 17.1 | ENERGYON | ENERGYON – indicates whether energy is detected on the line (see Section 5.4.5.2, "Energy Detect Power-Down," on page 51); it goes to "0" if no valid energy is detected within 256ms. Reset to "1" by hardware reset, unaffected by SW reset. | RO | 1 |
| 17.0 | Reserved | Write as 0, ignore on read. | RW | 0 |

Table 5.39 Register 18 - Special Modes

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|----------|----------|---|-------------|--------------------------------------|
| 18.15:14 | MIIMODE | MII Mode: set the mode of the MII: 0 – MII interface. 1 – RMII interface | RW, NASR | |
| 18.13:8 | Reserved | Write as 0, ignore on read. | RW, NASR | 000000 |
| 18.7:5 | MODE | PHY Mode of operation. Refer to Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 53 for more details. | RW, NASR | XXX EVB8700 default 111 |
| 18.4:0 | PHYAD | PHY Address. The PHY Address is used for the SMI address and for the initialization of the Cipher (Scrambler) key. Refer to Section 5.4.9.1, "Physical Address Bus - PHYAD[4:0]," on page 53 for more details. | RW, NASR | PHYAD EVB8700 default 11111 |

Table 5.40 Register 27 - Special Control/Status Indications

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|-------------|--|------|---------|
| 27.15 | AMDIXIOCTRL | Enables the external AMDIX and CH_SELECT pins 0 - External pins AMDIX_EN and CH_SELECT control the AMDIX. 1 - Internal bits 27.14 and 27.13 control the AMDIX. Note: Please see Table 4.3, "Auto-MDIX Control," on page 30 | RW | 0 |

**Table 5.40 Register 27 - Special Control/Status Indications (continued)**

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|--------------|--|-------------|---------|
| 27.14 | AMDIX_ENABLE | HP Auto-MDIX control 0 - Auto-MDIX disabled (use 27.13 to control channel) 1 - Auto-MDIX enable Note: This bit can only be used if 27.15 is a 1. | RW | 0 |
| 27.13 | CH_SELECT | Manual Channel Select 0 - MDI -TX transmits RX receives 1 - MDIX -TX receives RX transmits Note: This bit can only be used if 27.15 is a 1 and 27.14 is a 0. | RW | 0 |
| 27.12 | Reserved | Write as 0. Ignore on read. | RW | 0 |
| 27:11 | SQEOFF | Disable the SQE (Signal Quality Error) test (Heartbeat): 0 - SQE test is enabled. 1 - SQE test is disabled. | RW, NASR | 0 |
| 27.10:5 | Reserved | Write as 0. Ignore on read. | RW | 000000 |
| 27.4 | XPOL | Polarity state of the 10Base-T: 0 - Normal polarity 1 - Reversed polarity | RO | 0 |
| 27.3:0 | Reserved | Reserved | RO | XXXXb |

Table 5.41 Register 28 - Special Internal Testability Controls

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|----------|--|------|---------|
| 28.15:0 | Reserved | Do not write to this register. Ignore on read. | RW | N/A |

Table 5.42 Register 29 - Interrupt Source Flags

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|----------|--|-----------|---------|
| 29.15:8 | Reserved | Ignore on read. | RO/ LH | 0 |
| 29.7 | INT7 | 1 = ENERGYON generated 0 = not source of interrupt | RO/ LH | X |
| 29.6 | INT6 | 1 = Auto-Negotiation complete 0 = not source of interrupt | RO/ LH | X |
| 29.5 | INT5 | 1 = Remote Fault Detected 0 = not source of interrupt | RO/ LH | X |
| 29.4 | INT4 | 1 = Link Down (link status negated) 0 = not source of interrupt | RO/ LH | X |
| 29.3 | INT3 | 1 = Auto-Negotiation LP Acknowledge 0 = not source of interrupt | RO/ LH | X |
| 29.2 | INT2 | 1 = Parallel Detection Fault 0 = not source of interrupt | RO/ LH | X |

Table 5.42 Register 29 - Interrupt Source Flags (continued)

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|----------|---|-----------|---------|
| 29.1 | INT1 | 1 = Auto-Negotiation Page Received 0 = not source of interrupt | RO/ LH | X |
| 29.0 | Reserved | Ignore on read. | RO/ LH | 0 |

Table 5.43 Register 30 - Interrupt Mask

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|-----------|---|------|---------|
| 30.15:8 | Reserved | Write as 0; ignore on read. | RO | 0 |
| 30.7:0 | Mask Bits | 1 = interrupt source is enabled 0 = interrupt source is masked | RW | 0 |

Table 5.44 Register 31 - PHY Special Control/Status

| ADDRESS | NAME | DESCRIPTION | MODE | DEFAULT |
|---------|------------------|---|------|---------|
| 31.15 | Reserved | Do not write to this register. Ignore on read. | RW | 0 |
| 31.14 | Reserved | | | |
| 31.13 | Reserved | Must be set to 0 | RW | 0 |
| 31.12 | Autodone | Auto-negotiation done indication: 0 = Auto-negotiation is not done or disabled (or not active) 1 = Auto-negotiation is done | RO | 0 |
| 31.11 | Reserved | Write as 0, ignore on Read. | RW | X |
| 31.10 | Reserved | Reserved | RW | 0 |
| 31.9:7 | GPO[2:0] | General Purpose Output connected to signals GPO[2:0] | RW | 0 |
| 31.6 | Enable 4B5B | 0 = Bypass encoder/decoder. 1 = enable 4B5B encoding/decoding. MAC Interface must be configured in MII mode. | RW | 1 |
| 31.5 | Reserved | Write as 0, ignore on Read. | RW | 0 |
| 31.4:2 | Speed Indication | HCDSPEED value: [001]=10Mbps Half-duplex [101]=10Mbps Full-duplex [010]=100Base-TX Half-duplex [110]=100Base-TX Full-duplex | RO | 000 |
| 31.1 | Reserved | Write as 0; ignore on Read | RW | 0 |
| 31.0 | Scramble Disable | 0 = enable data scrambling 1 = disable data scrambling, | RW | 0 |



5.3 Interrupt Management

The Management interface supports an interrupt capability that is not a part of the IEEE 802.3 specification. It generates an active low asynchronous interrupt signal on the nINT output whenever certain events are detected as setup by the Interrupt Mask Register 30.

The Interrupt system on the SMSC LAN8187/8187I has two modes, a Primary Interrupt mode and an Alternative Interrupt mode. Both systems will assert the nINT pin low when the corresponding mask bit is set, the difference is how they de-assert the output interrupt signal nINT.

The Primary interrupt mode is the default interrupt mode after a power-up or hard reset, the Alternative interrupt mode would need to be setup again after a power-up or hard reset.

5.3.1 Primary Interrupt System

The Primary Interrupt system is the default interrupt mode, (Bit 17.6 = '0'). The Primary Interrupt System is always selected after power-up or hard reset.

To set an interrupt, set the corresponding mask bit in the interrupt Mask register 30 (see [Table 5.45](#)). Then when the event to assert nINT is true, the nINT output will be asserted.

When the corresponding Event to De-Assert nINT is true, then the nINT will be de-asserted.

Table 5.45 Interrupt Management Table.

| Mask | Interrupt Source Flag | | Interrupt Source | | Event to Assert nINT | Event to De-Assert nINT |
|------|-----------------------|---------------------------------|------------------|--------------------------|--------------------------|--|
| 30.7 | 29.7 | ENERGYON | 17.1 | ENERGYON | Rising 17.1 ^a | Falling 17.1 or Reading register 29 |
| 30.6 | 29.6 | Auto-Negotiation complete | 1.5 | Auto-Negotiate Complete | Rising 1.5 | Falling 1.5 or Reading register 29 |
| 30.5 | 29.5 | Remote Fault Detected | 1.4 | Remote Fault | Rising 1.4 | Falling 1.4, or Reading register 1 or Reading register 29 |
| 30.4 | 29.4 | Link Down | 1.2 | Link Status | Falling 1.2 | Reading register 1 or Reading register 29 |
| 30.3 | 29.3 | Auto-Negotiation LP Acknowledge | 5.14 | Acknowledge | Rising 5.14 | Falling 5.14 or Read register 29 |
| 30.2 | 29.2 | Parallel Detection Fault | 6.4 | Parallel Detection Fault | Rising 6.4 | Falling 6.4 or Reading register 6, or Reading register 29 or Re-AutoNegotaite or Link down |
| 30.1 | 29.1 | Auto-Negotiation Page Received | 6.1 | Page Received | Rising 6.1 | Falling of 6.1 or Reading register 6, or Reading register 29 Re-AutoNegotatie, or Link Down. |

- a. If the mask bit is enabled and nINT has been de-asserted while ENERGYON is still high, nINT will assert for 256 ms, approximately one second after ENERGYON goes low when the Cable is unplugged. To prevent an unexpected assertion of nINT, the ENERGYON interrupt mask should always be cleared as part of the ENERGYON interrupt service routine.

Note: The ENERGYON bit 17.1 is defaulted to a '1' at the start of the signal acquisition process, therefore the Interrupt source flag 29.7 will also read as a '1' at power-up. If no signal is present, then both 17.1 and 29.7 will clear within a few milliseconds.

5.3.2 Alternate Interrupt System

The Alternative method is enabled by writing a '1' to 17.6 (ALTINT).

To set an interrupt, set the corresponding bit of the in the Mask Register 30, (see [Table 5.46](#)).

To Clear an interrupt, either clear the corresponding bit in the Mask Register (30), this will de-assert the nINT output, or Clear the Interrupt Source, and write a '1' to the corresponding Interrupt Source Flag. Writing a '1' to the Interrupt Source Flag will cause the state machine to check the Interrupt Source to determine if the Interrupt Source Flag should clear or stay as a '1'. If the Condition to De-Assert is true, then the Interrupt Source Flag is cleared, and the nINT is also de-asserted. If the Condition to De-Assert is false, then the Interrupt Source Flag remains set, and the nINT remains asserted.

Table 5.46 Alternative Interrupt System Management Table.

| Mask | Interrupt Source Flag | | Interrupt Source | | Event to Assert nINT | Condition to De-Assert. | Bit to Clear nINT |
|------|-----------------------|---------------------------------|------------------|--------------------------|----------------------|-------------------------|-------------------|
| 30.7 | 29.7 | ENERGYON | 17.1 | ENERGYON | Rising 17.1 | 17.1 low | 29.7 |
| 30.6 | 29.6 | Auto-Negotiation complete | 1.5 | Auto-Negotiate Complete | Rising 1.5 | 1.5 low | 29.6 |
| 30.5 | 29.5 | Remote Fault Detected | 1.4 | Remote Fault | Rising 1.4 | 1.4 low | 29.5 |
| 30.4 | 29.4 | Link Down | 1.2 | Link Status | Falling 1.2 | 1.2 high | 29.4 |
| 30.3 | 29.3 | Auto-Negotiation LP Acknowledge | 5.14 | Acknowledge | Rising 5.14 | 5.14 low | 29.3 |
| 30.2 | 29.2 | Parallel Detection Fault | 6.4 | Parallel Detection Fault | Rising 6.4 | 6.4 low | 29.2 |
| 30.1 | 29.1 | Auto-Negotiation Page Received | 6.1 | Page Received | Rising 6.1 | 6.1 low | 29.1 |

Note: The ENERGYON bit 17.1 is defaulted to a '1' at the start of the signal acquisition process, therefore the Interrupt source flag 29.7 will also read as a '1' at power-up. If no signal is present, then both 17.1 and 29.7 will clear within a few milliseconds.

5.3.2.1 Example Alternative Interrupts system

For example 30.7 is set to '1' to enable the ENERGYON interrupt. After a cable is plugged in, ENERGYON (17.1) goes active and nINT will be asserted low.

To de-assert the nINT interrupt output, either.

1. Clear the ENERGYON bit (17.1), by removing the cable, then writing a '1' to register 29.7.
- Or

2. Clear the Mask bit 30.1

5.4 Miscellaneous Functions

5.4.1 Carrier Sense

The carrier sense is output on CRS. CRS is a signal defined by the MII specification in the IEEE 802.3u standard. The PHY asserts CRS based only on receive activity whenever the PHY is either in repeater mode or full-duplex mode. Otherwise the PHY asserts CRS based on either transmit or receive activity.

The carrier sense logic uses the encoded, unscrambled data to determine carrier activity status. It activates carrier sense with the detection of 2 non-contiguous zeros within any 10 bit span. Carrier sense terminates if a span of 10 consecutive ones is detected before a /J/K/ Start-of Stream Delimiter pair. If an SSD pair is detected, carrier sense is asserted until either /T/R/ End-of-Stream Delimiter pair or a pair of IDLE symbols is detected. Carrier is negated after the /T/ symbol or the first IDLE. If /T/ is not followed by /R/, then carrier is maintained. Carrier is treated similarly for IDLE followed by some non-IDLE symbol.

5.4.2 Collision Detect

A collision is the occurrence of simultaneous transmit and receive operations. The COL output is asserted to indicate that a collision has been detected. COL remains active for the duration of the collision. COL is changed asynchronously to both RX_CLK and TX_CLK. The COL output becomes inactive during full duplex mode.

COL may be tested by setting register 0, bit 7 high. This enables the collision test. COL will be asserted within 512 bit times of TX_EN rising and will be de-asserted within 4 bit times of TX_EN falling.

In 10M mode, COL pulses for approximately 10 bit times (1us), 2us after each transmitted packet (de-assertion of TX_EN). This is the Signal Quality Error (SQE) signal and indicates that the transmission was successful. The user can disable this pulse by setting bit 11 in register 27.

5.4.3 Isolate Mode

The PHY data paths may be electrically isolated from the MII by setting register 0, bit 10 to a logic one. In isolation mode, the PHY does not respond to the TXD, TX_EN and TX_ER inputs. The PHY still responds to management transactions.

Isolation provides a means for multiple PHYs to be connected to the same MII without contention occurring. The PHY is not isolated on power-up (bit 0:10 = 0).

5.4.4 Link Integrity Test

The LAN8187/LAN8187I performs the link integrity test as outlined in the IEEE 802.3u (Clause 24-15) Link Monitor state diagram. The link status is multiplexed with the 10Mbps link status to form the reportable link status bit in Serial Management Register 1, and is driven to the LINK LED.

The DSP indicates a valid MLT-3 waveform present on the RXP and RXN signals as defined by the ANSI X3.263 TP-PMD standard, to the Link Monitor state-machine, using internal signal called DATA_VALID. When DATA_VALID is asserted the control logic moves into a Link-Ready state, and waits for an enable from the Auto Negotiation block. When received, the Link-Up state is entered, and the Transmit and Receive logic blocks become active. Should Auto Negotiation be disabled, the link integrity logic moves immediately to the Link-Up state, when the DATA_VALID is asserted.

Note that to allow the line to stabilize, the link integrity logic will wait a minimum of 330 μsec from the time DATA_VALID is asserted until the Link-Ready state is entered. Should the DATA_VALID input be negated at any time, this logic will immediately negate the Link signal and enter the Link-Down state.

When the 10/100 digital block is in 10Base-T mode, the link status is from the 10Base-T receiver logic.

5.4.5 Power-Down modes

There are 2 power-down modes for the Phy:

5.4.5.1 General Power-Down

This power-down is controlled by register 0, bit 11. In this mode the entire PHY, except the management interface, is powered-down and stays in that condition as long as bit 0.11 is HIGH. When bit 0.11 is cleared, the PHY powers up and is automatically reset.

5.4.5.2 Energy Detect Power-Down

This power-down mode is activated by setting bit 17.13 to 1. In this mode when no energy is present on the line the PHY is powered down, except for the management interface, the SQUELCH circuit and the ENERGYON logic. The ENERGYON logic is used to detect the presence of valid energy from 100Base-TX, 10Base-T, or Auto-negotiation signals

In this mode, when the ENERGYON signal is low, the PHY is powered-down, and nothing is transmitted. When energy is received - link pulses or packets - the ENERGYON signal goes high, and

the PHY powers-up. It automatically resets itself into the state it had prior to power-down, and asserts the nINT interrupt if the ENERGYON interrupt is enabled. The first and possibly the second packet to activate ENERGYON may be lost.

When 17.13 is low, energy detect power-down is disabled.

5.4.6 Reset

The PHY has 3 reset sources:

Hardware reset (HWRST): connected to the nRST input, and to the internal POR signal.

If the nRST input is driven by an external source, it should be held LOW for at least 100 us to ensure that the Phy is properly reset.

The Phy has an internal Power-On-Reset (POR) signal which is asserted for 21ms following a VDD33 (+3.3V) and VDDCORE (+1.8V) power-up. This internal POR is internally “OR”-ed with the nRST input.

During a Hardware reset, either external or POR, an external clock **must** be supplied to the CLKIN signal.

Software (SW) reset: Activated by writing register 0, bit 15 high. This signal is self-clearing. After the register-write, internal logic extends the reset by 256µs to allow PLL-stabilization before releasing the logic from reset.

The IEEE 802.3u standard, clause 22 (22.2.4.1.1) states that the reset process should be completed within 0.5s from the setting of this bit.

Power-Down reset: Automatically activated when the PHY comes out of power-down mode. The internal power-down reset is extended by 256µs after exiting the power-down mode to allow the PLLs to stabilize before the logic is released from reset.

These 3 reset sources are combined together in the digital block to create the internal “general reset”, SYSRST, which is an asynchronous reset and is active HIGH. This SYSRST directly drives the PCS, DSP and MII blocks. It is also input to the Central Bias block in order to generate a short reset for the PLLs.

The SMI mechanism and registers are reset only by the Hardware and Software resets. During Power-Down, the SMI registers are not reset. Note that some SMI register bits are not cleared by Software reset – these are marked “NASR” in the register tables.

For the first 16us after coming out of reset, the MII will run at 2.5 MHz. After that it will switch to 25 MHz if auto-negotiation is enabled.

5.4.7 LED Description

The PHY provides four LED signals. These provide a convenient means to determine the mode of operation of the Phy. All LED signals are either active high or active low.

The four LED signals can be either active-high or active-low. Polarity depends upon the Phy address latched in on reset. The LAN8187/LAN8187I senses each Phy address bit and changes the polarity of the LED signal accordingly. If the address bit is set as level “1”, the LED polarity will be set to an active-low. If the address bit is set as level “0”, the LED polarity will be set to an active-high.

The ACTIVITY LED output is driven active when CRS is active (high). When CRS becomes inactive, the Activity LED output is extended by 128ms.

The LINK LED output is driven active whenever the PHY detects a valid link. The use of the 10Mbps or 100Mbps link test status is determined by the condition of the internally determined speed selection.

The SPEED100 LED output is driven active when the operating speed is 100Mbit/s or during Auto-negotiation. This LED will go inactive when the operating speed is 10Mbit/s or during line isolation (register 31 bit 5).



The Full-Duplex LED output is driven active low when the link is operating in Full-Duplex mode.

5.4.8 Loopback Operation

The 10/100 digital has two independent loop-back modes: Internal loopback and far loopback.

5.4.8.1 Internal Loopback

The internal loopback mode is enabled by setting bit register 0 bit 14 to logic one. In this mode, the scrambled transmit data (output of the scrambler) is looped into the receive logic (input of the descrambler). The COL signal will be inactive in this mode, unless collision test (bit 0.7) is active.

In this mode, during transmission (TX_EN is HIGH), nothing is transmitted to the line and the transmitters are powered down.

5.4.9 Configuration Signals

The PHY has 11 configuration signals whose inputs should be driven continuously, either by external logic or external pull-up/pull-down resistors.

5.4.9.1 Physical Address Bus - PHYAD[4:0]

The PHYAD[4:0] signals are driven high or low to give each PHY a unique address. This address is latched into an internal register at end of hardware reset. In a multi-PHY application (such as a repeater), the controller is able to manage each PHY via the unique address. Each PHY checks each management data frame for a matching address in the relevant bits. When a match is recognized, the PHY responds to that particular frame. The PHY address is also used to seed the scrambler. In a multi-PHY application, this ensures that the scramblers are out of synchronization and disperses the electromagnetic radiation across the frequency spectrum.

5.4.9.2 Mode Bus – MODE[2:0]

The MODE[2:0] bus controls the configuration of the 10/100 digital block.

Table 5.47 MODE[2:0] Bus

| MODE[2:0] | MODE DEFINITIONS | DEFAULT REGISTER BIT VALUES | |
|-----------|--|-----------------------------|------------|
| | | REGISTER 0 | REGISTER 4 |
| | | [13,12,10,8] | [8,7,6,5] |
| 000 | 10Base-T Half Duplex. Auto-negotiation disabled. | 0000 | N/A |
| 001 | 10Base-T Full Duplex. Auto-negotiation disabled. | 0001 | N/A |
| 010 | 100Base-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive. | 1000 | N/A |
| 011 | 100Base-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive. | 1001 | N/A |
| 100 | 100Base-TX Half Duplex is advertised. Auto-negotiation enabled. CRS is active during Transmit & Receive. | 1100 | 0100 |
| 101 | Repeater mode. Auto-negotiation enabled. 100Base-TX Half Duplex is advertised. CRS is active during Receive. | 1100 | 0100 |
| 110 | Power Down mode. In this mode the PHY wake-up in Power-Down mode. | N/A | N/A |

Table 5.47 MODE[2:0] Bus (continued)

| MODE[2:0] | MODE DEFINITIONS | DEFAULT REGISTER BIT VALUES | |
|-----------|--|-----------------------------|------------|
| | | REGISTER 0 | REGISTER 4 |
| | | [13,12,10,8] | [8,7,6,5] |
| 111 | All capable. Auto-negotiation enabled. | X10X | 1111 |

Chapter 6 AC Electrical Characteristics

The timing diagrams and limits in this section define the requirements placed on the external signals of the Phy.

6.1 Serial Management Interface (SMI) Timing

The Serial Management Interface is used for status and control as described in [Section 4.13](#).

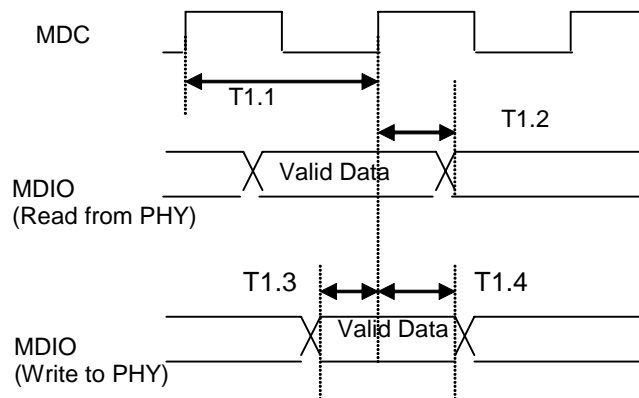


Figure 6.1 SMI Timing Diagram

Table 6.1 SMI Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|---------------------------|-----|-----|-----|-------|-------|
| T1.1 | MDC minimum cycle time | 400 | | | ns | |
| T1.2 | MDC to MDIO (Write) delay | 0 | | 300 | ns | |
| T1.3 | MDIO (Read) to MDC setup | 10 | | | ns | |
| T1.4 | MDIO (Read) to MDC hold | 10 | | | ns | |

6.2 MII 10/100Base-TX/RX Timings

6.2.1 MII 100Base-T TX/RX Timings

6.2.1.1 100M MII Receive Timing

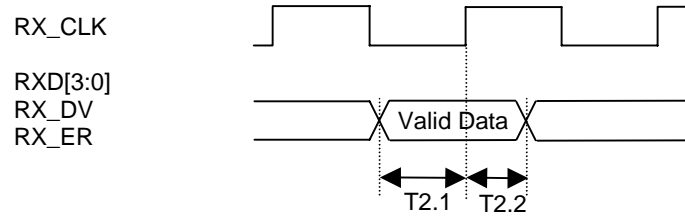


Figure 6.2 100M MII Receive Timing Diagram

Table 6.2 100M MII Receive Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|---|-----|-----|-----|-------|-------|
| T2.1 | Receive signals setup to RX_CLK rising | 10 | | | ns | |
| T2.2 | Receive signals hold from RX_CLK rising | 10 | | | ns | |
| | RX_CLK frequency | | 25 | | MHz | |
| | RX_CLK Duty-Cycle | | 40 | | % | |

6.2.1.2 100M MII Transmit Timing

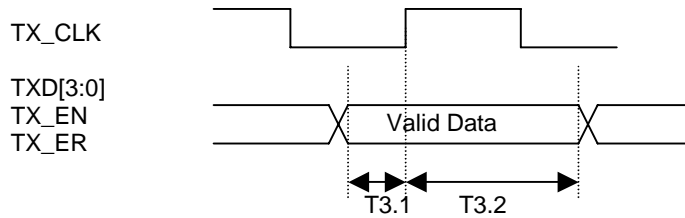


Figure 6.3 100M MII Transmit Timing Diagram

Table 6.3 100M MII Transmit Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|---|-----|-----|-----|-------|-------|
| T3.1 | Transmit signals setup to TX_CLK rising | 12 | | | ns | |
| T3.2 | Transmit signals hold after TX_CLK rising | 0 | | | ns | |
| | TX_CLK frequency | | 25 | | MHz | |
| | TX_CLK Duty-Cycle | | 40 | | % | |

6.2.2 MII 10Base-T TX/RX Timings

6.2.2.1 10M MII Receive Timing

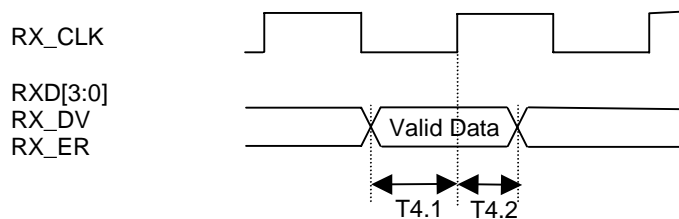
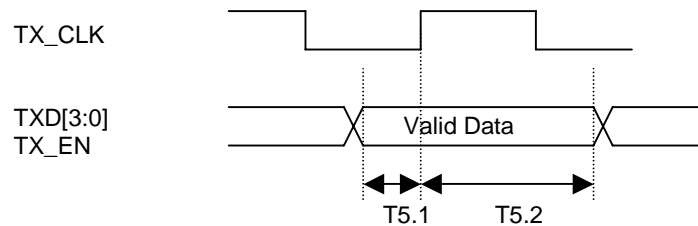


Figure 6.4 10M MII Receive Timing Diagram

Table 6.4 10M MII Receive Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|---|-----|-----|-----|-------|-------|
| T4.1 | Receive signals setup to RX_CLK rising | 10 | | | ns | |
| T4.2 | Receive signals hold from RX_CLK rising | 10 | | | ns | |
| | RX_CLK frequency | | 25 | | MHz | |
| | RX_CLK Duty-Cycle | | 40 | | % | |
| | Receive signals setup to RX_CLK rising | 10 | | | ns | |

6.2.2.2 10M MII Transmit Timing


Figure 6.5 10M MII Transmit Timing Diagrams
Table 6.5 10M MII Transmit Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|---|-----|-----|-----|-------|-------|
| T5.1 | Transmit signals setup to TX_CLK rising | 12 | | | ns | |
| T5.2 | Transmit signals hold after TX_CLK rising | | | 0 | ns | |
| | TX_CLK frequency | | 2.5 | | MHz | |
| | TX_CLK Duty-Cycle | | 50 | | % | |

6.3 RMII 10/100Base-TX/RX Timings

6.3.1 RMII 100Base-T TX/RX Timings

6.3.1.1 100M RMII Receive Timing

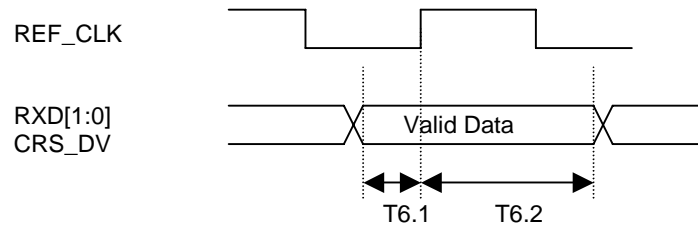


Figure 6.6 100M RMII Receive Timing Diagram

Table 6.6 100M RMII Receive Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|--|-----|-----|-----|-------|-------|
| T6.1 | Rising edge of REF_CLK to receive signals output valid | 4 | | | ns | |
| T6.2 | Rising edge of REF_CLK to receive signals output not valid | 2 | | | ns | |
| | REF_CLK frequency | | 50 | | MHz | |

6.3.1.2 100M RMII Transmit Timing

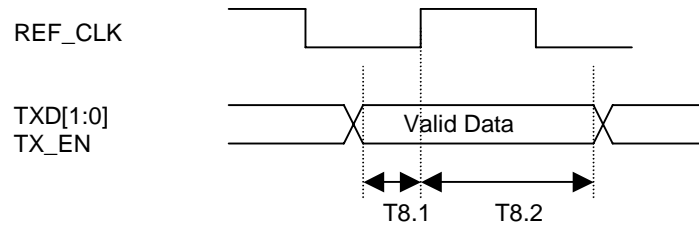


Figure 6.7 100M RMII Transmit Timing Diagram

Table 6.7 100M RMII Transmit Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|--|-----|-----|-----|-------|-------|
| T8.1 | Transmit signals setup to rising edge of REF_CLK | 4 | | | ns | |
| T8.2 | Transmit signals hold after rising edge of REF_CLK | | | 2 | ns | |
| | REF_CLK frequency | | 50 | | MHz | |

6.3.2 RMII 10Base-T TX/RX Timings

6.3.2.1 10M RMII Receive Timing

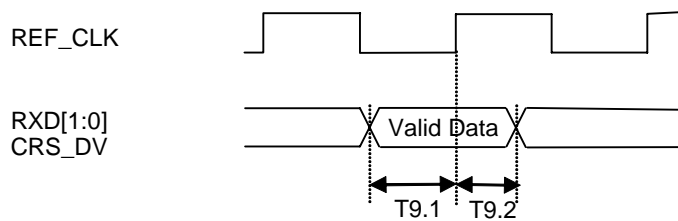
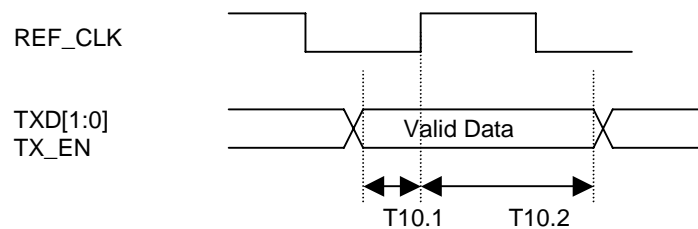


Figure 6.8 10M RMII Receive Timing Diagram

Table 6.8 10M RMII Receive Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|--|-----|-----|-----|-------|-------|
| T9.1 | Rising edge of REF_CLK to receive signals output valid | 4 | | | ns | |
| T9.2 | Rising edge of REF_CLK to receive signals output not valid | 2 | | | ns | |
| | REF_CLK frequency | | 50 | | MHz | |

6.3.2.2 10M RMII Transmit Timing**Figure 6.9 10M RMII Transmit Timing Diagram****Table 6.9 10M RMII Transmit Timing Values**

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|--|-----|-----|-----|-------|-------|
| T10.1 | Transmit signals setup to REF_CLK rising | 4 | | | ns | |
| T10.2 | Transmit signals hold after REF_CLK rising | | | 2 | ns | |

6.4 REF_CLK Timing**Table 6.10 REF_CLK Timing Values**

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|-------------------------|-----|-----|--------|-------|---------------|
| | REF_CLK frequency | | 50 | | MHz | |
| | REF_CLK Frequency Drift | | | +/- 50 | ppm | |
| | REF_CLK Duty Cycle | 40 | | 60 | % | |
| | REF_CLK Jitter | | | 150 | psec | p-p – not RMS |

6.5 Reset Timing

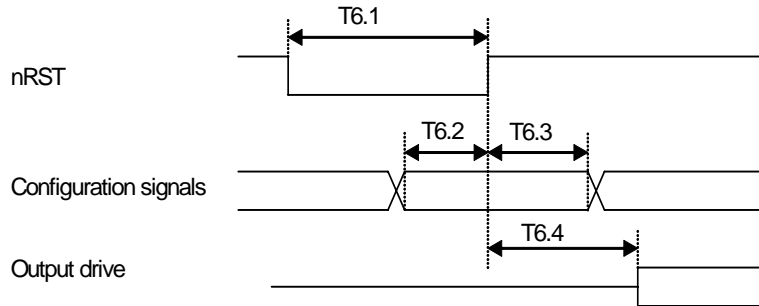


Figure 6.10 Reset Timing Diagram

Table 6.11 Reset Timing Values

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|-----------|--|-----|-----|-----|-------|---|
| T6.1 | Reset Pulse Width | 100 | | | us | |
| T6.2 | Configuration input setup to nRST rising | 200 | | | ns | |
| T6.3 | Configuration input hold after nRST rising | 400 | | | ns | |
| T6.4 | Output Drive after nRST rising | 20 | | 800 | ns | 20 clock cycles for 25 MHz clock or 40 clock cycles for 50MHz clock |

Chapter 7 DC Electrical Characteristics

7.1 DC Characteristics

7.1.1 Maximum Guaranteed Ratings

Stresses beyond those listed in [Table 7.1](#) may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7.1 Maximum Conditions.

| Parameter | Conditions | MIN | TYP | MAX | UNITS | Comment |
|-----------------------|-------------------------------|------|-----|------|-------|--|
| VDD33,VDDIO | Power pins to all other pins. | -0.5 | | +3.6 | V | |
| Digital IO | To VSS ground | -0.5 | | +3.6 | V | Table 7.5, "MII Bus Interface Signals," on page 66 |
| VSS | VSS to all other pins | -0.5 | | +4.0 | V | |
| Operating Temperature | LAN8187-JT | 0 | | +70 | C | Commercial temperature parts. |
| Operating Temperature | LAN8187I-JT | -40 | | +85 | C | Industrial temperature parts. |
| Storage Temperature | | -55 | | +150 | C | |

Table 7.2 ESD and LATCH-UP Performance

| Parameter | Conditions | MIN | TYP | MAX | UNITS | Comments |
|-----------------------------|--------------------------------|-----|-----|-------|-------|----------|
| ESD PERFORMANCE | | | | | | |
| All Pins | Human Body Model | | | +/-8 | kV | |
| All Pins | IED61000-4-2 Contact Discharge | | | +/-8 | kV | |
| All Pins | IEC61000-4-2 Air-gap Discharge | | | +/-15 | kV | |
| LATCH-UP PERFORMANCE | | | | | | |
| All Pins | EIA/JESD 78, Class II | | | 100 | mA | |

7.1.1.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand the ESD strikes like those that occur during handling and manufacturing. The device must work normally after the stress has ended, meaning no latch-up on any pins. All pins on the LAN8187 provide +/- 8kV HBM protection.

7.1.1.2 IEC61000-4-2 Performance

The IEC61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. In contrast, the HBM ESD tests are performed at the device level with the device powered down.

In addition to defining the ESD tests, IEC 61000-4-2 also categorizes the impact to equipment operation when the strike occurs (ESD Result Classification). The LAN8187 maintains an ESD Result Classification 1 or 2 when subjected to an IEC 61000-4-2 (level 4) ESD strike.

Both air discharge and contact discharge test techniques for applying stress conditions are defined by the IEC61000-4-2 ESD document.

AIR DISCHARGE

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. All pins of the LAN8187 can safely dissipate +/- 15kV air discharges per the IEC61000-4-2 specification without additional board level protection. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

CONTACT DISCHARGE

The uncharged electrode first contacts the pin to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. All pins of the LAN8187 can safely dissipate +/- 8kV contact discharges per the IEC61000-4-2 specification without the need for additional board level protection.

7.1.2 Operating Conditions

Table 7.3 Recommended Operating Conditions

| Parameter | Conditions | MIN | TYP | MAX | UNIT | Comment |
|---------------------------------------|------------------------------|-----|-----|--------|------|----------------------------|
| VDD33 | VDD33 to VSS | 3.0 | 3.3 | 3.6 | V | |
| INPUT VOLTAGE ON DIGITAL PINS | | 0.0 | | VDD IO | V | |
| VOLTAGE ON ANALOG I/O PINS (RXP, RXN) | | 0.0 | | +3.6 V | V | |
| AMBIENT TEMPERATURE | T _A LAN8187-JT | 0 | | 70 | C | For Commercial Temperature |
| | T _A LAN8187I-AEZG | -40 | | +85 | C | For Industrial Temperature |

7.1.3 Power Consumption

7.1.3.1 Power Consumption Device Only

Power measurements taken over the operating conditions specified. See [Section 5.4.5](#) for a description of the power down modes



Table 7.4 Power Consumption Device Only

| POWER PIN GROUP | | 3.3V POWER PIN(MA) | 1.8V POWER PINS(MA) | VDDIO POWER PIN | TOTAL CURRENT (MA) | TOTAL POWER (MW) |
|--------------------------|---------|--------------------------|---------------------------|-----------------------|--------------------------|------------------------|
| 100BASE-T /W TRAFFIC | Max | 35.6 | 41.3 | 4.7 | 81.6 | 269.28 |
| | Typical | 33.3 | 37.4 | 4.1 | 74.8 | 246.84 |
| | Min | 31.3 | 33.4 | 1.3 | 66 | 165.75 ^a |
| 10BASE-T /W TRAFFIC | Max | 15.6 | 22.3 | 1.1 | 39 | 128.7 |
| | Typical | 15.3 | 20.8 | 0.9 | 37 | 122.1 |
| | Min | 14.9 | 19.1 | 0.1 | 34.1 | 83.88 ^b |
| ENERGY DETECT POWER DOWN | Max | 10.5 | 3.3 | 0.5 | 13.85 | 45.7 |
| | Typical | 9.9 | 2.7 | 0.4 | 13.0 | 42.9 |
| | Min | 9.8 | 2.3 | 0.3 | 12.4 | 37.02 ^c |
| GENERAL POWER DOWN | Max | 0.21 | 2.92 | 0.39 | 3.52 | 11.62 |
| | Typical | 0.124 | 2.6 | 0.345 | 3.07 | 10.131 |
| | Min | 0.038 | 2.1 | 0.3 | 2.44 | 4.4454 ^d |

- a. This is calculated with full SMSC FlexPWR features activated: VDDIO = 1.8V and internal regulator disabled.
- b. This is calculated with full SMSC FlexPWR features activated: VDDIO = 1.8V and internal regulator disabled.
- c. This is calculated with full SMSC FlexPWR features activated: VDDIO = 1.8V and internal regulator disabled.
- d. This is calculated with full SMSC FlexPWR features activated: VDDIO = 1.8V and internal regulator disabled.

Note 7.1 Current measurements do not include power applied to the magnetics or the optional external LEDs. Current measurements taken with VDDIO = +3.3V, unless otherwise indicated.

7.1.4 DC Characteristics - Input and Output Buffers

Table 7.5 MII Bus Interface Signals

| NAME | V _{IH} | V _{IL} | I _{OH} | I _{OL} | V _{OL} | V _{OH} |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| TXD0 | VDDIO – +0.4 V | +0.5 V | | | | |
| TXD1 | VDDIO – +0.4 V | +0.5 V | | | | |
| TXD2 | VDDIO – +0.4 V | +0.5 V | | | | |
| TXD3 | VDDIO – +0.4 V | +0.5 V | | | | |
| TX_EN | VDDIO – +0.4 V | +0.5 V | | | | |
| TX_CLK | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RXD0 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RXD1 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RXD2 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RXD3 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RX_ER/RXD4 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RX_DV | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| RX_CLK | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| CRS | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| COL | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| MDC | VDDIO – +0.4 V | +0.5 V | | | | |
| MDIO | VDDIO – +0.4 V | +0.5 V | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| nINT/TX_ER/TXD4 | VDDIO – +0.4 V | +0.5 V | -8 mA | +8 mA | +0.4 V | 3.6V |

**Table 7.6 LAN Interface Signals**

| NAME | V_{IH} | V_{IL} | I_{OH} | I_{OL} | V_{OL} | V_{OH} |
|------|--|----------|----------|----------|----------|----------|
| TXP | See Table 7.12, "100Base-TX Transceiver Characteristics," on page 69 and Table 7.13, "10BASE-T Transceiver Characteristics," on page 69. | | | | | |
| TXN | | | | | | |
| RXP | | | | | | |
| RXN | | | | | | |

Table 7.7 LED Signals

| NAME | V_{IH} | V_{IL} | I_{OH} | I_{OL} | V_{OL} | V_{OH} |
|----------|----------------|----------|----------|----------|----------|----------------|
| SPEED100 | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| LINK | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| ACTIVITY | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| FDUPLEX | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |

Table 7.8 Configuration Inputs

| NAME | V_{IH} | V_{IL} | I_{OH} | I_{OL} | V_{OL} | V_{OH} |
|--------|----------------|----------|----------|----------|----------|----------------|
| PHYAD0 | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| PHYAD1 | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| PHYAD2 | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| PHYAD3 | VDDIO – +0.4 V | +0.5 V | -12 mA | +12 mA | +0.4 V | VDDIO – +0.4 V |
| PHYAD4 | | | -8 mA | +8 mA | +0.4 V | 3.7 V |
| MODE0 | VDDIO – +0.4 V | +0.5 V | | | | |
| MODE1 | VDDIO – +0.4 V | +0.5 V | | | | |
| MODE2 | VDDIO – +0.4 V | +0.5 V | | | | |
| REG_EN | VDDIO – +0.4 V | +0.5 V | | | | |
| MII | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |

Table 7.9 General Signals

| NAME | V _{IH} | V _{IL} | I _{OH} | I _{OL} | V _{OL} | V _{OH} |
|-------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| GPO0 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| GPO1 | | | -8 mA | +8 mA | +0.4 V | 3.7 V |
| GPO2 | | | -8 mA | +8 mA | +0.4 V | VDDIO – +0.4 V |
| nRST | VDDIO – +0.4 V | +0.5 V | | | | |
| CLKIN/XTAL1 Note 7.2 | +1.40 V | +0.5 V | | | | |
| XTAL2 | - | - | | | | |
| NC | | | | | | |

Note 7.2 These levels apply when a 0-3.3V Clock is driven into CLKIN/XTAL1 and XTAL2 is floating. The maximum input voltage on XTAL1 is VDDIO + 0.4V.

Table 7.10 Analog References

| NAME | BUFFER TYPE | V _{IH} | V _{IL} | I _{OH} | I _{OL} | V _{OL} | V _{OH} |
|--------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| EXRES1 | AI | | | | | | |
| NC | AI/O | | | | | | |

Table 7.11 Internal Pull-Up / Pull-Down Configurations

| NAME | PULL-UP OR PULL-DOWN |
|-----------------|----------------------|
| SPEED100/PHYAD0 | Pull-up |
| LINK/PHYAD1 | Pull-up |
| ACTIVITY/PHYAD2 | Pull-up |
| FDUPLEX//PHYAD3 | Pull-up |
| GPO1/PHYAD4 | Pull-up |
| MODE0 | Pull-up |
| MODE1 | Pull-up |
| MODE2 | Pull-up |
| nINT/TX_ER/TXD4 | Pull-up |
| nRST | Pull-up |
| RXD3/nINTSEL | Pull-up |
| MDIO | Pull-down |
| MDC | Pull-down |
| GPO0/RMII | Pull-down |
| TXEN | Pull-down |
| COL | Pull-down |

**Table 7.12 100Base-TX Transceiver Characteristics**

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------------|-----------|------|-----|-------|-------|----------|
| Peak Differential Output Voltage High | V_{PPH} | 950 | - | 1050 | mVpk | Note 7.3 |
| Peak Differential Output Voltage Low | V_{PPL} | -950 | - | -1050 | mVpk | Note 7.3 |
| Signal Amplitude Symmetry | V_{SS} | 98 | - | 102 | % | Note 7.3 |
| Signal Rise & Fall Time | T_{RF} | 3.0 | - | 5.0 | nS | Note 7.3 |
| Rise & Fall Time Symmetry | T_{RFS} | - | - | 0.5 | nS | Note 7.3 |
| Duty Cycle Distortion | D_{CD} | 35 | 50 | 65 | % | Note 7.4 |
| Overshoot & Undershoot | V_{OS} | - | - | 5 | % | |
| Jitter | | | | 1.4 | nS | Note 7.5 |

Note 7.3 Measured at the line side of the transformer, line replaced by 100Ω (+/- 1%) resistor.

Note 7.4 Offset from 16 nS pulse width at 50% of pulse peak

Note 7.5 Measured differentially.

Table 7.13 10BASE-T Transceiver Characteristics

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--|-----------|-----|-----|-----|-------|----------|
| Transmitter Peak Differential Output Voltage | V_{OUT} | 2.2 | 2.5 | 2.8 | V | Note 7.6 |
| Receiver Differential Squelch Threshold | V_{DS} | 300 | 420 | 585 | mV | |

Note 7.6 Min/max voltages guaranteed as measured with 100Ω resistive load.



Chapter 8 Application Notes

8.1 Magnetics Selection

For a list of magnetics selected to operate with the SMSC LAN8187, please refer to the Application note "AN 8-13 Suggested Magnetics".

<http://www.smSC.com/main/appnotes.html#Ethernet%20Products>

8.2 Application Notes

Application examples are given in pdf format on the SMSC LAN8187 web site. The link to the web site is shown below.

<http://www.smSC.com/main/catalog/lan8187.html>

Please check the web site periodically for the latest updates.

8.3 Reference Designs

The LAN8187 Reference designs are available on the SMSC LAN8187 web site link below.

<http://www.smSC.com/main/catalog/lan8187.html>

The reference designs are available in four variations:

- a. MII with +3.3V IO
- b. RMII with +3.3V IO
- c. MII with +1.8V IO
- d. RMII with +1.8V IO.

8.4 Evaluation board

The EVB-LAN8187 is a a PHY Evaluation Board (EVB) that interfaces a MAC controller to the SMSC LAN8187 Ethernet PHY through an MII connector, and out to an RJ-45 Ethernet Jack through industrial temperature magnetics for 10/100 connectivity.

Schematics(*.pdf and *.dsn), BOM (bill of materials), user guide, gerber files and Layout board file are all available on the EVB web site link below.

<http://www.smSC.com/main/catalog/evblan8187.html>

The EVB-LAN8187 is designed to plug into a user's test system using a 40 pin Media Independent Interface (MII) connector. The MII connector is an AMP 40 pin Right Angle through hole MII connector, PN AMP- 174218-2. The mating connector is PN AMP 174217-2.

FEATURES:

- Industrial temperature PHY and Magnetics
- 8 pin SOIC for user configurable Magnetics
- On board LED indicators for Speed 100
- Full Duplex
- RJ-45 Connector LEDs for Link and Activity
- Interfaces Through 40-pin Connector as Defined in the MII Specification
- Powered by 5.0V from the 40-Pin MII Connector

- Standard RJ45 Connector with LED indicators for Link and Activity
- Includes Probe Points on All MII Data and Control Signals for Troubleshooting
- Includes 25MHz Crystal for Internal PHY Reference; RX_CLK is Supplied to the 40-Pin Connector
- Supports user configuration options including PHY address selection
- Integrated 3.3V Regulator

APPLICATIONS

The EVB8187 Evaluation board simplifies the process of testing and evaluating an Ethernet Connection in your application. The LAN8187 device is installed on the EVB board and all associated circuitry is included, along with all configuration options.

The Benefits of adding an external MII interface are:

- Easier system and software development
- Verify MAC to PHY interface
- Support testing of FPGA implementations of MAC
- Assist interoperability test of various networks
- Verify MII compliance
- Verify performance of HP AutoMDIX feature
- Verify Variable IO compliance

Chapter 9 Package Outline

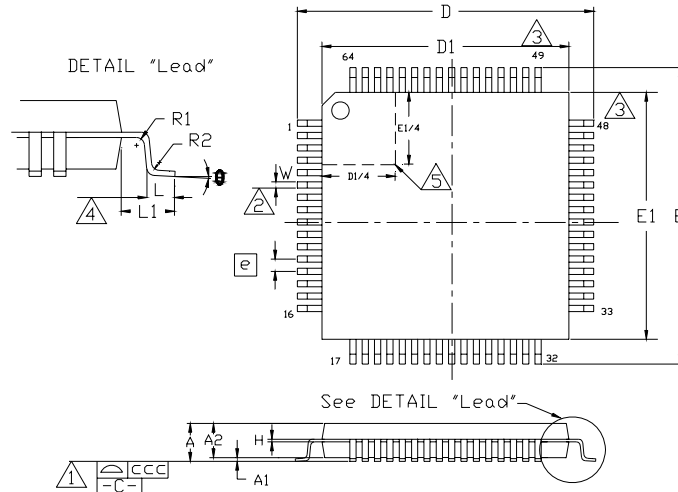


Figure 9.1 64 Pin TQFP Package Outline, 10X10X1.4 Body, 12x12 mm Footprint

Table 9.1 64 Pin TQFP Package Parameters

| | MIN | NOMINAL | MAX | REMARKS |
|-----|------------|---------|-------|------------------------|
| A | ~ | ~ | 1.60 | Overall Package Height |
| A1 | 0.05 | ~ | 0.15 | Standoff |
| A2 | 1.35 | ~ | 1.45 | Body Thickness |
| D | 11.80 | ~ | 12.20 | X Span |
| D1 | 9.80 | ~ | 10.20 | X body Size |
| E | 11.80 | ~ | 12.20 | Y Span |
| E1 | 9.80 | ~ | 10.20 | Y body Size |
| H | 0.09 | ~ | 0.20 | Lead Frame Thickness |
| L | 0.45 | 0.60 | 0.75 | Lead Foot Length |
| L1 | ~ | 1.00 | ~ | Lead Length |
| e | 0.50 Basic | | | Lead Pitch |
| θ | 0° | ~ | 7° | Lead Foot Angle |
| W | 0.17 | 0.22 | 0.27 | Lead Width |
| R | 0.08 | ~ | ~ | Lead Shoulder Radius |
| R2 | 0.08 | ~ | 0.20 | Lead Foot Radius |
| ccc | ~ | ~ | 0.08 | Coplanarity |

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm per side.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.