L6997S

STEP DOWN CONTROLLER FOR LOW VOLTAGE OPERATIONS

1 Features

- FROM 3V TO 5.5V V_{CC} RANGE
- MINIMUM OUTPUT VOLTAGE AS LOW AS 0.6V
- 1V TO 35V INPUT VOLTAGE RANGE
- CONSTANT ON TIME TOPOLOGY
- VERY FAST LOAD TRANSIENTS
- 0.6V, ±1% VREF
- SELECTABLE SINKING MODE
- LOSSLESS CURRENT LIMIT, AVAILABLE ALSO IN SINKING MODE
- REMOTE SENSING
- OVP,UVP LATCHED PROTECTIONS
- 600μA TYP QUIESCENT CURRENT
- POWER GOOD AND OVP SIGNALS
- PULSE SKIPPING AT LIGTH LOADS
- 94% EFFICIENCY FROM 3.3V TO 2.5V

2 Applications

- NETWORKING
- DC/DC MODULES
- DISTRIBUTED POWER
- MOBILE APPLICATIONS
- CHIP SET, CPU, DSP AND MEMORIES SUPPLY

Figure 1. Package

TSSOP20

Table 1. Order Codes

Part Number	Package
L6997S	TSSOP20
L6997STR	Tape & Reel

3 Description

The device is a high efficient solution for networking dc/dc modules and mobile applications compatible with 3.3V bus and 5V bus.

It's able to regulate an output voltage as low as 0.6V.

The constant on time topology assures fast load transient response. The embedded voltage feed-forward provides nearly constant switching frequency operation in spite of a wide input voltage range.

An integrator can be introduced in the control loop to reduce the static output voltage error.

The remote sensing improves the static and dynamic regulation, recovering the wires voltage drop.

Pulse skipping technique reduces power consumption at light loads. Drivers current capability allows output currents in excess of 20A.

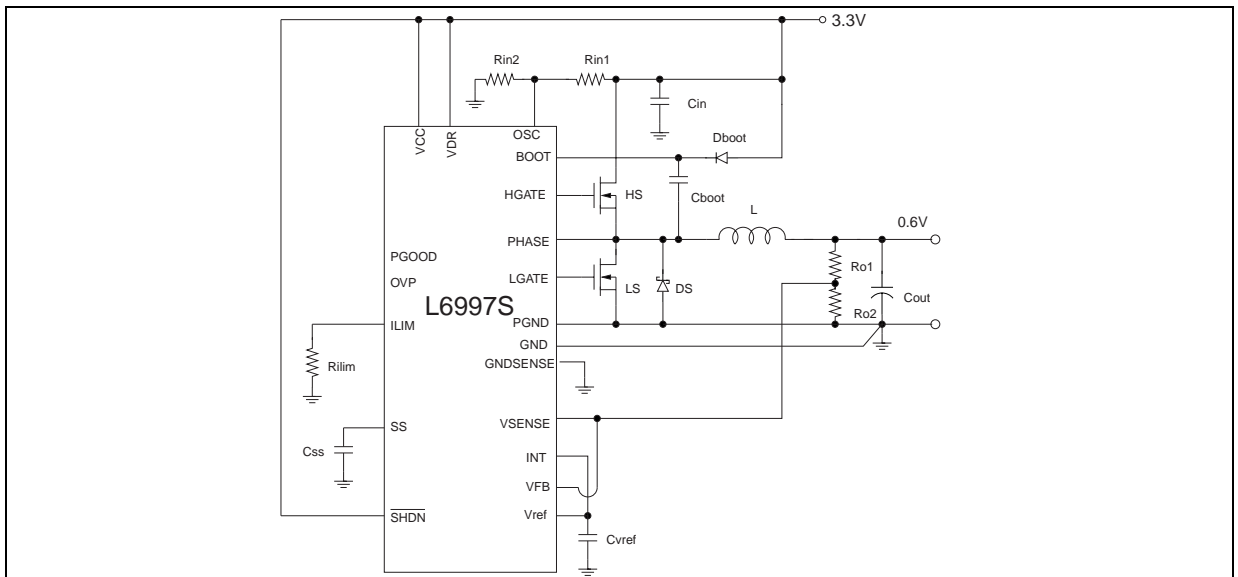**Figure 2. Minimum Component Count Application**

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	-0.3 to 6	V
V_{DR}	V_{DR} to GND	-0.3 to 6	V
	HGATE and BOOT, to PHASE	-0.3 to 6	V
	HGATE and BOOT, to PGND	-0.3 to 42	V
V_{PHASE}	PHASE	-0.3-to 36	V
	LGATE to PGND	-0.3 to V_{DR}+0.3	V
	ILIM, VFB, VSENSE, NOSKIP, SHDN, PGOOD, OVP, VREF, INT, GND$_{SENSE}$ to GND	-0.3 to V_{CC}+0.3	V
BOOT, HGATE and PHASE PINS	Maximum Withstanding Voltage Range Test Condition:CDF-AEC-Q100-002 "Human Body Model" Accepatance Criteria: "Normal Performance"	±750	V
OTHER PINS		±2000	V
P_{tot}	Power dissipation at T_{amb} = 25°C	1	W
T_{stg}	Storage temperature range	-40 to 150	°C

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction to Ambient	125	°C/W
T_j	Junction operating temperature range	-40 to 125	°C

Figure 3. Pin Connection (Top View)

TSSOP20
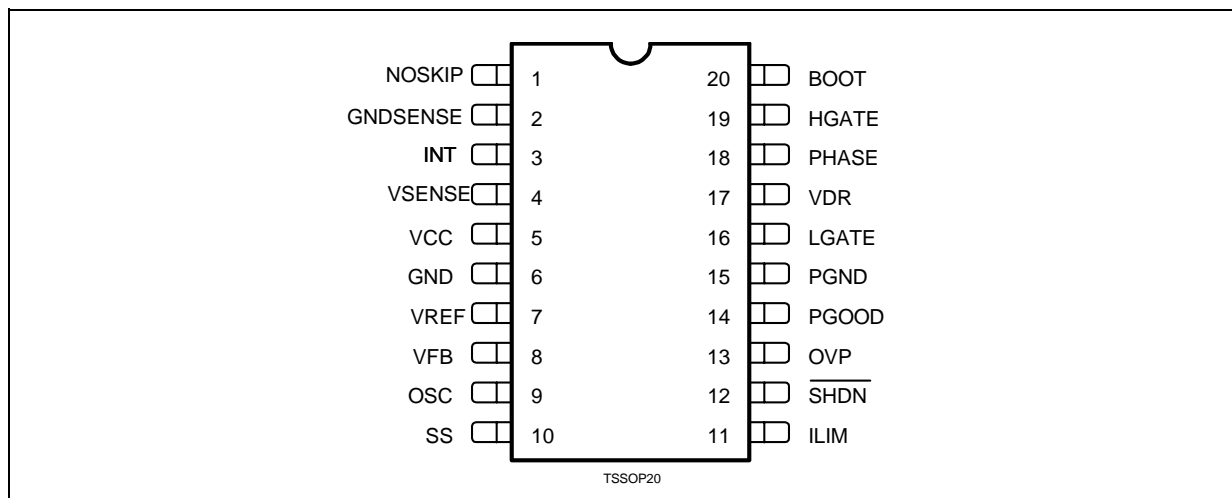
Table 4. Pin Function

N°	Name	Description
1	NOSKIP	Connect to V_{CC} to force continuous conduction mode and sink mode.
2	GNDSENSE	Remote ground sensing pin
3	INT	Integrator output. Short this pin to VFB pin and connect it via a capacitor to V_{OUT} to insert the integrator in the control loop. If the integrator is not used, short this pin to VREF.
4	VSENSE	This pin must be connected to the remote output voltage to detect overvoltage and undervoltage conditions and to provide integrator feedback input.

Table 4. Pin Function (continued)

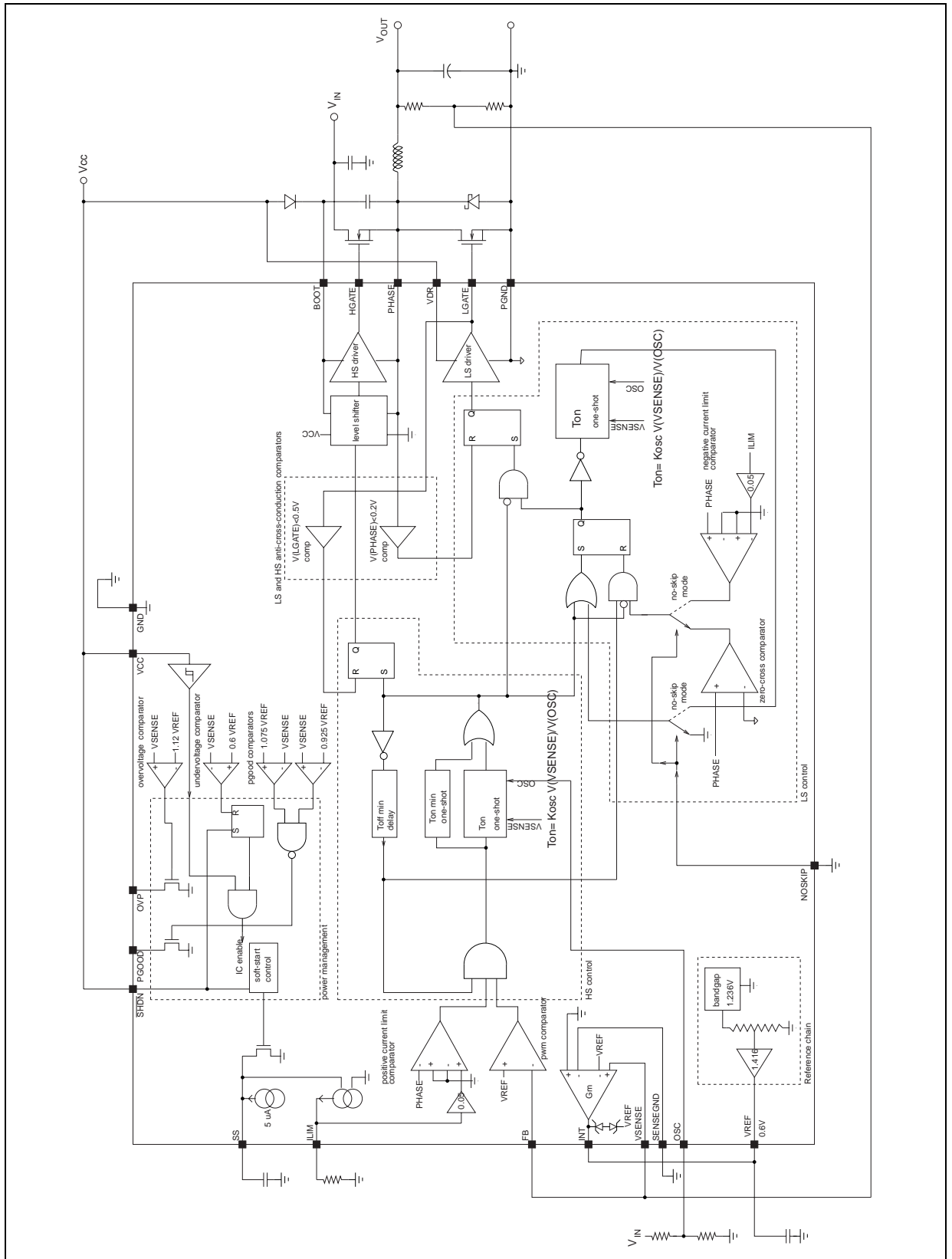| N°	Name	Description
5	V$_{CC}$	IC Supply Voltage.
6	GND	Signal ground
7	VREF	0.6V voltage reference. Connect a ceramic capacitor (max. 10nF) between this pin and ground. This pin is capable to source or sink up to 250uA
8	VFB	PWM comparator feedback input. Short this pin to INT pin to enable the integrator function, or to VSENSE to disable the integrator function.
9	OSC	Connect this pin to the input voltage through a voltage divider in order to provide the feed-forward function don't leave floating.
10	SS	Soft Start pin. A 5µA constant current charges an external capacitor. Itsvalue sets the soft-start time don't leave floating.
11	ILIM	An external resistor connected between this pin and GND sets the current limit threshold don't leave floating..
12	SHDN	Shutdown. When connected to GND the device and the drivers are OFF. It cannot be left floating.
13	OVP	Open drain output. During the over voltage condition it is pulled up by an external resistor.
14	PGOOD	Open drain output. It is pulled down when the output voltage is not within the specified thresholds. Otherwise is pulled up by external resistor. If not used it can be left floating.
15	PGND	Low Side driver ground.
16	LGATE	Low Side driver output.
17	V$_{DR}$	Low Side driver supply.
18	PHASE	Return path of the High Side driver.
19	HGATE	High side driver output.
20	BOOT	Bootstrap capacitor pin. High Side driver is supplied through this pin.

Table 5. Electrical Characteristics

(V$_{CC}$ = V$_{DR}$ = 3.3V; T$_{amb}$ = 0°C to 85°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
Vin	Input voltage range	Vout=Vref Fsw=110Khz Iout=1A	1		35	V
V$_{CC}$, V$_{DR}$			3		5.5	V
V$_{CC}$	Turn-onvoltage		2.86		2.97	V
	Turn-off voltage		2.75		2.9	V
	Hysteresis			90		mV
IqV$_{DR}$	Drivers Quiescent Current	VFB > VREF		7	20	µA
IqVcc	Device Quiescent current	VFB > VREF		400	600	µA
SHUTDOWN SECTION						
SHDN	Device On		1.2			V
	Device Off				0.6	V
I$_{SH}$V$_{DR}$	Drivers shutdown current	SHDN to GND			5	µA
I$_{SH}$V$_{CC}$	Devices shutdown current	SHDN to GND		1	15	µA
SOFT START SECTION						
I$_{SS}$	Soft Start current	V$_{SS}$ = 0.4V	4		6	µA
ΔV$_{SS}$	Active Soft start and voltage		300	400	500	mV

Table 5. Electrical Characteristics (continued)

($V_{CC} = V_{DR} = 3.3V$; $T_{amb} = 0°C$ to $85°C$ unless otherwise specified)

| Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CURRENT LIMIT AND ZERO CURRENT COMPARATOR						
I_{LIM}	Input bias current	R_{ILIM} = 2KΩ to 200KΩ	4.6	5	5.4	μA
	Zero Crossing Comparator offset Phase-gnd		-2		2	mV
K_{ILIM}	Current limit factor		1.6	1.8	2	μA
ON TIME						
Ton	On time duration	$V_{REF}=V_{SENSE}$ OSC=125mV	720	800	880	ns
		$V_{REF}=V_{SENSE}$ OSC=250mV	370	420	470	ns
		$V_{REF}=V_{SENSE}$ OSC=500mV	200	230	260	ns
		$V_{REF}=V_{SENSE}$ OSC=1000mV	90	115	140	ns
OFF TIME						
T_{OFFMIN}	Minimum off time				600	ns
	K_{OSC}/T_{OFFMIN}	OSC=250mV	0.20		0.40	
VOLTAGE REFERENCE						
VREF	Voltage Accuracy	0μA < I_{REF} < 100μA	0.594	0.6	0.606	V
PWM COMPARATOR						
	Input voltage offset		-2		+2	mV
I_{FB}	Input Bias Current			20		nA
INTEGRATOR						
	Over Voltage Clamp	V_{SENSE} = V_{CC}	0.62	0.75	0.88	V
	Under Voltage Clamp	V_{SENSE} = GND	0.45	0.55	0.65	V
	Integrator Input Offset Voltage V_{SENSE}-V_{REF}		-4		-4	mV
I_{VSENSE}	Input Bias Current			20		nA
GATE DRIVERS						
	High side rise time	V_{DR}=3.3V; C=7nF HGATE - PHASE from 1 to 3V		50	90	ns
	High side fall time			50	100	ns
	Low side rise time	V_{DR}=3.3V; C=14nF LGATE from 1 to 3V		50	90	ns
	Low side fall time			50	90	ns
P_{GOOD} UVP/OVP PROTECTIONS						
OVP	Over voltage threshold	with respect to V_{REF}	118	121	124	%
UVP	Under voltage threshold		67	70	73	%
	Upper threshold (V_{SENSE}-V_{REF})	V_{SENSE} rising	110	112	116	%
	Lower threshold (V_{SENSE}-V_{REF})	V_{SENSE} falling	85	88	91	%
V_{PGOOD}		I_{Sink}=2mA		0.2	0.4	V

Figure 4. Functional & Block Diagram

4   DEVICE DESCRIPTION

4.1   Constant On Time PWM topology

Figure 5. Loop block schematic diagram
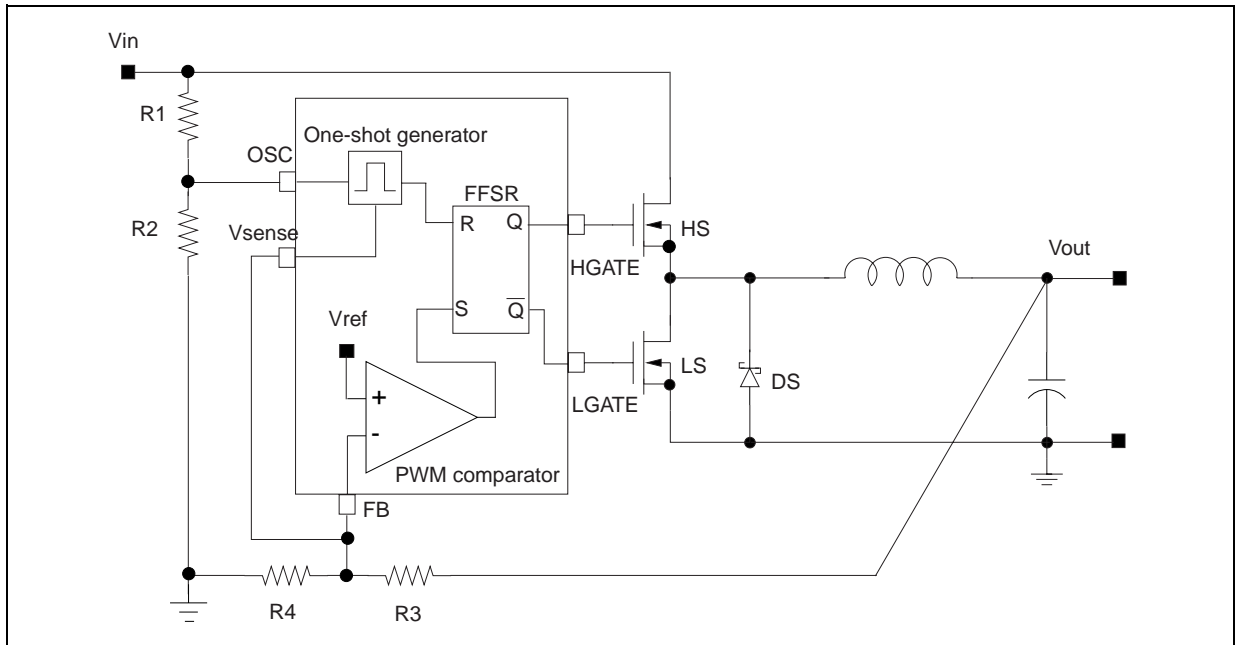
The device implements a Constant On Time control scheme, where the Ton is the high side MOSFET on time duration forced by the one-shot generator. The On Time is directly proportional to VSENSE pin voltage and inverse to OSC pin voltage as in Eq1:

$$T_{ON} = K_{OSC}\frac{V_{SENSE}}{V_{OSC}} + \tau \qquad (1)$$

where K_{OSC} = 180ns and τ is the internal propagation delay time (typ. 40ns). The system imposes in steady state a minimum On Time corresponding to V_{OSC} = 1V. In fact if the V_{OSC} voltage increases above 1V the corresponding Ton will not decrease. Connecting the OSC pin to a voltage partition from V_{IN} to GND, it allows a steady-state switching frequency F_{SW} independent of V_{IN}. It results:

$$f_{SW} = \frac{V_{OUT}}{V_{IN}}\frac{1}{T_{ON}} = \frac{\alpha_{OSC}}{\alpha_{OUT}}\frac{1}{K_{OSC}} \rightarrow \alpha_{OSC} = f_{SW}K_{OSC}\alpha_{OUT} \ (2)$$

where

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}} = \frac{R_2}{R_2 + R_1} \qquad (3)$$

$$\alpha_{OUT} = \frac{V_{FB}}{V_{OUT}} = \frac{R_4}{R_3 + R_4} \qquad (4)$$

The above equations allow setting the frequency divider ratio α_{OSC} once output voltage has been set; note that such equations hold only if V_{OSC}<1V. Further the Eq2 shows how the system has a switching frequency ideally independent from the input voltage. The delay introduces a light dependence from V_{IN}. A minimum Off-Time constraint of about 500ns is introduced in order to assure the boot capacitor charge and to

limit the switching frequency after a load transient as well as to mask PWM comparator output against noise and spikes.

The system has not an internal clock, because this is a hysteretic controller, so the turn on pulse will start if three conditions are met contemporarily: the FB pin voltage is lower than the reference voltage, the minimum off time is passed and the current limit comparator is not triggered (i.e. the inductor current is below the current limit value). The voltage at the OSC pin must range between 50mV and 1V to ensure the system linearity.

4.2 Closing the loop

The loop is closed connecting the output voltage (or the output divider middle point) to the FB pin. The FB pin is internally conncted to the comparator negative pin while the positive pin is connected to the reference voltage (0.6V Typ.) as in Figure 5. When the FB goes lower than the reference voltage, the PWM comparator output goes high and sets the flip-flop output, turning on the high side MOSFET. This condition is latched to avoid noise. After the On-Time (calculated as described in the previous section) the system resets the flip-flop, turns off the high side MOSFET and turns on the low side MOSFET. For more details refers to the Figure 4.

The voltage drop along ground and supply metal paths connecting output capacitor to the load is a source of DC error. Further the system regulates the output voltage valley value not the average, as shown in Figure 6. So, the voltage ripple on the output capacitor is a source of DC static error (well as the PCB traces). To compensate the DC errors, an integrator network must be introduced in the control loop, by connecting the output voltage to the INT pin through a capacitor and the FB pin to the INT pin directly as in Figure 7. The internal integrator amplifier with the external capacitor C_{INT1} introduces a DC pole in the control loop. C_{INT1} also provides an AC path for output ripple.

Figure 6. Valley regulation
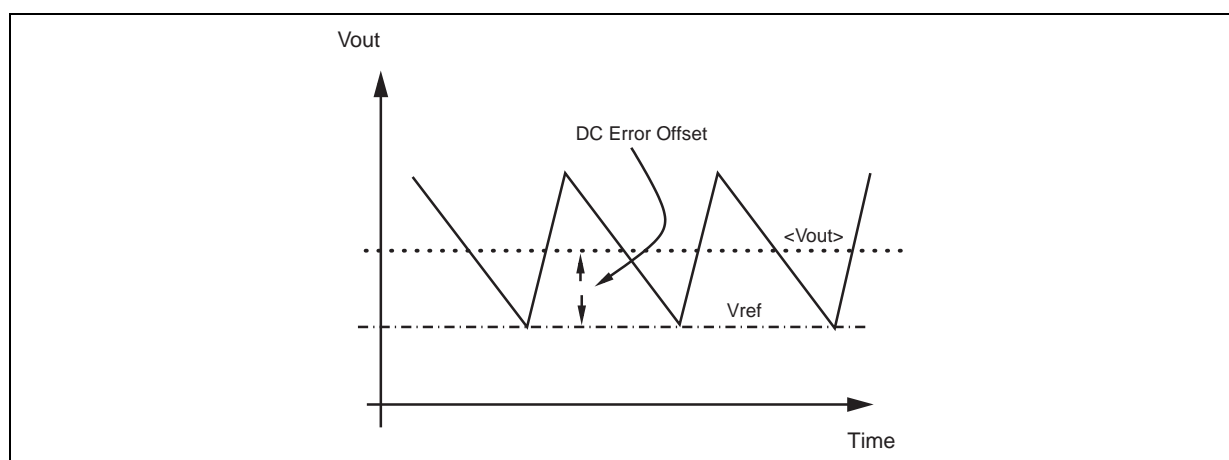
The integrator amplifier generates a current, proportional to the DC errors, that increases the output capacitance voltage in order to compensate the total static error. A voltage clamp within the device forces anINT pin voltage range (V_{REF}-50mV, V_{REF}+150mV). This is useful to avoid or smooth output voltage overshoot during a load transient. Also, this means that the integrator is capable of recovering output error due to ripple when its peak-to-peak amplitude is less than 150mV in steady state.

In case the ripple amplitude is larger than 150mV, a capacitor C_{INT2} can be connected between INT pin and ground to reduce ripple amplitude at INT pin, otherwise the integrator will operate out of its linear range. Choose C_{INT1} according to the following equation:

$$C_{INT1} = \frac{g_{INT} \cdot \alpha_{OUT}}{2 \cdot \pi \cdot F_u} \qquad (5)$$

where g_{INT}=50 μs is the integrator transconductance, α_{OUT} is the output divider ratio given from Eq4 and F_U is the close loop bandwidth. This equation holds if C_{INT2} is connected between INT pin and ground. C_{INT2} is given by:

$$\frac{C_{INT2}}{C_{INT1}} = \frac{\Delta V_{OUT}}{\Delta V_{INT}} \qquad\qquad (6)$$

Where ΔV_{OUT} is the output ripple and ΔV_{INT} is the required ripple at the INT pin (100mV typ).

Figure 7. Integrator loop block diagram
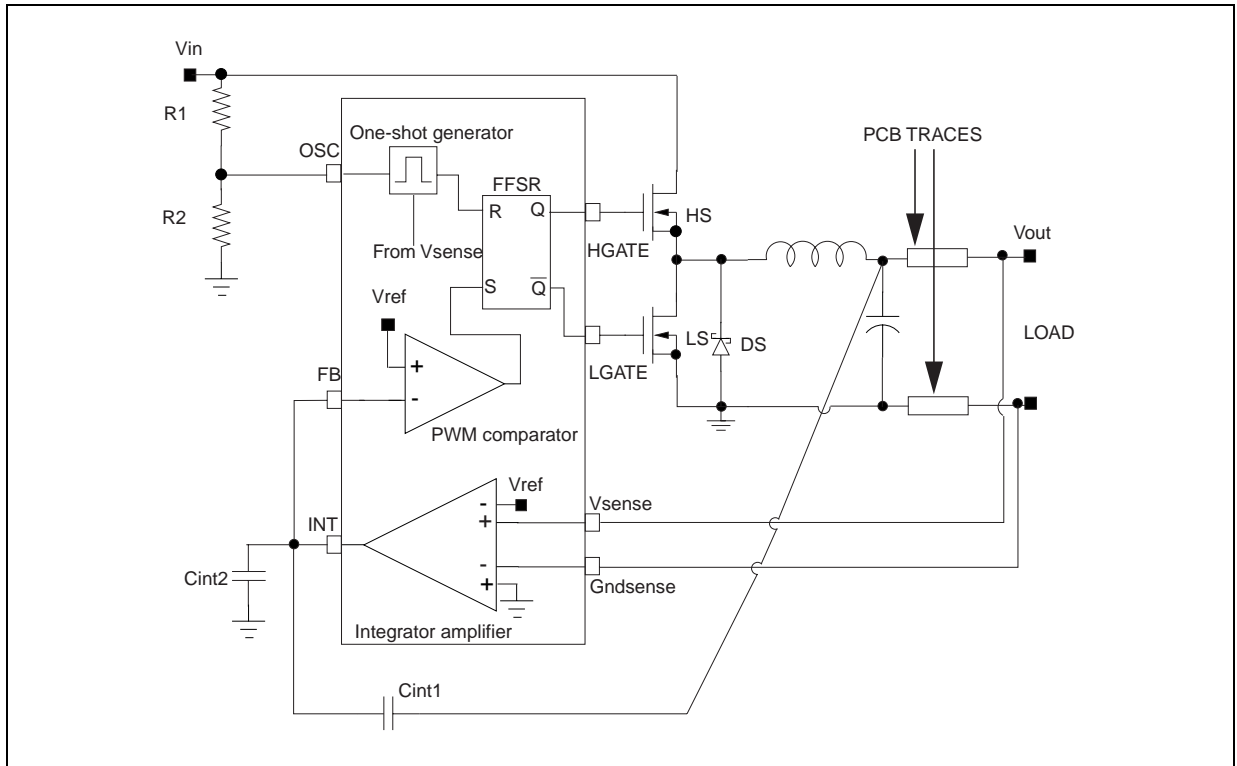
Respect to a traditional PWM controller, that has an internal oscillator setting the switching frequency, in a hysteretic system the frequency can change with some parameters. For example, while in a standard fixed switching frequency topology, the increase of the losses (increasing the output current, for example) generates a variation in the On Time and Off Time, in a fixed On Time topology , the increase of the losses generates only a variation on the Off Time, changing the switching frequency. In the device is implemented the voltage feed-forward circuit that allows constant switching frequency during steady-sate operation and withinthe input range variation. Any way there are many factors affecting switching frequency accuracy in steady-state operation. Some of these are internal as dead times, which depends on high side MOSFET driver. Others related to the external components as high side MOSFET gate charge and gate resistance, voltage drops on supply and ground rails, low side and high side RDSON and inductor parasitic resistance.

During a positive load transient, (the output current increases), the converter switches at its maximum frequency (the period is TON+TOFFmin) to recover the output voltage drop. During a negative load transient, (the output current decreases), the device stops to switch (high side MOSFET remains off).

4.3 Transition from PWM to PFM/PSK

To achieve high efficiency at light load conditions, PFM mode is provided. The PFM mode differs from the PWM mode essentially for the off phase; the on phase is the same. In PFM after a On cycle the system turns-on the low side MOSFET until the inductor current goes down zero, when the zero-crossing comparator turns off the low side MOSFET. In PWM mode, after On cycle, the system keeps the low side MOSFET on until the next turn-on cycle, so the energy stored in the output capacitor will flow through the low side MOSFET to ground. The PFM mode is naturally implemented in an hysteretic controller enabling the zero current comparator by enabling, in fact in PFM mode the system reads the output voltage with a comparator and then turns on the high side MOSFET when the output voltage goes down to reference value. The device works in discontinuous mode

at light load and in continuous mode at high load. The transition from PFM to PWM occurs when load current is around half the inductor current ripple. This threshold value depends on V_{IN}, L, and V_{OUT}. Note that the higher the inductor value is, the smaller the threshold is. On the other hand, the bigger the inductor value is, the slower the transient response is. The PFM waveforms may appear more noisy and asynchronous than normal operation, but this is normal behaviour mainly due to the very low load. If the PFM is not compatible with the application it can be disabled connecting to V_{CC} the NOSKIP pin.

4.4 Softstart

After the device is turned on the SS pin voltage begins to increase and the system starts to switch. The softstart is realized by gradually increasing the current limit threshold to avoid output overvoltage. The active soft start range for the V_{SS} voltage (where the output current limit increase linearly) is from 0.6V to 1V. In this range an internal current source (5µA Typ) charges the capacitor on the SS pin; the reference current (for the current limit comparator) forced through ILIM pin is proportional to SS pin voltage and it saturates at 5µA (Typ.). When SS voltage is close to 1V the maximum current limit is active. Output protections OVP & UVP are disabled until the SS pin voltage reaches 1V (see figure 8).

Once the SS pin voltage reaches the 1V value, the voltage on SS pin doesn't impact the system operation anymore. If the SHDN pin is turned on before the supplies, the power section must be turned on before the logic section. While if the supplies are applied with the SHND pin off, the start up sequence doesn't meter.

Figure 8. Soft -Start Diagram
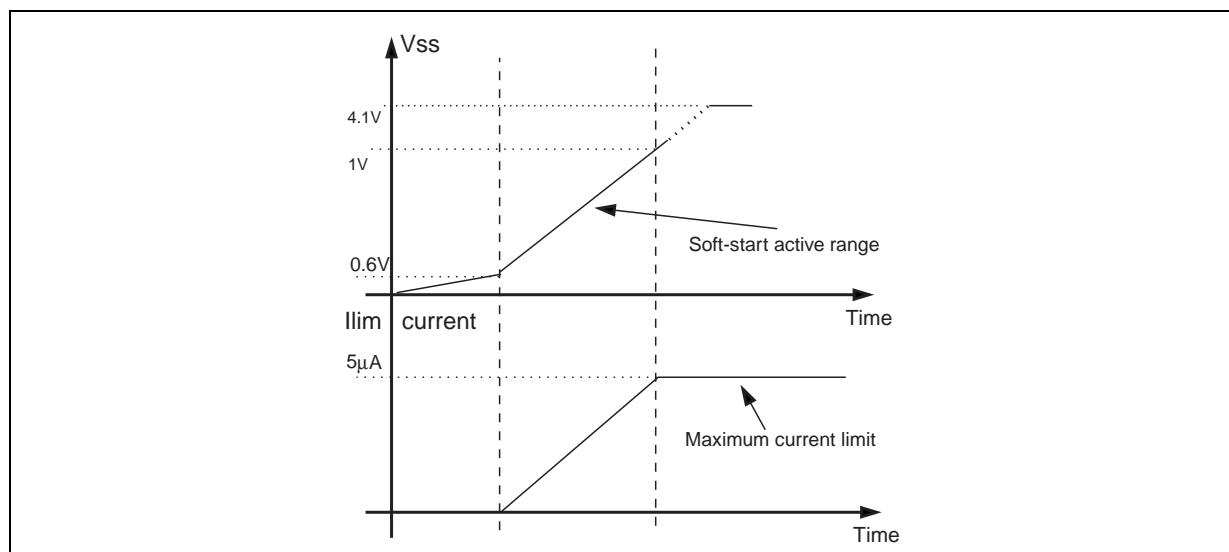
Because the system implements the soft start by controlling the inductor current, the soft start capacitor should be selected based on of the output capacitance, the current limit and the soft start active range (ΔV_{SS}).

In order to select the softstart capacitor it must be imposed that the output voltage reaches the final value before the soft start voltage reaches the under voltage value (1V). After this UVP and OVP are enable.

The time necessary to charge the SS capacitor up to 1V is given by:

$$T_{SS}(C_{SS}) = \frac{1V}{Iss} \cdot C_{SS} \qquad (7)$$

In order to calculate the output voltage chargin time it should be considered that the inductor current function can be supposed linear function of the time.

$$I_L(t,C_{SS}) = \frac{(R_{ilim}/R_{dson} \cdot K_{ILIM} \cdot I_{SS} \cdot t)}{(\Delta V_{SS} \cdot C_{SS})} \qquad (8)$$

so considering zero the output load the output voltage is given by:

$$V_{out}(t, C_{SS}) = \frac{Q(t, C_{SS})}{C_{out}} = \frac{(R_{ilim}/R_{dson} \cdot K_{ILIM} \cdot I_{SS} \cdot t^2)}{(C_{out} \cdot \Delta V_{SS} \cdot C_{SS} \cdot 2)} \quad (9))$$

indicating with V_{out} the final value, the output charging time can be estimated as:

$$V_{out}(C_{SS}) = \left[\frac{(V_{out} \cdot C_{out} \cdot \Delta V_{SS} \cdot C_{SS} \cdot 2)}{(R_{ilim}/R_{dson} \cdot K_{ILIM} \cdot I_{SS})} \right]^{0.5} \quad (10)$$

the minimum C_{SS} value is given imposing this condition:

$$T_{out} = T_{SS} \quad (11)$$

4.5 Current limit

The current limit comparator senses the inductor current through the low side MOSFET RDS_{ON} drop and compares this value with the ILIM pin voltage value. While the current is above the current limit value, the control inhibits the high side MOSFET Turn On.
To properly set the current limit threshold, it should be noted that this is a valley current limit. The Average current depends on the inductor value, V_{IN} V_{OUT} and switching frequency.
The average output current in current limit is given by:

$$I_{OUT_{CL}} = I_{max\ valley} + \frac{\Delta I}{2} \quad (12)$$

Thus, to set the current threshold, choose RILIM according to the following equation:

$$I_{max\ valley} = \frac{R_{ILim}}{Rds_{on}} \cdot K_{ILIM} \quad (13)$$

In overcurrent conditions the system keeps the current constant until the output voltage meets the undervoltage threshold. The negative valley current limit, for the sink mode, is set automatically at the same value of the positive valley current limit. The average negative current limit differs from the positive average current limit by the ripple current; this difference is due to the valley control technique.

The current limit system accuracy is function of the precision of the resistance connected to the ILIM pin and the low side MOSFET RDS_{ON} accuracy. Moreover the voltage on ILIM pin must range between 10mV and 1V to ensure the system linearity.

Figure 9. Current limit schematic
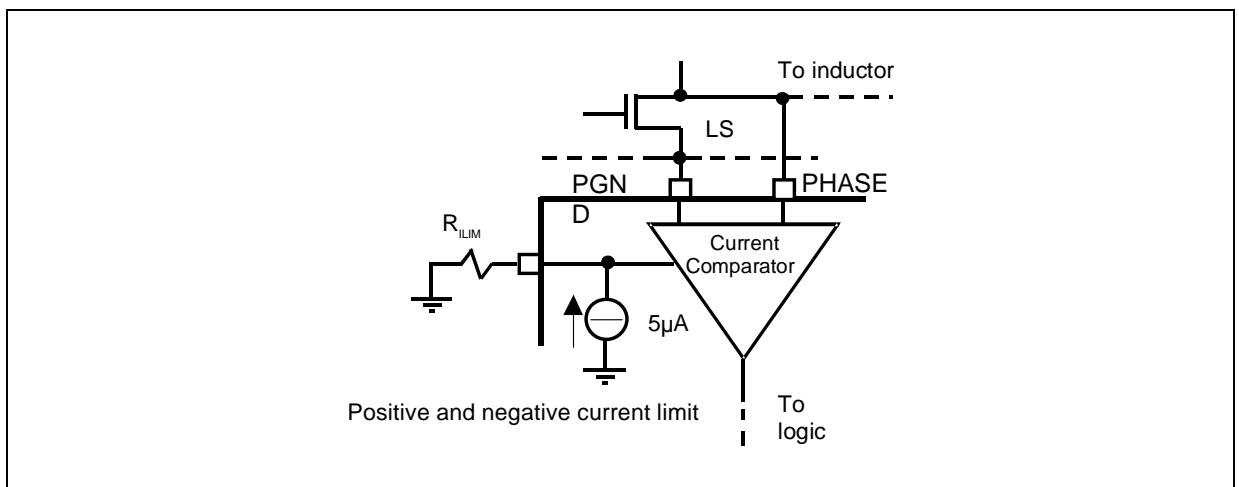
4.6 Protection and fault

The load protection is realized by using the VSENSE pin. Both OVP and UVP are latched, and the fault condition is indicated by the PGOOD and the OVP pins. If the output voltage is between the 89% (typ.) and 110% (typ) of the regulated value, PGOOD is high. If a hard overvoltage or an undervoltage occurs, the device is latched: low side MOSFET and, high side MOSFET are turned off and PGOOD goes low. In case the system detects an overvoltage the OVP pin goes high.

To recover the functionality the device must be shut down and restarted the SHDN pin, or by removing the supply, and restarting the devicewith the correct sequence.

4.7 Drivers

The integrated high-current drivers allow using different size of power MOSFET, maintaining fast switching transitions. The driver for the high side MOSFET uses the BOOT pin for supply and PHASE pin for return (floating driver). The driver for the low side MOSFET uses the VDR pin for the supply and PGND pin for the return. The drivers have the adaptive anti-cross-conduction protection, which prevents from having bothhigh side and low side MOSFET on at the same time, avoiding a high current to flow from VIN to GND. When high side MOSFET is turned off the voltage on the PHASE pin begins to fall; the low side MOSFET is turned on only when the voltage on PHASE pin reaches 250mV. When low side is turned off, high side remains off until LGATE pin voltage reaches 500mV. This is important since the driver can work properly with a large range of external power MOS-FETS.

The current necessary to switch the external MOSFETS flows through the device, and it is proportional to the MOSFET gate charge the switching frequency and the driver voltage. So the power dissipation of the device is function of the external power MOSFET gate charge and switching frequency.

$$P_{driver} = V_{cc} \cdot Q_{gTOT} \cdot F_{SW} \quad (14)$$

The maximum gate charge values for the low side and high side are given by:

$$Q_{MAXHS} = \frac{f_{SW0}}{f_{SW}} \cdot 75nC \quad (15)$$

$$Q_{MAXLS} = \frac{f_{SW0}}{f_{SW}} \cdot 125nC \quad (16)$$

Where f_{SW0} = 500Khz. The equations above are valid for T_J = 150°C. If the system temperature is lower the Q_G can be higher.

For the Low Side driver the max output gate charge meets another limit due to the internal traces degradation; in this case the maximum value is Q_{MAXLS} = 125nC.

The low side driver has been designed to have a low resistance pull-down transistor, approximately 0.5 ohms. This prevents undesired LS MOSFET Turn On during the fast rise-time of the pin PHASE, due to the Miller effect.

When the 3.3V bus is used to supply the drivers, ULTRA LOGIC LEVEL MOSFETs should be selected , to be sure that the MOSFETs work in properly way.

5 APPLICATION INFORMATION

5.1 5A Demo board description

The demo board shows the device operation in this condition: VI_{IN} from 3.3V to 5V, I_{OUT}=5A V_{OUT}=1.25V. The evaluation board let use the system with 2 different voltages (V_{CC} the supply for the IC and V_{IN} the power input for the conversion) so replacing the input capacitors the power input voltage could be also 35V. When instead the input voltage (V_{IN}) is equal to the V_{CC} it should be better joining them with a 10Ω resistor in order to filter the device input voltage. On the topside demo there are two different jumpers: one jumper, near the OVP and POWER GOOD test points, is used to shut down the device; when the jumper is present the device is in SHUTDOWN mode, to run the device remove the jumper. The other jumper, near the V_{REF} test point, is used to set the PFM/PSK mode. When the jumper is present, at light load, the system will go in PFM mode; if there is not the jumper, at light load, the system will remain in PWM mode. In the demo bottom side there are two others different jumpers. They are used to set or remove the INTEGRATOR configuration. When the jumpers named with INT label are closed AND the jumpers named with the NOINT label are open the integrator configuration is set. Sometimes the integrator configuration needs a low frequency filter the to reduce the noise interaction. In this case instead close the INT jumpers put there a resistor and after a capacitor to ground (as in the schematic diagram); the pole value is around 500Khz but it should be higher enough than the switching frequency (ten times). On the opposite when the jumpers named with the NOINT are closed and the jumpers named with INT are open the NON INTEGRATOR configuration is selected. Refer to the Table 1 and 2 for the jumpers connection.

Figure 10. Demoboard Schematic Diagram
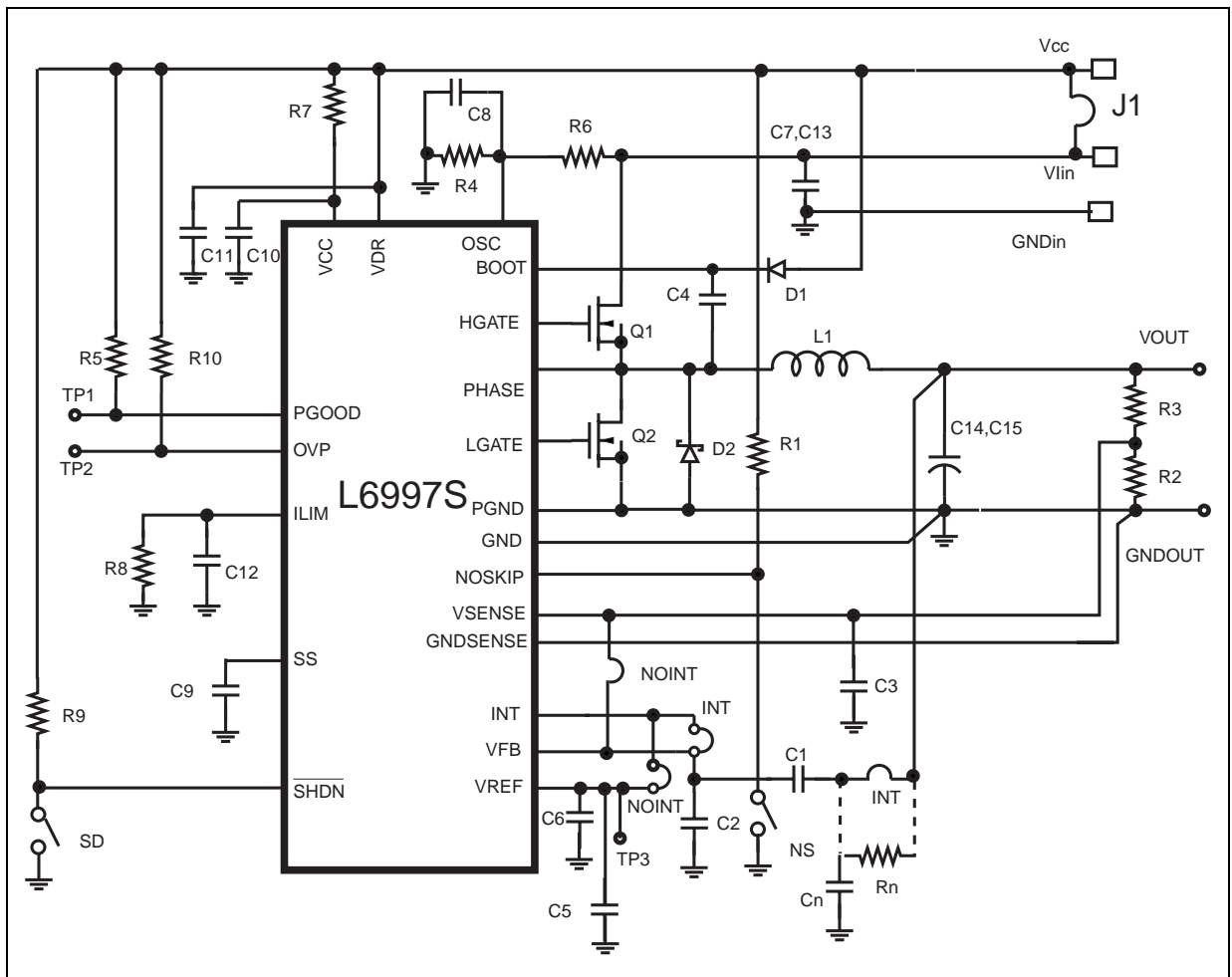
5.2 Jumper Connection

Table 6. Jumper connection with integrator

Component	Connection
C1	Mounted
C2	Mounted *
INT	Close
NOINT	Open

* This component is not necessary, depends from the output ESR capacitor. See the integrator section.

Table 7. Jumper connection without integrator

Component	Connection
C1	Not mounted
C2	Not Mounted
INT	Open
NOINT	Close

5.3 DEMOBOARD LAYOUT

Real dimensions: 4,7 cm X 2,7 cm (1.85 inch X 1. 063 inch)

Figure 11. Top side components placement
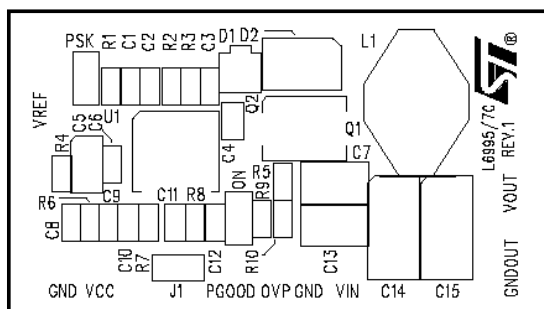
Figure 13. Top side layout
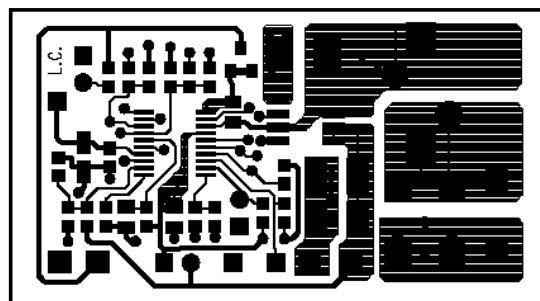
Figure 12. Bottom side Jumpers distribution
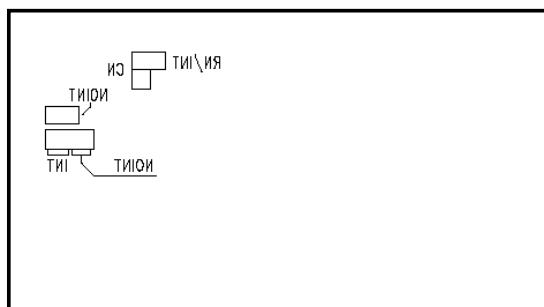
Figure 14. Bottom side layout
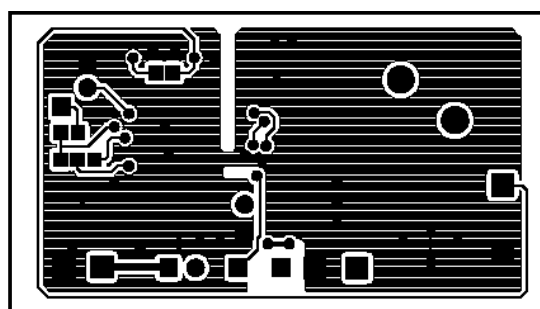
Table 8. PCB Layout guidelines

Goal	Suggestion
To minimize radiation and magnetic coupling with the adjacent circuitry.	1) Minimize switching current loop areas. (For example placing C_{IN}, High Side and Low side MOSFETS, Shottky diode as close as possible). 2) Place controller placed as close as possible to the power MOSFETs. 3) Group the gate drive components (Boot cap and diode) near the IC.
To maximize the efficiency.	Keep power traces and load connections short and wide.
To ensure high accuracy in the current sense system.	Make Kelvin connection for Phase pin and PGND pin and keep them as close as possible to the Low Side MOSFETS.
To reduce the noise effect on the IC.	1) Put the feedback component (like output divider, integrator network, etc) as close as possible to the IC. 2) Keep the feedback traces parallel and as close as possible. Moreover they must be routed as far as possible from the switching current loops. 3) Make the controller ground connection like the figure 8.

Table 9. Component list

The component list is shared in two sections: the first for the general-purpose component, the second for power section:

Part name	Value	Dimension	Notes
GENERAL-PURPOSE SECTION			
RESISTOR			
R1, R5, R9, R10	33kΩ	0603	Pull-up resistor
R2	1kΩ	0603	Output resistor divider (To set output voltage)
R3	1.1kΩ	0603	
R4		0603	Input resistor divider (To set switching frequency)
R6	470kΩ	0603	
R7	0Ω	0603	
R8		0603	Current limit resistor
CAPACITOR			
C1	330pF	0603	First integrator capacitor
C2	N.M.	0603	Second integrator capacitor
C3	1nF	0603	
C4	100nF	0603	
C5	1µF	Tantalum	
C6	10nF	0603	
C9	10nF	0603	Softstart capacitor
C10	100nF	0603	
C11	100nF	0603	
C8, C12	47pF	0603	
DIODE			
D1	BAR18		
POWER SECTION			
INPUT CAPACITORS			
C7, C13	47µF	ECJ4XF0J476Z PANASONIC	

Table 9. Component list (continued)

The component list is shared in two sections: the first for the general-purpose component, the second for power section:

Part name	Value	Dimension	Notes
OUTPUT CAPACITORS			
C14, C15	220μF	2R5TPE220M POSCAP	
INDUCTOR			
L1	2.7 μH	DO3316P-272HC COILCRAFT	
POWER MOS			
Q1,Q2	STS5DNF20V	STMicroelectronics	Double mosfet in sigle package
DIODE			
D2	STPS340U	STMicroelectronics	3

Notes: 1. N.M.=Not Mounted
2. The demoboard with this component list is set to give: V_{OUT} = 1.25V, F_{SW} = 270kHz with an input voltage around V_{IN} = V_{CC} = 3.3V-5V and with the integrator feature.
3. The diode efficiency impact is very low; it is not a necessary component.
4. All capacitors are intended ceramic type otherwise specified.

5.4 EFFICIENCY CURVES

Source mode

V_{IN} = 3.3V V_{OUT} = 1.25V F_{SW} = 270kHz

Figure 15. Efficiency vs output current
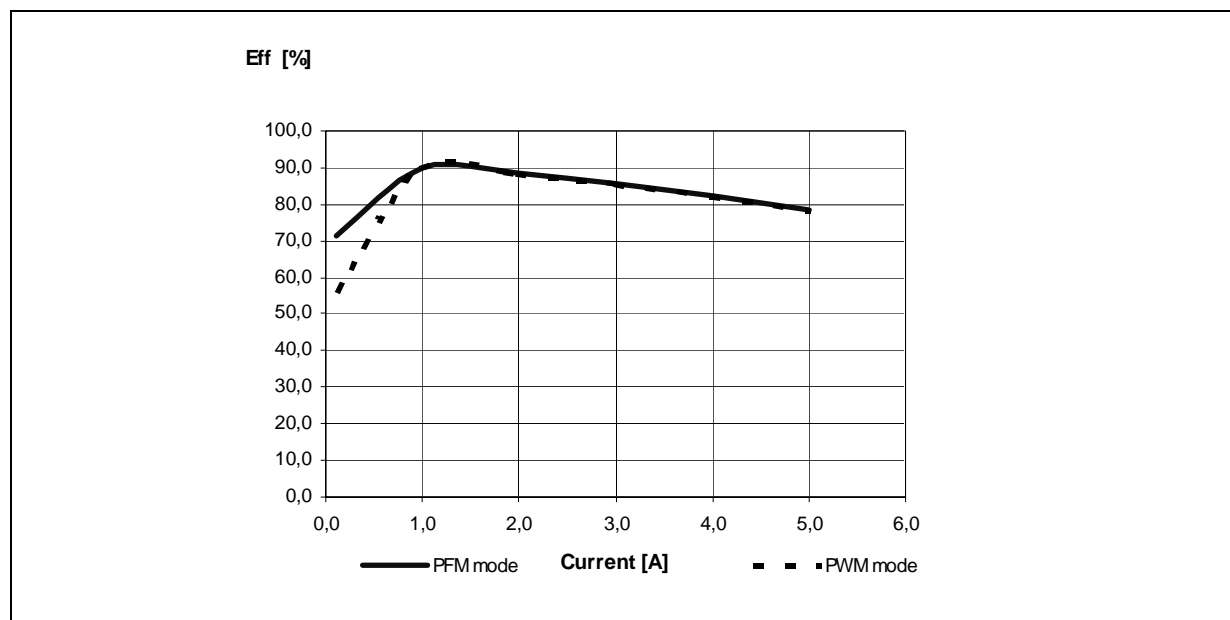
6 STEP BY STEP DESIGN

Application conditions: V_{IN} = 3.3V, ±10% V_{OUT} = 1.25V I_{OUT} = 5A F_{SW} = 270kHz

6.1 Input capacitor.

A pulsed current (with zero average value) flows through the input capacitor of a buck converter. The AC component of this current is quite high and dissipates a considerable amount of power on the ESR of the capacitor:

$$P_{CIN} = ESR_{CIN} \cdot Iout^2 \cdot \frac{Vin \cdot (Vin - Vout)}{Vin^2} \quad (17)$$

The RMS current, which the capacitor must provide, is given by:

$$Icin_{rms} = \sqrt{Iout^2 \delta(1 - \delta) + \frac{\delta}{12}(\Delta I_L)^2} \quad (18)$$

Where δ is the duty cycle of the application

Neglecting the last term, the equation reduces to:

$$Icin_{rms} = Iout \sqrt{\delta(1 - \delta)} \quad (19)$$

which maximum value corresponds to to δ = 1/2 and is equal I_{out}/2

Therefore, in worst case, the input capacitors should be selected with a RMS ripple current rating as high as half the respective maximum output current.

Electrolytic capacitors are the most used because theyare the cheapest ones and are available with a wide range of RMS current ratings. The only drawback is that, for a givenripple current rating, they are physically larger than other capacitors. Very good tantalum capacitors are coming available, with very low ESR and small size. The only problem is that they occasionally can burn if subjected to very high current during the charge. So, it is better avoid this type of capacitors for the input filter of the device. In fact, they can be subjected to high surge current when connected to the power supply. If available for the requested capacitance value and voltage rating, the ceramic capacitors have usually a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is the quite high cost. Possible solutions:

10μF	C34Y5U1E106ZTE12 TOKIN
22μF	JMK325BJ226MM TAIYO-YUDEN
47μF	ECJ4XF0J476Z PANASONIC
33μF	C3225X5R0J476M TDK

With our parameter from the equation 3 it is found:

$$Icin_{rms} = 2.42A$$

6.2 Inductor

To define the inductor, it is necessary to determine firstly the inductance value. Its minimum value is given by:

$$Lmin \geq \frac{V_o \cdot (Vin_{max} - V_o)}{F_{SW} \cdot I_{out} \cdot RF \cdot Vin_{max}} \quad (20)$$

where RF = $\Delta I/I_{OUT}$ (basically it is approximately 30%).

With our parameters:

$$Lmin \geq 2\mu H$$

The saturation current must be higher then 5A

6.3 Output capacitor and ripple voltage

The output capacitor is selected based on both static and dynamic output voltage accuracy. The static output voltage accuracy depends mostly on the ERS of the output capacitor, while the dynamic accuracy usually depends both on the ESR and capacitance value.

If the static precision is ±1% for the 1.25V output voltage, the output ripple is ±12.5mV.

To determine the ESR value from the output precision is necessary to calculate the ripple current:

$$\Delta I = \frac{Vin - Vo}{L} \cdot \frac{Vo}{Vin} \cdot T_{sw} \quad (21)$$

Where F_{SW} = 270kHz.

From the Eq. above the ripple current is around 1.25A.

So the ESR is given by:

$$ESR = \frac{\Delta V_{ripple}}{\frac{\Delta I}{2}} = \frac{25mV}{1.25} = 20m\Omega \quad (22)$$

The dynamic specifications are sometimes more relaxed than the static requirements, Anyway a minimum output capacitance must be ensured to avoid output voltage variation due to the charge and discharge of Cout during load transients.

To allow the device control loop to work properly, the zero introduced by the output capacitor ESR (τ = ESR · Cout) must be at least ten times smaller than switching frequency. Low ESR tantalum capacitors, which ESR zero is close to ten kHz, are suitable for output filtering. Output capacitor value C_{OUT} and its ESR, $ESRC_{OUT}$, should be large enough and small enough, respectively, to keep output voltage within the accuracy range during a load transient, and to give the device a minimum signal to noise ratio.

The current ripple flows through the output capacitors, so the should be calculated also to sustain this ripple: the RMS current value is given by Eq. 18.

$$Icout_{rms} = \frac{1}{2\sqrt{3}}\Delta I_L \quad (23)$$

But this is usually a negligible constrain.

Possible solutions:

330μF	EEFUE0D331R PANASONIC
220μF	2R5TPE220M POSCAP

Multilayer capacitors can not be used because their very low ESR.

6.4 MOSFET's and Schottky Diodes

A 3.3V bus powers the gate drivers of the device, the use ultra low level MOSFET is highly recommended, especially for high current applications. The MOSFET breakdown voltage V_{BRDSS} must be greater than VINMAX with a certain margin.

The RDS_{ON} can be selected once the allowable power dissipation has been established. By selecting identical

Power MOSFET for us and ls, the total power they dissipate does not depend on the duty cycle. Thus, if PON is this power loss (few percent of the rated output power), the required

RDS_{ON} (@ 25 °C) can be derived from:

$$RDS_{ON} = \frac{P_{ON}}{Iout^2 \cdot (1 + \alpha \cdot \Delta T)} \quad (24)$$

α is the temperature coefficient of RDS_{ON} (typically, $\alpha = 510^{-3}$ °C^{-1} for these low-voltage classes) and T the admitted temperature rise. It is worth noticing, however, that generally the lower RDS_{ON}, the higher is the gate charge Q_G, which leads to a higher gate drive consumption. In fact, each switching cycle, a charge Q_G moves from the input source to ground, resulting in an equivalent drive current:

$$Iq = Qg \cdot F_{SW} \quad (25)$$

A SCHOTTKY diode can be added to increase the system efficiency at high switching frequency (where the dead times could be an important part of total switching period).

This optional diode must be placed in parallel to the synchronous rectifier must have a reverse voltage VRRM greater than VIN_{MAX}. The current size of the diode must be selected in order to keep it in safe operating conditions. In order to use less space than possible, a double MOSFET in a single package is chosen: STS5DNF20V

6.5 Output voltage setting

The first step is choosing the output divider to set the output voltage. To select this value there isn't a criteria, but a low divider network value (around 100Ω) decries the efficiency at low current; instead a high value divider network (100KΩ) increase the noise effects. A network divider values from 1KΩ to 10KΩ is right. We chose:

R3 = 1KΩ

R2 = 1.1KΩ

The device output voltage is adjustable by connecting a voltage divider from output to VSENSE pin. Minimum output voltage is V_{OUT}=VREF=0.6V. Once output divider and frequency divider have been designed as to obtain the required output voltage and switching frequency, the following equation gives the smallest input voltage, which allows L6997S to regulate (which corresponds to $T_{OFF}=T_{OFFMIN}$):

$$\delta < 1 - \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{\left(\frac{K_{OSC}}{T_{OFF,MIN}}\right)MAX} \quad (26)$$

6.6 Voltage Feedforward

From the equations 1,2 and 3, choosing the switching frequency of 270kHz the resistor divider can be selected. For example:
R3 = 470KΩ
R4 = 8.5KΩ

6.7 Current limit resistor

From the equation 8 the valley current limit can be set considering the RDS_{ON} STS5DNF20V and I_{CIR} = 5A:

R8 = 120KΩ

6.8 Integrator capacitor

Let's assume F_U = 15kHz, V_{OUT} = 1.25V.

Since V_{REF} = 0.6V, from equation 2, of the device description, it follows αO_{UT} = 0.348 and, from equation 5 it follows C = 250pF. The output ripple is around 22mV, so the system doesn't need the second integrator capacitor.

6.9 Soft start capacitor

Considering the soft start equations (Eq. 11) at page 10, it can be found:

C_{SS} = 150pF

The equations are valid without load. When an active load is present the equations result more complex; further some active loads have unexpected effect, as higher current than the expected one during the soft start, can change the start up time.

In this case the capacitor value can be selected on the application; anyway the Eq11 gives an idea about the C_{SS} value.

6.10 Sink mode

Figure 16. Efficiency vs output current
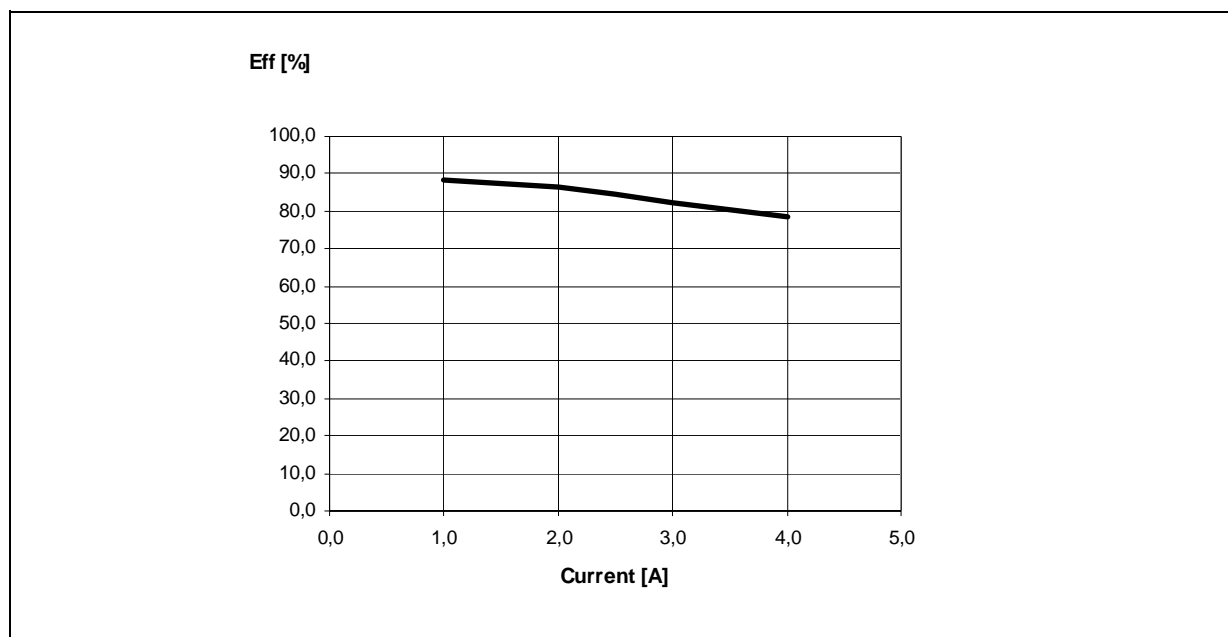
7   15A DEMO BOARD DESCRIPTION

The evaluation board shows the device operation in these conditions: V_{IN} = 3.3V V_{OUT} = 1.8V I_{OUT} = 15A, F_{SW} = 200KHz without the integrator feature. The evaluation board has two different input voltages: V_{CC} [from 3V to 5.5V] used to supply the device and the V_{IN} [up to 35V] for the power conversion. In this way, changing the power components configuration (C_{IN}, C_{OUT}, MOSFETs, L) it is possible evaluate the device performance in different conditions. It is also possible to mount a linear regulator on board used to generate the V_{CC}. On the top side are also present two switches and four jumpers. The two switches have different goals: the one nearest to the V_{CC} is used to turn on/off the device when the V_{CC} and V_{IN} are both present; the other one, near to R11 is used to turn on/off the PFM feature. The device can be turned on also with the power supply, but a correct start up sequence is mandatory. V_{IN} has to be raised first and then the V_{CC} can be applied too. If the correct sequence is not respected the device will not start up. The jumpers are used to set the integrator feature and to use the remote sensing; for more information refers to the Jumpers table. Sometimes when using the integrator configuration a low frequency filter is required in order to reduce the noise interaction. The pole value should be at least five times higher than the switching frequency. The low pass filter should be inserted in this way: the resistor, in the place of the INT jumper position and the capacitor between the resistor and ground (refers to the schematic).

Figure 17. L6997S Schematic diagram
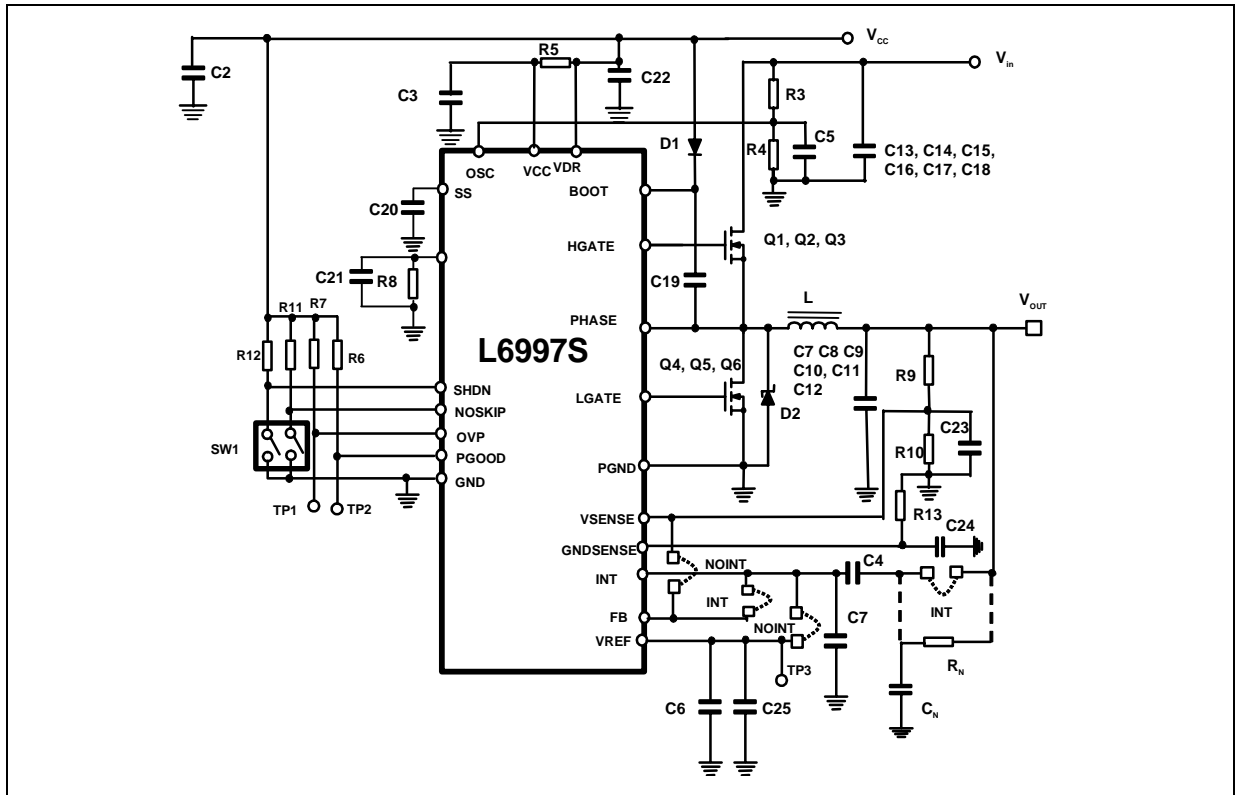
7.1 UMPERS CONNECTION

Table 10. Jumper connection with integrator

Component	Connection
C4	Mounted
C7	Mounted*
INT	Close
NOINT	Open

*This component is not necessary, depends from the output ESR capacitor. See the integrator section.

Table 11. Jumper connection without integrator

Component	Connection
C4	Not mounted
C7	Not Mounted
INT	Open
NOINT	Close

7.2 DEMO BOARD LAYOUT

Real dimensions: 5.7cm x 7.7cm (2.28inch x 3. 08inch)

Figure 18. PCB layout: bottom side
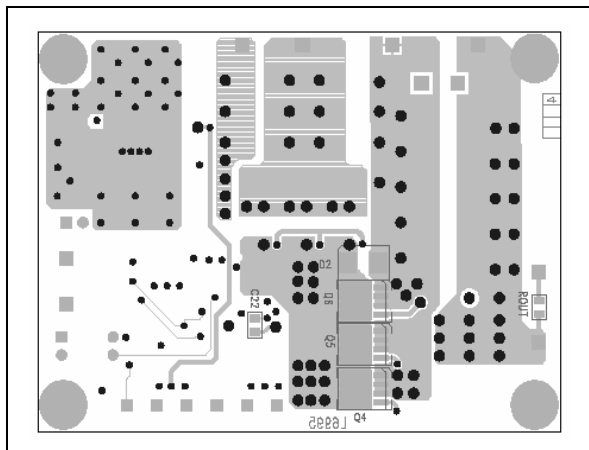
Figure 20. Internal ground plane
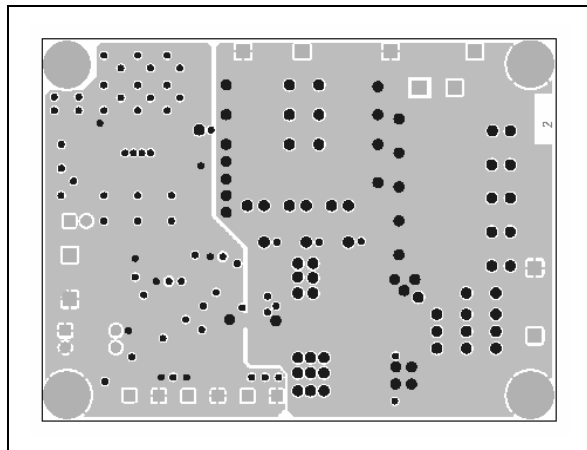
Figure 19. PCB Layout: Top side
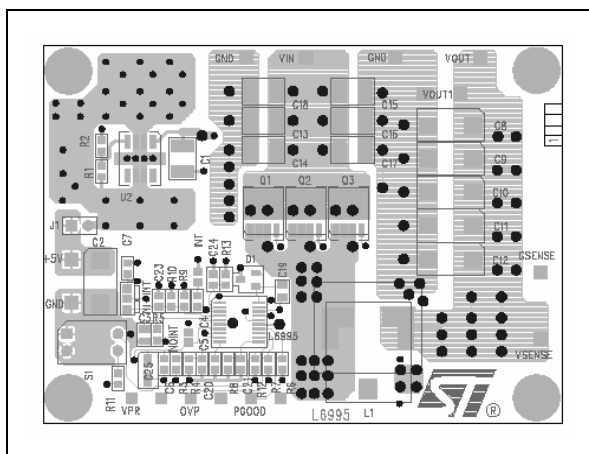
Figure 21. Power & signal plane
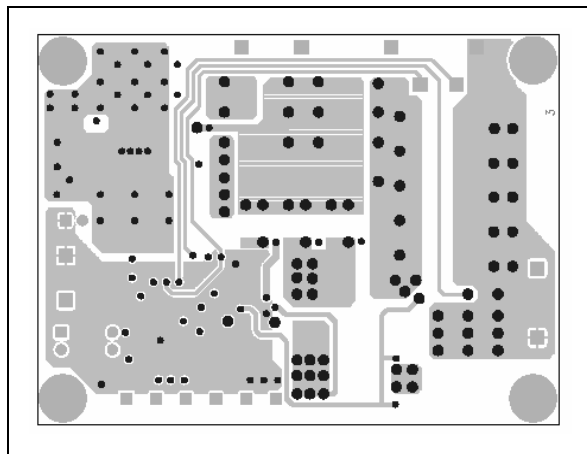
Table 12. PCB Layout guidelines

Goal	Suggestion
To minimize radiation and magnetic coupling with the adjacent circuitry.	1) Minimize switching current loop areas. (For example placing C_{IN}, High Side and Low side MOSFETS, Shottky diode as close as possible). 2) Place controller placed as close as possible to the power MOSFETs. 3) Group the gate drive components (Boot cap and diode) near the IC.
To maximize the efficiency.	Keep power traces and load connections short and wide.
To ensure high accuracy in the current sense system.	Make Kelvin connection for Phase pin and PGND pin and keep them as close as possible to the Low Side MOSFETS.
To reduce the noise effect on the IC.	1) Put the feedback component (like output divider, integrator network, etc) as close as possible to the IC. 2) Keep the feedback traces parallel and as close as possible. Moreover they must be routed as far as possible from the switching current loops. 3) Make the controller ground connection like the figure 8.

Table 13. Component list

The component list is shared in two sections: the first for the general-purpose component, the second for power section:

Part name	Value	Dimension	Notes
GENERAL-PURPOSE SECTION			
RESISTOR			
R1	N.M.	0603	Output resistor divider for the linear regulator.
R2	N.M.	0603	
R3	560kΩ	0603	Input resistor divider (To set switching frequency)
R4	5.6kΩ	0603	
R5	47Ω	0603	
R6, R7, R11, R12	33kΩ	0603	
R8	62kΩ	0603	Current limit resistor (To set current limit)
R9	2.7kΩ	0603	Output resistor divider (To set output voltage)
R10	1.3kΩ	0603	
R13	220Ω	0603	
CAPACITOR			
C1	220nF	0805	
C2	47μF	KEMET-16V	
C3	220nF	0805	
C4	150pF	0603	First integrator capacitor
C5	47pF	0603	
C6	10nF	0603	
C7	N.M.	0603	Second integrator capacitor
C19	220nF	0805	
C20	220nF	0603	Softstart capacitor
C21	47pF	0603	
C22	220nF	0805	
C23		0603	N.M.
C24	1nF	0603	
C25	1μF	Tantalum	
DIODES			
D1	BAT54		25V
POWER SECTION			
OUTPUT CAPACITORS			
C11-C12	2X680μF	T510x687(1)004AS KEMET	Output capacitor C8, C9, C10 N.M.
INPUT CAPACITORS			
C13, C14, C16, C17, C15 C18	100μF	ECJ5YF0J1072 PANASONIC	Input capacitor
	47μF	ECJ5YF1A4767 PANASONIC	
INDUCTOR			
L1	1.8μH	ETQF6F1R8BFA PANASONIC	
POWER MOS			
Q1,Q2	SI4442DY	VISHAY Siliconix	Q3 N.M.
Q5,Q6	SI4442DY	VISHAY Siliconix	Q4 N.M.
INTEGRATED CIRCUIT			
U1	L6997S		

7.3 EFFICIENCY CURVES

Figure 22. Efficiency vs output Current
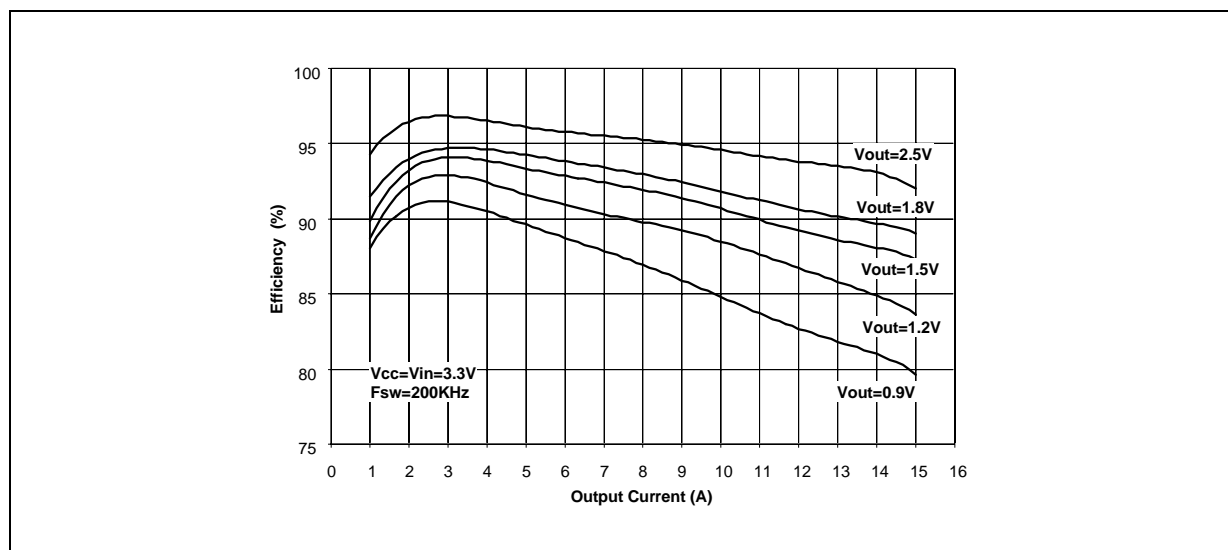
Table 14. Efficiency Curves For Different Applications (V_{IN} up to 25V)

Part name	Value	Dimension	Notes
GENERAL-PURPOSE SECTION			
RESISTOR			
R1	100Ω	0603	Output resistor divider for the linear regulator.
R2	300Ω	0603	
R3	560kΩ	0603	Input resistor divider (To set switching frequency)
R4	10kΩ	0603	
R5	47Ω	0603	
R6, R7, R11, R12	33kΩ	0603	
R8	47kΩ	0603	Current limit resistor (To set current limit)
R9	2,7kΩ	0603	Output resistor divider (To set output voltage)
R10	1kΩ	0603	
R13	220Ω	0603	
CAPACITOR			
C1	220 nF	0805	
C2	47μF	KEMET-16V	
C3	220nF	0805	
C4	150pF	0603	First integrator capacitor
C5	47pF	0603	
C6	10nF	0603	
C7	330pF	0603	Second integrator capacitor
C19	220nF	0805	
C20	10nF	0603	Softstart capacitor
C21	47pF	0603	
C22	220nF	0805	
C23		0603	N.M.

Table 14. Efficiency Curves For Different Applications (V$_{IN}$ up to 25V) (continued)

Part name	Value	Dimension	Notes
C24	1nF	0603	
C25	1µF	Tantalum	
DIODES			
D1	BAT54		25V
POWER SECTION			
OUTPUT CAPACITORS			
C11-C12	2X100µF	B45197-A3107-K409 EPCOS	Output capacitor C8, C9, C10 N.M.
INPUT CAPACITORS			
C13, C14, C16, C17, C15 C18	10µF	C34Y5U1E106Z TOKIN	Input capacitor
	10µF	C3225Y5V1E106Z TDK	
	10µF	ECJ4XF1E106Z PANASONIC	
	10µF	TMK325F106ZH TAIYO YUDEN	
INDUCTOR			
L1	3 µH	T50-52 Core, 7T AWG15	
POWER MOS			
Q1,Q2	STS11NF3LL	STMicroelectronics	Q3 N.M.
Q5,Q6	STS11NH3LL	STMicroelectronics	Q4 N.M.
DIODES			
D2	STPS2L25U	STMicroelectronics	25V
INTEGRATED CIRCUIT			
U1	L6997S		

NOTE: For the 25V to 12V conversion the inductor used is: 77120A core 7T.

7.4 EFFICIENCY CURVES

Figure 23. Efficiency vs output Current
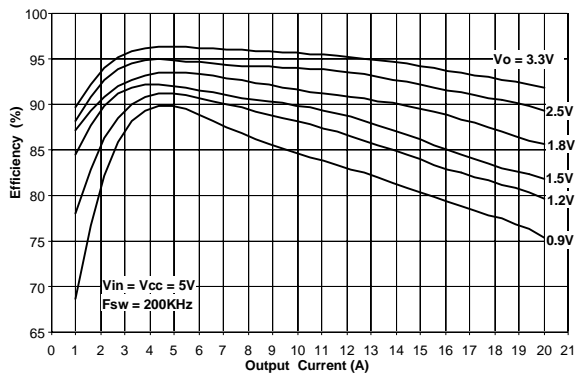
Figure 24. Efficiency vs output Current
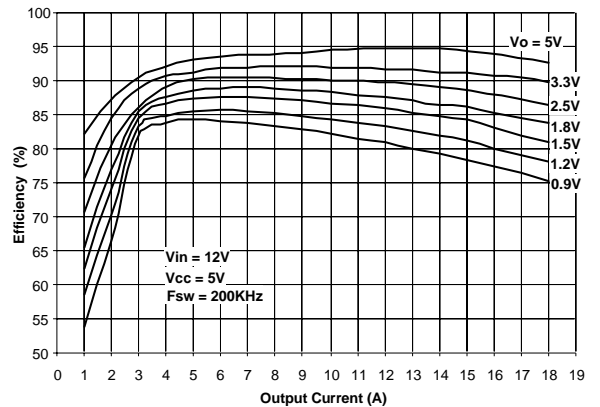
Figure 25. Efficiency Vs Output Current
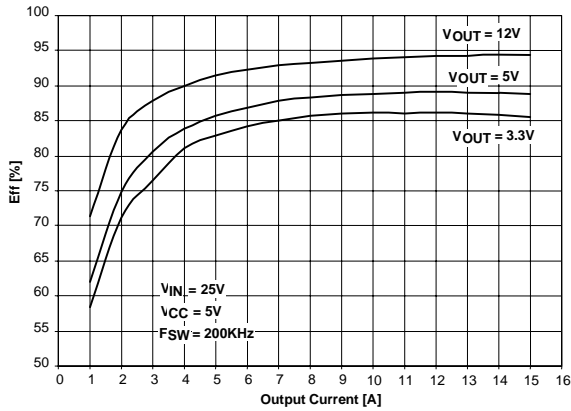
Figure 26. Efficiency Vs Output Current
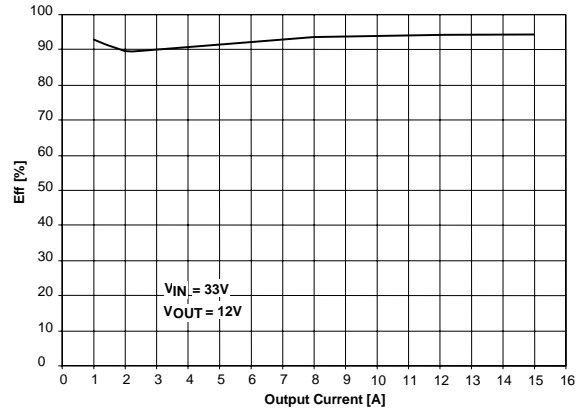
7.5 DDR MEMORY AND TERMINATION SUPPLY

Double data rate (DDR) memories require a particular Power Management Architecture. This is due to fact that the trace between the driving chipset and the memory input must be terminated with resistors. Since the Chipset driving the Memory has a push pull output buffer, the Termination voltage must be capable of sourcing and sinking current. Moreover, the Termination voltage must be equal to one half of the memory supply (the input of the memory is a differential stage requiring a reference bias midpoint) and in tracking with it. For DDRI the Memory Supply is 2.5V and the Termination voltage is 1.25Vwhile for the DDRII the Memory Supply is 1.8V and the Termination voltage is 0.9V. Figure 27 shows a complete DDRII Memory and Termination Supply realized by using 2 x L6997S. The 1.8V section is powering the memory, while the 0.9V section is providing the termination voltage.

Figure 27. Application Idea: DDRII Memory Supply
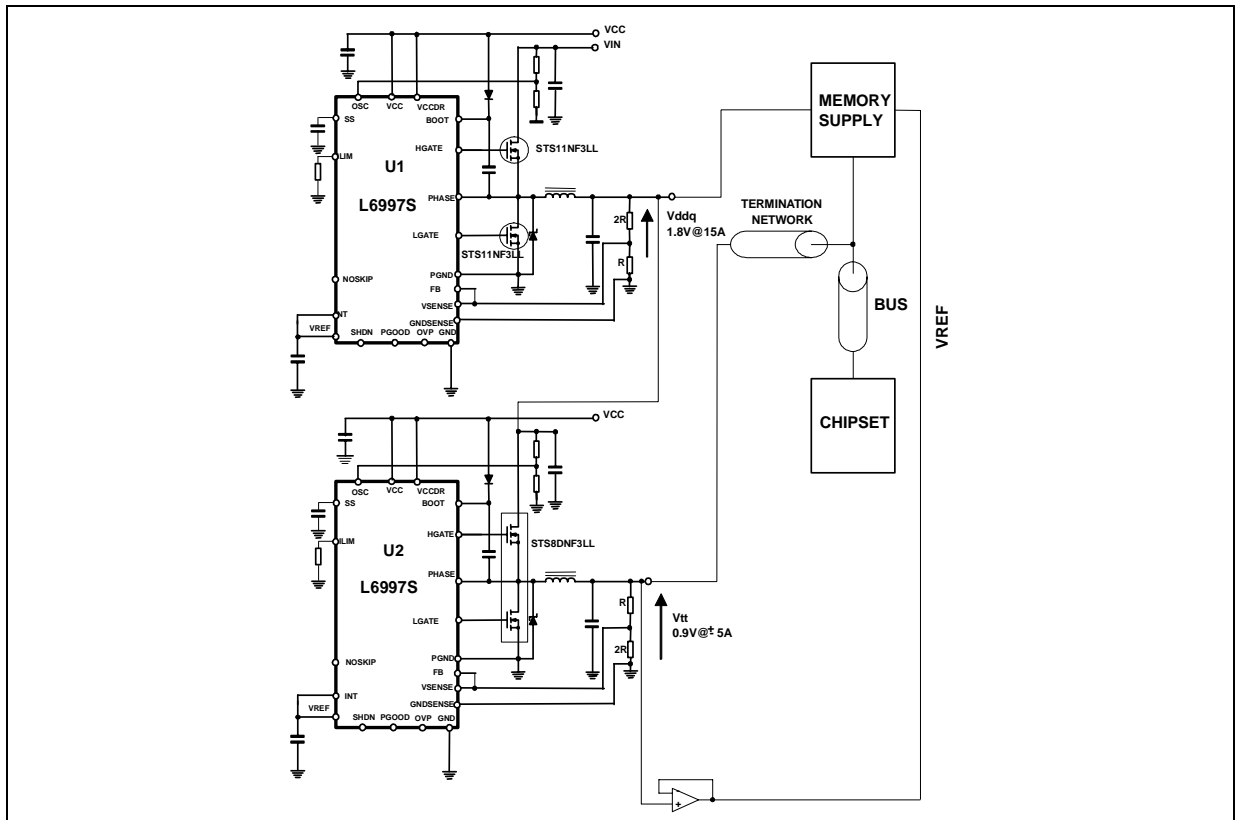
The current required by the Memory and Termination supply, depends on the memory type and size. The figures 28 and 29 show the efficiency for the termination section of the application shown in fig. 27.

Figure 28. Eff. vs. Output Current Source Mode
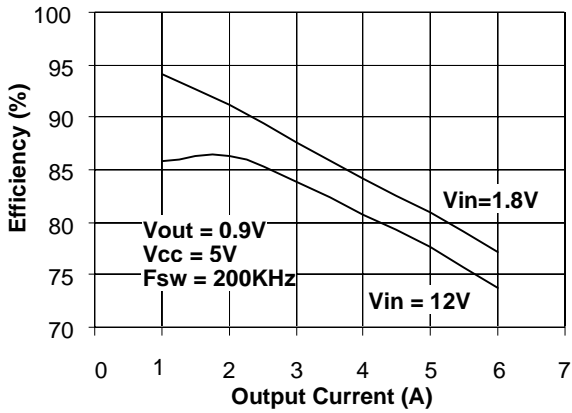
Figure 29. Eff. vs Output Current sink mode
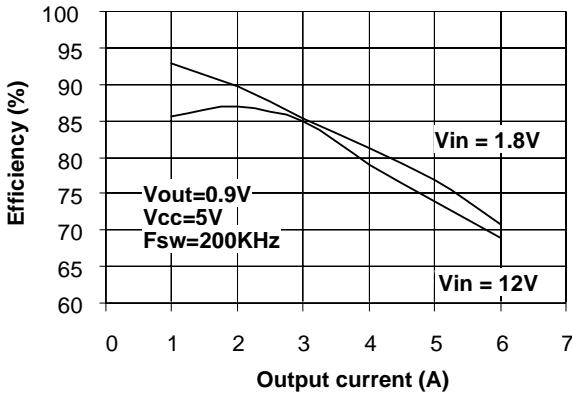
8 Typical Operating Characteristics

Figure 30. Load transient response from 0A to 5A..
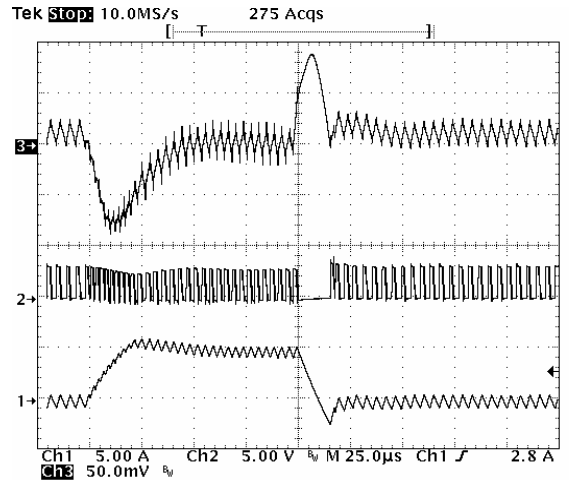
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 31. Normal functionality in SINK mode..
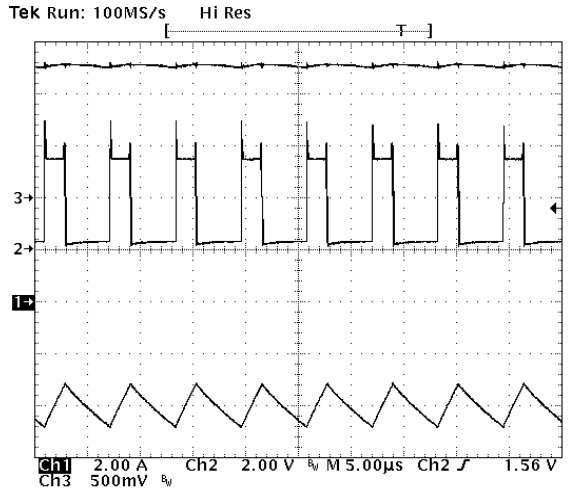
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 32. Normal functionality in PWM mode.
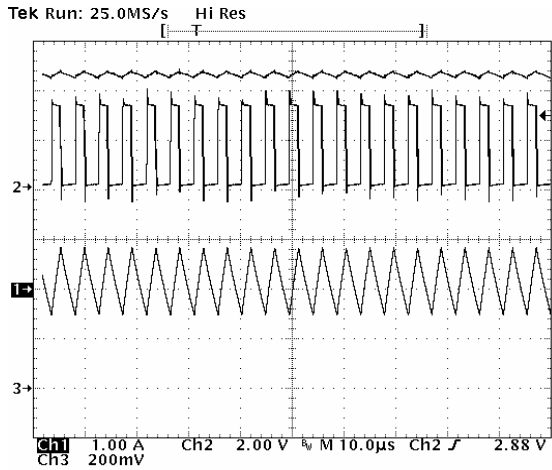
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 34. Start up waveform with 0A load.
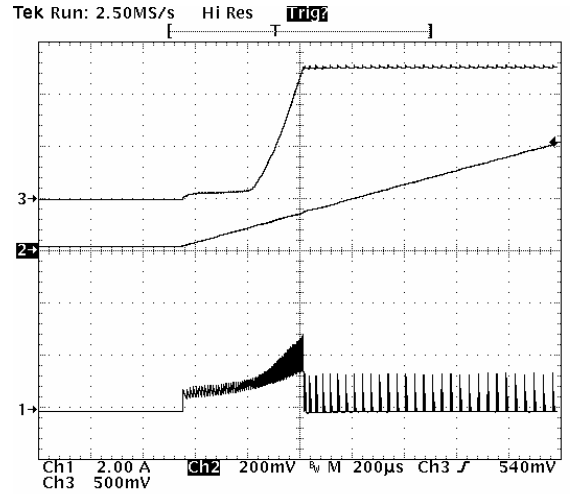
Ch1-> Inductor current
Ch2-> Soft start Voltage
Ch3-> Output voltage

Figure 33. Normal functionality in PFM mode.
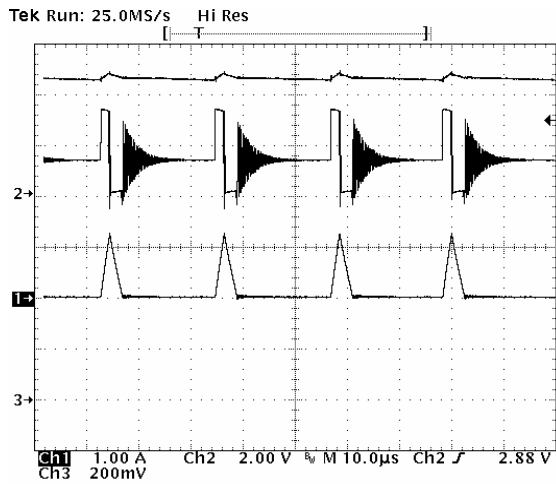
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 35. Start up waveform with 5A load..
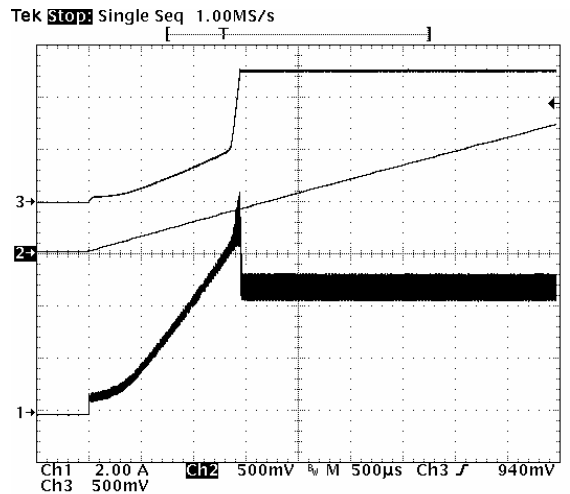
Ch1-> Inductor current
Ch2-> Soft start Voltage
Ch3-> Output voltage

Figure 36. TSSOP20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D (1)	6.400	6.500	6.600	0.252	0.256	0.260
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.) 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

OUTLINE AND MECHANICAL DATA
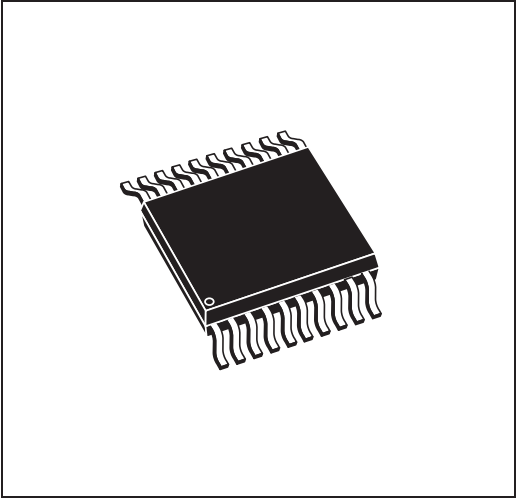
TSSOP20
Thin Shrink Small Outline Package

0087225 (Jedec MO-153-AC)
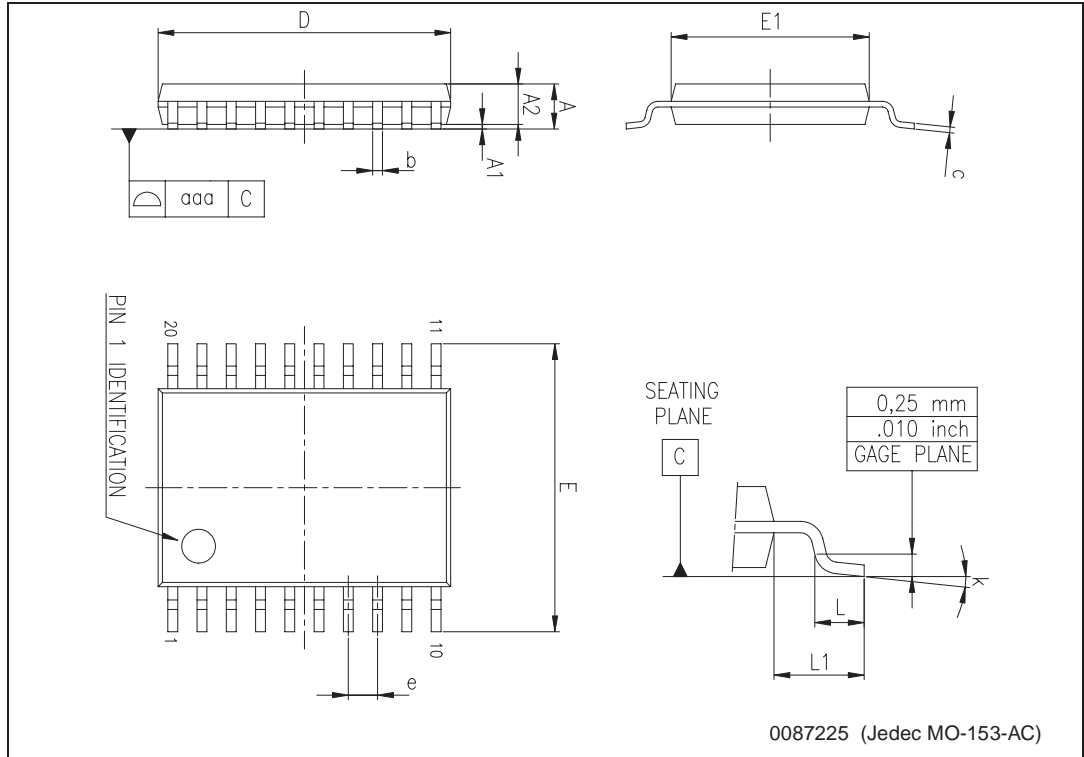
Table 15. Revision History

Date	Revision	Description of Changes
June 2004	1	First Issue.