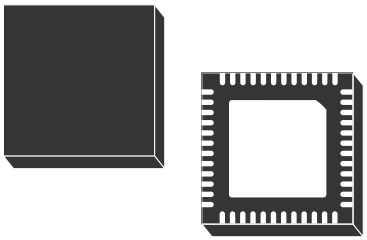
L6758A

High performance (4+1) dual controller for the VR12

Datasheet - production data



VFQFPN48 - 6x6 mm

Features

- VR12 compliant with 25 MHz SVID bus rev 1.5
  - serialVID with programmable IMAX, TMAX, VBOOT, ADDRESS
- Second generation LTB Technology™
- Dual controller:
  - two-to-four phase for core
  - 1 phase for graphics (GFX) or system agent (VSA)
- Single NTC design for TM, LL and IMON thermal compensation (for each section)
- VFDE and GDC - gate drive control for efficiency optimization
- DPM - dynamic phase management
- Dual remote sense
- 0.5% output voltage accuracy
- Fully-differential current sense across DCR
- AVP - adaptive voltage positioning
- Dual independent adjustable oscillator
- Dual current monitor
- Pre-biased output management
- 5 V supply, 12 V monitor
- Average and per-phase OC protection
- OV, UV and FB disconnection protection
- Dual VR_RDY
- VFQFPN48 6x6 mm package

Applications

- High-current VRM / VRD for desktops / servers / workstations / new generation CPUs

Description

L6758A is a dual controller designed to power Intel® VR12 processors: all required parameters are programmable through dedicated pinstrapping.

The device features two-to-four phase programmable operation for multi-phase sections and a single-phase with independent control loops. Both sections feature second generation LTB Technology to provide fast load transient response, minimizing and optimizing the output filter composition.

The L6758A supports power state transitions featuring VFDE, programmable DPM and GDC, maintaining the best efficiency over all loading conditions without compromising transient responses. The device assures fast and independent protection against load overcurrent, under/overvoltage and feedback disconnections.

The device is available in VFQFPN48 package.

Table 1. Device summary

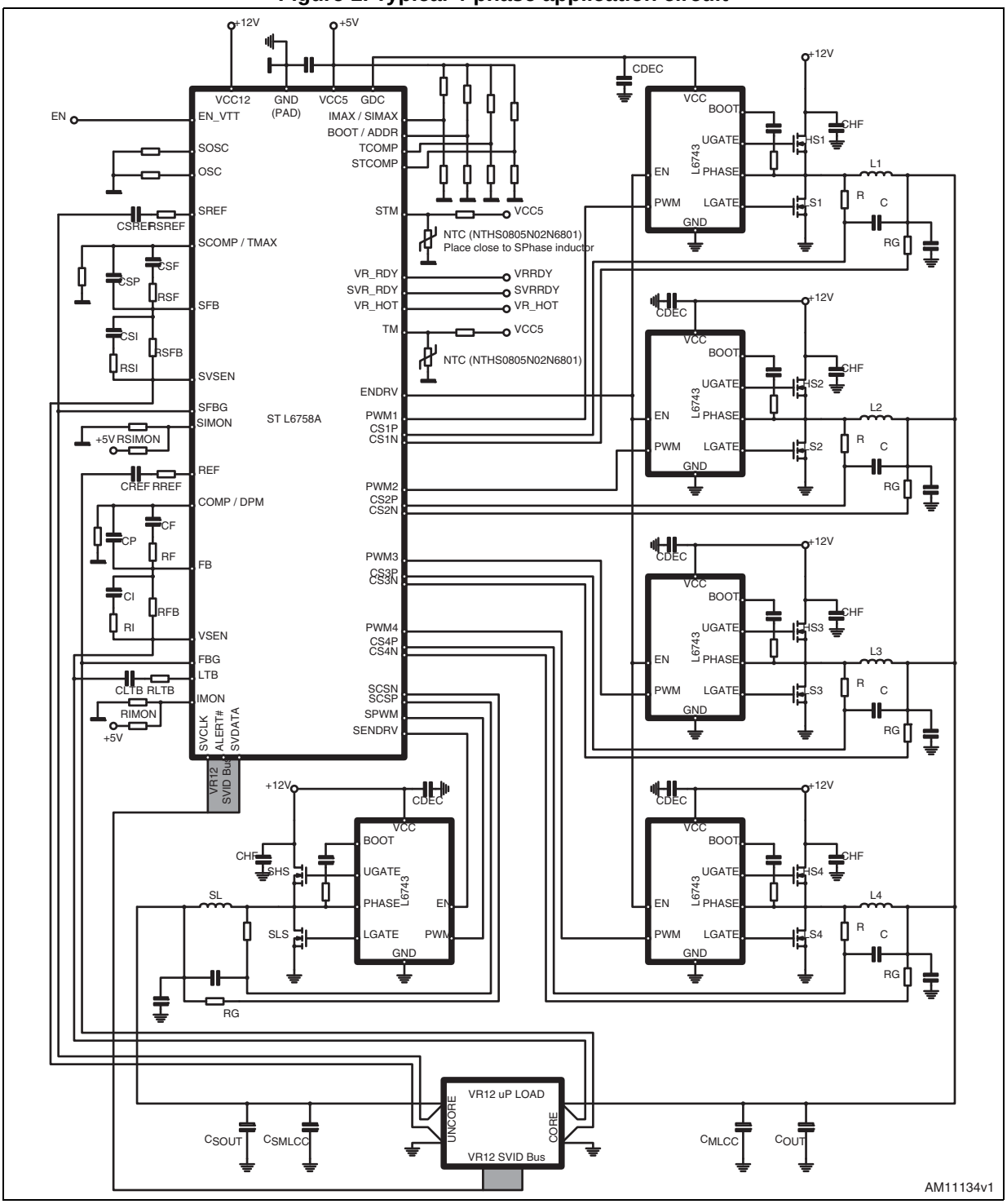
Order code	Package	Packaging
L6758A	VFQFPN48 6x6 mm	Tray
L6758ATR	VFQFPN48 6x6 mm	Tape and reel

Contents

1 Typical application circuit and block diagram

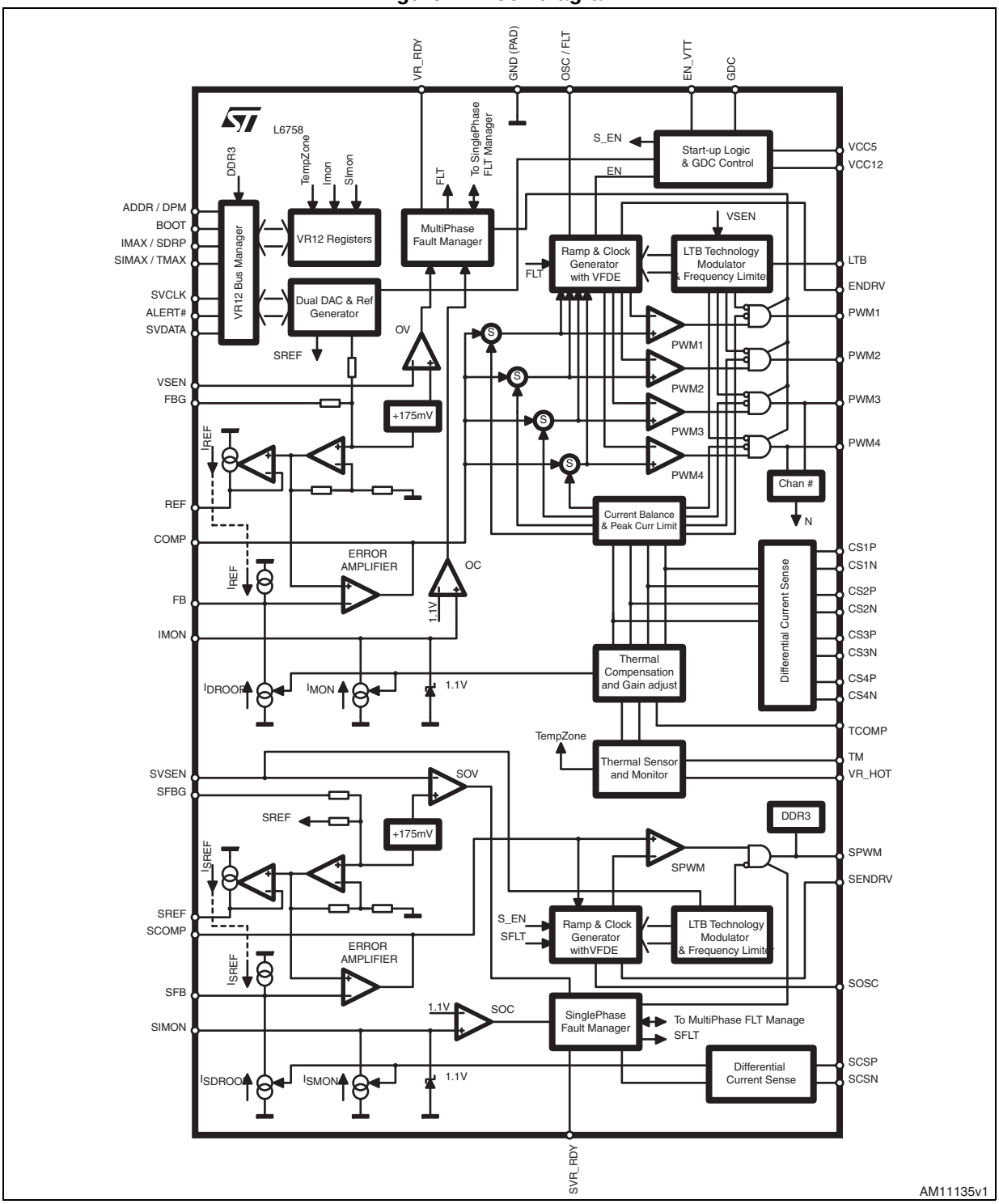
1.1 Application circuit

Figure 1. Typical 4-phase application circuit



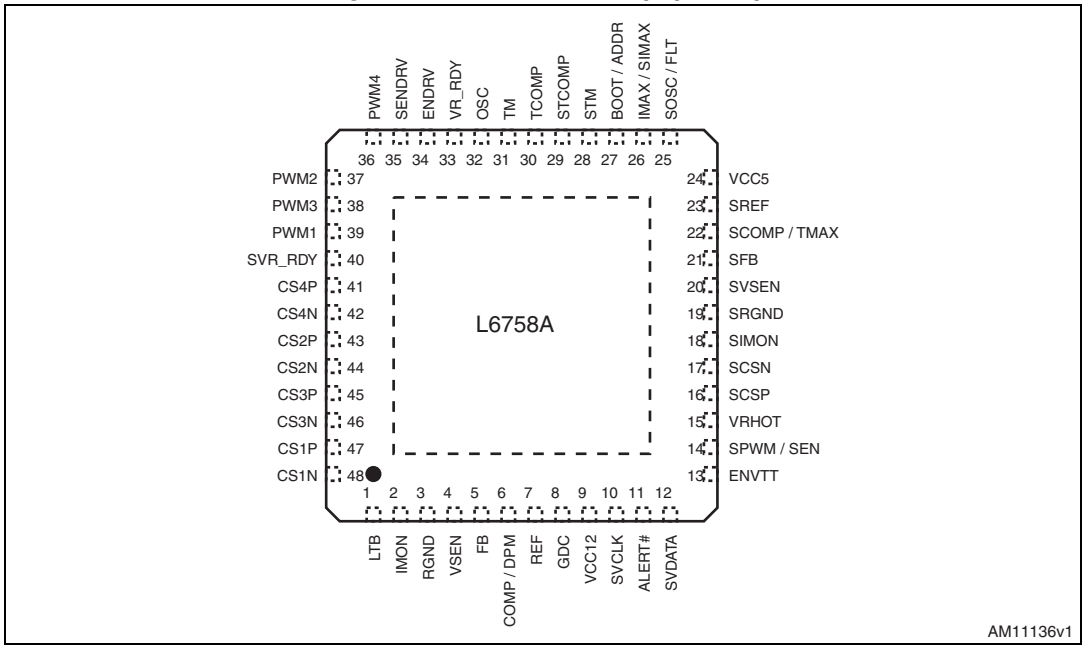
1.2 Block diagram

Figure 2. Block diagram



2 Pin description and connection diagrams

Figure 3. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin#	Name	Function	
1	LTB	Multi-phase section	LTB Technology input pin. See *Section 11.2* for details.
2	IMON		Current monitor output. A current proportional to the multi-phase load current is sourced from this pin. Connect through a resistor R_{MON} to local GND. When the pin voltage reaches 1.55 V, overcurrent protection is set and the IC latches. Filtering through C_{IMON} to GND allows to control the delay for OC intervention.
3	RGND		Remote ground sense. Connect to the negative side of the load to perform remote sense.
4	VSEN		Output voltage monitor, manages OV and UV protection. Connect to the positive side of the load to perform remote sense. A fixed 50 µA current is sunk from this pin.
5	FB		Error amplifier inverting input. Connect with a resistor R_{FB} to VSEN and with an (R_F - C_F)// C_P to COMP.
6	COMP / DPM		Error amplifier output. Connect with an (R_F - C_F)// C_P to FB. The device cannot be disabled by pulling low this pin. Connect a proper resistor R_{DPM} to GND to define DPM strategy.

Table 2. Pin description (continued)

Pin#	Name	Function	
7	REF	Multi-phase section	The reference used for the regulation of the multi-phase section is available on this pin with -100 mV offset. Connect through an R_{REF}-C_{REF} to RGND to optimize DVID transitions. Connect through an R_{OS} resistor to FB pin to implement small positive offset to the regulation.
8	GDC		Gate drive control pin. Used for efficiency optimization, see *Section 9* for details. If not used, it can be left floating.
9	VCC12		+12 V bus monitor to synchronize startup. The IC waits for the 12 V to become available before implementing soft-start when enabled. Connect directly to the +12 V bus (i.e. the high-side MOSFET drain).
10	SVCLK	SVI bus	Serial clock.
11	ALERT#		Alert.
12	SVDATA		Serial data.
13	EN_VTT		VTT level sensitive enable pin (3.3 V compatible). Pull low to disable the device, pull up above the turn-on threshold to enable the controller.
14	SPWM / SEN	Single-ph section	PWM output. Connect to external driver PWM input. During normal operation the device is able to manage HiZ status by setting and holding the pin to a fixed voltage defined by PWMx strapping. Connect to VCC5 with 1 kΩ to disable single-phase section.
15	VR_HOT		Voltage regulator HOT. Open drain output; this is an alarm signal asserted by the controller when the temperature sensed through the TM and or ST pins exceed TMAX (active low). See *Section 8* for details.
16	SCSP	Single-phase section	Single-phase section current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
17	SCSN		Single-phase section current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
18	SIMON		Current monitor output. A current proportional to the single-phase current is sourced from this pin. Connect through a resistor R_{SIMON} to local GND. When the pin voltage reaches 1.55 V, overcurrent protection is set and the IC latches. Filtering through C_{SIMON} to GND allows to control the delay for OC intervention.
19	SRGND		Remote ground sense. Connect to the negative side of the load to perform remote sense.
20	SVSEN		Output voltage monitor, manages OV and UV protection. Connect to the positive side of the load to perform remote sense.
21	SFB		Error amplifier inverting input. Connect with a resistor R_{SFB} to SVSEN and with an (R_{SF} - C_{SF})// C_{SP} to SCOMP.

Table 2. Pin description (continued)

Pin#	Name	Function	
22	SCOMP / TMAX	Single-phase section	Error amplifier output. Connect with an (R_{SF} - C_{SF})// C_{SP} to SFB. The device cannot be disabled by pulling low this pin. Connect proper resistor R_{TMAX} to GND to define TMAX register.
23	SREF		The reference used for the regulation of the single-phase section is available on this pin with -100 mV offset. Connect through an R_{SREF}-C_{SREF} to SRGND to optimize DVID transitions. Connect through an R_{SOS} resistor to the SFB pin to implement small positive offset to the regulation.
24	VCC5		Main IC power supply. Operative voltage is 5 V ±5%. Filter with 1 µF MLCC to GND (typ.).
25	SOSC	Single-phase section	Oscillator pin. It allows the programming of the switching frequency F_{SSW} for the single-phase section. The pin is internally set to 1.0 V, frequency for single-phase is programmed according to the resistor connected to GND or VCC with a gain of 10 kHz/µA. Leaving the pin floating programs a switching frequency of 200 kHz. See *Section 10* for details.
26	IMAX / SIMAX	Pinstrapping	Connect a resistor divider to GND/VCC5 in order to define the IMAX register for both single-phase and multi-phase sections. See *Table 8*, *Table 10* and *Section 6* for details.
27	BOOT / ADDR		Connect a resistor divider to GND/VCC5 in order to define BOOT register and SVI address. See *Table 8* and *Section 6* for details.
28	STM	Single-phase section	Thermal monitor sensor. Connect with proper network embedding NTC to the single-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature zone register. By programming proper STCOMP gain, the IC also implements load-line thermal compensation for the single-phase section. Short to GND if not used. See *Section 8* for details.
29	STCOMP		Thermal monitor sensor gain. Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by ST to implement thermal compensation for the single-phase section. Short to GND to disable thermal compensation for single-phase. See *Section 8* for details.
30	TCOMP	Multi-ph section	Thermal monitor sensor gain. Connect proper resistor divider between VCC5 and GND to define the gain to apply to the signal sensed by TM to implement thermal compensation for the multi-phase section. Short to GND to disable thermal compensation for multi-phase. See *Section 8* for details.
31	TM	Multi-ph section	Thermal monitor sensor. Connect with proper network embedding NTC to the multi-phase power section. The IC senses the power section temperature and uses the information to define the VR_HOT signal and temperature zone register. By programming proper TCOMP gain, the IC also implements load-line thermal compensation for the multi-phase section. Short to GND if not used. See *Section 8* for details.

Table 2. Pin description (continued)

Pin#	Name	Function	
32	OSC	Multi-phase section	Oscillator pin. It allows the programming of the switching frequency F_{SW} for the multi-phase section. The pin is internally set to 1.0 V, frequency for multi-phase is programmed according to the resistor connected to GND or VCC with a gain of 10 kHz/µA. Leaving the pin floating programs a switching frequency of 200 kHz. Effective frequency observable on the load results as being multiplied by the number of active phases N. See *Section 10* for details.
33	VR_RDY		VR ready. Open drain output set free after SS has finished in multi-phase section and pulled low when triggering any protection. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
34	ENDRV		Enable driver. CMOS output driven high when the IC commands the drivers. Used in conjunction with the HiZ window on the PWM pins to optimize the multi-phase section overall efficiency. Connect directly to external driver enable pin.
35	SENDRV	Single-ph section	Enable driver. CMOS output driven high when the IC commands the drivers. Used in conjunction with the HiZ window on the PWM pins to optimize the single-phase section overall efficiency. Connect directly to external driver enable pin.
36	PWM4	Multi-phase section	PWM4 output. Connect to external driver PWM input. During normal operation the device is able to manage HiZ status by setting and holding the PWMx pin to fixed voltage. Pull to 5 V through a 1 k resistor to configure the multi-phase section to work at 3 phases.
37	PWM2		PWM2 output. Connect to external driver PWM input. This pin is also used to configure HiZ levels for compatibility with drivers and DrMOS. During normal operation the device is able to manage HiZ status by setting and holding the PWMx pin to pre-defined fixed voltage.
38	PWM3		PWM3 output. Connect to external driver PWM input. During normal operation the device is able to manage HiZ status by setting and holding the PWMx pin to fixed voltage. Pull to 5 V through 1 k resistor in conjunction with PWM4 to configure the multi-phase section to work at 2 phases.
39	PWM1	Multi-phase section	PWM1 output. Connect to external driver PWM input. This pin is also used to configure HiZ levels for compatibility with drivers and DrMOS. During normal operation the device is able to manage HiZ status by setting and holding the PWMx pin to pre-defined fixed voltage.

Table 2. Pin description (continued)

Pin#	Name	Function	
40	SVR_RDY	Single-ph section	VR ready. Open drain output set free after SS has finished in single-phase section and pulled low when triggering any protection. Pull up to a voltage lower than 3.3 V (typ.), if not used it can be left floating.
41	CS4P	Multi-phase section	Channel 4 current sense positive input. Connect through an R-C filter to the phase-side of the channel 4 inductor. When working at 2 or 3 phases, short to the regulated voltage.
42	CS4N		Channel 4 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at 2 or 3 phases, still connect through Rg to CS4+ and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.
43	CS2P		Channel 2 current sense positive input. Connect through an R-C filter to the phase-side of the channel 2 inductor.
44	CS2N		Channel 2 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
45	CS3P		Channel 3 current sense positive input. Connect through an R-C filter to the phase-side of the channel 3 inductor. When working at 2 phases, short to the regulated voltage.
46	CS3N		Channel 3 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. When working at 2 phases, still connect through Rg to CS3P and then to the regulated voltage. Filter the output-side of Rg with 100 nF (typ.) to GND.
47	CS1P		Channel 1 current sense positive input. Connect through an R-C filter to the phase-side of the channel 1 inductor.
48	CS1N		Channel 1 current sense negative input. Connect through an Rg resistor to the output-side of the channel inductor. Filter the output-side of Rg with 100 nF (typ.) to GND.
PAD	GND		GND connection. All internal references and logic are referenced to this pin. Filter to VCC with proper MLCC capacitor and connect to the PCB GND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction-to-ambient (device soldered on 2s2p PC board)	40	°C/W
R_{THJC}	Thermal resistance junction-to-case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC12, GDC	to GND	-0.3 to 14	V
VCC, STM, TM, SPWM, PWMx, SIMAX/IMAX, BOOT/ADDR, SENDRV, ENDRV,	to GND	-0.3 to 7	V
All other pins	to GND	-0.3 to 3.6	V

3.2 Electrical characteristics

Table 5. Electrical characteristics (V_{CC} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	EN = high		22		mA
		EN = low		15		mA
$UVLO_{VCC5}$	VCC turn-ON	VCC rising			4.1	V
	VCC turn-OFF	VCC falling	3.0			V
$UVLO_{VCC12}$	VCC12 turn-ON	VCC12 rising			6.5	V
	VCC12 turn-OFF	VCC12 falling	4.5			V
Oscillator, soft-start and enable						
F_{SW}	Main oscillator accuracy		180	200	220	kHz
	Oscillator adjustability	R_{OSC} = 30 kΩ to GND	450	500	550	kHz
F_{SSW}	Main oscillator accuracy		207	230	253	kHz
	Oscillator adjustability	R_{SOSC} = 30 kΩ to GND	493	580	667	kHz
ΔV_{OSC}	PWM ramp amplitude			1.5		V
FAULT	Voltage at pin SOSC	After any latch	3.0			V
	Voltage at pin OSC	After OVP latch	3.0			V
SOFT START	SS time	VBOOT > 0, from pinstrapping; multi-phase section	4	5	6	mV/µs
		VBOOT > 0, from pinstrapping; single-phase section	2	2.5	3	mV/µs

Table 5. Electrical characteristics (V_{CC} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
EN_VTT	Turn-ON	V_{ENVTT} rising			0.6	V
	Turn-OFF	V_{ENVTT} falling	0.4			V
	Leakage current			1		µA
SVI serial bus						
SVCLCK, SVDATA	Input high		0.6			V
	Input low				0.4	V
SVDATA, ALERT#	Voltage low (ACK)	I_{SINK} = -5 mA			50	mV
Reference and current reading						
k_{VID}	V_{OUT} accuracy (MPhase)	I_{OUT}=0 A; N=4; R_G=1 kΩ; R_{FB}=2.125 kΩ; VID > 1.000 V	-0.5	-	0.5	%
k_{SVID}	V_{OUT} accuracy (SPhase)	I_{OUT}=0 A; R_G=1.3 kΩ; R_{FB}=6.663 kΩ; VID > 1.000 V	-0.5	-	0.5	%
k_{VID}, k_{SVID}	V_{OUT} accuracy	VID = 0.8 V to 1 V	-5	-	5	mV
		VID < 0.8 V	-8	-	8	mV
Δ_{DROOP}	LL accuracy (MPhase) 0 to full load	I_{INFOx}=0; N=4; R_G=1 kΩ; R_{FB}=2.125 kΩ	-2	-	2	µA
		I_{INFOx}= 25 µA; N=4; R_G=1 kΩ; R_{FB}=2.125 kΩ	-3.5	-	3.5	µA
Δ_{SDROOP}	LL accuracy (SPhase) 0 to full load	I_{SCSN}=0; R_G=1.3 kΩ; R_{FB}=6.663 kΩ	-0.75	-	0.75	µA
		I_{SCSN}= 25 µA; R_G=1.3 kΩ; R_{FB}=6.663 kΩ	-1.5	-	1.5	µA
k_{IMON}	IMON accuracy (MPhase)	I_{INFOx}=0 µA; N=4; R_G=1 kΩ; R_{FB}=2.125 kΩ	0		1.5	µA
		I_{INFOx}=25 µA; N=4; R_G=1 kΩ; R_{FB}=2.125 kΩ	-2	-	2	µA
k_{SIMON}	SIMON accuracy (SPhase)	I_{SCSN}=25 µA; R_G=1.3 kΩ; R_{FB}=6.663 kΩ	0		0.75	µA
		I_{SCSN}=25 µA; R_G=1.3 kΩ; R_{FB}=6.663 kΩ	-1	-	1	µA
A_0	EA DC gain			100		dB
SR	Slew rate	COMP to SGND = 10 pF		20		V/µs
DVID	Slew rate fast	Multi-phase section	20			mV/µs
	Slew rate slow		5			mV/µs
DVID	Slew rate fast	Single-phase sections	10			mV/µs
	Slew rate slow		2.5			mV/µs

Table 5. Electrical characteristics (V_{CC} = 5 V ± 5%, T_J = 0 °C to 70 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IMON ADC	GetReg(15h)	V_{IMON} = 0.992 V		CC		Hex
	Accuracy		C0		CF	Hex
PWM outputs and ENDRV						
PWMx, SPWM	Output high	I = 1 mA		5		V
	Output low	I = -1 mA			0.2	V
I_{PWM1}	Test current	Sourced from pin, EN_VTT=0.		10		µA
I_{PWM2}	Test current			0		µA
$I_{PWMx, SPWM}$	Test current	Sourced from pin, EN_VTT=0.		-10		µA
(S) ENDRV	Voltage low	$I_{(S)ENDRV}$ = -4 mA; both sections			0.4	V
Protections (both sections)						
OVP	Overvoltage protection	VSEN rising; wrt Ref.	+125		+200	mV
UVP	Undervoltage protection	VSEN falling; wrt Ref; Ref > 500 mV	-525		-375	mV
FBR Disc	FB disconnection	V_{CS-} rising, above VSEN/SVSEN	650	700	750	mV
FBG Disc	FBG disconnection	EA NI input wrt VID	450	500	550	mV
VR_RDY, SVR_RDY	Voltage low	I = -4 mA			0.4	V
V_{OC_TOT}	Overcurrent threshold	V_{IMON}, V_{SIMON} rising	1.50	1.55	1.60	V
I_{OC_TH}	Constant current	MPhase only		35		µA
VR_HOT	Voltage low	I_{SINK} = -5 mA			13	Ω
GATE DRIVE CONTROL						
GDC	Max. current	Any PS.		200		mA
	Impedance	PS00h (GDC=VCC12)		6		Ω
		> PS00h; (GDC=VCC5)		6		Ω

4 VR12 serial data bus and IC configuration

The L6758A is fully compliant with Intel VR12/IMVP7 SVID protocol rev 1.5, document # 456098. To guarantee proper device and CPU operation, refer to this document for bus design and layout guidelines. Different platforms may require different pull-up impedance on the SVI bus. Impedance matching and spacing among SVDATA, SVCLK and ALERT# must be followed.

Table 6. VID table, both sections

HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]
0	0	0.000	4	0	0.565	8	0	0.885	C	0	1.205
0	1	0.250	4	1	0.570	8	1	0.890	C	1	1.210
0	2	0.255	4	2	0.575	8	2	0.895	C	2	1.215
0	3	0.260	4	3	0.580	8	3	0.900	C	3	1.220
0	4	0.265	4	4	0.585	8	4	0.905	C	4	1.225
0	5	0.270	4	5	0.590	8	5	0.910	C	5	1.230
0	6	0.275	4	6	0.595	8	6	0.915	C	6	1.235
0	7	0.280	4	7	0.600	8	7	0.920	C	7	1.240
0	8	0.285	4	8	0.605	8	8	0.925	C	8	1.245
0	9	0.290	4	9	0.610	8	9	0.930	C	9	1.250
0	A	0.295	4	A	0.615	8	A	0.935	C	A	1.255
0	B	0.300	4	B	0.620	8	B	0.940	C	B	1.260
0	C	0.305	4	C	0.625	8	C	0.945	C	C	1.265
0	D	0.310	4	D	0.630	8	D	0.950	C	D	1.270
0	E	0.315	4	E	0.635	8	E	0.955	C	E	1.275
0	F	0.320	4	F	0.640	8	F	0.960	C	F	1.280
1	0	0.325	5	0	0.645	9	0	0.965	D	0	1.285
1	1	0.330	5	1	0.650	9	1	0.970	D	1	1.290
1	2	0.335	5	2	0.655	9	2	0.975	D	2	1.295
1	3	0.340	5	3	0.660	9	3	0.980	D	3	1.300
1	4	0.345	5	4	0.665	9	4	0.985	D	4	1.305
1	5	0.350	5	5	0.670	9	5	0.990	D	5	1.310
1	6	0.355	5	6	0.675	9	6	0.995	D	6	1.315
1	7	0.360	5	7	0.680	9	7	1.000	D	7	1.320
1	8	0.365	5	8	0.685	9	8	1.005	D	8	1.325
1	9	0.370	5	9	0.690	9	9	1.010	D	9	1.330
1	A	0.375	5	A	0.695	9	A	1.015	D	A	1.335
1	B	0.380	5	B	0.700	9	B	1.020	D	B	1.340

Table 6. VID table, both sections (continued)

HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]
1	C	0.385	5	C	0.705	9	C	1.025	D	C	1.345
1	D	0.390	5	D	0.710	9	D	1.030	D	D	1.350
1	E	0.395	5	E	0.715	9	E	1.035	D	E	1.355
1	F	0.400	5	F	0.720	9	F	1.040	D	F	1.360
2	0	0.405	6	0	0.725	A	0	1.045	E	0	1.365
2	1	0.410	6	1	0.730	A	1	1.050	E	1	1.370
2	2	0.415	6	2	0.735	A	2	1.055	E	2	1.375
2	3	0.420	6	3	0.740	A	3	1.060	E	3	1.380
2	4	0.425	6	4	0.745	A	4	1.065	E	4	1.385
2	5	0.430	6	5	0.750	A	5	1.070	E	5	1.390
2	6	0.435	6	6	0.755	A	6	1.075	E	6	1.395
2	7	0.440	6	7	0.760	A	7	1.080	E	7	1.400
2	8	0.445	6	8	0.765	A	8	1.085	E	8	1.405
2	9	0.450	6	9	0.770	A	9	1.090	E	9	1.410
2	A	0.455	6	A	0.775	A	A	1.095	E	A	1.415
2	B	0.460	6	B	0.780	A	B	1.100	E	B	1.420
2	C	0.465	6	C	0.785	A	C	1.105	E	C	1.425
2	D	0.470	6	D	0.790	A	D	1.110	E	D	1.430
2	E	0.475	6	E	0.795	A	E	1.115	E	E	1.435
2	F	0.480	6	F	0.800	A	F	1.120	E	F	1.440
3	0	0.485	7	0	0.805	B	0	1.125	F	0	1.445
3	1	0.490	7	1	0.810	B	1	1.130	F	1	1.450
3	2	0.495	7	2	0.815	B	2	1.135	F	2	1.455
3	3	0.500	7	3	0.820	B	3	1.140	F	3	1.460
3	4	0.505	7	4	0.825	B	4	1.145	F	4	1.465
3	5	0.510	7	5	0.830	B	5	1.150	F	5	1.470
3	6	0.515	7	6	0.835	B	6	1.155	F	6	1.475
3	7	0.520	7	7	0.840	B	7	1.160	F	7	1.480
3	8	0.525	7	8	0.845	B	8	1.165	F	8	1.485
3	9	0.530	7	9	0.850	B	9	1.170	F	9	1.490
3	A	0.535	7	A	0.855	B	A	1.175	F	A	1.495
3	B	0.540	7	B	0.860	B	B	1.180	F	B	1.500
3	C	0.545	7	C	0.865	B	C	1.185	F	C	1.505
3	D	0.550	7	D	0.870	B	D	1.190	F	D	1.510

Table 6. VID table, both sections (continued)

HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]	HEX code		V_{OUT} [V]
3	E	0.555	7	E	0.875	B	E	1.195	F	E	1.515
3	F	0.560	7	F	0.880	B	F	1.200	F	F	1.520

Table 7. Phase number programming

	PWM1	PWM2	PWM3	PWM4	SPWM
3+1 phase	to driver			1 kΩ pull up to VCC5	to driver
2+1 phase	to driver		1 kΩ to VCC5		
3+0 phase	to driver			1 kΩ pull up to VCC5	1 kΩ pull up to VCC5
2+0 phase	to driver		1 kΩ to VCC5		

Table 8. IMAX / SIMAX pinstrapping (1)

R down [kΩ]	R up [kΩ]	IMAX / SIMAX		
		IMAX [A](2)	SIMAX [A]	
			GFX	VSA
10	1.5	N · 30 + 35	40	29
10	2.7		35	21
22	6.8		30	13
10	3.6		25	5
27	11	N · 30 + 30	40	29
12	5.6		35	21
82	43		30	13
13	7.5		25	5
56	36	N · 30 + 25	40	29
18	13		35	21
15	12		30	13
18	16		25	5
15	14.7	N · 30 + 20	40	29
10	11		35	21
18	22		30	13
56	75		25	5

Table 8. IMAX / SIMAX pinstrapping (1) (continued)

R down [kΩ]	R up [kΩ]	IMAX / SIMAX		
		IMAX [A](2)	SIMAX [A]	
			GFX	VSA
10	15	N · 30 + 15	40	29
12	20		35	21
12	22.6		30	13
39	82		25	5
47	110	N · 30 + 10	40	29
10	27		35	21
22	68		30	13
10	36		25	5
18	75	N · 30 + 5	40	29
15	75		35	21
10	59		30	13
10	75		25	5
10	100	N · 30	40	29
10	150		35	21
10	220		30	13
10	Open		25	5

1. Suggested values, divider must be connected between VCC5 pin and GND.
2. N is the number of phases programmed for the multi-phase section.

Table 9. BOOT / ADDR pinstrapping(1)

R down [kΩ]	R up [kΩ]	BOOT				ADDR[h](2)
		Multi-phase [V]	Single-phase [V]	Single-phase mode	Link-Rest	
10	1.5	0.000	1.100	VSA	1 µs	06
10	3.6	0.000	1.100	VSA	1 µs	00
27	11	0.000	1.000	VSA		06
13	7.5	0.000	1.000	VSA	1 µs	00
56	36	0.000	0.900	VSA		06
18	16	0.000	0.900	VSA	1 µs	00
15	14.7	0.000	1.100	GFX	32 µs	06
56	75	0.000	1.100	GFX	32 µs	00
10	15	1.100	1.100	GFX		06

Table 9. BOOT / ADDR pinstrapping(1) (continued)

R down [kΩ]	R up [kΩ]	BOOT				ADDR[h](2)
		Multi-phase [V]	Single-phase [V]	Single-phase mode	Link-Rest	
39	82	1.100	1.100	GFX	32 µs	00
47	110	1.000	1.000	GFX		06
10	36	1.000	1.000	GFX	32 µs	00
18	75	0.900	0.900	GFX		06
10	75	0.900	0.900	GFX	32 µs	00
10	100	0.000	0.000	GFX	1 µs	06
10	Open	0.000V	0.000	GFX	1 µs	00

1. Suggested values, divider must be connected between VCC5 pin and GND.
2. N is the number of phases programmed for the multi-phase section.

Table 10. Device configuration - single - phase section

Mode (from VBOOT)	VBOOT	DROOP	SIMAX [A]
GFX	See *Table 9*	Enabled	25 to 40
VSA		Disabled	5 to 29

Table 11. DPM and TMAX pinstrapping (see *Section 9.1*)

COMP/SCOMP	DPM threshold set	TMAX [C]
33 k to GND	Set 3	130
17.5 k to GND	Set 2	120
12.5 k to GND	Set 1	110
5.6 k to GND	OFF	100

5 Device description and operation

The L6758A is a programmable two-to-four phase PWM controller that provides complete control logic and protection to implement a high performance step-down DC-DC voltage regulator optimized for advanced microprocessor power supply. The device features 2nd generation LTB Technology: through a load transient detector, it is able to simultaneously turn on all the phases. This allows the output voltage deviation to be minimized and, in turn, the system cost to be minimized by providing the fastest response to a load transition.

The L6758A implements current reading across the inductor in fully-differential mode. A sense resistor in series to the inductor can be also considered in order to improve reading precision. The current information read corrects the PWM output in order to equalize the average current carried by each phase.

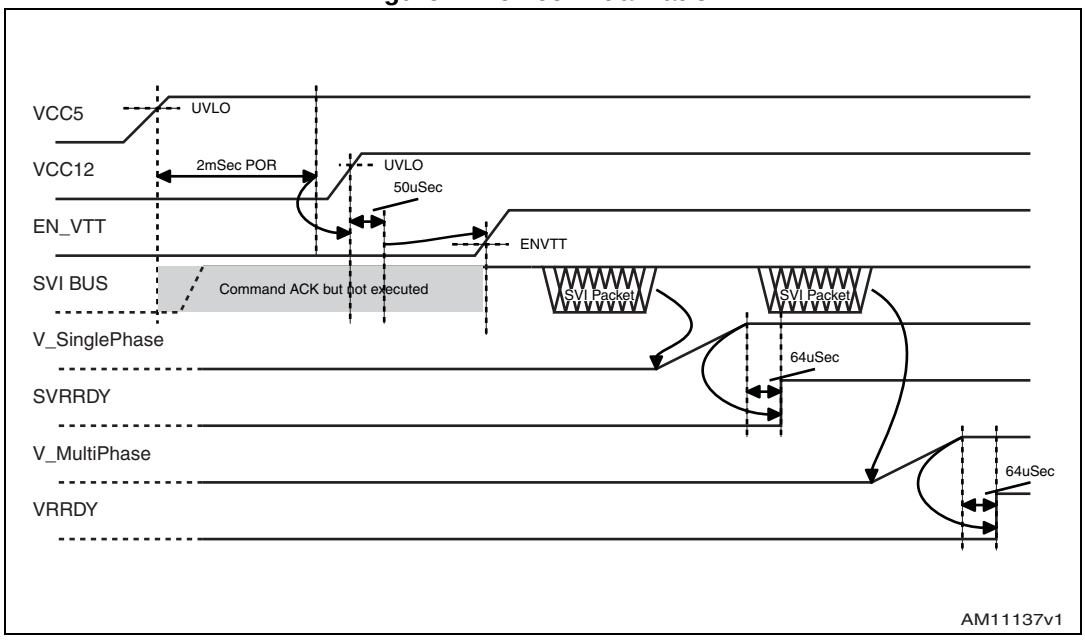
The controller supports VR12 specifications featuring 25 MHz SVI bus and all the required registers. The platform may program the defaults for these registers through dedicated pinstrapping.

A complete set of protection is available: overvoltage, undervoltage, overcurrent (per-phase and total) and feedback disconnection guarantee the load to be safe under all conditions.

Special power management features like DPM, VFDE and GDC modify phase number, gate driving voltage and switching frequency to optimize the efficiency over the load range.

The L6758A is available in VFQFPN48 with 6x6 mm body package.

Figure 4. Device initialization

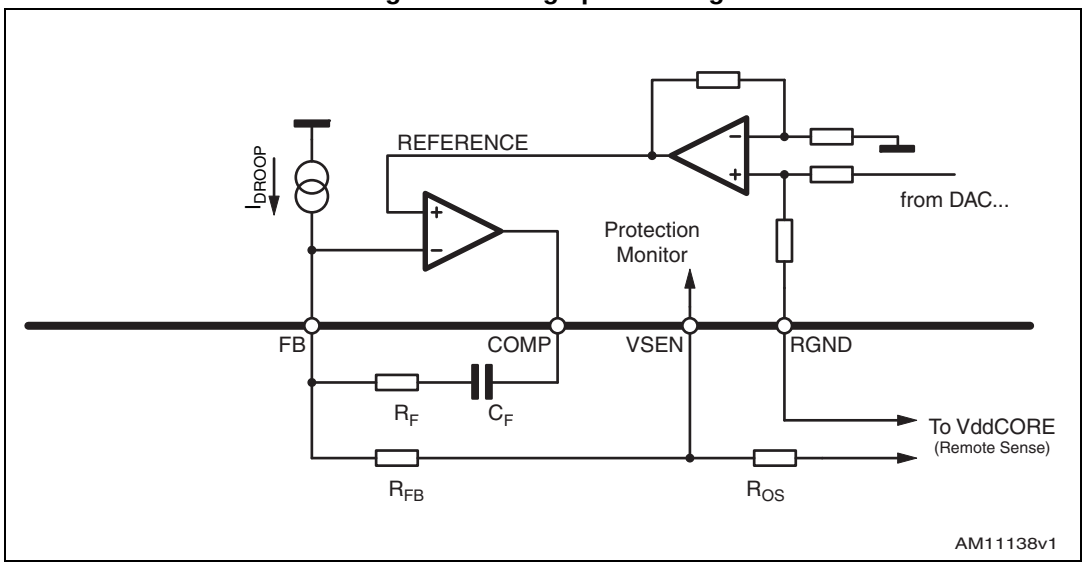


6 Output voltage positioning

Output voltage positioning is performed by selecting the controller operative-mode (*CPU, VSA* and *GFX*) for the two sections and by programming the droop function effect (see *Figure 5*). The controller reads the current delivered by each section by monitoring the voltage drop across the DCR inductors. The current (I_{DROOP} / I_{SDROOP}) sourced from the FB / SFB pins, directly proportional to the read current, causes the related section output voltage to vary according to the external R_{FB} / R_{SFB} resistor, therefore implementing the desired load-line effect.

The L6758A embeds a dual remote-sense buffer to sense remotely the regulated voltage of each section without any additional external components. In this way, the output voltage programmed is regulated compensating for board and socket losses. Keeping the sense traces parallel and guarded by a power plane results in common mode coupling for any picked-up noise.

Figure 5. Voltage positioning



6.1 Multi-phase section: phase # programming

The multi-phase section implements a flexible two-to-four interleaved-phase converter. To program the desired number of phases, pull up to VCC5 the PWMx signal that is not required to be used, according to *Table 6*.

Caution: For the disabled phase(s), the current reading pins must be properly connected to avoid errors in current sharing and voltage positioning: CSxP must be connected to the regulated output voltage while CSxN must be connected to CSxP through the same R_G resistor used for the active phases.

6.2 Multi-phase section: current reading and current sharing loop

The L6758A embeds a flexible, fully-differential current sense circuitry that is able to read across inductor parasitic resistance or across a sense resistor placed in series to the inductor element. The fully-differential current reading rejects noise and allows the placing of sensing elements in different locations without affecting the measurement accuracy. The trans-conductance ratio is issued by the external resistor R_G placed outside the chip between the CSxN pin toward the reading points. The current sense circuit always tracks the current information, the CSxP pin is used as a reference keeping the CSxN pin to this voltage. To correctly reproduce the inductor current an R-C filtering network must be introduced in parallel to the sensing element. The current that flows from the CSxN pin is then given by the following equation (see *Figure 6*):

Equation 1

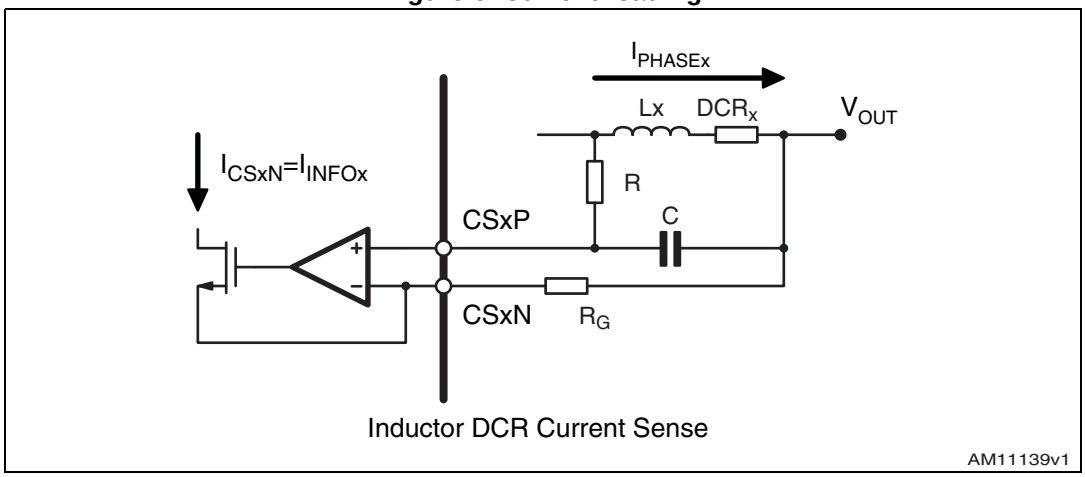
$$I_{CSxN} = \frac{DCR}{R_G} \cdot \frac{1 + s \cdot L/DCR}{1 + s \cdot R \cdot C} \cdot I_{PHASEx}$$

Considering now to match the time constant between the inductor and the R-C filter applied (time constant mismatches cause the introduction of poles into the current reading network causing instability. In addition, it is also important for the load transient response and to let the system show resistive equivalent output impedance), it results:

Equation 2

$$\frac{L}{DCR} = R \cdot C \quad \Rightarrow \quad I_{CSxN} = \frac{R_L}{R_G} \cdot I_{PHASEx} = I_{INFOx}$$

Figure 6. Current reading



The current read through the CSxP / CSxN pairs is converted into a current I_{INFOx} proportional to the current delivered by each phase and the information about the average current $I_{AVG} = \Sigma I_{INFOx} / N$ is internally built into the device (N is the number of working phases). The error between the read current I_{INFOx} and the reference I_{AVG} is then converted

into a voltage that, with a proper gain, is used to adjust the duty cycle whose dominant value is set by the voltage error amplifier in order to equalize the current carried by each phase.

6.3 Multi-phase section: defining load-line

The L6758A introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 6 shows the current sense circuit used to implement the load-line. The current flowing across the inductor(s) is read through the R-C filter across the CSxP and CSxN pins. R_G programs a trans-conductance gain and generates a current I_{CSx} proportional to the current of the phase. The sum of the I_{CSx} current is then sourced by the FB pin (I_{DROOP}). R_{FB} gives the final gain to program the desired load-line slope (*Figure 5*).

Time constant matching between the inductor (L / DCR) and the current reading filter (RC) is required to implement a real equivalent output impedance of the system and so avoiding over and/or undershoot of the output voltage as a consequence of a load transient. The output voltage characteristic vs. load current is then given by:

Equation 3

$$V_{OUT} = VID - R_{FB} \cdot I_{DROOP} = VID - R_{FB} \cdot \frac{DCR}{R_G} \cdot I_{OUT} = VID - R_{LL} \cdot I_{OUT}$$

where R_{LL} is the resulting load-line resistance implemented by the multi-phase section.

The R_{FB} resistor can be then designed according to the R_{LL} specifications as follows:

Equation 4

$$R_{FB} = R_{LL} \cdot \frac{R_G}{DCR}$$

6.4 Multi-phase section: IMON information

IMON is the analog information related to the current delivered by the VR which has a voltage digitized for VR12 current reporting. The pin sources a copy of the droop current:

Equation 5

$$I_{MON} = I_{DROOP} = \frac{DCR}{R_G} \cdot I_{OUT}$$

See *Section 6.2* for details about current reading.

The Iout register contains analog-to-digital conversion of the voltage present on the IMON pin considering the following relationships:

a) $V_{MON}=I_{MON} \cdot R_{IMON}$, where R_{IMON} is the resistor connected between IMON and GND.

b) IMON=1.24 V corresponds to IMAX. R_{IMON} is designed according to this relationship.

c) IMON=1.55 V sets the OC protection.

6.5 Single-phase section: current reading

The single-phase section performs the same differential current reading across DCR as the multi-phase section. According to *Section 6.2*, the current that flows from the SCSN pin is then given by the following equation (see *Figure 6*):

Equation 6

$$I_{SCSN} = \frac{DCR}{R_{SG}} \cdot I_{SOUT} = I_{SDROOP}$$

6.6 Single-phase section: defining load-line

This method introduces a dependence of the output voltage on the load current recovering part of the drop due to the output capacitor ESR in the load transient. Introducing a dependence of the output voltage on the load current, a static error, proportional to the output current, causes the output voltage to vary according to the sensed current.

Figure 6 shows the current sense circuit used to implement the load-line. The current flowing across the inductor DCR is read through R_{SG}. R_{SG} programs a trans-conductance gain and generates a current I_{SDROOP} proportional to the current delivered by the single-phase section that is then sourced from the SFB pin. R_{SFB} gives the final gain to program the desired load-line slope (*Figure 5*).

The output characteristic vs. load current is then given by:

Equation 7

$$V_{SOUT} = VID - R_{SFB} \cdot I_{SDROOP}$$

$$VID - R_{SFB} \cdot \frac{DCR}{R_{SG}} \cdot I_{SOUT} = VID - R_{SLL} \cdot I_{SOUT}$$

where R_{SLL} is the resulting load-line resistance implemented by the single-phase section.

The R_{SFB} resistor can be then designed according to the R_{SLL} as follows:

Equation 8

$$R_{SFB} = R_{SLL} \cdot \frac{R_{SG}}{DCR}$$

6.7 Dynamic VID transition support

The L6758A manages dynamic VID transitions that allow the output voltage of both sections to be modified during normal device operation for power management purposes. OV, UV signals are masked during every DVID transition and they are re-activated with proper delay to prevent from false triggering.

When changing dynamically the regulated voltage (DVID), the system needs to charge or discharge the output capacitor accordingly. This means that an extra-current I_{DVID} needs to be delivered (especially when increasing the output regulated voltage) and it must be considered when setting the overcurrent threshold of both sections. This current results:

Equation 9

$$I_{DVID} = C_{OUT} \cdot \frac{dV_{OUT}}{dT_{VID}}$$

where dV_{OUT} / dT_{VID} depends on the specific command issued (20 mV/µsec. for SetVID_Fast and 5 mV/µsec. for SetVID_Slow).

Overcoming the OC threshold during the dynamic VID causes the device to latch and disable.

As soon as the controller receives a new valid command to set the VID level for one (or both) of the two sections, the reference of the involved section steps up or down according to the target-VID with the programmed slope until the new code is reached. If a new valid command is issued during the transition, the device updates the target-VID level and performs the dynamic transition up to the new code. OV, UV are masked during the transition and re-activated with proper delay after the end of the transition to prevent from false triggering.

6.8 DVID optimization: REF/SREF

High slew rate for dynamic VID transitions cause overshoot and undershoot on the regulated voltage causing a violation in the microprocessor requirement. To compensate this behavior and to remove any over/undershoot in the transition, each section features DVID optimization circuit.

The reference used for the regulation is available on the REF/SREF pin (see *Figure 7*). Connect an R_{REF}/C_{REF} to GND (R_{SREF} / C_{SREF} for the single-phase) to optimize the DVID behavior. Components may be designed as follows (multi-phase, same equations apply to single-phase):

Equation 10

$$C_{REF} = C_F \cdot \left(1 - \frac{\Delta V_{OSC}}{k_V \cdot V_{IN}}\right)$$

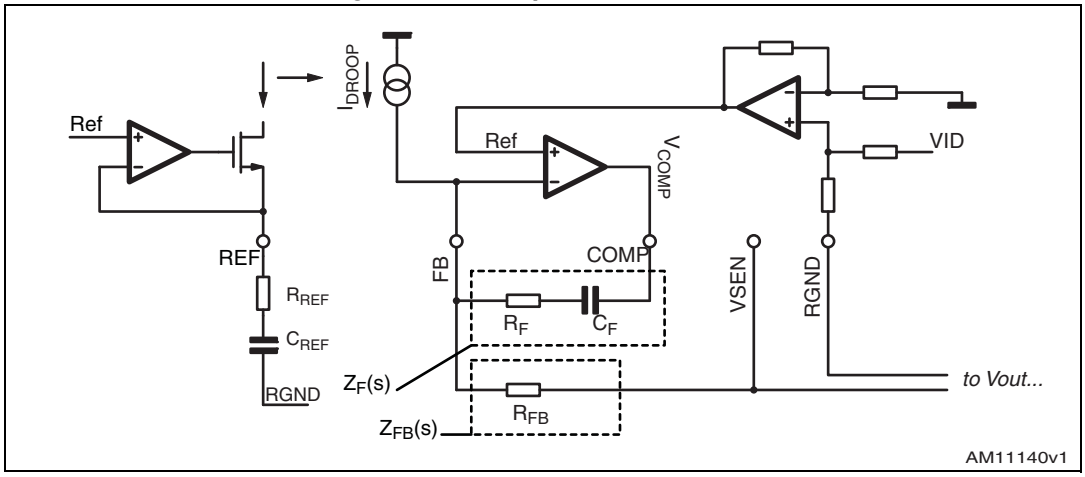
$$R_{REF} = \frac{R_F \cdot C_F}{C_{REF}}$$

where ΔVosc is the PWM ramp and k_V the gain for the voltage loop (see *Section 11*).

During a DVID transition, the REF pin moves according to the command issued (SetVIDFast, SetVIDSlow); the current requested to charge/discharge the R_{REF}/C_{REF}

network is mirrored and added to the droop current compensating for over/undershoot on the regulated voltage.

Figure 7. DVID optimization circuit



7 Output voltage monitoring and protection

The L6758A monitors the regulated voltage of both sections through pin VSEN and SVSEN in order to manage OV and UV. The device shows different thresholds when in different operative conditions but the behavior in response to a protection event is still the same as described below.

Protection is active also during soft-start while it is properly masked during DVID transitions with an additional delay to avoid false triggering.

Table 12. L6758A protection at a glance

	Section	
	Multi-phase	**Single-phase**
Overvoltage (OV)	VSEN, SVSEN = +175 mV above reference. *Action:* IC Latch; DVIDFast to 250 mV, LS=ON & PWMx = 0 if required to keep the regulation to 250 mV; other section: HiZ.	
Undervoltage (UV)	VSEN, SVSEN = 500 mV below reference. Active after Ref > 500 mV *Action:* IC Latch; both sections HiZ.	
Overcurrent (OC)	Current monitor across inductor DCR. Dual protection, per-phase and average. *Action:* UV-Like.	
Dynamic VID	Protection masked with additional delay to prevent from false triggering.	

7.1 Overvoltage

When the voltage sensed by VSEN and/or SVSEN overcomes the OV threshold, the controller acts in order to protect the load from excessive voltage levels avoiding any possible undershoot. To reach this target, a special sequence is performed as per the following list:

- The reference performs a DVID_Fast transition down to 250 mV on the section which triggered the OV protection.
- The PWMs of the section which triggered the protection are switched between HiZ and zero (ENDRV is kept high) in order to follow the voltage imposed by the DVID_Fast on-going. This limits the output voltage excursion, protects the load and assures no undershoot is generated (if V_{OUT} < 250 mV, the section is HiZ).
- The PWMs of the non-involved section are set permanently to HiZ (ENDRV is kept low) in order to realize a HiZ condition.
- OSC/ FLT pin is driven high.
- Power supply or EN pin cycling is required to restart operations.

If the cause of the failure is removed, the converter ends the transition with all PWMs in HiZ state and the output voltage of the section which triggered the protection lower than 250 mV.

7.2 Overcurrent

The overcurrent threshold must be programmed to a safe value, in order to be sure that each section does not enter OC during normal operation of the device. This value must take into consideration also the extra current needed during the DVID transition (I_{DVID}) and the process spread and temperature variations of the sensing elements (inductor DCR).

7.2.1 Multi-phase section

The L6758A performs two different types of OC protection for the multi-phase section: it monitors both the total current and the per-phase current and allows an OC threshold to be set for both.

- Per-phase OC
  - Maximum information current per-phase (I_{INFOx}) is internally limited to 35 µA. This end-of-scale current (I_{OC_TH}) is compared with the information current generated for each phase (I_{INFOx}). If the current information for the single-phase exceeds the end-of-scale current (i.e. if $I_{INFOx} > I_{OC\_TH}$), the device turns on the LS MOSFET until the threshold is re-crossed (i.e. until $I_{INFOx} < I_{OC\_TH}$).
- Total current OC
  - The IMON pin allows a maximum total output current to be defined for the system (I_{OC_TOT}). I_{MON} current is sourced from the IMON pin. By connecting a resistor R_{IMON} to SGND, a load indicator with 1.55 V (V_{OC_TOT}) end-of-scale can be implemented. When the voltage present at the ILIM pin crosses V_{OC_TOT}, the device detects an OC and immediately latches with all the MOSFETs of all the sections OFF (HiZ).

Typical design considers the intervention of the total current OC before the per-phase OC, leaving this last one as an extreme-protection in case of hardware failures in the external components. Total current OC is dependant on the IMON design and on the application TDC and MAX current supported. The typical design flow is the following:

- Define the maximum total output current (I_{OC_TOT}) according to system requirements (I_{MAX}, I_{TDC}). Considering I_{MON} design, I_{MAX} must correspond to 1.24 V (for correct IMAX detection) so, I_{OC_TOT} results as defined, as a consequence:

$$I_{OC\_TOT} = I_{MAX} \cdot 1.55 / 1.24$$

- Design per-phase OC and RG resistor in order to have IINFOx = IOC_TH (35 mA) when IOUT is about 10% higher than the IOC_TOT current. It results:

$$R_G = \frac{(1.1 \cdot I_{OC\_TOT}) \cdot DCR}{N \cdot I_{OCTH}}$$

  where N is the number of phases and DCR the DC resistance of the inductors. R_G should be designed in worst-case conditions.
- Design the total current OC and R_{IMON} in order to have the IMON pin voltage to 1.24 V at the I_{MAX} current specified by the design. It results:

$$R_{IMON} = \frac{1.24V \cdot R_G}{I_{MAX} \cdot DCR} \qquad \left(I_{MON} = \frac{DCR}{R_G} \cdot I_{OUT}\right)$$

where I_{MAX} is max. current requested by the processor (see Intel docs for details).

– Adjust the defined values according to the bench test of the application.

– C_{IMON} in parallel to R_{IMON} can be added with proper time constant to prevent false OC tripping.

Note: This is the typical design flow. Custom design and specifications may require different settings and ratios between the per-phase OC threshold and the total current OC threshold. Applications with big ripple across inductors may be required to set per-phase OC to values different than 110%: design flow should be modified accordingly.

7.2.2 Overcurrent and power states

When the controller receives an SetPS command through the SVI interface, it automatically changes the number of working phases. In particular, the maximum number of phases which the L6758A may work in >PS00h is limited to 2 phases regardless of the number N configured in PS00h. The OC level is then scaled as the controller enters >PS00h, as per *Table 13*.

Table 13. Multi-phase section OC scaling and power states

N (active phases in PS00h)	OC level in PS00h	OC level in PS01h, PS02h
4	1.550 V	0.800 V
3		1.050 V
2		1.550 V

7.2.3 Single-phase section

The single-phase section features the same protection as the multi-phase section. All the previous relationships remain applicable upon updating variables, referencing them to the single-phase section and considering it is working in single-phase.

8 Single NTC thermal monitor and compensation

The L6758A features single NTC for thermal sensing for both thermal monitoring and compensation. The feature is per section, i.e. it is required to have one NTC per section which drives both thermal monitoring and thermal compensation. The thermal monitor consists of monitoring the converter temperature eventually reporting an alarm by asserting the VR_HOT signal. This is the base for the temperature zone register fill. Thermal compensation consists of compensating the inductor DCR derating with temperature, so preventing drifts in any variable correlated to the DCR: voltage positioning, overcurrent, IMON, current reporting. Both functions share the same thermal sensor (NTC) to optimize the overall application cost without compromising the performance.

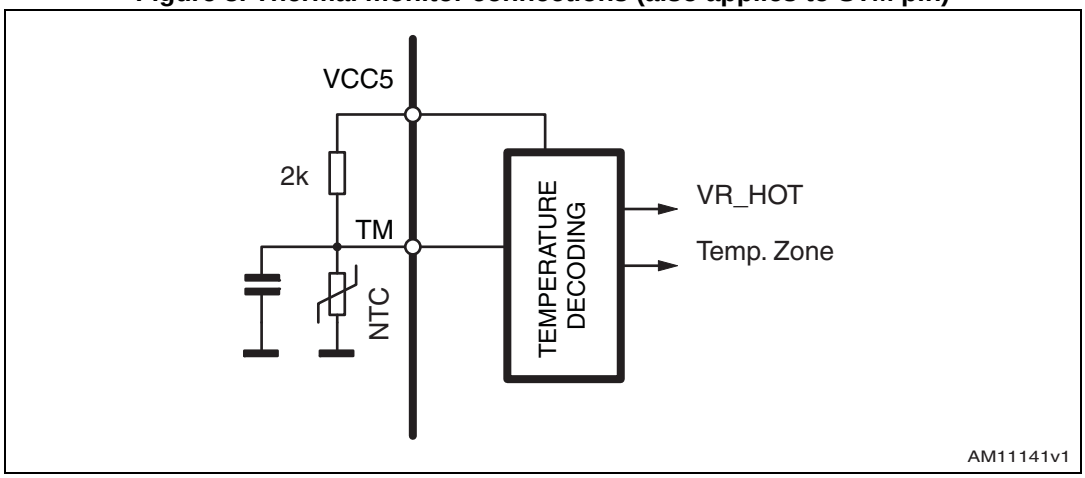
8.1 Thermal monitor and VR_HOT

The diagram for the thermal monitor is reported in *Figure 8*. NTC should be placed close to the power stage hot-spot in order to sense the regulator temperature. As the temperature of the power stage increases, the NTC resistive value decreases, therefore reducing the voltage observable at the TM and STM pins.

The recommended NTC is NTHS0805N02N6801 (or equivalent with $\beta_{25/75}$=3500 +/-10%) for accurate temperature sensing and thermal compensation. Different NTC may be used: to reach the required accuracy in temperature reporting, a proper resistive network must be used in order to match the resulting characteristic with the one coming from the recommended NTC.

The voltage observed at the TM / STM pins is internally converted and then used to fill in the temperature zone register of the related section. When the temperature observed exceeds TMAX (programmed via pinstrapping), the L6758A asserts VR_HOT (active low - as long as the overtemperature event lasts) and the ALERT# line (until reset by the GetReg command on the status register).

Figure 8. Thermal monitor connections (also applies to STM pin)



8.2 Thermal compensation

The L6758A supports DCR sensing for output voltage positioning: the same current information used for voltage positioning is used to define the overcurrent protection and the current reporting (register 15h in SVI). Having imprecise and temperature-dependant information leads to a violation of the specifications and misleading information returned to the SVI master: positive thermal coefficient specific to DCR must be compensated to obtain stable behavior of the converter as temperature increases. Uncompensated systems show temperature dependencies on the regulated voltage, overcurrent protection and current reporting (register 15h).

The temperature information available on the TM pin and used for the thermal monitor may be used also for this purpose. By comparing the voltage on the TM pin with the voltage present on the TCOMP pin, the L6758A corrects the I_{DROOP} current used for voltage positioning (see *Section 6.3*), therefore recovering the DCR temperature deviation. Depending on NTC location and distance from the inductors and the available airflow, the correlation between NTC temperature and DCR temperature may be different: TCOMP adjustments allow the gain between the sensed temperature and the correction made upon the I_{DROOP} current to be modified.

Short TCOMP to GND to disable thermal compensation (no correction is given to I_{DROOP}).

The same behavior also applies to the single-phase section (STM/STCOMP pins involved).

8.3 TM and TCOMP design

This procedure applies to both single-phase and multi-phase sections.

1. Properly choose the resistive network to be connected to the TM pin. The recommended values/network is reported in *Figure 8*.
2. Connect voltage generator to the TCOMP pin (default value 3.3 V).
3. Power on the converter and load the thermal design current (TDC) with the desired cooling conditions. Record the output voltage regulated as soon as the load is applied.
4. Wait for thermal steady-state. Adjust down the voltage generator on the TCOMP pin in order to get the same output voltage recorded at point #3.
5. Design the voltage divider connected to TCOMP (between VCC5 and GND) in order to get the same voltage set to TCOMP at point #4.
6. Repeat the test with the TCOMP divider designed at point #5 and verify the thermal drift is acceptable. In the case of positive drift (i.e. output voltage at thermal steady-state is bigger than output voltage immediately after loading TDC current), change the divider at the TCOMP pin in order to reduce the TCOMP voltage. In the case of negative drift (i.e. output voltage at thermal steady-state is smaller than output voltage immediately after loading TDC current), change the divider at the TCOMP pin in order to increase the TCOMP voltage.
7. The same procedure can be implemented with a variable resistor in place of one of the resistors of the divider. In this case, once the compensated configuration is found, simply replace the variable resistor with a resistor of the same value.

9 Efficiency optimization

As per VR12 specifications, the SVI master may define different power states for the VR controller. This is performed by SetPS commands. The L6758A re-configures itself to improve overall system efficiency according to *Table 14*.

Table 14. Efficiency optimization

Feature	PS00h	PS01h
DPM	According to pinstrapping	Active. 1phase/2phase according to Iout
VFDE	Active when in single-phase and DPM enabled	Active when in single-phase
GDC	12 V driving	GDC set to 5 V

9.1 Dynamic phase management (DPM)

Dynamic phase management allows the number of working phases to be adjusted according to the delivered current still maintaining the benefits of the multi-phase regulation.

Phase number is reduced by monitoring the voltage level across the IMON pin: the L6758A reduces the number of working phases according to the strategy defined by the DPM pinstrapping, see *Table 11*.

The current at which the transition happens (I_{DPM}) can be estimated as:

Equation 11

$$I_{DPM} = \frac{V_{DPM}}{R_{IMON}} \cdot \frac{R_G}{DCR}$$

where V_{DPM} thresholds are defined in *Table 15*. A hysteresis (50 mV typ.) is provided for each threshold in order to avoid multiple DPM actions triggering in steady load conditions.

Table 15. V_{DPM} Thresholds (I_{MON} rising-50 mV Hyst)

Comp/Scomp	DPM threshold set	1/2 phase transition	2/N phase transition
33 k to GND	Set 3	Vimon=200 mV	Vimon=350 mV
17.5 k to GND	Set 2	Vimon=150 mV	Vimon=275 mV
12.5 k to GND	Set 1	n/a	Vimon=150 mV
5.6 k to GND	OFF	n/a	n/a

When DPM is enabled, L6758A starts monitoring the IMON voltage for phase number modifications after VR_RDY has transition high: the soft-start is then implemented in interleaving mode with all the available phases enabled.

DPM is reset in case of a Set VID command that affects the CORE section and when LTB Technology detects a load transient. After being reset, if the voltage across IMON is compatible, DPM is re-enabled after proper delay.

Delay in the intervention of DPM can be adjusted by properly sizing the filter across the IMON pin. Increasing the capacitance results in increased delay in the DPM intervention.

9.2 Variable frequency diode emulation (VFDE)

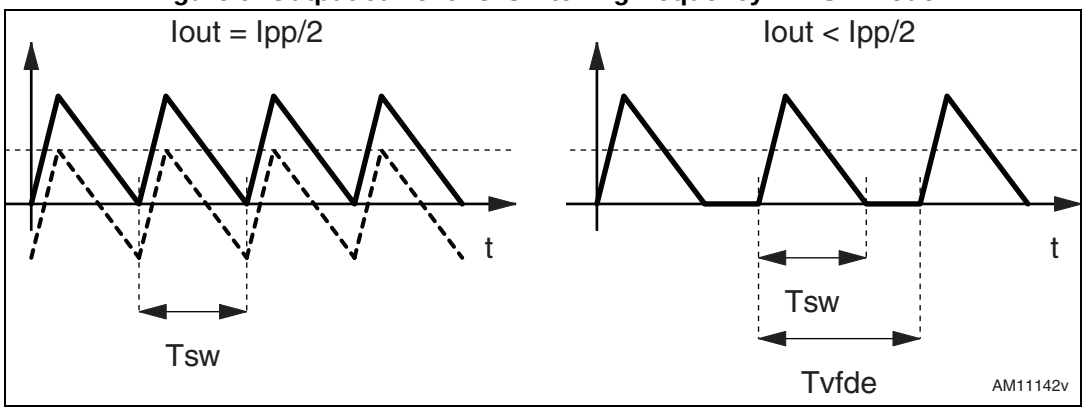
As the current required by the load is reduced, the L6758A progressively reduces the number of switching phases according to DPM settings on the multi-phase section. If single-phase operation is configured, when the delivered current approaches the CCM/DCM boundary, the controller enters VFDE operation. The single-phase section, being a single-phase, enters VFDE operation always when the delivered current approaches the CCM/DCM boundary.

In a common single-phase DC-DC converter, the boundary between CCM and DCM is when the delivered current is perfectly equal to 1/2 of the peak-to-peak ripple in the inductor (Iout = Ipp/2). Further decreasing the load in this condition maintaining CCM operation would cause the current in the inductor to reverse, therefore sinking current from the output for a part of the OFF-time. This results in a poorly efficient system.

The L6758A is able (via CSPx/CSNx pins) to detect the sign of the current across the inductor (zero cross detection, ZCD) so it is able to recognize when the delivered current approaches the CCM/DCM boundary. In VFDE operation, the controller fires the high-side MOSFET for a TON and the low side MOSFET for a TOFF (the same as when the controller works in CCM mode) and waits the necessary time until next firing in high-impedance (HiZ). The consequence of this behavior is a linear reduction of the “apparent” switching frequency that, in turn, results in an improvement of the efficiency of the converter when in very light load conditions.

To prevent entering the audible range, “apparent” switching frequency is reduced until 30 kHz.

Figure 9. Output current vs. switching frequency in PSK mode



10 Main oscillator

The internal oscillator generates the triangular waveform for the PWM, charging and discharging with a constant current an internal capacitor. The switching frequency for each channel, F_{SW}, F_{SSW}, is internally fixed at 200 kHz: the resulting switching frequency at the load side for the multi-phase section results in being multiplied by N (number of configured phases).

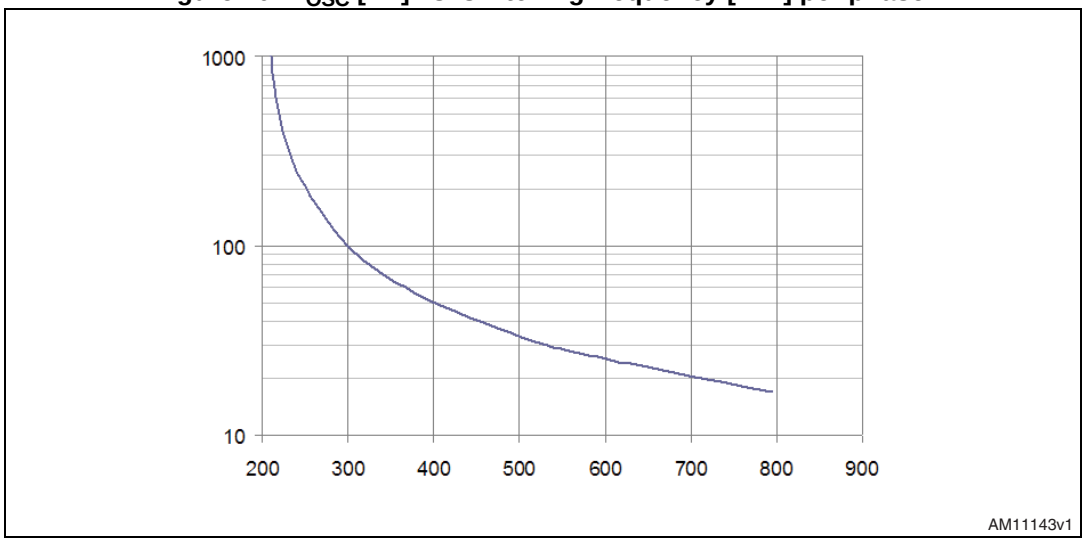
The current delivered to the oscillator is typically 20 µA (corresponding to the freerunning frequency F_{SW}=200 kHz) and it may be varied using an external resistor (R_{OSC}, R_{SOSC}) typically connected between the OSC, SOSC pins and GND. Since the OSC/SOSC pins are fixed at 1 V, the frequency is varied proportionally to the current sunk from the pin considering the internal gain of 10 KHz/µA for F_{SW} or 11 KHz/µA for F_{SSW} (see *Figure 10*).

Connecting R_{OSC} to SGND the frequency is increased (current is sunk from the pin), according to the following relationships:

Equation 12

$$F_{SW} = 200kHz + \frac{1.000V}{R_{OSC(k\Omega)}} \cdot 10\frac{kHz}{\mu A}$$

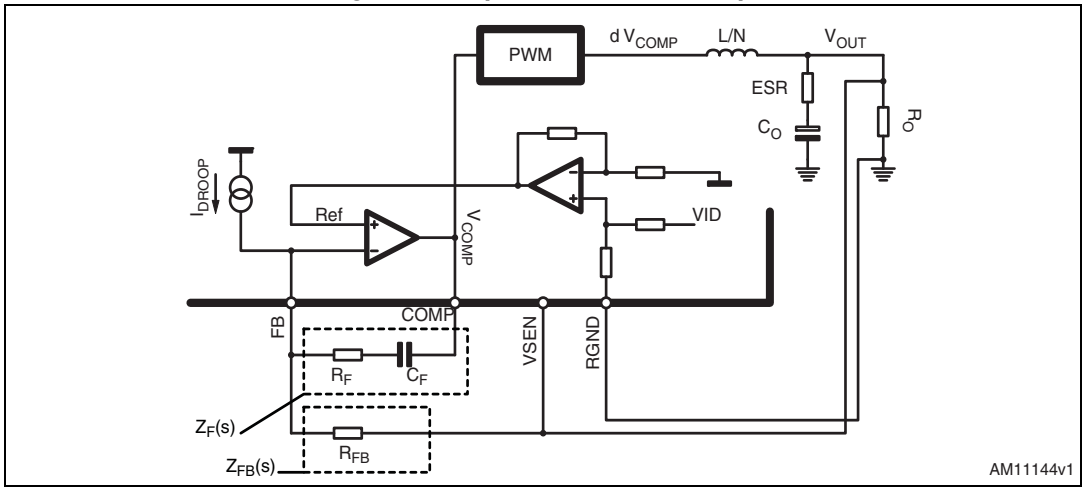
Figure 10. R_{OSC} [kΩ] vs. switching frequency [kHz] per phase.



11 System control loop compensation

The control system can be modeled with an equivalent single-phase converter whose only difference is the equivalent inductor L/N (where each phase has an L inductor and N is the number of the configured phases), see *Figure 11*.

Figure 11. Equivalent control loop.



The control loop gain results (obtained opening the loop after the COMP pin):

Equation 13

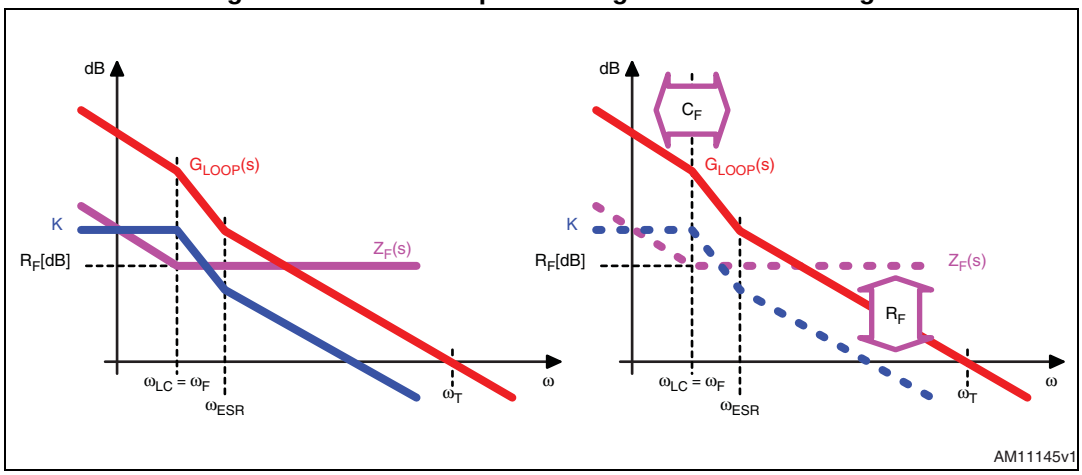
$$G_{LOOP}(s) = -\frac{PWM \cdot Z_F(s) \cdot (R_{LL} + Z_P(s))}{[Z_P(s) + Z_L(s)] \cdot \left[\frac{Z_F(s)}{A(s)} + \left(1 + \frac{1}{A(s)}\right) \cdot R_{FB}\right]}$$

where:

- R_{LL} is the equivalent output resistance determined by the droop function (voltage positioning)
- $Z_P(s)$ is the impedance resulting from the parallel of the output capacitor (and its ESR) and the applied load R_O
- $Z_F(s)$ is the compensation network impedance
- $Z_L(s)$ is the equivalent inductor impedance
- A(s) is the error amplifier gain
- $PWM = \frac{9}{10} \cdot \frac{V_{IN}}{\Delta V_{OSC}}$ is the PWM transfer function.

The control loop gain is designed in order to obtain a high DC gain to minimize static error and to cross the 0 dB axes with a constant -20 dB/dec slope with the desired crossover frequency ω_T. Neglecting the effect of $Z_F(s)$, the transfer function has one zero and two poles; both poles are fixed once the output filter is designed (LC filter resonance ω_{LC}) and the zero (ω_{ESR}) is fixed by ESR and the droop resistance.

Figure 12. Control loop bode diagram and fine tuning.



To obtain the desired shape, an R_F-C_F series network is considered for the $Z_F(s)$ implementation. A zero at $\omega_F=1/R_FC_F$ is then introduced together with an integrator. This integrator minimizes the static error while placing the zero ω_F in correspondence with the L-C resonance, assuring a simple -20 dB/dec shape of the gain.

In fact, considering the usual value for the output filter, the LC resonance results at a frequency lower than the above reported zero.

The compensation network can be designed as follows:

Equation 14

$$R_F = \frac{R_{FB} \cdot \Delta V_{OSC}}{V_{IN}} \cdot \frac{10}{9} \cdot \frac{F_{SW} \cdot L}{(R_{LL} + ESR)}$$

Equation 15

$$C_F = \frac{\sqrt{C_O \cdot L}}{R_F}$$

11.1 Compensation network guidelines

The compensation network design assures that the system responds according to the crossover frequency selected and to the output filter considered: it is anyway possible to further fine-tune the compensation network modifying the bandwidth in order to get the best response of the system, as follows (see *Figure 12*):

- Increase R_F to increase the system bandwidth accordingly
- Decrease R_F to decrease the system bandwidth accordingly
- Increase C_F to move ω_F to low frequencies increasing, as a consequence, the system phase margin.

Even though a fastest compensation network helps to satisfy the requirement of the load, the inductor still limits the maximum dI/dt that the system can afford. In fact, when a load transient is applied, the best that the controller can do is to “saturate” the duty cycle to its maximum (d_{MAX}) or minimum (0) value. The output voltage dV/dt is then limited by the inductor charge/discharge time and by the output capacitance. In particular, the most

limiting transition corresponds to the load-removal since the inductor results as being discharged only by V_{OUT} (while it is charged by V_{IN}-V_{OUT} during a load appliance).

Note: The introduction of a capacitor (C_I) in parallel to R_{FB} significantly speeds up the transient response by coupling the output voltage dV/dt on the FB pin, therefore using the error amplifier as a comparator. The COMP pin suddenly reacts and, also thanks to the LTB Technology control scheme, all the phases can be turned on together to immediately give the required energy to the output. Typical design considers starting from values in the range of 100 pF and validating the effect by bench testing. An additional series resistor (R_I) can also be used.

11.2 LTB technology

LTB technology further enhances the performance of the controller by reducing the system latencies and immediately turning ON all the phases to provide the correct amount of energy to the load optimizing the output capacitor count.

LTB technology monitors the output voltage through a dedicated pin detecting load-transients with selected dV/dt, it cancels the interleaved phase-shift, simultaneously turning on all phases.

The LTB detector is able to detect output load transients by coupling the output voltage through an R_{LTB} - C_{LTB} network. After detecting a load transient, all the phases are turned on together and the EA latencies result as bypassed as well.

Sensitivity of the load transient detector can be programmed in order to control precisely both the undershoot and the ring-back.

LTB technology design tips.

- Decrease R_{LTB} to increase the system sensitivity making the system sensitive to smaller dV_{OUT}.
- Increase C_{LTB} to increase the system sensitivity making the system sensitive to higher dV/dt.
- Increase R_i to increase the width of the LTB pulse.
- Increase C_i to increase the LTB sensitivity over frequency.

12 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at *www.st.com*. ECOPACK is an ST trademark.

Table 16. VFQFPN48 6x6x1.0 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.25	4.40	4.50
E2	4.25	4.40	4.50
e		0.40	
L	0.35	0.45	0.55

Figure 13. VFQFPN48 6x6x1.0 drawing

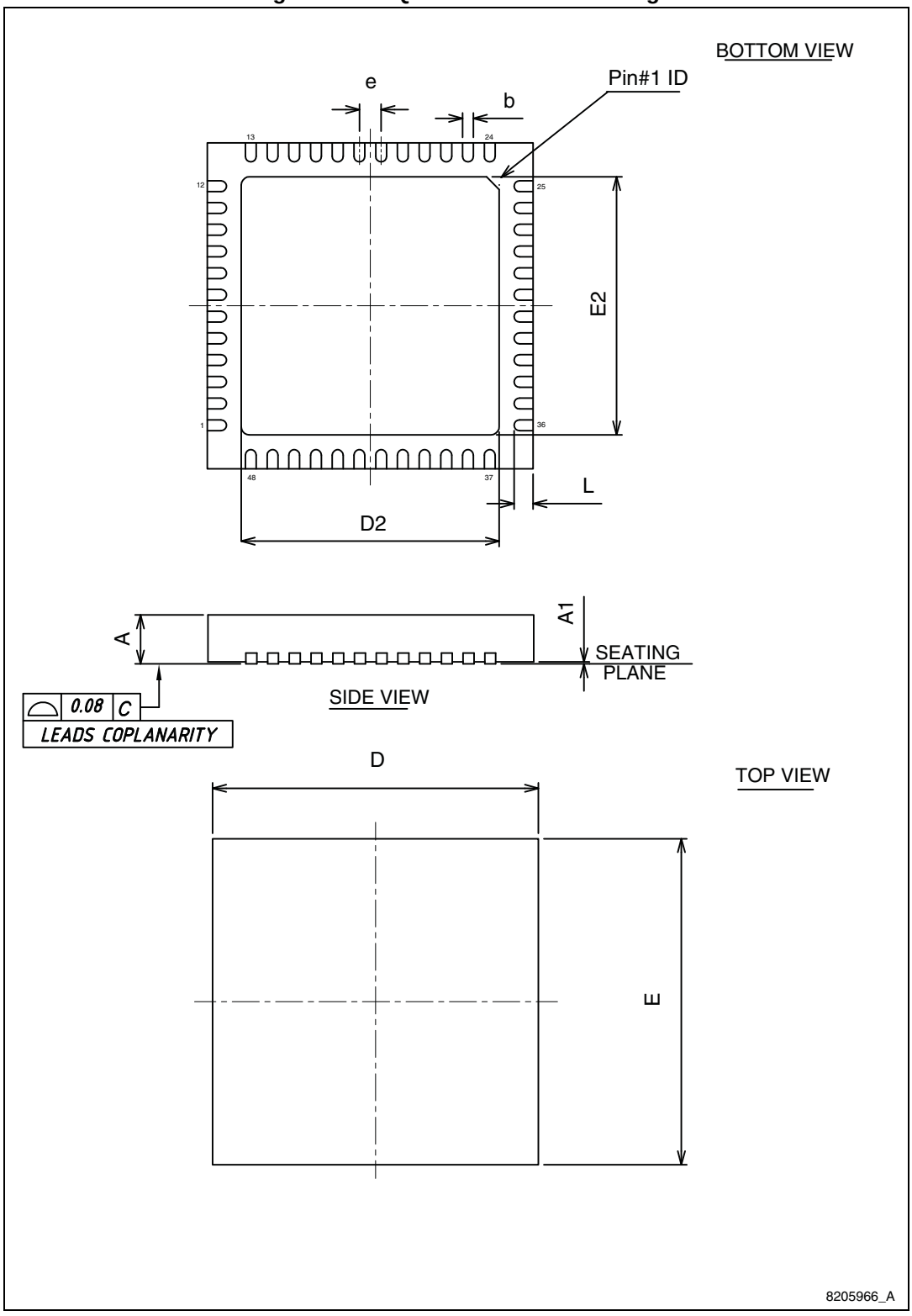
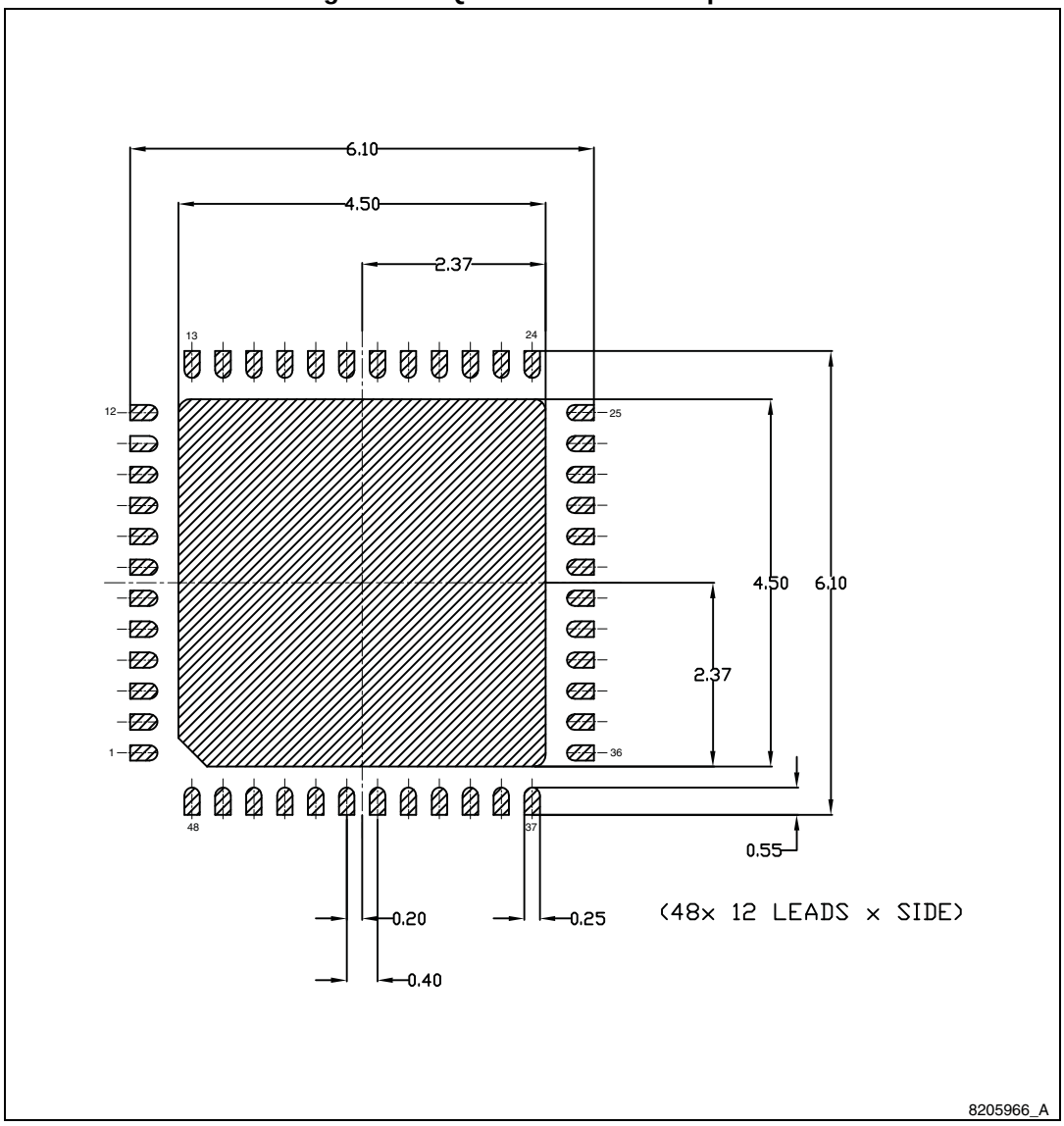


Figure 14. FQFPN48 6x6x1.0 footprint



13 Revision history

Table 17. Document revision history

Date	Revision	Changes
03-Sep-2012	1	Initial release.
10-Jul-2013	2	Updated *Table 16: VFQFPN48 6x6x1.0 mechanical data*.