
IWR1642 Single-Chip 76- to 81-GHz mmWave Sensor

1 Device Overview

1.1 Features

- FMCW Transceiver
 - Integrated PLL, Transmitter, Receiver, Baseband, and A2D
 - 76- to 81-GHz Coverage With 4-GHz Continuous Bandwidth
 - Four Receive Channels
 - Two Transmit Channels
 - Ultra-Accurate Chirp (Timing) Engine Based on Fractional-N PLL
 - TX Power: 12.5 dBm
 - RX Noise Figure:
 - 14 dB (76 to 77 GHz)
 - 15 dB (77 to 81 GHz)
 - Phase Noise at 1 MHz:
 - –95 dBc/Hz (76 to 77 GHz)
 - –93 dBc/Hz (77 to 81 GHz)
- Built-in Calibration and Self-Test (Monitoring)
 - ARM® Cortex®-R4F-Based Radio Control System
 - Built-in Firmware (ROM)
 - Self-calibrating System Across Frequency and Temperature
- C674x DSP for FMCW Signal Processing
- On-Chip Memory: 1.5MB
- Cortex-R4F Microcontroller for Object Tracking, Classification, and Interface Control
 - Supports Autonomous Mode (Loading User Application from QSPI Flash Memory)
- Internal Memories With ECC
- Integrated Peripherals
 - Up to 6 ADC Channels
 - Up to 2 SPI Channels
 - Up to 2 UARTs
 - CAN Interface
 - I²C
 - GPIOs
 - 2-Lane LVDS Interface for Raw ADC Data and Debug Instrumentation
- IWR1642 Advanced Features
 - Embedded Self-monitoring With No Host Processor Involvement
 - Complex Baseband Architecture
 - Embedded Interference Detection Capability
- Power Management
 - Built-in LDO Network for Enhanced PSRR
 - I/Os Support Dual Voltage 3.3 V/1.8 V
- Clock Source
 - Supports External Oscillator at 40 MHz
 - Supports Externally Driven Clock (Square/Sine) at 40 MHz
 - Supports 40 MHz Crystal Connection with Load Capacitors
- Easy Hardware Design
 - 0.65-mm Pitch, 161-Pin 10.4 mm × 10.4 mm Flip Chip BGA Package for Easy Assembly and Low-Cost PCB Design
 - Small Solution Size
- Operating Conditions
 - Junction Temp Range: –40°C to 105°C

1.2 Applications

- Industrial Sensor for Measuring Range, Velocity, and Angle
- Tank Level Probing Radar
- Displacement Sensing
- Field Transmitters
- Traffic Monitoring
- Proximity Sensing
- Security and Surveillance
- Factory Automation Safety Guards
- People Counting
- Motion Detection



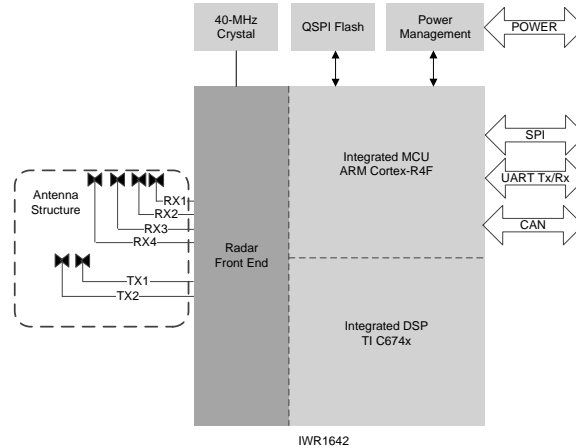


Figure 1-1. Autonomous Sensor For Industrial Applications

1.3 Description

The IWR1642 device is an integrated single-chip mmWave sensor based on FMCW radar technology capable of operation in the 76- to 81-GHz band with up to 4 GHz continuous chirp. The device is built with TI's low-power 45-nm RFCMOS process, and this solution enables unprecedented levels of integration in an extremely small form factor. The IWR1642 is an ideal solution for low-power, self-monitored, ultra-accurate radar systems in industrial applications such as building automation, factory automation, drones, material handling, traffic monitoring, and surveillance.

The IWR1642 device is a self-contained, single-chip solution that simplifies the implementation of mmWave sensors in the band of 76 to 81 GHz. IWR1642 includes a monolithic implementation of a 2TX, 4RX system with built-in PLL and A2D converters. The IWR1642 also integrates a DSP subsystem, which contains TI's high-performance C674x DSP for the radar signal processing. The device includes an ARM R4F-based processor subsystem, which is responsible for front-end configuration, control, and calibration. Simple programming model changes can enable a wide variety of sensor implementation with the possibility of dynamic reconfiguration for implementing a multimode sensor. Additionally, the device is provided as a complete platform solution including reference hardware design, software drivers, sample configurations, API guide, training, and user documentation.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE |
|-------------------------------|-------------|-------------------|
| IWR1642AQAGABL (Tray) | FCBGA (161) | 10.4 mm × 10.4 mm |
| IWR1642AQAGABLR (Tape & Reel) | | |

(1) For more information, see [Section 10, Mechanical Packaging and Orderable Information](#).

1.4 Functional Block Diagram

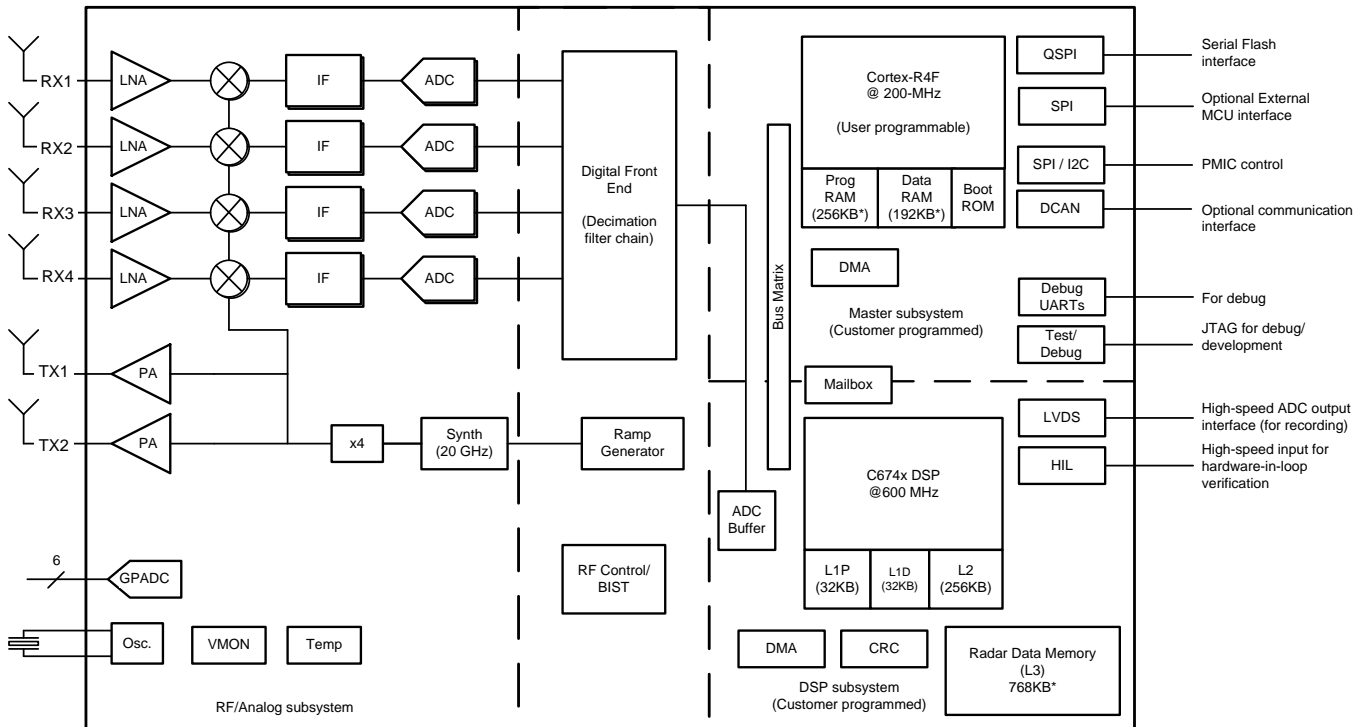


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| 5.8 CPU Specifications | 36 | 10 Mechanical, Packaging, and Orderable Information | 77 |
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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from August 31, 2017 to April 30, 2018 | Page |
|--|--------------------|
| • Updated/Changed TX Power from "12 dBm" to "12.5 dBm" | 1 |
| • Updated/Changed RX Noise Figure from "15 dB (76 to 77 GHz)" to "14 dB (76 to 77 GHz)" | 1 |
| • Updated/Changed RX Noise Figure from "16 dB (77 to 81 GHz)" to "15 dB (77 to 81 GHz)" | 1 |
| • Updated/Changed Phase Noise at 1 MHz from "–93 dBc/Hz (76 to 77 GHz)" to "–95 dBc/Hz (76 to 77 GHz)" | 1 |
| • Updated/Changed Phase Noise at 1 MHz from "–91 dBc/Hz (77 to 81 GHz)" to "–93 dBc/Hz (77 to 81 GHz)" | 1 |
| • Updated/Changed Features from "...Object Detection and Interface Control" to "...Object Tracking, Classification, and Interface Control" | 1 |
| • Updated/Changed Features from "Supports Crystal Connection..." to "Supports 40 MHz Crystal Connection..." | 1 |
| • Added "People Counting" and "Motion Detection" to Applications | 1 |
| • Updated/Changed caption from "Autonomous Radar Sensor..." to "Automotive Sensor..." | 2 |
| • Added Tray PART NUMBER to Device Information | 2 |
| • Updated/Changed Device Information from "XI1642QGABL (Reel)" to "IWR1642AQAGABLR (Reel)" | 2 |
| • Updated RX and TX connections in <i>Functional Block Diagram</i> | 3 |
| • Added RF Control/BIST block to <i>Functional Block Diagram</i> | 3 |
| • Removed "Cascade (20-GHz sync)" from Device Features Comparison | 7 |
| • Updated/Changed pin B15 to GPIO_41 in <i>Pin Diagram</i> | 10 |
| • Corrected A10 pin to "VOUT_14APLL" | 10 |
| • Updated/Changed pin N14 from "RESERVED" to "DMM_SYNC" in <i>Pin Diagram</i> | 10 |
| • Updated/Changed Pin Attributes (ABL0161 Package) to match the AWR1642 device | 14 |
| • Updated/Changed all instances of "CAN_FD_tx" to "Reserved" in Pin Attributes (ABL0161 Package) | 15 |
| • Updated/Changed all instances of "CAN_FD_rx" to "Reserved" in Pin Attributes (ABL0161 Package) | 15 |
| • Added two register tables after Pin Attributes | 21 |
| • Updated/Changed PAD IO Control Registers | 21 |
| • Cleaned up CLKP and CLKM signals in Signal Descriptions - Analog | 27 |
| • Removed R14 from Power supply VIOIN | 27 |
| • Added pin R15 to Power supply VSS | 28 |
| • Removed duplicate Pin Multiplexing table | 29 |
| • Updated/Changed all CAN_FD to Reserved | 29 |
| • Cleaned up VIN_13RF1 and VIN_13F2 in Absolute Maximum Ratings | 32 |
| • Updated/Changed CLKP, CLKM row in Absolute Maximum ratings from "Input ports for reference crystal" to "Input ports for reference crystal, or external oscillator input" | 32 |
| • Added table note to ESD Ratings | 32 |
| • Updated/Changed Power-On Hours (POH) | 32 |
| • Added VIN_18VCO row to Recommended Operating Conditions | 33 |
| • Updated/Changed V _{IL} in Recommended Operating Conditions | 33 |
| • Updated/Changed V _{OH} MIN from "85% VIOIN" to "VIOIN – 450" | 33 |
| • Updated/Changed V _{OL} MAX from "350" to "450" | 33 |
| • Added NRESET row to Recommended Operating Conditions | 33 |
| • Updated/Changed <i>Ripple Specifications</i> FREQUENCY from "4200" to "4400" | 34 |
| • Updated Average Power Consumption at Power Terminals | 34 |
| • Updated/Changed RF Specification to match AWR16 | 35 |
| • Updated/Changed IMRR TYP from 40 dB to 21 dB | 35 |
| • Updated/Changed Power Supply Sequencing and Reset Timing image | 37 |
| • Updated/Changed Clock Specifications text from "(that is, a 40-MHz crystal) " to "(that is, a 40-MHz crystal or external oscillator to CLKP) " | 38 |
| • Updated/Changed <i>Crystal Implementation</i> image from "40 and 50 MHz" to "40 MHz" | 38 |
| • Updated/Changed f _p Parallel resonance crystal frequency from " 40, 50" to "40" | 38 |
| • Added External Clock Mode Specifications | 39 |
| • Removed External Clock Electrical Characteristics table | 39 |
| • Updated/Changed External Clock Mode Specifications table to match AWR16 | 39 |
| • Updated SPI Slave Mode Switching Parameters | 45 |
| • Updated SPI Slave Mode Timing Requirements | 45 |
| • Updated/Changed all MIN values in Timing Requirements for QSPI Input (Read) Timings | 54 |
| • Added "People Counting" and "Gesturing" to Detailed Description Overview | 60 |

- Updated/Changed *Clock Subsystem* diagram..... [61](#)
- Updated/Changed Host Interrupt bullet in Host Interface [64](#)
- Removed Security Modules from *Master Subsystem, Cortex-R4F Memory Map* [65](#)
- Removed "...and ENOB of ~9 bits" from ADC Channels (Service) for User Application [68](#)
- Updated/Changed text from "ADC channel mapped to B12" to "GPADC channel 6" [68](#)
- Updated/Changed *GP-ADC Parameter* table to match AWR16 [68](#)
- Updated/Changed Monitoring and Diagnostic Mechanisms [70](#)
- Added "People counting", "Gesturing", and "Motion detection" to Application Information..... [72](#)
- Updated/Changed the *Device Nomenclature* image [75](#)

3 Device Comparison

Table 3-1. Device Features Comparison

| FUNCTION | | IWR1443 | IWR1642 |
|---|---|-------------------|-------------------|
| Number of receivers | | 4 | 4 |
| Number of transmitters | | 3 | 2 |
| On-chip memory | | 576KB | 1.5MB |
| Max I/F (Intermediate Frequency) (MHz) | | 15 | 5 |
| Max real sampling rate (Msps) | | 37.5 | 12.5 |
| Max complex sampling rate (Msps) | | 18.75 | 6.25 |
| Processor | | | |
| MCU (R4F) | | Yes | Yes |
| DSP (C674x) | | — | Yes |
| Peripherals | | | |
| Serial Peripheral Interface (SPI) ports | | 1 | 2 |
| Quad Serial Peripheral Interface (QSPI) | | Yes | Yes |
| Inter-Integrated Circuit (I ² C) interface | | 1 | 1 |
| Controller Area Network (DCAN) interface | | Yes | Yes |
| Trace | | — | Yes |
| PWM | | — | Yes |
| Hardware In Loop (HIL/DMM) | | — | Yes |
| GPADC | | Yes | Yes |
| LVDS/Debug | | Yes | Yes |
| CSI2 | | Yes | — |
| Hardware accelerator | | Yes | — |
| 1-V bypass mode | | Yes | Yes |
| JTAG | | Yes | Yes |
| Product status | Product Preview (PP), Advance Information (AI), or Production Data (PD) | AI ⁽¹⁾ | PD ⁽²⁾ |

- (1) ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
- (2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

3.1 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for industrial applications.

mmWave IWR The Texas Instruments IWR1xxx family of mmWave Sensors are highly integrated and built on RFCMOS technology operating in 76- to 81-GHz frequency band. The devices have a closed-loop PLL for precise and linear chirp synthesis, includes a built-in radio processor (BIST) for RF calibration and safety monitoring. The devices have a very small-form factor, low power consumption, and are highly accurate. Industrial applications from long range to ultra short range can be realized using these devices.

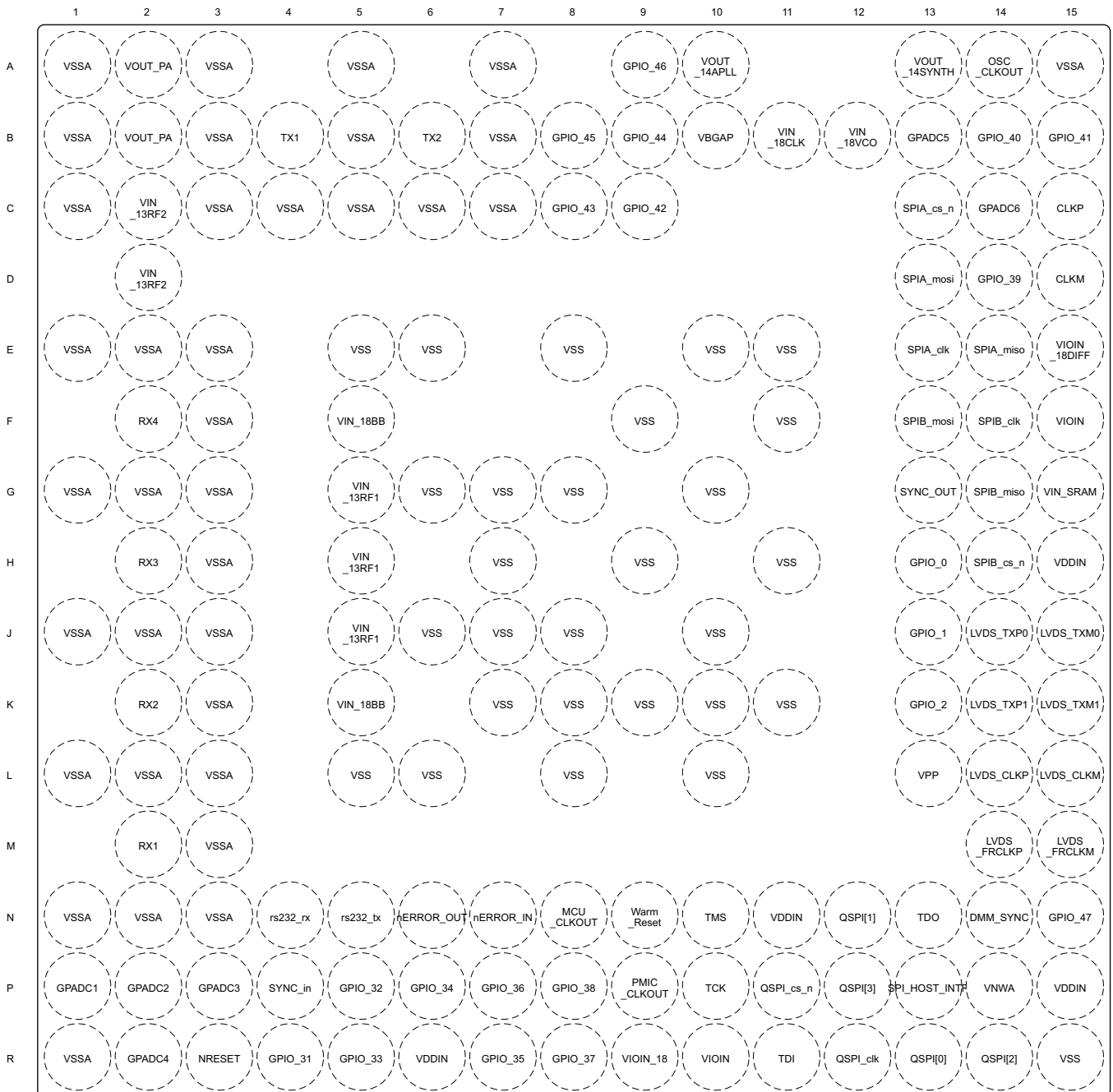
Companion Products for IWR1642 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for IWR1642 The IWR1642 TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

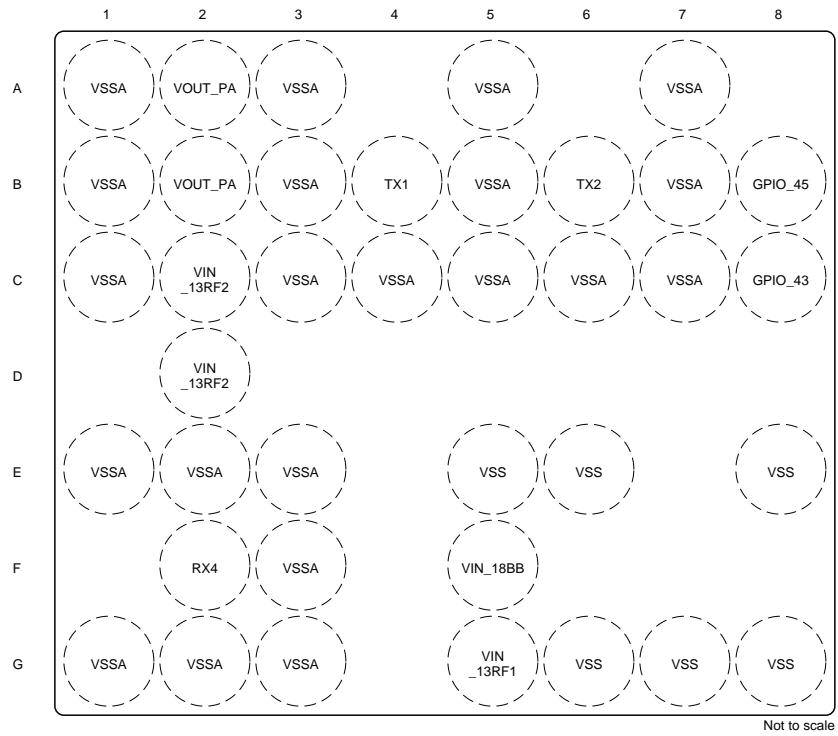
4.1 Pin Diagram

Figure 4-1 shows the pin locations for the 161-pin FCBGA package. Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5 show the same pins, but split into four quadrants.



Not to scale

Figure 4-1. Pin Diagram



| | |
|---|---|
| 1 | 2 |
| 3 | 4 |

Figure 4-2. Top Left Quadrant

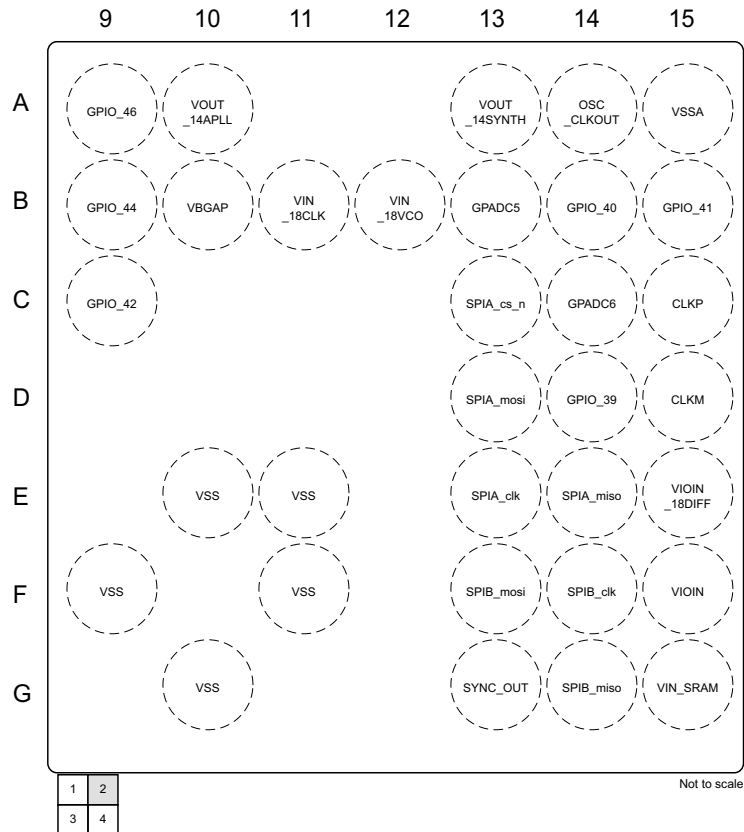


Figure 4-3. Top Right Quadrant

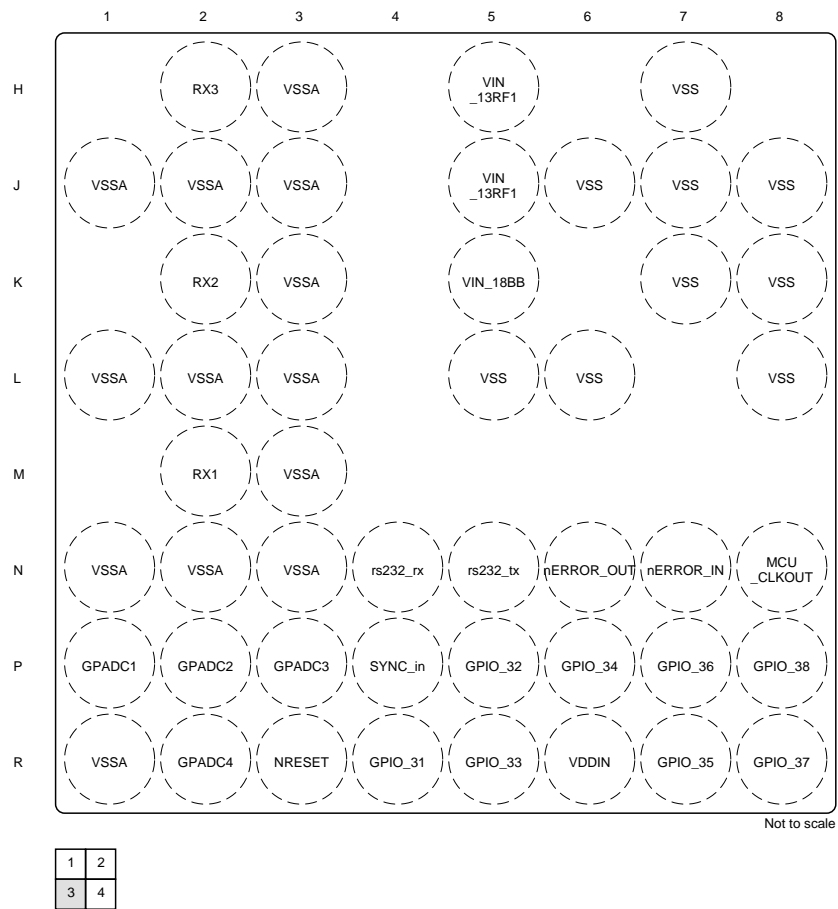
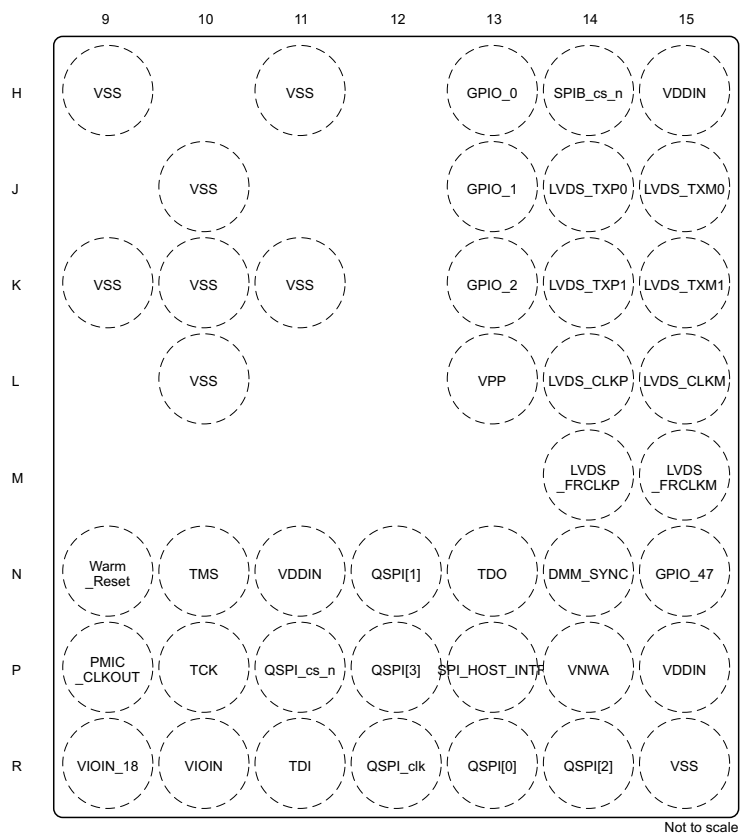


Figure 4-4. Bottom Left Quadrant



Not to scale

| | |
|---|---|
| 1 | 2 |
| 3 | 4 |

Figure 4-5. Bottom Right Quadrant

4.2 Pin Attributes

Table 4-1. Pin Attributes (ABL0161 Package)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|-----------------|---------------|-----------------|---------------------|----------|--------------|----------------------|-----------------------|
| H13 | GPIO_0 | GPIO_13 | 0xFFFFEA04 | 0 | IO | Output Disabled | Pull Down |
| | | GPIO_0 | | 1 | IO | | |
| | | PMIC_CLKOUT | | 2 | O | | |
| | | ePWM1b | | 10 | O | | |
| | | ePWM2a | | 11 | O | | |
| J13 | GPIO_1 | GPIO_16 | 0xFFFFEA08 | 0 | IO | Output Disabled | Pull Down |
| | | GPIO_1 | | 1 | IO | | |
| | | SYNC_OUT | | 2 | O | | |
| | | DMM_MUX_IN | | 12 | I | | |
| | | SPIB_cs_n_1 | | 13 | IO | | |
| | | SPIB_cs_n_2 | | 14 | IO | | |
| | | ePWM1SYNCl | | 15 | I | | |
| K13 | GPIO_2 | GPIO_26 | 0xFFFFEA64 | 0 | IO | Output Disabled | Pull Down |
| | | GPIO_2 | | 1 | IO | | |
| | | OSC_CLKOUT | | 2 | O | | |
| | | MSS_uartb_tx | | 7 | O | | |
| | | BSS_uart_tx | | 8 | O | | |
| | | SYNC_OUT | | 9 | O | | |
| | | PMIC_CLKOUT | | 10 | O | | |
| | | R4 | | GPIO_31 | TRACE_DATA_0 | | |
| GPIO_31 | 1 | | IO | | | | |
| DMM0 | 2 | | I | | | | |
| MSS_uarta_tx | 4 | | IO | | | | |
| P5 | GPIO_32 | TRACE_DATA_1 | 0xFFFFEA80 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_32 | | 1 | IO | | |
| | | DMM1 | | 2 | I | | |
| R5 | GPIO_33 | TRACE_DATA_2 | 0xFFFFEA84 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_33 | | 1 | IO | | |
| | | DMM2 | | 2 | I | | |
| P6 | GPIO_34 | TRACE_DATA_3 | 0xFFFFEA88 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_34 | | 1 | IO | | |
| | | DMM3 | | 2 | I | | |
| | | ePWM3SYNCO | | 4 | O | | |
| R7 | GPIO_35 | TRACE_DATA_4 | 0xFFFFEA8C | 0 | O | Output Disabled | Pull Down |
| | | GPIO_35 | | 1 | IO | | |
| | | DMM4 | | 2 | I | | |
| | | ePWM2SYNCO | | 4 | O | | |

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|-----------------|---------------|-----------------|---------------------|----------|----------|----------------------|-----------------------|
| P7 | GPIO_36 | TRACE_DATA_5 | 0xFFFFEA90 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_36 | | 1 | IO | | |
| | | DMM5 | | 2 | I | | |
| | | MSS_uartb_tx | | 5 | O | | |
| R8 | GPIO_37 | TRACE_DATA_6 | 0xFFFFEA94 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_37 | | 1 | IO | | |
| | | DMM6 | | 2 | I | | |
| | | BSS_uart_tx | | 5 | O | | |
| P8 | GPIO_38 | TRACE_DATA_7 | 0xFFFFEA98 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_38 | | 1 | IO | | |
| | | DMM7 | | 2 | I | | |
| | | DSS_uart_tx | | 5 | O | | |
| D14 | GPIO_39 | TRACE_DATA_8 | 0xFFFFEA9C | 0 | O | Output Disabled | Pull Down |
| | | GPIO_39 | | 1 | IO | | |
| | | DMM8 | | 2 | I | | |
| | | Reserved | | 4 | IO | | |
| | | ePWM1SYNCl | | 5 | I | | |
| B14 | GPIO_40 | TRACE_DATA_9 | 0xFFFFEAA0 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_40 | | 1 | IO | | |
| | | DMM9 | | 2 | I | | |
| | | Reserved | | 4 | IO | | |
| | | ePWM1SYNCO | | 5 | O | | |
| B15 | GPIO_41 | TRACE_DATA_10 | 0xFFFFEAA4 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_41 | | 1 | IO | | |
| | | DMM10 | | 2 | I | | |
| | | ePWM3a | | 4 | O | | |
| C9 | GPIO_42 | TRACE_DATA_11 | 0xFFFFEAA8 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_42 | | 1 | IO | | |
| | | DMM11 | | 2 | I | | |
| | | ePWM3b | | 4 | O | | |
| C8 | GPIO_43 | TRACE_DATA_12 | 0xFFFFEAAc | 0 | O | Output Disabled | Pull Down |
| | | GPIO_43 | | 1 | IO | | |
| | | DMM12 | | 2 | I | | |
| | | ePWM1a | | 4 | O | | |
| | | CAN_tx | | 5 | IO | | |

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|-----------------|---------------|-----------------|---------------------|-----------------|----------|----------------------|-----------------------|
| B9 | GPIO_44 | TRACE_DATA_13 | 0xFFFFEAB0 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_44 | | 1 | IO | | |
| | | DMM13 | | 2 | I | | |
| | | ePWM1b | | 4 | O | | |
| | | CAN_rx | | 5 | I | | |
| B8 | GPIO_45 | TRACE_DATA_14 | 0xFFFFEAB4 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_45 | | 1 | IO | | |
| | | DMM14 | | 2 | I | | |
| | | ePWM2a | | 4 | O | | |
| A9 | GPIO_46 | TRACE_DATA_15 | 0xFFFFEAB8 | 0 | O | Output Disabled | Pull Down |
| | | GPIO_46 | | 1 | IO | | |
| | | DMM15 | | 2 | I | | |
| | | ePWM2b | | 4 | O | | |
| N15 | GPIO_47 | TRACE_CLK | 0xFFFFEABC | 0 | O | Output Disabled | Pull Down |
| | | GPIO_47 | | 1 | IO | | |
| | | DMM_CLK | | 2 | I | | |
| N14 | DMM_SYNC | TRACE_CTL | 0xFFFFEAC0 | 0 | O | Output Disabled | Pull Down |
| | | RESERVED | | 1 | IO | | |
| | | DMM_SYNC | | 2 | I | | |
| N8 | MCU_CLKOUT | GPIO_25 | 0xFFFFEA60 | 0 | IO | Output Disabled | Pull Down |
| | | MCU_CLKOUT | | 1 | O | | |
| | | ePWM1a | | 12 | O | | |
| N7 | nERROR_IN | nERROR_IN | 0xFFFFEA44 | 0 | I | Input | |
| N6 | nERROR_OUT | nERROR_OUT | 0xFFFFEA4C | 0 | O | Hi-Z (Open Drain) | |
| P9 | PMIC_CLKOUT | SOP[2] | 0xFFFFEA68 | During Power Up | I | Output Disabled | Pull Down |
| | | GPIO_27 | | 0 | IO | | |
| | | PMIC_CLKOUT | | 1 | O | | |
| | | ePWM1b | | 11 | O | | |
| | | ePWM2a | | 12 | O | | |
| R13 | QSPI[0] | GPIO_8 | 0xFFFFEA2C | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[0] | | 1 | IO | | |
| | | SPIB_miso | | 2 | IO | | |
| N12 | QSPI[1] | GPIO_9 | 0xFFFFEA30 | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[1] | | 1 | IO | | |
| | | SPIB_mosi | | 2 | IO | | |
| | | SPIB_cs_n_2 | | 8 | IO | | |
| R14 | QSPI[2] | GPIO_10 | 0xFFFFEA34 | 0 | IO | Output Disabled | Pull Down |
| | | QSPI[2] | | 1 | I | | |
| | | Reserved | | 8 | O | | |

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] | | | | | |
|-----------------|---------------|-----------------|---------------------|----------|------------|----------------------|-----------------------|------------|-----------------|---------|----------------|--|
| P12 | QSPI[3] | GPIO_11 | 0xFFFFEA38 | 0 | IO | Output Disabled | Pull Down | | | | | |
| | | QSPI[3] | | 1 | IO | | | | | | | |
| | | Reserved | | 8 | I | | | | | | | |
| R12 | QSPI_clk | GPIO_7 | 0xFFFFEA3C | 0 | IO | Output Disabled | Pull Down | | | | | |
| | | QSPI_clk | | 1 | IO | | | | | | | |
| | | SPIB_clk | | 2 | IO | | | | | | | |
| | | DSS_uart_tx | | 6 | O | | | | | | | |
| P11 | QSPI_cs_n | GPIO_6 | 0xFFFFEA40 | 0 | IO | Output Disabled | Pull Up | | | | | |
| | | QSPI_cs_n | | 1 | IO | | | | | | | |
| | | SPIB_cs_n | | 2 | IO | | | | | | | |
| N4 | rs232_rx | GPIO_15 | 0xFFFFEA74 | 0 | IO | Input Enabled | Pull Up | | | | | |
| | | rs232_rx | | 1 | I | | | | | | | |
| | | MSS_uarta_rx | | 2 | I | | | | | | | |
| | | BSS_uart_tx | | 6 | IO | | | | | | | |
| | | MSS_uartb_rx | | 7 | IO | | | | | | | |
| | | Reserved | | 8 | I | | | | | | | |
| | | I2C_scl | | 9 | IO | | | | | | | |
| | | ePWM2a | | 10 | O | | | | | | | |
| | | ePWM2b | | 11 | O | | | | | | | |
| | | ePWM3a | | 12 | O | | | | | | | |
| | | N5 | | rs232_tx | GPIO_14 | | | 0xFFFFEA78 | 0 | IO | Output Enabled | |
| | | | | | rs232_tx | | | | 1 | O | | |
| MSS_uarta_tx | 5 | | IO | | | | | | | | | |
| MSS_uartb_tx | 6 | | IO | | | | | | | | | |
| BSS_uart_tx | 7 | | IO | | | | | | | | | |
| Reserved | 10 | | O | | | | | | | | | |
| I2C_sda | 11 | | IO | | | | | | | | | |
| ePWM1a | 12 | | O | | | | | | | | | |
| ePWM1b | 13 | | O | | | | | | | | | |
| NDMM_EN | 14 | | I | | | | | | | | | |
| ePWM2a | 15 | | O | | | | | | | | | |
| E13 | SPIA_clk | | GPIO_3 | | 0xFFFFEA14 | 0 | IO | | Output Disabled | Pull Up | | |
| | | | SPIA_clk | | | 1 | IO | | | | | |
| | | | CAN_rx | | | 6 | I | | | | | |
| | | | DSS_uart_tx | | | 7 | O | | | | | |
| C13 | SPIA_cs_n | GPIO_30 | 0xFFFFEA18 | 0 | IO | Output Disabled | Pull Up | | | | | |
| | | SPIA_cs_n | | 1 | IO | | | | | | | |
| | | CAN_tx | | 6 | O | | | | | | | |

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|-----------------|---------------|-----------------|---------------------|----------|----------|----------------------|-----------------------|
| E14 | SPIA_miso | GPIO_20 | 0xFFFFEA10 | 0 | IO | Output Disabled | Pull Up |
| | | SPIA_miso | | 1 | IO | | |
| | | Reserved | | 2 | O | | |
| D13 | SPIA_mosi | GPIO_19 | 0xFFFFEA0C | 0 | IO | Output Disabled | Pull Up |
| | | SPIA_mosi | | 1 | IO | | |
| | | Reserved | | 2 | I | | |
| | | DSS_uart_tx | | 8 | O | | |
| F14 | SPIB_clk | GPIO_5 | 0xFFFFEA24 | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_clk1 | | 1 | IO | | |
| | | MSS_uarta_rx | | 2 | I | | |
| | | MSS_uartb_tx | | 6 | O | | |
| | | BSS_uart_tx | | 7 | O | | |
| | | Reserved | | 8 | I | | |
| H14 | SPIB_cs_n | GPIO_4 | 0xFFFFEA28 | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_cs_n | | 1 | IO | | |
| | | MSS_uarta_tx | | 2 | O | | |
| | | MSS_uartb_tx | | 6 | O | | |
| | | BSS_uart_tx | | 7 | IO | | |
| | | QSPI_clk_ext | | 8 | I | | |
| | | Reserved | | 9 | O | | |
| G14 | SPIB_miso | GPIO_22 | 0xFFFFEA20 | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_miso | | 1 | IO | | |
| | | I2C_scl | | 2 | IO | | |
| | | DSS_uart_tx | | 6 | O | | |
| F13 | SPIB_mosi | GPIO_21 | 0xFFFFEA1C | 0 | IO | Output Disabled | Pull Up |
| | | SPIB_mosi | | 1 | IO | | |
| | | I2C_sda | | 2 | IO | | |
| P13 | SPI_HOST_INTR | GPIO_12 | 0xFFFFEA00 | 0 | IO | Output Disabled | Pull Down |
| | | SPI_HOST_INTR | | 1 | O | | |
| | | SPIB_cs_n_1 | | 6 | IO | | |
| P4 | SYNC_in | GPIO_28 | 0xFFFFEA6C | 0 | IO | Output Disabled | Pull Down |
| | | SYNC_IN | | 1 | I | | |
| | | MSS_uartb_rx | | 6 | IO | | |
| | | DMM_MUX_IN | | 7 | I | | |
| | | SYNC_OUT | | 9 | O | | |

Table 4-1. Pin Attributes (ABL0161 Package) (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | PINCNTL ADDRESS [4] | MODE [5] | TYPE [6] | BALL RESET STATE [7] | PULL UP/DOWN TYPE [8] |
|-----------------|---------------|-----------------|---------------------|-----------------|----------|-------------------------|-----------------------|
| G13 | SYNC_OUT | SOP[1] | 0xFFFFEA70 | During Power Up | I | Output Disabled | Pull Down |
| | | GPIO_29 | | 0 | IO | | |
| | | SYNC_OUT | | 1 | O | | |
| | | DMM_MUX_IN | | 9 | I | | |
| | | SPIB_cs_n_1 | | 10 | IO | | |
| | | SPIB_cs_n_2 | | 11 | IO | | |
| P10 | TCK | GPIO_17 | 0xFFFFEA50 | 0 | IO | Input Enabled | Pull Down |
| | | TCK | | 1 | I | | |
| | | MSS_uartb_tx | | 2 | O | | |
| | | Reserved | | 8 | O | | |
| R11 | TDI | GPIO_23 | 0xFFFFEA58 | 0 | IO | Input Enabled | Pull Up |
| | | TDI | | 1 | I | | |
| | | MSS_uarta_rx | | 2 | I | | |
| N13 | TDO | SOP[0] | 0xFFFFEA5C | During Power Up | I | Output Enabled | |
| | | GPIO_24 | | 0 | IO | | |
| | | TDO | | 1 | O | | |
| | | MSS_uarta_tx | | 2 | O | | |
| | | MSS_uartb_tx | | 6 | O | | |
| | | BSS_uart_tx | | 7 | O | | |
| | | NDMM_EN | | 9 | I | | |
| N10 | TMS | GPIO_18 | 0xFFFFEA54 | 0 | IO | Input Enabled | Pull Down |
| | | TMS | | 1 | I | | |
| | | BSS_uart_tx | | 2 | O | | |
| | | Reserved | | 6 | I | | |
| N9 | Warm_Reset | Warm_Reset | 0xFFFFEA48 | 0 | IO | Hi-Z Input (Open Drain) | |

The following list describes the table column headers:

- BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
- BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
- SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).
- PINCNTL ADDRESS:** MSS Address for PinMux Control
- MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.
- TYPE:** Signal type and direction:
 - I = Input
 - O = Output

- IO = Input or Output
- 7. **BALL RESET STATE:** The state of the terminal at power-on reset
- 8. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
 - Pull Up: Internal pullup
 - Pull Down: Internal pulldown
 - An empty box means No pull.
- 9. Pin Mux Control Value maps to lower 4 bits of register.

IO MUX registers are available in the MSS memory map and the respective mapping to device pins is as follows:

Table 4-2. PAD IO Control Registers

| Default Pin/Ball Name | Package Ball /Pin (Address) | Pin Mux Config Register |
|-----------------------|-----------------------------|-------------------------|
| SPI_HOST_INTR | P13 | 0xFFFFEA00 |
| GPIO_0 | H13 | 0xFFFFEA04 |
| GPIO_1 | J13 | 0xFFFFEA08 |
| SPIA_mosi | D13 | 0xFFFFEA0C |
| SPIA_miso | E14 | 0xFFFFEA10 |
| SPIA_clk | E13 | 0xFFFFEA14 |
| SPIA_cs_n | C13 | 0xFFFFEA18 |
| SPIB_mosi | F13 | 0xFFFFEA1C |
| SPIB_miso | G14 | 0xFFFFEA20 |
| SPIB_clk | F14 | 0xFFFFEA24 |
| SPIB_cs_n | H14 | 0xFFFFEA28 |
| QSPI[0] | R13 | 0xFFFFEA2C |
| QSPI[1] | N12 | 0xFFFFEA30 |
| QSPI[2] | R14 | 0xFFFFEA34 |
| QSPI[3] | P12 | 0xFFFFEA38 |
| QSPI_clk | R12 | 0xFFFFEA3C |
| QSPI_csn_n | P11 | 0xFFFFEA40 |
| nERROR_IN | N7 | 0xFFFFEA44 |
| Warm_Reset | N9 | 0xFFFFEA48 |
| nERROR_OUT | N6 | 0xFFFFEA4C |
| TCK | P10 | 0xFFFFEA50 |
| TMS | N10 | 0xFFFFEA54 |
| TDI | R11 | 0xFFFFEA58 |
| TDO | N13 | 0xFFFFEA5C |
| MCU_CLKOUT | N8 | 0xFFFFEA60 |
| GPIO_2 | K13 | 0xFFFFEA64 |
| PMIC_CLKOUT | P9 | 0xFFFFEA68 |
| SYNC_in | P4 | 0xFFFFEA6C |
| SYNC_OUT | G13 | 0xFFFFEA70 |
| rs232_rx | N4 | 0xFFFFEA74 |
| rs232_tx | N5 | 0xFFFFEA78 |

Table 4-2. PAD IO Control Registers (continued)

| Default Pin/Ball Name | Package Ball /Pin (Address) | Pin Mux Config Register |
|-----------------------|-----------------------------|-------------------------|
| GPIO_31 | R4 | 0xFFFFEA7C |
| GPIO_32 | P5 | 0xFFFFEA80 |
| GPIO_33 | R5 | 0xFFFFEA84 |
| GPIO_34 | P6 | 0xFFFFEA88 |
| GPIO_35 | R7 | 0xFFFFEA8C |
| GPIO_36 | P7 | 0xFFFFEA90 |
| GPIO_37 | R8 | 0xFFFFEA94 |
| GPIO_38 | P8 | 0xFFFFEA98 |
| GPIO_39 | D14 | 0xFFFFEA9C |
| GPIO_40 | B14 | 0xFFFFEAA0 |
| GPIO_41 | B15 | 0xFFFFEAA4 |
| GPIO_42 | C9 | 0xFFFFEAA8 |
| GPIO_43 | C8 | 0xFFFFEAA8 |
| GPIO_44 | B9 | 0xFFFFEAB0 |
| GPIO_45 | B8 | 0xFFFFEAB4 |
| GPIO_46 | A9 | 0xFFFFEAB8 |
| GPIO_47 | N15 | 0xFFFFEABC |
| DMM_SYNC | N14 | 0xFFFFEAC0 |

The register layout is as follows:

Table 4-3. PAD IO Register Bit Descriptions

| BIT | FIELD | TYPE | RESET (POWER ON DEFAULT) | DESCRIPTION |
|-------|------------------|------|--------------------------------|--|
| 31-11 | NU | RW | 0 | Reserved |
| 10 | SC | RW | 0 | IO slew rate control: 0 = Higher slew rate 1 = Lower slew rate |
| 9 | PUPDSEL | RW | 0 | Pullup/PullDown Selection 0 = Pull Down 1 = Pull Up (This field is valid only if Pull Inhibit is set as '0') |
| 8 | PI | RW | 0 | Pull Inhibit/Pull Disable 0 = Enable 1 = Disable |
| 7 | OE_OVERRIDE | RW | 1 | Output Override |
| 6 | OE_OVERRIDE_CTRL | RW | 1 | Output Override Control: (A '1' here overrides any o/p manipulation of this IO by any of the peripheral block hardware it is associated with for example a SPI Chip select) |
| 5 | IE_OVERRIDE | RW | 0 | Input Override |
| 4 | IE_OVERRIDE_CTRL | RW | 0 | Input Override Control: (A '1' here overrides any i/p value on this IO with a desired value) |
| 3-0 | FUNC_SEL | RW | 1 | Function select for Pin Multiplexing (Refer to the Pin Mux Sheet) |

4.3 Signal Descriptions

Table 4-4. Signal Descriptions - Digital

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|-------------|----------|---|-------------------------------------|
| BSS_UART_TX | O | Debug UART Transmit [Radar Block] | F14, H14, K13, N10, N13, N4, N5, R8 |
| CAN_RX | I | CAN (DCAN) Receive Signal | B9, E13 |
| CAN_TX | IO | CAN (DCAN) Transmit Signal | C13, C8 |
| DMM0 | I | Debug Interface (Hardware In Loop) - Data Line | R4 |
| DMM1 | I | Debug Interface (Hardware In Loop) - Data Line | P5 |
| DMM2 | I | Debug Interface (Hardware In Loop) - Data Line | R5 |
| DMM3 | I | Debug Interface (Hardware In Loop) - Data Line | P6 |
| DMM4 | I | Debug Interface (Hardware In Loop) - Data Line | R7 |
| DMM5 | I | Debug Interface (Hardware In Loop) - Data Line | P7 |
| DMM6 | I | Debug Interface (Hardware In Loop) - Data Line | R8 |
| DMM7 | I | Debug Interface (Hardware In Loop) - Data Line | P8 |
| DMM8 | I | Debug Interface (Hardware In Loop) - Data Line | D14 |
| DMM9 | I | Debug Interface (Hardware In Loop) - Data Line | B14 |
| DMM10 | I | Debug Interface (Hardware In Loop) - Data Line | B15 |
| DMM11 | I | Debug Interface (Hardware In Loop) - Data Line | C9 |
| DMM12 | I | Debug Interface (Hardware In Loop) - Data Line | C8 |
| DMM13 | I | Debug Interface (Hardware In Loop) - Data Line | B9 |
| DMM14 | I | Debug Interface (Hardware In Loop) - Data Line | B8 |
| DMM15 | I | Debug Interface (Hardware In Loop) - Data Line | A9 |
| DMM_CLK | I | Debug Interface (Hardware In Loop) - Clock | N15 |
| DMM_MUX_IN | I | Debug Interface (Hardware In Loop) Mux Select between DMM1 and DMM2 (Two Instances) | G13, J13, P4 |
| DMM_SYNC | I | Debug Interface (Hardware In Loop) - Sync | N14 |
| DSS_UART_TX | O | Debug UART Transmit [DSP] | D13, E13, G14, P8, R12 |
| EPWM1A | O | PWM Module 1 - OutPut A | C8, N5, N8 |
| EPWM1B | O | PWM Module 1 - OutPut B | B9, H13, N5, P9 |
| EPWM1SYNCI | I | | D14, J13 |
| EPWM1SYNCO | O | | B14 |
| EPWM2A | O | PWM Module 2- OutPut A | B8, H13, N4, N5, P9 |
| EPWM2B | O | PWM Module 2 - OutPut B | A9, N4 |
| EPWM2SYNCO | O | | R7 |
| EPWM3A | O | PWM Module 3 - OutPut A | B15, N4 |
| EPWM3B | O | PWM Module 3 - OutPut B | C9 |
| EPWM3SYNCO | O | | P6 |
| GPIO_0 | IO | General-purpose I/O | H13 |
| GPIO_1 | IO | General-purpose I/O | J13 |
| GPIO_2 | IO | General-purpose I/O | K13 |
| GPIO_3 | IO | General-purpose I/O | E13 |
| GPIO_4 | IO | General-purpose I/O | H14 |
| GPIO_5 | IO | General-purpose I/O | F14 |
| GPIO_6 | IO | General-purpose I/O | P11 |
| GPIO_7 | IO | General-purpose I/O | R12 |
| GPIO_8 | IO | General-purpose I/O | R13 |
| GPIO_9 | IO | General-purpose I/O | N12 |
| GPIO_10 | IO | General-purpose I/O | R14 |

Table 4-4. Signal Descriptions - Digital (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|-------------|----------|--------------------------------|----------|
| GPIO_11 | IO | General-purpose I/O | P12 |
| GPIO_12 | IO | General-purpose I/O | P13 |
| GPIO_13 | IO | General-purpose I/O | H13 |
| GPIO_14 | IO | General-purpose I/O | N5 |
| GPIO_15 | IO | General-purpose I/O | N4 |
| GPIO_16 | IO | General-purpose I/O | J13 |
| GPIO_17 | IO | General-purpose I/O | P10 |
| GPIO_18 | IO | General-purpose I/O | N10 |
| GPIO_19 | IO | General-purpose I/O | D13 |
| GPIO_20 | IO | General-purpose I/O | E14 |
| GPIO_21 | IO | General-purpose I/O | F13 |
| GPIO_22 | IO | General-purpose I/O | G14 |
| GPIO_23 | IO | General-purpose I/O | R11 |
| GPIO_24 | IO | General-purpose I/O | N13 |
| GPIO_25 | IO | General-purpose I/O | N8 |
| GPIO_26 | IO | General-purpose I/O | K13 |
| GPIO_27 | IO | General-purpose I/O | P9 |
| GPIO_28 | IO | General-purpose I/O | P4 |
| GPIO_29 | IO | General-purpose I/O | G13 |
| GPIO_30 | IO | General-purpose I/O | C13 |
| GPIO_31 | IO | General-purpose I/O | R4 |
| GPIO_32 | IO | General-purpose I/O | P5 |
| GPIO_33 | IO | General-purpose I/O | R5 |
| GPIO_34 | IO | General-purpose I/O | P6 |
| GPIO_35 | IO | General-purpose I/O | R7 |
| GPIO_36 | IO | General-purpose I/O | P7 |
| GPIO_37 | IO | General-purpose I/O | R8 |
| GPIO_38 | IO | General-purpose I/O | P8 |
| GPIO_39 | IO | General-purpose I/O | D14 |
| GPIO_40 | IO | General-purpose I/O | B14 |
| GPIO_41 | IO | General-purpose I/O | B15 |
| GPIO_42 | IO | General-purpose I/O | C9 |
| GPIO_43 | IO | General-purpose I/O | C8 |
| GPIO_44 | IO | General-purpose I/O | B9 |
| GPIO_45 | IO | General-purpose I/O | B8 |
| GPIO_46 | IO | General-purpose I/O | A9 |
| GPIO_47 | IO | General-purpose I/O | N15 |
| I2C_SCL | IO | I2C Clock | G14, N4 |
| I2C_SDA | IO | I2C Data | F13, N5 |
| LVDS_TXP[0] | O | Differential data Out – Lane 0 | J14 |
| LVDS_TXM[0] | O | | J15 |
| LVDS_TXP[1] | O | Differential data Out – Lane 1 | K14 |
| LVDS_TXM[1] | O | | K15 |
| LVDS_CLKP | O | Differential clock Out | L14 |
| LVDS_CLKM | O | | L15 |
| LVDS_FRCLKP | O | Differential Frame Clock | M14 |
| LVDS_FRCLKM | O | | M15 |

Table 4-4. Signal Descriptions - Digital (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---------------|----------|---|---------------------------------|
| MCU_CLKOUT | O | Programmable clock given out to external MCU or the processor | N8 |
| MSS_UARTA_RX | I | Master Subsystem - UART A Receive | F14, N4, R11 |
| MSS_UARTA_TX | O | Master Subsystem - UART A Transmit | H14, N13, N5, R4 |
| MSS_UARTB_RX | IO | Master Subsystem - UART B Receive | N4, P4 |
| MSS_UARTB_TX | O | Master Subsystem - UART B Transmit | F14, H14, K13, N13, N5, P10, P7 |
| NDMM_EN | I | Debug Interface (Hardware In Loop) Enable - Active Low Signal | N13, N5 |
| nERROR_IN | I | Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware | N7 |
| nERROR_OUT | O | Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset. | N6 |
| PMIC_CLKOUT | O | Output Clock from IWR1642 device for PMIC | H13, K13, P9 |
| QSPI[0] | IO | QSPI Data Line #0 (Used with Serial Data Flash) | R13 |
| QSPI[1] | IO | QSPI Data Line #1 (Used with Serial Data Flash) | N12 |
| QSPI[2] | I | QSPI Data Line #2 (Used with Serial Data Flash) | R14 |
| QSPI[3] | IO | QSPI Data Line #3 (Used with Serial Data Flash) | P12 |
| QSPI_CLK | IO | QSPI Clock (Used with Serial Data Flash) | R12 |
| QSPI_CLK_EXT | I | QSPI Clock (Used with Serial Data Flash) | H14 |
| QSPI_CS_N | IO | QSPI Chip Select (Used with Serial Data Flash) | P11 |
| RS232_RX | I | Debug UART (Operates as Bus Master) - Receive Signal | N4 |
| RS232_TX | O | Debug UART (Operates as Bus Master) - Transmit Signal | N5 |
| SOP[0] | I | Sense On Power - Line#0 | N13 |
| SOP[1] | I | Sense On Power - Line#1 | G13 |
| SOP[2] | I | Sense On Power - Line#2 | P9 |
| SPIA_CLK | IO | SPI Channel A - Clock | E13 |
| SPIA_CS_N | IO | SPI Channel A - Chip Select | C13 |
| SPIA_MISO | IO | SPI Channel A - Master In Slave Out | E14 |
| SPIA_MOSI | IO | SPI Channel A - Master Out Slave In | D13 |
| SPIB_CLK | IO | SPI Channel B - Clock | F14, R12 |
| SPIB_CS_N | IO | SPI Channel B Chip Select (Instance ID 0) | H14, P11 |
| SPIB_CS_N_1 | IO | SPI Channel B Chip Select (Instance ID 1) | G13, J13, P13 |
| SPIB_CS_N_2 | IO | SPI Channel B Chip Select (Instance ID 2) | G13, J13, N12 |
| SPIB_MISO | IO | SPI Channel B - Master In Slave Out | G14, R13 |
| SPIB_MOSI | IO | SPI Channel B - Master Out Slave In | F13, N12 |
| SPI_HOST_INTR | O | Out of Band Interrupt to an external host communicating over SPI | P13 |
| SYNC_IN | I | Low frequency Synchronization signal input | P4 |
| SYNC_OUT | O | Low Frequency Synchronization Signal output | G13, J13, K13, P4 |
| TCK | I | JTAG Test Clock | P10 |
| TDI | I | JTAG Test Data Input | R11 |
| TDO | O | JTAG Test Data Output | N13 |
| TMS | I | JTAG Test Mode Signal | N10 |
| TRACE_CLK | O | Debug Trace Output - Clock | N15 |
| TRACE_CTL | O | Debug Trace Output - Control | N14 |
| TRACE_DATA_0 | O | Debug Trace Output - Data Line | R4 |
| TRACE_DATA_1 | O | Debug Trace Output - Data Line | P5 |
| TRACE_DATA_2 | O | Debug Trace Output - Data Line | R5 |
| TRACE_DATA_3 | O | Debug Trace Output - Data Line | P6 |

Table 4-4. Signal Descriptions - Digital (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|---------------|----------|--|----------|
| TRACE_DATA_4 | O | Debug Trace Output - Data Line | R7 |
| TRACE_DATA_5 | O | Debug Trace Output - Data Line | P7 |
| TRACE_DATA_6 | O | Debug Trace Output - Data Line | R8 |
| TRACE_DATA_7 | O | Debug Trace Output - Data Line | P8 |
| TRACE_DATA_8 | O | Debug Trace Output - Data Line | D14 |
| TRACE_DATA_9 | O | Debug Trace Output - Data Line | B14 |
| TRACE_DATA_10 | O | Debug Trace Output - Data Line | B15 |
| TRACE_DATA_11 | O | Debug Trace Output - Data Line | C9 |
| TRACE_DATA_12 | O | Debug Trace Output - Data Line | C8 |
| TRACE_DATA_13 | O | Debug Trace Output - Data Line | B9 |
| TRACE_DATA_14 | O | Debug Trace Output - Data Line | B8 |
| TRACE_DATA_15 | O | Debug Trace Output - Data Line | A9 |
| WARM_RESET | IO | Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset. | N9 |

Table 4-5. Signal Descriptions - Analog

| INTERFACE | SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|----------------------|--------------|----------|--|-------------------|
| Transmitters | TX1 | O | Single ended transmitter1 o/p | B4 |
| | TX2 | O | Single ended transmitter2 o/p | B6 |
| Receivers | RX1 | I | Single ended receiver1 i/p | M2 |
| | RX2 | I | Single ended receiver2 i/p | K2 |
| | RX3 | I | Single ended receiver3 i/p | H2 |
| | RX4 | I | Single ended receiver4 i/p | F2 |
| Reset | NRESET | I | Power on reset for chip. Active low | R3 |
| Reference Oscillator | CLKP | I | In XTAL mode: Differential port for reference crystal In External clock mode: Single ended input reference clock port | C15 |
| | CLKM | I | In XTAL mode: Differential port for reference crystal In External clock mode: Connect this port to ground | D15 |
| Reference clock | OSC_CLKOUT | O | Reference clock output from clocking sub system after cleanup PLL (1.8V output voltage swing). | A14 |
| Bandgap voltage | VBGAP | O | | B10 |
| Power supply | VDDIN | Power | 1.2V digital power supply | H15, N11, P15, R6 |
| | VIN_SRAM | Power | 1.2V power rail for internal SRAM | G15 |
| | VNWA | Power | 1.2V power rail for SRAM array back bias | P14 |
| | VIOIN | Power | I/O Supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply | R10, F15 |
| | VIOIN_18 | Power | 1.8V supply for CMOS IO | R9 |
| | VIN_18CLK | Power | 1.8V supply for clock module | B11 |
| | VIOIN_18DIFF | Power | 1.8V supply for LVDS port | E15 |
| | VPP | Power | Voltage supply for fuse chain | L13 |

Table 4-5. Signal Descriptions - Analog (continued)

| INTERFACE | SIGNAL NAME | PIN TYPE | DESCRIPTION | BALL NO. |
|--|---------------------|----------|--|---|
| Power supply | VIN_13RF1 | Power | 1.3V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board | G5, H5, J5 |
| | VIN_13RF2 | Power | 1.3V Analog and RF supply | C2, D2 |
| | VIN_18BB | Power | 1.8V Analog base band power supply | K5, F5 |
| | VIN_18VCO | Power | 1.8V RF VCO supply | B12 |
| | VSS | Ground | Digital ground | L5, L6, L8, L10, K7, K8, K9, K10, K11, J6, J7, J8, J10, H7, H9, H11, G6, G7, G8, G10, F9, F11, E5, E6, E8, E10, E11, R15 |
| | VSSA | Ground | Analog ground | A1, A3, A5, A7, A15, B1, B3, B5, B7, C1, C3, C4, C5, C6, C7, E1, E2, E3, F3, G1, G2, G3, H3, J1, J2, J3, K3, L1, L2, L3, M3, N1, N2, N3, R1 |
| Internal LDO output/inputs | VOUT_14APLL | O | | A10 |
| | VOUT_14SYNTH | O | | A13 |
| | VOUT_PA | O | | A2, B2 |
| Test and Debug output for pre-production phase. Can be pinned out on production hardware for field debug | Analog Test1 / ADC1 | IO | ADC Channel 1 ⁽¹⁾ | P1 |
| | Analog Test2 / ADC2 | IO | ADC Channel 2 ⁽¹⁾ | P2 |
| | Analog Test3 / ADC3 | IO | ADC Channel 3 ⁽¹⁾ | P3 |
| | Analog Test4 / ADC4 | IO | ADC Channel 4 ⁽¹⁾ | R2 |
| | ANAMUX / ADC5 | IO | ADC Channel 5 ⁽¹⁾ | B13 |
| | VSENSE / ADC6 | IO | ADC Channel 6 ⁽¹⁾ | C14 |

(1) For details, see [Section 6.4.1](#).

4.4 Pin Multiplexing

Table 4-6. Pin Multiplexing

| ADDRESS | BALL NUMBER | MUXMODE[15:During Power Up] SETTINGS | | | | | | | | | | | | | | | |
|------------|-------------|--------------------------------------|------------|---------------|--------------|---|---|--------------|-------------|--------------|----------|--------|--------|------------|-------------|-------------|------------|
| | | During Power Up | 0 | 1 | 2 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0xFFFFEA00 | P13 | | GPIO_12 | SPI_HOST_INTR | | | | SPIB_cs_n_1 | | | | | | | | | |
| 0xFFFFEA04 | H13 | | GPIO_13 | GPIO_0 | PMIC_CLK_OUT | | | | | | | ePWM1b | ePWM2a | | | | |
| 0xFFFFEA08 | J13 | | GPIO_16 | GPIO_1 | SYNC_OUT | | | | | | | | | DMM_MUX_IN | SPIB_cs_n_1 | SPIB_cs_n_2 | ePWM1SYNCl |
| 0xFFFFEA0C | D13 | | GPIO_19 | SPIA_mosi | Reserved | | | | | DSS_uart_tx | | | | | | | |
| 0xFFFFEA10 | E14 | | GPIO_20 | SPIA_miso | Reserved | | | | | | | | | | | | |
| 0xFFFFEA14 | E13 | | GPIO_3 | SPIA_clk | | | | CAN_rx | DSS_uart_tx | | | | | | | | |
| 0xFFFFEA18 | C13 | | GPIO_30 | SPIA_cs_n | | | | CAN_tx | | | | | | | | | |
| 0xFFFFEA1C | F13 | | GPIO_21 | SPIB_mosi | I2C_sda | | | | | | | | | | | | |
| 0xFFFFEA20 | G14 | | GPIO_22 | SPIB_miso | I2C_scl | | | DSS_uart_tx | | | | | | | | | |
| 0xFFFFEA24 | F14 | | GPIO_5 | SPIB_clk | MSS_uarta_rx | | | MSS_uartb_tx | BSS_uart_tx | Reserved | | | | | | | |
| 0xFFFFEA28 | H14 | | GPIO_4 | SPIB_cs_n | MSS_uarta_tx | | | MSS_uartb_tx | BSS_uart_tx | QSPL_clk_ext | Reserved | | | | | | |
| 0xFFFFEA2C | R13 | | GPIO_8 | QSPI[0] | SPIB_miso | | | | | | | | | | | | |
| 0xFFFFEA30 | N12 | | GPIO_9 | QSPI[1] | SPIB_mosi | | | | | SPIB_cs_n_2 | | | | | | | |
| 0xFFFFEA34 | R14 | | GPIO_10 | QSPI[2] | | | | | | Reserved | | | | | | | |
| 0xFFFFEA38 | P12 | | GPIO_11 | QSPI[3] | | | | | | Reserved | | | | | | | |
| 0xFFFFEA3C | R12 | | GPIO_7 | QSPL_clk | SPIB_clk | | | DSS_uart_tx | | | | | | | | | |
| 0xFFFFEA40 | P11 | | GPIO_6 | QSPL_cs_n | SPIB_cs_n | | | | | | | | | | | | |
| 0xFFFFEA44 | N7 | | nERROR_IN | | | | | | | | | | | | | | |
| 0xFFFFEA48 | N9 | | Warm_Reset | | | | | | | | | | | | | | |
| 0xFFFFEA4C | N6 | | nERROR_OUT | | | | | | | | | | | | | | |
| 0xFFFFEA50 | P10 | | GPIO_17 | TCK | MSS_uartb_tx | | | | | Reserved | | | | | | | |
| 0xFFFFEA54 | N10 | | GPIO_18 | TMS | BSS_uart_tx | | | Reserved | | | | | | | | | |
| 0xFFFFEA58 | R11 | | GPIO_23 | TDI | MSS_uarta_rx | | | | | | | | | | | | |
| 0xFFFFEA5C | N13 | SOP[0] | GPIO_24 | TDO | MSS_uarta_tx | | | MSS_uartb_tx | BSS_uart_tx | | NDMM_EN | | | | | | |

Table 4-6. Pin Multiplexing (continued)

| ADDRESS | BALL NUMBER | MUXMODE[15:During Power Up] SETTINGS | | | | | | | | | | | | | | | |
|-------------|-------------|--------------------------------------|----------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|--------------|-------------|--------|--------|---------|--------|
| | | During Power Up | 0 | 1 | 2 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0xFFFFEA60 | N8 | | GPIO_25 | MCU_CLK OUT | | | | | | | | | | ePWM1a | | | |
| 0xFFFFEA64 | K13 | | GPIO_26 | GPIO_2 | OSC_CLK OUT | | | | MSS_uart_tx | BSS_uart_tx | SYNC_OUT | PMIC_CLK OUT | | | | | |
| 0xFFFFEA68 | P9 | SOP[2] | GPIO_27 | PMIC_CLK OUT | | | | | | | | | ePWM1b | ePWM2a | | | |
| 0xFFFFEA6C | P4 | | GPIO_28 | SYNC_IN | | | | MSS_uart_rx | DMM_MUX_IN | | SYNC_OUT | | | | | | |
| 0xFFFFEA70 | G13 | SOP[1] | GPIO_29 | SYNC_OUT | | | | | | | DMM_MUX_IN | SPIB_cs_n_1 | SPIB_cs_n_2 | | | | |
| 0xFFFFEA74 | N4 | | GPIO_15 | rs232_rx | MSS_uart_rx | | | BSS_uart_tx | MSS_uart_rx | Reserved | I2C_scl | ePWM2a | ePWM2b | ePWM3a | | | |
| 0xFFFFEA78 | N5 | | GPIO_14 | rs232_tx | | | MSS_uart_tx | MSS_uart_tx | BSS_uart_tx | | | Reserved | I2C_sda | ePWM1a | ePWM1b | NDMM_EN | ePWM2a |
| 0xFFFFEA7C | R4 | | TRACE_D ATA_0 | GPIO_31 | DMM0 | MSS_uart_tx | | | | | | | | | | | |
| 0xFFFFEA80 | P5 | | TRACE_D ATA_1 | GPIO_32 | DMM1 | | | | | | | | | | | | |
| 0xFFFFEA84 | R5 | | TRACE_D ATA_2 | GPIO_33 | DMM2 | | | | | | | | | | | | |
| 0xFFFFEA88 | P6 | | TRACE_D ATA_3 | GPIO_34 | DMM3 | ePWM3SY NCO | | | | | | | | | | | |
| 0xFFFFEA8C | R7 | | TRACE_D ATA_4 | GPIO_35 | DMM4 | ePWM2SY NCO | | | | | | | | | | | |
| 0xFFFFEA90 | P7 | | TRACE_D ATA_5 | GPIO_36 | DMM5 | | MSS_uart_tx | | | | | | | | | | |
| 0xFFFFEA94 | R8 | | TRACE_D ATA_6 | GPIO_37 | DMM6 | | BSS_uart_tx | | | | | | | | | | |
| 0xFFFFEA98 | P8 | | TRACE_D ATA_7 | GPIO_38 | DMM7 | | DSS_uart_tx | | | | | | | | | | |
| 0xFFFFEA9C | D14 | | TRACE_D ATA_8 | GPIO_39 | DMM8 | Reserved | ePWM1SY NCI | | | | | | | | | | |
| 0xFFFFEAA0 | B14 | | TRACE_D ATA_9 | GPIO_40 | DMM9 | Reserved | ePWM1SY NCO | | | | | | | | | | |
| 0xFFFFEAA4 | B15 | | TRACE_D ATA_10 | GPIO_41 | DMM10 | ePWM3a | | | | | | | | | | | |
| 0xFFFFEAA8 | C9 | | TRACE_D ATA_11 | GPIO_42 | DMM11 | ePWM3b | | | | | | | | | | | |
| 0xFFFFEAA C | C8 | | TRACE_D ATA_12 | GPIO_43 | DMM12 | ePWM1a | CAN_tx | | | | | | | | | | |
| 0xFFFFEAB0 | B9 | | TRACE_D ATA_13 | GPIO_44 | DMM13 | ePWM1b | CAN_rx | | | | | | | | | | |
| 0xFFFFEAB4 | B8 | | TRACE_D ATA_14 | GPIO_45 | DMM14 | ePWM2a | | | | | | | | | | | |
| 0xFFFFEAB8 | A9 | | TRACE_D ATA_15 | GPIO_46 | DMM15 | ePWM2b | | | | | | | | | | | |

Table 4-6. Pin Multiplexing (continued)

| ADDRESS | BALL NUMBER | MUXMODE[15:During Power Up] SETTINGS | | | | | | | | | | | | | | | |
|------------|-------------|--------------------------------------|-----------|----------|----------|---|---|---|---|---|---|----|----|----|----|----|----|
| | | During Power Up | 0 | 1 | 2 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0xFFFFEABC | N15 | | TRACE_CLK | GPIO_47 | DMM_CLK | | | | | | | | | | | | |
| 0xFFFFEAC0 | N14 | | TRACE_CTL | RESERVED | DMM_SYNC | | | | | | | | | | | | |

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

T_j junction temperature range (unless otherwise noted)

| PARAMETERS | | MIN | MAX | UNIT |
|--------------------------------|---|--|-------------|------|
| VDDIN | 1.2 V digital power supply | -0.5 | 1.4 | V |
| VIN_SRAM | 1.2 V power rail for internal SRAM | -0.5 | 1.4 | V |
| VNWA | 1.2 V power rail for SRAM array back bias | -0.5 | 1.4 | V |
| VIOIN | I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply. | -0.5 | 3.8 | V |
| VIOIN_18 | 1.8 V supply for CMOS IO | -0.5 | 2 | V |
| VIN_18CLK | 1.8 V supply for clock module | -0.5 | 2 | V |
| VIOIN_18DIFF | 1.8 V supply for port | | | |
| VIOIN_18DIFF | 1.8 V supply for LVDS port | -0.5 | 2 | V |
| VIN_13RF1 | 1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board. | -0.5 | 1.45 | V |
| VIN_13RF2 | | | | |
| VIN_13RF1 | 1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed. | -0.5 | 1.4 | V |
| VIN_13RF2 | | | | |
| VIN_18BB | 1.8-V Analog baseband power supply | -0.5 | 2 | V |
| VIN_18VCO supply | 1.8-V RF VCO supply | -0.5 | 2 | V |
| Input and output voltage range | Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State) | -0.3V | VIOIN + 0.3 | V |
| | Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input | VIOIN + 20% up to 20% of signal period | | |
| CLKP, CLKM | Input ports for reference crystal or external oscillator input | -0.5 | 2 | V |
| Clamp current | Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O. | -20 | 20 | mA |
| T _J | Operating junction temperature range | -40 | 105 | °C |
| T _{STG} | Storage temperature range after soldered onto PC board | -55 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM) ⁽¹⁾ | ±1000 |
| | | Charged-device model (CDM) | ±250 |

- (1) ANSI/ESDA/JEDEC JS0991 specification.

5.3 Power-On Hours (POH)⁽¹⁾

| JUNCTION TEMPERATURE (T _J) | OPERATING CONDITION | NOMINAL CVDD VOLTAGE (V) | POWER-ON HOURS [POH] (HOURS) |
|---|---------------------|--------------------------|------------------------------|
| 90% at 85°C T _J 10% at 105°C T _J | 50% duty cycle | 1.2 | 80,000 |
| 100% at 85°C T _J | | | 100,000 |

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

5.4 Recommended Operating Conditions

Tjunction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|---|-------------|-----|-----------|--------|
| VDDIN | 1.2 V digital power supply | 1.14 | 1.2 | 1.32 | V |
| VIN_SRAM | 1.2 V power rail for internal SRAM | 1.14 | 1.2 | 1.32 | V |
| VNWA | 1.2 V power rail for SRAM array back bias | 1.14 | 1.2 | 1.32 | V |
| VIOIN | I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply. | 3.15 | 3.3 | 3.45 | V |
| | | 1.71 | 1.8 | 1.89 | |
| VIOIN_18 | 1.8 V supply for CMOS IO | 1.71 | 1.8 | 1.9 | V |
| VIN_18CLK | 1.8 V supply for clock module | 1.71 | 1.8 | 1.9 | V |
| VIOIN_18DIFF | 1.8 V supply for LVDS port | 1.71 | 1.8 | 1.9 | V |
| VIN_13RF1 | 1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board | 1.23 | 1.3 | 1.36 | V |
| VIN_13RF2 | | 1.23 | 1.3 | 1.36 | V |
| VIN_13RF1 (1-V Internal LDO bypass mode) | Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed. | 0.95 | 1 | 1.05 | V |
| VIN_13RF2 (1-V Internal LDO bypass mode) | | 0.95 | 1 | 1.05 | V |
| VIN18BB | 1.8-V Analog baseband power supply | 1.71 | 1.8 | 1.9 | V |
| VIN_18VCO | 1.8V RF VCO supply | 1.71 | 1.8 | 1.9 | V |
| V _{IH} | Voltage Input High (1.8 V mode) | 1.17 | | | V |
| | Voltage Input High (3.3 V mode) | 2.25 | | | |
| V _{IL} | Voltage Input Low (1.8 V mode) | | | 0.3*VIOIN | V |
| | Voltage Input Low (3.3 V mode) | | | 0.62 | |
| V _{OH} | High-level output threshold (I _{OH} = 6 mA) | VIOIN – 450 | | | mV |
| V _{OL} | Low-level output threshold (I _{OL} = 6 mA) | | | | 450 mV |
| NRESET SOP[2:0] | V _{IL} (1.8V Mode) | | | 0.2 | V |
| | V _{IH} (1.8V Mode) | 0.96 | | | |
| | V _{IL} (3.3V Mode) | | | 0.3 | |
| | V _{IH} (3.3V Mode) | 1.57 | | | |

5.5 Power Supply Specifications

Table 5-1 describes the four rails from an external power supply block of the IWR1642 device.

Table 5-1. Power Supply Rails Characteristics

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOS IN THE DEVICE |
|--|---|---|
| 1.8 V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS | Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18IO LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.3 V (or 1 V in internal LDO bypass mode) | Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution | Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA |
| 3.3 V (or 1.8 V for 1.8 V I/O mode) | Digital I/Os | Input VIOIN |
| 1.2 V | Core Digital and SRAMs | Input: VDDIN, VIN_SRAM |

Table 5-2 lists tolerable ripple specifications for 1.3-V (1.0-V) and 1.8-V supply rails.

Table 5-2. Ripple Specifications

| FREQUENCY (kHz) | RF RAIL | | VCO/IF RAIL |
|-----------------|---|--------------------------------------|--------------------------------------|
| | 1.0 V (INTERNAL LDO BYPASS) (μV_{RMS}) | 1.3 V (μV_{RMS}) | 1.8 V (μV_{RMS}) |
| 137.5 | 7.76 | 648.73 | 83.41 |
| 275 | 5.83 | 76.48 | 21.27 |
| 550 | 3.44 | 22.74 | 11.43 |
| 1100 | 2.53 | 4.05 | 6.73 |
| 2200 | 11.29 | 82.44 | 13.39 |
| 4400 | 13.65 | 93.35 | 19.70 |
| 6600 | 22.91 | 117.78 | 29.63 |

5.6 Power Consumption Summary

Table 5-3 and summarize the power consumption at the power terminals.

Table 5-3. Maximum Current Ratings at Power Terminals

| PARAMETER | SUPPLY NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|--|--|-----|-----|------|------|
| Current consumption | VDDIN, VIN_SRAM, VNWA | Total current drawn by all nodes driven by 1.2V rail | | | 1000 | mA |
| | VIN_13RF1, VIN_13RF2 | Total current drawn by all nodes driven by 1.3V rail | | | 2000 | |
| | VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO | Total current drawn by all nodes driven by 1.8V rail | | | 850 | |
| | VIOIN | Total current drawn by all nodes driven by 3.3V rail | | | 50 | |

Table 5-4. Average Power Consumption at Power Terminals

| PARAMETER | CONDITION | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------------|---------------------------------|----------------|-------------|--|------|-----|------|
| Average power consumption | 1.0-V internal LDO bypass mode | 25% Duty Cycle | 1TX, 4RX | Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8- μs interchirp time (25% duty cycle), DSP active | 1.3 | | W |
| | | | 2TX, 4RX | | 1.38 | | |
| | | 50% Duty Cycle | 1TX, 4RX | | 1.77 | | |
| | | | 2TX, 4RX | | 1.92 | | |
| | 1.3-V internal LDO enabled mode | 25% Duty Cycle | 1TX, 4RX | Use Case: Low power mode, 3.2 MSps complex transceiver, 25-ms frame time, 128 chirps, 128 samples/chirp, 8- μs interchirp time (25% duty cycle), DSP active | 1.4 | | |
| | | | 2TX, 4RX | | 1.48 | | |
| | | 50% Duty Cycle | 1TX, 4RX | | 1.94 | | |
| | | | 2TX, 4RX | | 2.14 | | |

5.7 RF Specification

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--------------------|--|--|------|------|--------|
| Receiver | Noise figure (Complex 1x mode) | 76 to 77 GHz | 14 | | dB |
| | | 77 to 81 GHz | 15 | | |
| | 1-dB compression point | | -8 | | dBm |
| | Maximum gain | | 48 | | dB |
| | Gain range | | 24 | | dB |
| | Gain step size | | 2 | | dB |
| | Image Rejection Ratio (IMRR) | | 21 | | dB |
| | IF bandwidth ⁽¹⁾ | | | 5 | MHz |
| | A2D sampling rate (real) | | | 12.5 | MSPS |
| | A2D sampling rate (complex) | | | 6.25 | MSPS |
| | A2D resolution | | 12 | | Bits |
| | Return loss (S11) | | <-10 | | dB |
| | Gain mismatch variation (over temperature) | | ±0.5 | | dB |
| | Phase mismatch variation (over temperature) | | ±3 | | ° |
| | In-band IIP2 | RX gain = 30dB IF = 1.5, 2 MHz at -12 dBFS | | 20 | |
| Out-of-band IIP2 | RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm | | 35 | | dBm |
| Idle Channel Spurs | | | -90 | | dBFS |
| Transmitter | Output power | | 12.5 | | dBm |
| | Amplitude noise | | -145 | | dBc/Hz |
| Clock subsystem | Frequency range | 76 | | 81 | GHz |
| | Ramp rate | | | 100 | MHz/μs |
| | Phase noise at 1-MHz offset | 76 to 77 GHz | | -95 | |
| 77 to 81 GHz | | | -93 | | |

(1) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)

| | |
|--------------------|----------------------|
| HPF1 | HPF2 |
| 175, 235, 350, 700 | 350, 700, 1400, 2800 |

The filtering performed by the baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

Figure 5-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

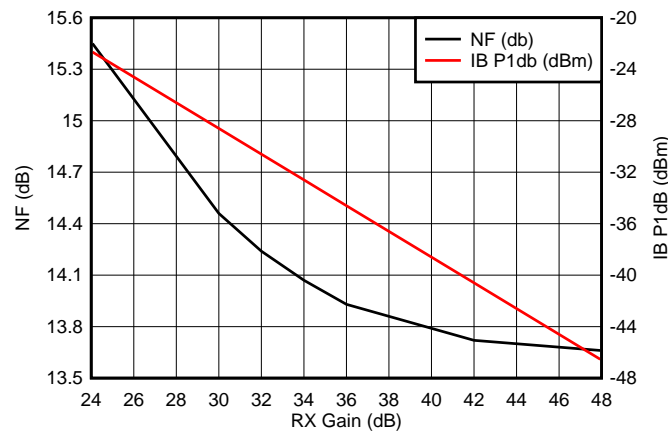


Figure 5-1. Noise Figure, In-band P1dB vs Receiver Gain

5.8 CPU Specifications

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--|--------------------------------------|-----|-----|-----|------|
| DSP Subsystem (C674 Family) | Clock Speed | | 600 | | MHz |
| | L1 Code Memory | | 32 | | KB |
| | L1 Data Memory | | 32 | | KB |
| | L2 Memory | | 256 | | KB |
| Master Controller Subsystem (R4F Family) | Clock Speed | | 200 | | MHz |
| | Tightly Coupled Memory - A (Program) | | 256 | | KB |
| | Tightly Coupled Memory - B (Data) | | 192 | | KB |
| Shared Memory | Shared L3 Memory | | 768 | | KB |

5.9 Thermal Resistance Characteristics for FCBGA Package [ABL0161]⁽¹⁾

| THERMAL METRICS ⁽²⁾ | | °C/W ^{(3) (4)} |
|--------------------------------|-------------------------|-------------------------|
| R _{θJC} | Junction-to-case | 4.92 |
| R _{θJB} | Junction-to-board | 6.57 |
| R _{θJA} | Junction-to-free air | 22.3 |
| R _{θJMA} | Junction-to-moving air | N/A ⁽¹⁾ |
| Psi _{JT} | Junction-to-package top | 4.92 |
| Psi _{JB} | Junction-to-board | 6.4 |

(1) N/A = not applicable

(2) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(3) °C/W = degrees Celsius per watt.

(4) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

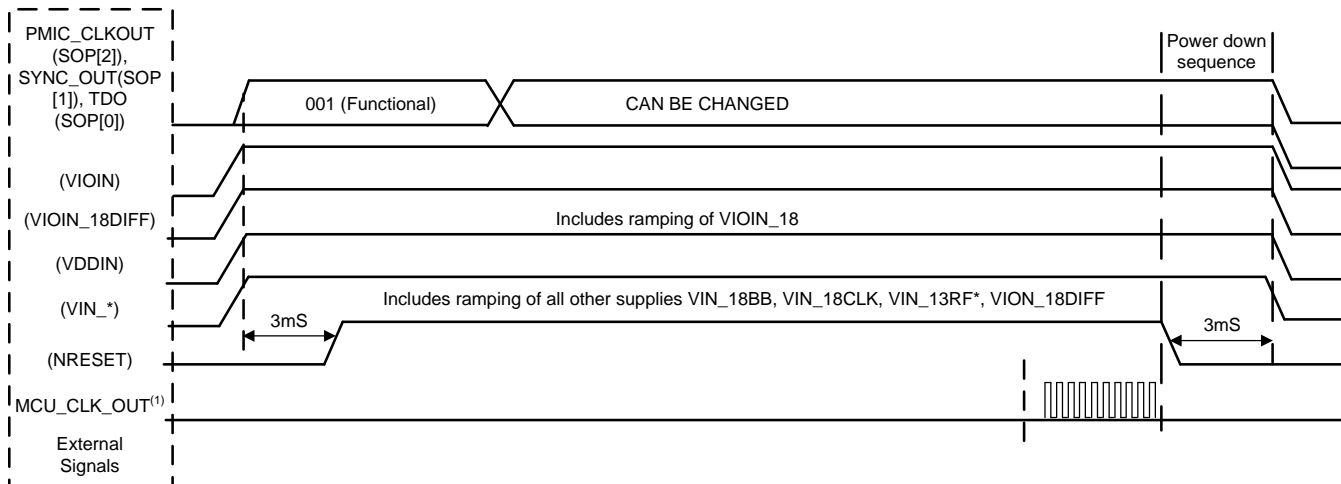
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 105°C is assumed.

5.10 Timing and Switching Characteristics

5.10.1 Power Supply Sequencing and Reset Timing

The IWR1642 device expects all external voltage rails to be stable before reset is deasserted. Figure 5-2 describes the device wake-up sequence.



(1) MCU_CLK_OUT in autonomous mode, where IWR1642 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

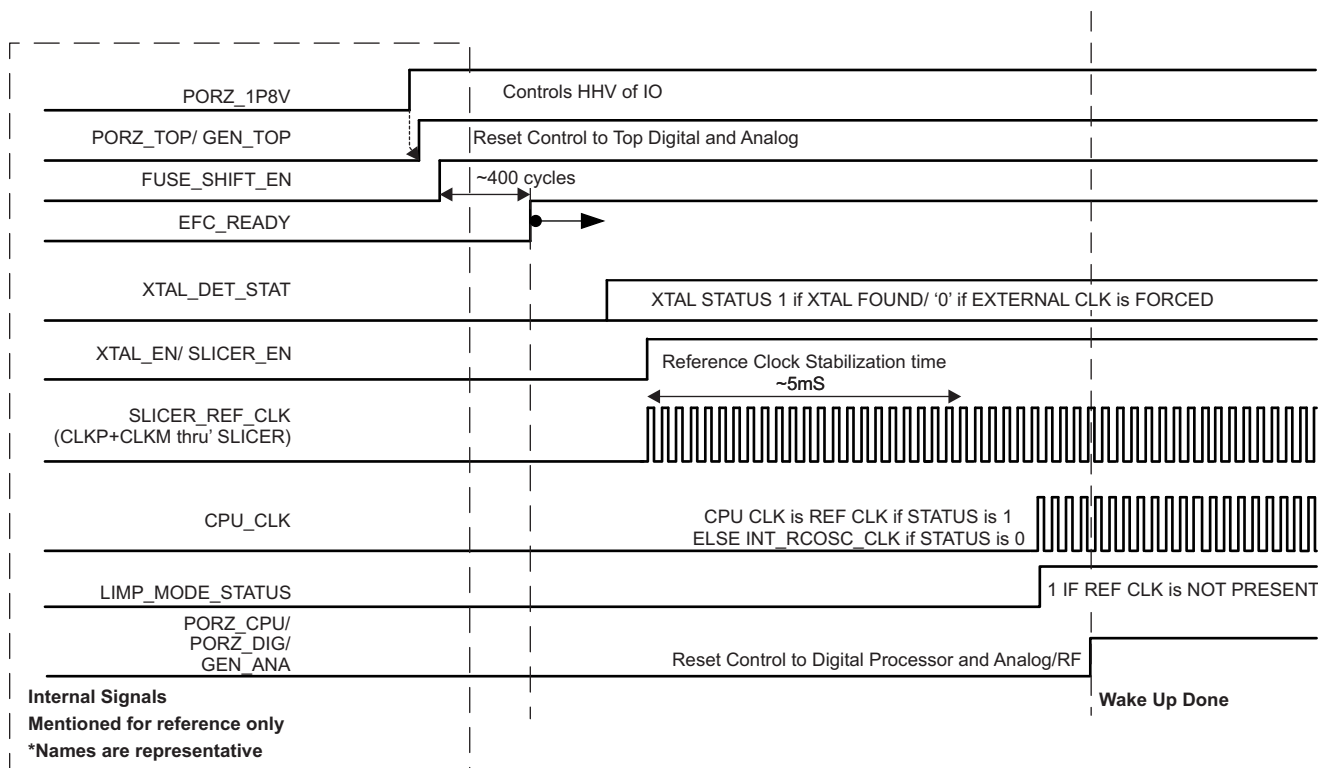


Figure 5-2. Device Wake-up Sequence

5.10.2 Input Clocks and Oscillators

5.10.2.1 Clock Specifications

The IWR1642 requires external clock source (that is, a 40-MHz crystal or external oscillator to CLKP) for initial boot and as a reference for an internal APLL hosted in the device.

An external crystal is connected to the device pins. [Figure 5-3](#) shows the crystal implementation.

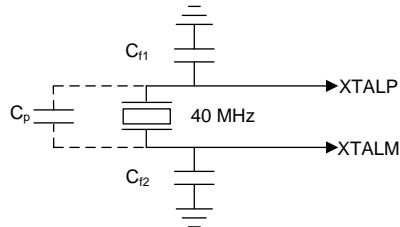


Figure 5-3. Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in [Figure 5-3](#), should be chosen such that [Equation 1](#) is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

[Table 5-5](#) lists the electrical characteristics of the clock crystal.

Table 5-5. Crystal Electrical Characteristics (Oscillator Mode)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|--|-----|-----|-----|--------------------|
| f_p | Parallel resonance crystal frequency | | 40 | | MHz |
| C_L | Crystal load capacitance | 5 | 8 | 12 | pF |
| ESR | Crystal ESR | | | 50 | Ω |
| Temperature range | Expected temperature range of operation | -40 | | 105 | $^{\circ}\text{C}$ |
| Frequency tolerance | Crystal frequency tolerance ⁽¹⁾⁽²⁾⁽³⁾ | -50 | | 50 | ppm |
| Drive level | | | 50 | 200 | μW |

(1) The crystal manufacturer's specification must satisfy this requirement.

(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

(3) Crystal tolerance affects radar sensor accuracy.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. [Table 5-6](#) lists the electrical characteristics of the external clock signal.

Table 5-6. External Clock Mode Specifications

| PARAMETER | | SPECIFICATION | | | UNIT |
|---|------------------------|---------------|-----|------|---------|
| | | MIN | TYP | MAX | |
| Input Clock: External AC-coupled sine wave or DC- coupled square wave Phase Noise referred to 40MHz (80GHz) | Frequency | | 40 | | MHz |
| | AC-Amplitude | 700 | | 1200 | mV (pp) |
| | DC- V_{il} | 0.00 | | 0.20 | V |
| | DC- V_{ih} | 1.6 | | 1.95 | V |
| | Phase Noise at 1 kHz | | | -132 | dBc/Hz |
| | Phase Noise at 10 kHz | | | -143 | dBc/Hz |
| | Phase Noise at 100 kHz | | | -152 | dBc/Hz |
| | Phase Noise at 1 MHz | | | -153 | dBc/Hz |
| | Duty Cycle | 35 | | 65 | % |
| | Freq Tolerance | -50 | | 50 | ppm |
| | Freq Tolerance | -50 | | 50 | ppm |

5.10.3 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

5.10.3.1 Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

5.10.3.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Table 5-8 to Table 5-11 assume the operating conditions stated in Table 5-7.

Table 5-7. SPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

Table 5-8. SPI Master Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|---------------------|--|--|--|----------------------------------|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK ⁽⁴⁾ | 25 | | $256t_{c(VCLK)}$ | ns |
| 2 ⁽⁴⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 3 ⁽⁴⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 4 ⁽⁴⁾ | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 3$ | | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 3$ | | | |
| 5 ⁽⁴⁾ | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 10.5$ | | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 10.5$ | | | |
| 6 ⁽⁵⁾ | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $(C2TDELAY+2) * t_{c(VCLK)} - 7.5$ | $(C2TDELAY+2) * t_{c(VCLK)} + 7$ | ns |
| | | | CSHOLD = 1 | $(C2TDELAY + 3) * t_{c(VCLK)} - 7.5$ | $(C2TDELAY+3) * t_{c(VCLK)} + 7$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $(C2TDELAY+2) * t_{c(VCLK)} - 7.5$ | $(C2TDELAY+2) * t_{c(VCLK)} + 7$ | |
| | | | CSHOLD = 1 | $(C2TDELAY + 3) * t_{c(VCLK)} - 7.5$ | $(C2TDELAY+3) * t_{c(VCLK)} + 7$ | |
| 7 ⁽⁵⁾ | $t_{T2CDELAY}$ | Hold time, SPICLK low until CS inactive (clock polarity = 0) | $0.5 * t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$ | ns | |
| | | Hold time, SPICLK high until CS inactive (clock polarity = 1) | $0.5 * t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (T2CDELAY + 1) * t_{c(VCLK)} + 7.5$ | | |

- (1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
- (2) $t_{c(MSS_VCLK)}$ = master subsystem clock time = $1 / f_{(MSS_VCLK)}$. For more details, see the [Technical Reference Manual](#).
- (3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25ns$.
- (4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
- (5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

Table 5-9. SPI Master Mode Input Timing Requirements (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)⁽¹⁾

| NO. | | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| 8 ⁽²⁾ | $t_{su(SOMI-SPCL)M}$ Setup time, SPISOMI before SPICLK low (clock polarity = 0) | 5 | | | ns |
| | $t_{su(SOMI-SPCH)M}$ Setup time, SPISOMI before SPICLK high (clock polarity = 1) | 5 | | | |
| 9 ⁽²⁾ | $t_{h(SPCL-SOMI)M}$ Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | 3 | | | ns |
| | $t_{h(SPCH-SOMI)M}$ Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | 3 | | | |

- (1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
- (2) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

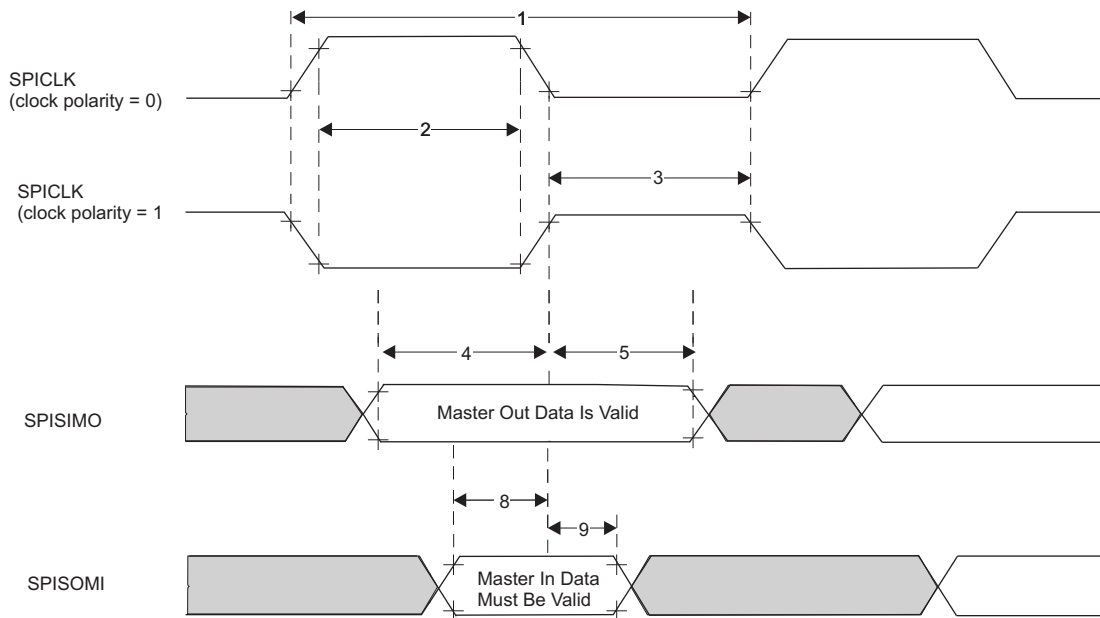


Figure 5-4. SPI Master Mode External Timing (CLOCK PHASE = 0)

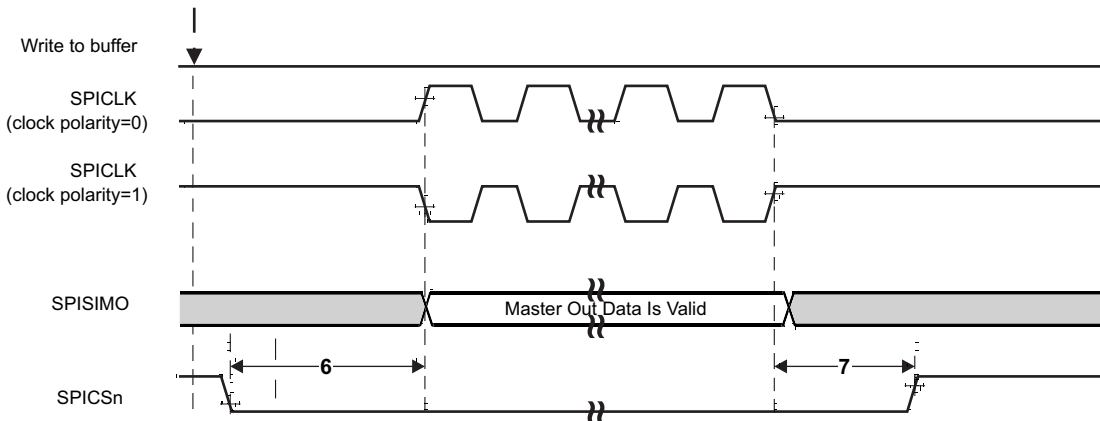


Figure 5-5. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

Table 5-10. SPI Master Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|---------------------|--|--------------------------------------|--|--|------|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK ⁽⁴⁾ | 25 | | $256t_{c(VCLK)}$ | ns |
| 2 ⁽⁴⁾ | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 3 ⁽⁴⁾ | $t_{w(SPCL)M}$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | ns |
| | $t_{w(SPCH)M}$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - 4$ | | $0.5t_{c(SPC)M} + 4$ | |
| 4 ⁽⁴⁾ | $t_{d(SPCH-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 3$ | | | ns |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 3$ | | | |
| 5 ⁽⁴⁾ | $t_{v(SPCL-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0) | $0.5t_{c(SPC)M} - 10.5$ | | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1) | $0.5t_{c(SPC)M} - 10.5$ | | | |
| 6 ⁽⁵⁾ | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | CSHOLD = 0 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} + 7.5$ | ns |
| | | | CSHOLD = 1 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} + 7.5$ | |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | CSHOLD = 0 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 2) * t_{c(VCLK)} + 7.5$ | |
| | | | CSHOLD = 1 | $0.5 * t_{c(SPC)M} + (C2TDELAY + 3) * t_{c(VCLK)} - 7$ | $0.5 * t_{c(SPC)M} + (C2TDELAY + 3) * t_{c(VCLK)} + 7.5$ | |
| 7 ⁽⁵⁾ | $t_{T2CDELAY}$ | Hold time, SPICLK low until CS inactive (clock polarity = 0) | $(T2CDELAY + 1) * t_{c(VCLK)} - 7.5$ | $(T2CDELAY + 1) * t_{c(VCLK)} + 7$ | ns | |
| | | Hold time, SPICLK high until CS inactive (clock polarity = 1) | $(T2CDELAY + 1) * t_{c(VCLK)} - 7.5$ | $(T2CDELAY + 1) * t_{c(VCLK)} + 7$ | | |

- (1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
- (2) $t_{c(MSS_VCLK)}$ = master subsystem clock time = $1 / f_{(MSS_VCLK)}$. For more details, see the [Technical Reference Manual](#).
- (3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
- (4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
- (5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

Table 5-11. SPI Master Mode Input Requirements (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)⁽¹⁾

| NO. | | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| 8 ⁽²⁾ | $t_{su(SOMI-SPCL)M}$ Setup time, SPISOMI before SPICLK low (clock polarity = 0) | 5 | | | ns |
| | $t_{su(SOMI-SPCH)M}$ Setup time, SPISOMI before SPICLK high (clock polarity = 1) | 5 | | | |
| 9 ⁽²⁾ | $t_{h(SPCL-SOMI)M}$ Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0) | 3 | | | ns |
| | $t_{h(SPCH-SOMI)M}$ Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1) | 3 | | | |

- (1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
- (2) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

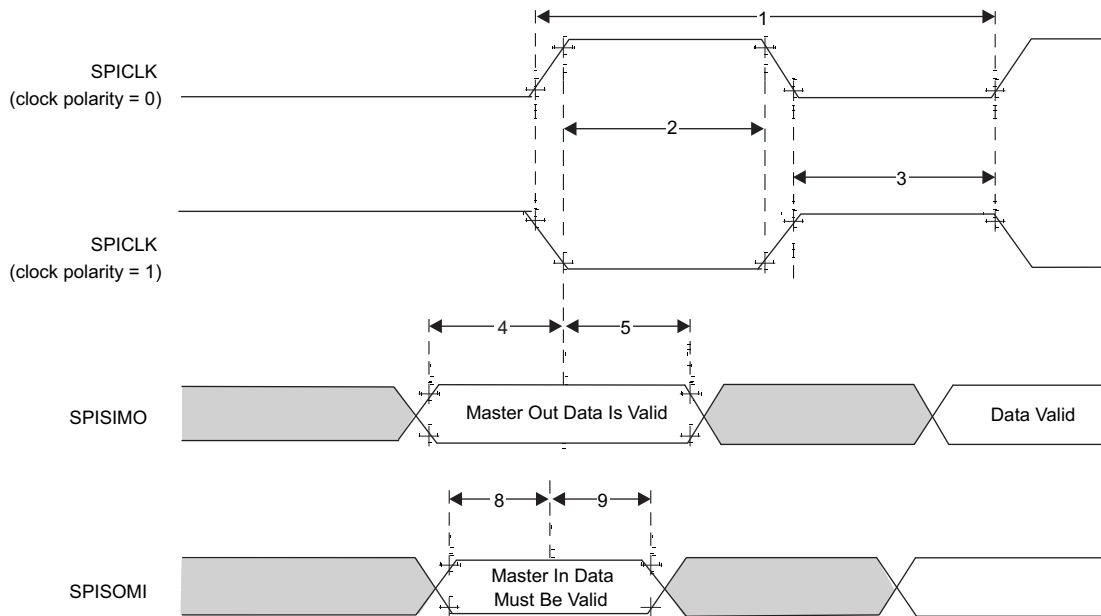


Figure 5-6. SPI Master Mode External Timing (CLOCK PHASE = 1)

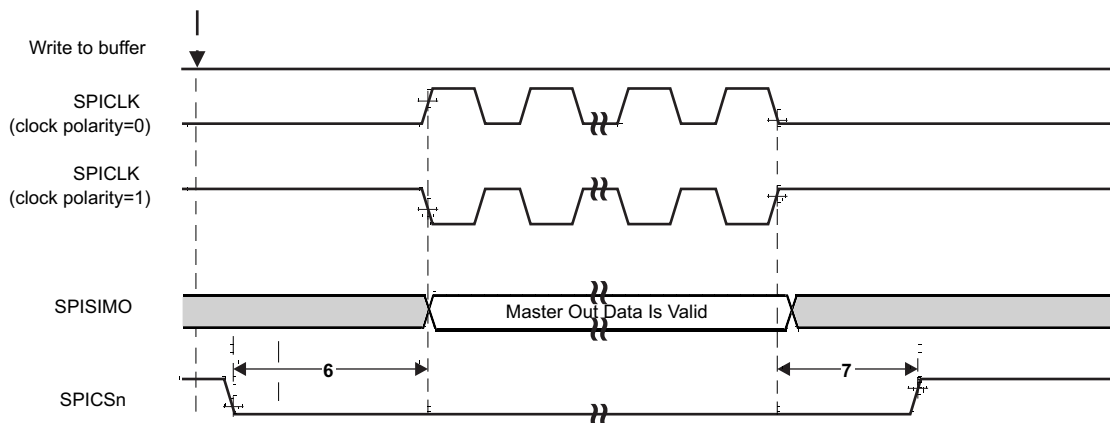


Figure 5-7. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

5.10.3.3 SPI Slave Mode I/O Timings

Table 5-12. SPI Slave Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)⁽¹⁾⁽²⁾⁽³⁾

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|---------------------|--|-----|-----|-----|------|
| 1 | $t_{c(SPC)}S$ | Cycle time, SPICLK ⁽⁴⁾ | 25 | | | ns |
| 2 ⁽⁵⁾ | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 0) | 10 | | | ns |
| | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 1) | 10 | | | |
| 3 ⁽⁵⁾ | $t_{w(SPCL)}S$ | Pulse duration, SPICLK low (clock polarity = 0) | 10 | | | ns |
| | $t_{w(SPCH)}S$ | Pulse duration, SPICLK high (clock polarity = 1) | 10 | | | |
| 4 ⁽⁵⁾ | $t_{d(SPCH-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0) | | | 10 | ns |
| | $t_{d(SPCL-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1) | | | 10 | |
| 5 ⁽⁵⁾ | $t_{h(SPCH-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0) | 2 | | | ns |
| | $t_{h(SPCL-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1) | 2 | | | |
| 4 ⁽⁵⁾ | $t_{d(SPCH-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | | | 10 | ns |
| | $t_{d(SPCL-SOMI)}S$ | Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | | | 10 | |
| 5 ⁽⁵⁾ | $t_{h(SPCH-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 2 | | | ns |
| | $t_{h(SPCL-SOMI)}S$ | Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 2 | | | |

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).

(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.

(3) $t_{c(MSS_VCLK)}$ = master subsystem clock time = $1 / f_{(MSS_VCLK)}$. For more details, see the [Technical Reference Manual](#).

(4) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)}S \geq (PS + 1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)}S = 2t_{c(MSS_VCLK)} \geq 25$ ns.

(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

Table 5-13. SPI Slave Mode Timing Requirements (SPICLK = input, SPISIMO = input, and SPISOMI = output)

| NO. | | | MIN | TYP | MAX | UNIT |
|------------------|----------------------|--|-----|-----|-----|------|
| 6 ⁽¹⁾ | $t_{su(SIMO-SPCL)}S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0) | 3 | | | ns |
| | $t_{su(SIMO-SPCH)}S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1) | 3 | | | |
| 7 ⁽¹⁾ | $t_{h(SPCL-SIMO)}S$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0) | 0 | | | ns |
| | $t_{h(SPCL-SIMO)}S$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0) | 0 | | | |
| 6 ⁽¹⁾ | $t_{su(SIMO-SPCL)}S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 3 | | | ns |
| | $t_{su(SIMO-SPCH)}S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 3 | | | |
| 7 ⁽¹⁾ | $t_{h(SPCL-SIMO)}S$ | Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) | 1 | | | ns |
| | $t_{h(SPCL-SIMO)}S$ | Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) | 1 | | | |

(1) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

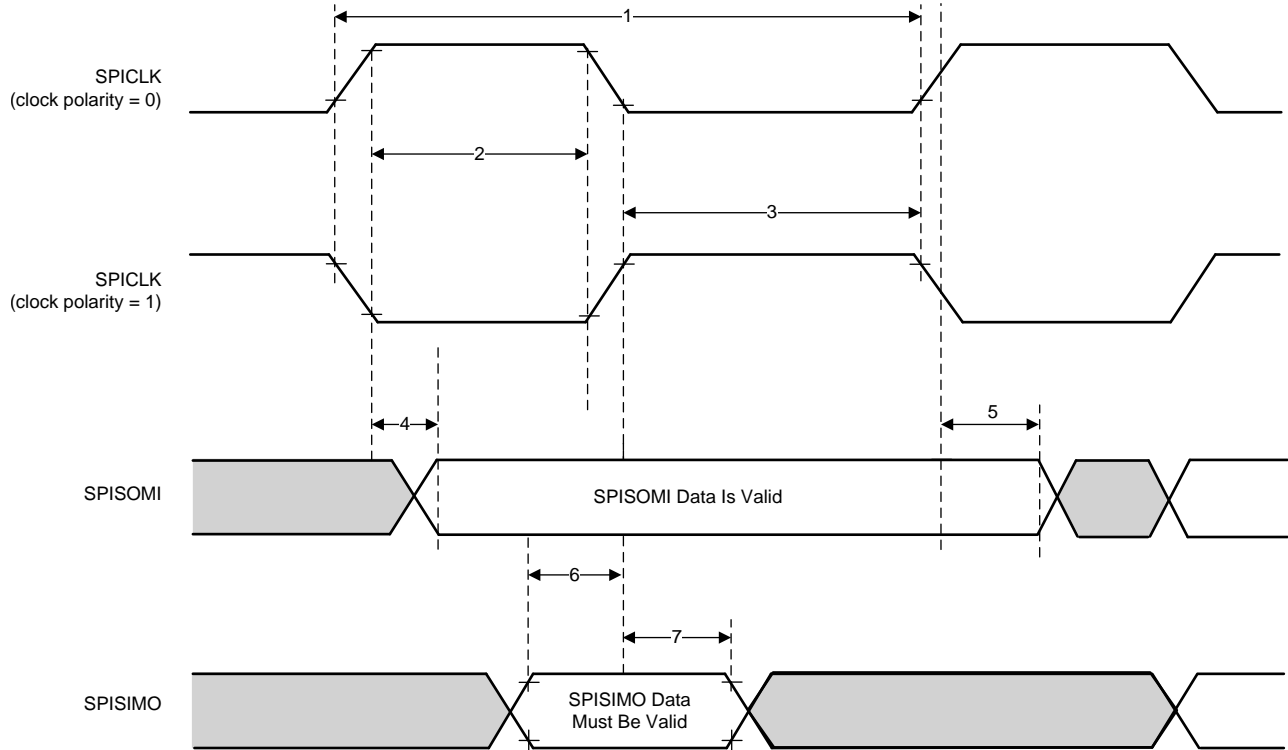


Figure 5-8. SPI Slave Mode External Timing (CLOCK PHASE = 0)

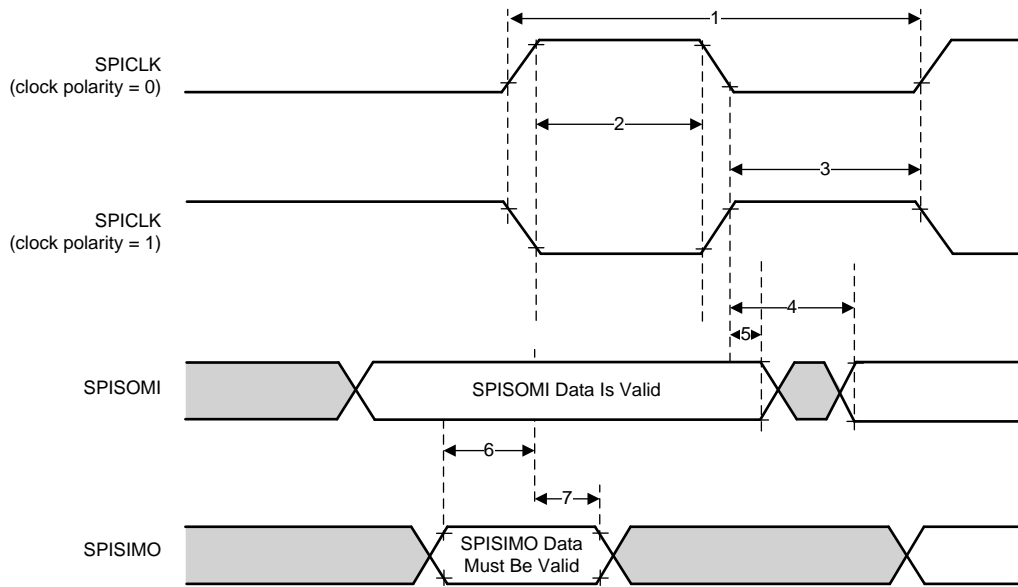


Figure 5-9. SPI Slave Mode External Timing (CLOCK PHASE = 1)

5.10.3.4 Typical Interface Protocol Diagram (Slave Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 5-10 shows the SPI communication timing of the typical interface protocol.

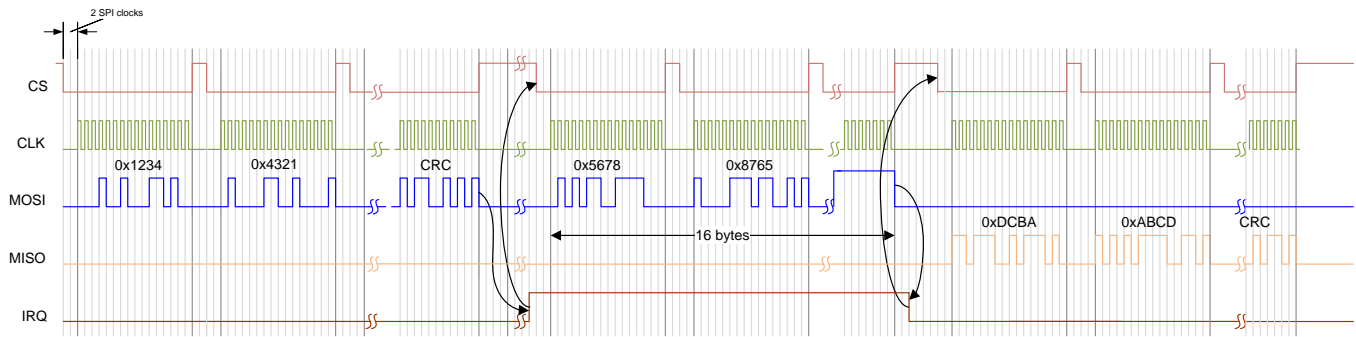


Figure 5-10. SPI Communication

5.10.4 LVDS Interface Configuration

The IWR1642 supports four differential LVDS IOs/Lanes. The lane configuration supported is two Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

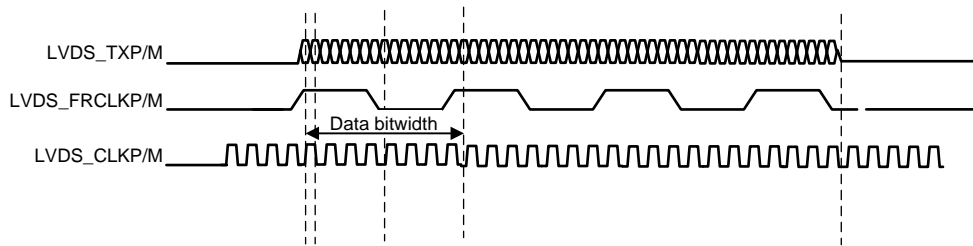
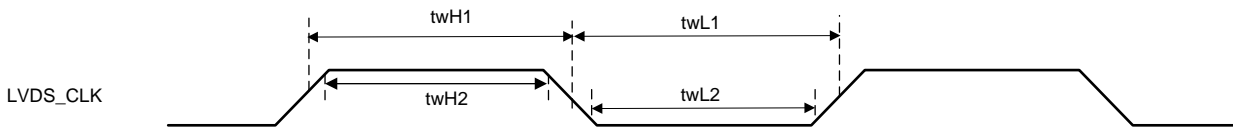


Figure 5-11. LVDS Interface Lane Configuration And Relative Timings

5.10.4.1 LVDS Interface Timings



Calculation showing tw parameters:

Freq = 900MHz, Period = 1.11ns
 At 50% $twH1/twL1 = 1.11ns/2 = 0.55ns$
 Rise time = Fall time = 200ps (as per LVDS IO spec @1pF load)
 $twH2/twL2 = (1.11ns - 2 * 200ps) / 2 = 0.35ns$

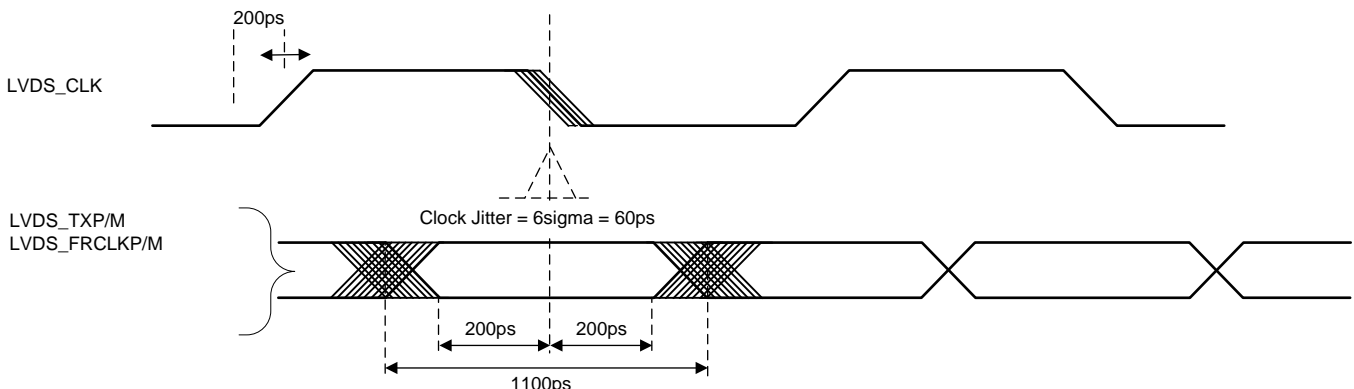


Figure 5-12. Timing Parameters

Table 5-14. LVDS Electrical Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------|---|------|------|------|------|
| | twH1 / twL1 | | | 0.55 | | ns |
| | twH2 / twL2 | | | 0.35 | | ns |
| | Duty Cycle Requirements | max 1 pF lumped capacitive load on LVDS lanes | 48% | | 52% | |
| | VOH | | | | 1475 | mV |
| | VOL | | 925 | | | mV |
| | Output Differential Voltage | peak-to-peak single-ended with 100 Ω resistive load between differential pairs | 250 | | 450 | mV |
| | Output Offset Voltage | | 1125 | | 1275 | mV |

5.10.5 General-Purpose Input/Output

Table 5-15 lists the switching characteristics of output timing relative to load capacitance.

Table 5-15. Switching Characteristics for Output Timing versus Load Capacitance (C_L)⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | VIOIN = 1.8V | VIOIN = 3.3V | UNIT | |
|-----------|---------------|------------------|---------------|--------------|--------|----|
| t_r | Max rise time | Slew control = 0 | $C_L = 20$ pF | 2.878 | 3.013 | ns |
| | | | $C_L = 50$ pF | 6.446 | 6.947 | |
| | | | $C_L = 75$ pF | 9.43 | 10.249 | |
| t_f | Max fall time | | $C_L = 20$ pF | 2.827 | 2.883 | ns |
| | | | $C_L = 50$ pF | 6.442 | 6.687 | |
| | | | $C_L = 75$ pF | 9.439 | 9.873 | |
| t_r | Max rise time | Slew control = 1 | $C_L = 20$ pF | 3.307 | 3.389 | ns |
| | | | $C_L = 50$ pF | 6.77 | 7.277 | |
| | | | $C_L = 75$ pF | 9.695 | 10.57 | |
| t_f | Max fall time | | $C_L = 20$ pF | 3.128 | 3.128 | ns |
| | | | $C_L = 50$ pF | 6.656 | 6.656 | |
| | | | $C_L = 75$ pF | 9.605 | 9.605 | |

- (1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

5.10.6 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- Configurable Message objects
- Individual identifier masks for each message object
- Programmable FIFO mode for message objects
- Suspend mode for debug support
- Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- Supports two interrupt lines - Level 0 and Level 1
- Automatic Message RAM initialization

Table 5-16. Dynamic Characteristics for the DCANx TX and RX Pins

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| $t_{d(CAN_tx)}$ | Delay time, transmit shift register to CAN_tx pin ⁽¹⁾ | | | 15 | ns |
| $t_{d(CAN_rx)}$ | Delay time, CAN_rx pin to receive shift register ⁽¹⁾ | | | 10 | ns |

(1) These values do not include rise/fall times of the output buffer.

5.10.7 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

Table 5-17. SCI Timing Requirements

| | | MIN | TYP | MAX | UNIT |
|---------|------------------------------|-----|-------|-----|------|
| f(baud) | Supported baud rate at 20 pF | | 921.6 | | kHz |

5.10.8 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I²C-bus™. This module will support any slave or master I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
 - Bit/Byte format transfer
 - 7-bit and 10-bit device addressing modes
 - General call
 - START byte
 - Multi-master transmitter/ slave receiver mode
 - Multi-master receiver/ slave transmitter mode
 - Combined master transmit/receive and receive/transmit mode
 - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

NOTE

This I2C module does not support:

- High-speed (HS) mode
 - C-bus compatibility mode
 - The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)
-

Table 5-18. I2C Timing Requirements⁽¹⁾

| | | STANDARD MODE | | FAST MODE | | UNIT |
|---------------------|---|---------------|---------------------|-----------|-----|---------------|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | μs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μs |
| $t_h(SCLL-SDAL)$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μs |
| $t_w(SCLL)$ | Pulse duration, SCL low | 4.7 | | 1.3 | | μs |
| $t_w(SCLH)$ | Pulse duration, SCL high | 4 | | 0.6 | | μs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | μs |
| $t_h(SCLL-SDA)$ | Hold time, SDA valid after SCL low | 0 | 3.45 ⁽¹⁾ | 0 | 0.9 | μs |
| $t_w(SDAH)$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μs |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | μs |
| $t_w(SP)$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| $C_b^{(2)(3)}$ | Capacitive load for each bus line | | 400 | | 400 | pF |

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) The maximum $t_h(SDA-SCLL)$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_w(SCLL)$) of the SCL signal.
- (3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

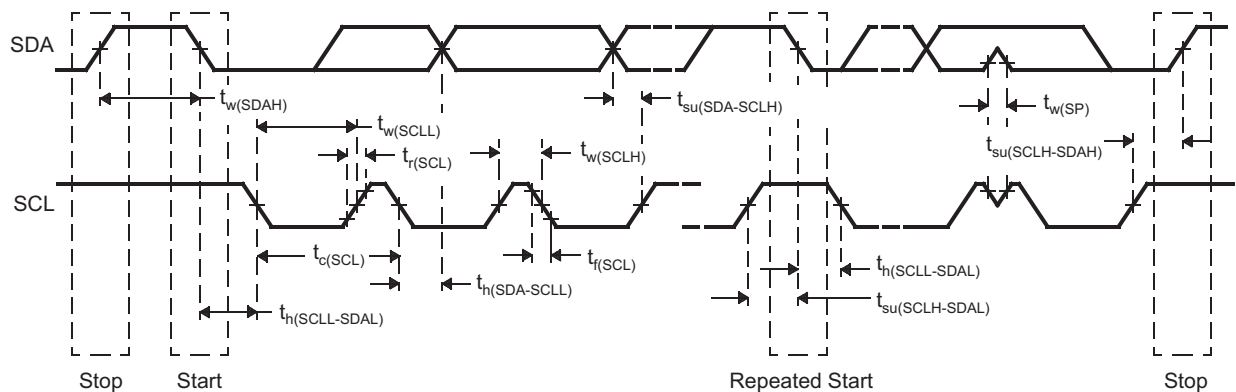


Figure 5-13. I2C Timing Diagram

NOTE

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_h(SDA-SCLL)$ has only to be met if the device does not stretch the LOW period ($t_w(SCLL)$) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r \max + t_{su(SDA-SCLH)}$.

5.10.9 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI™) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a master only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Refer to the [Technical Reference Manual](#) for details on QSPI SFDP register and power on values MSS BootROM required items.

[Table 5-20](#) and [Table 5-21](#) assume the operating conditions stated in [Table 5-19](#).

Table 5-19. QSPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

Table 5-20. Timing Requirements for QSPI Input (Read) Timings⁽¹⁾⁽²⁾

| | | MIN | TYP | MAX | UNIT |
|------------------|---|-----------------|-----|-----|------|
| $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | 7.3 | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge | 1.5 | | | ns |
| $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | $7.3 - P^{(3)}$ | | | ns |
| $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | $1.5 + P^{(3)}$ | | | ns |

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.

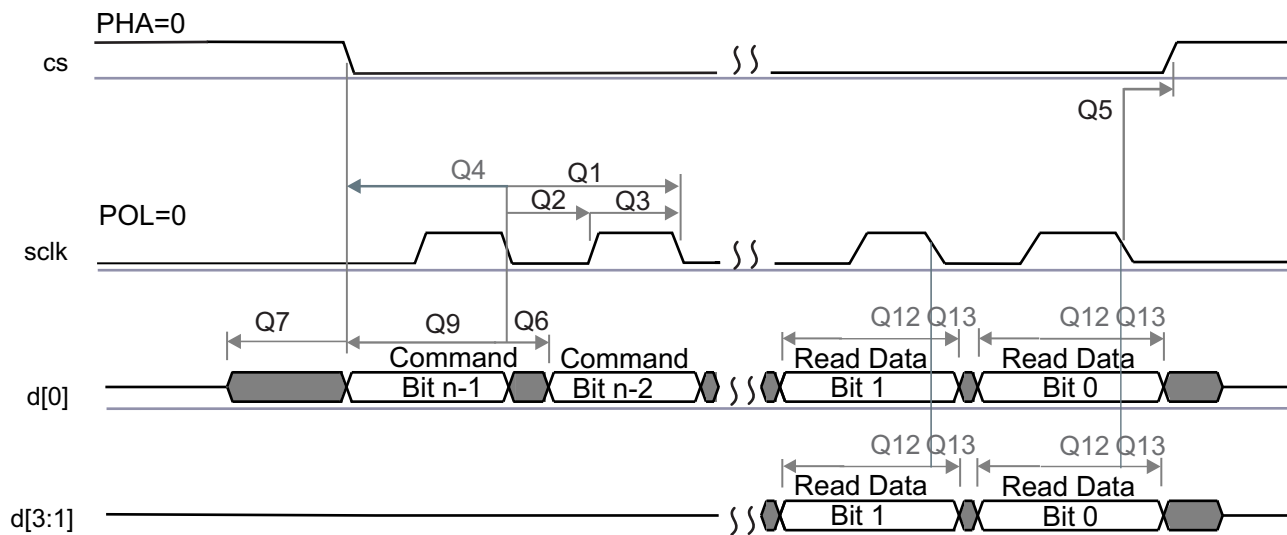
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.

(3) P = SCLK period in ns.

Table 5-21. QSPI Switching Characteristics

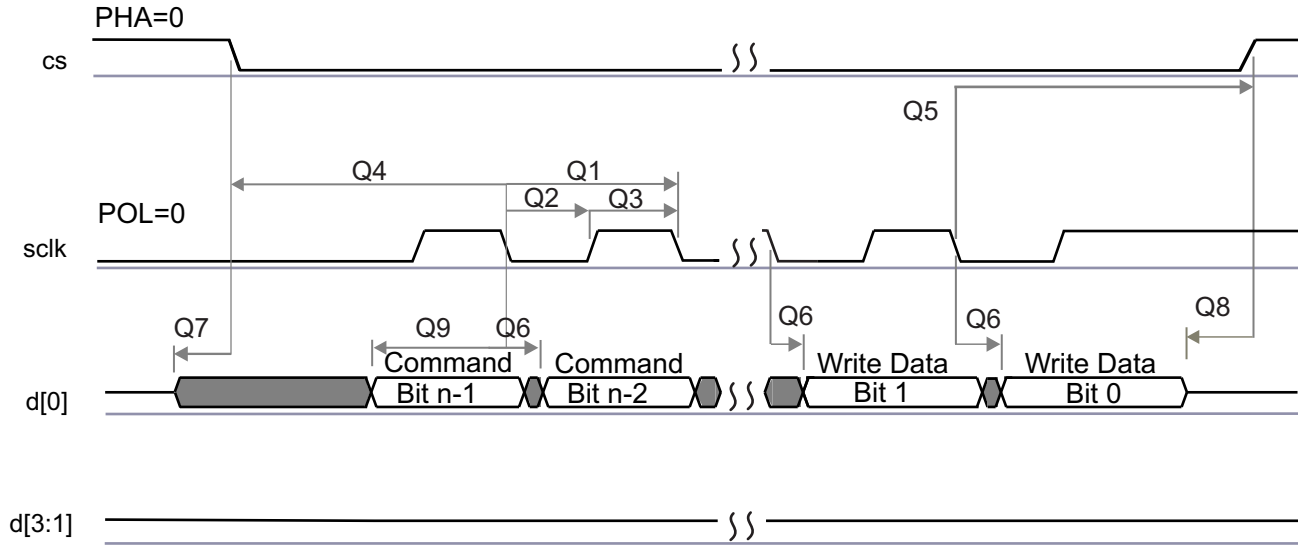
| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|----------------------------------|---|---------------------------|-----|-----------------------------|------|
| Q1 | $t_c(\text{SCLK})$ | Cycle time, sclk | 25 | | | ns |
| Q2 | $t_w(\text{SCLKL})$ | Pulse duration, sclk low | $Y \cdot P - 3^{(1)(2)}$ | | | ns |
| Q3 | $t_w(\text{SCLKH})$ | Pulse duration, sclk high | $Y \cdot P - 3^{(1)(1)}$ | | | ns |
| Q4 | $t_d(\text{CS-SCLK})$ | Delay time, sclk falling edge to cs active edge | $-M \cdot P - 1^{(1)(3)}$ | | $-M \cdot P + 2.5^{(1)(3)}$ | ns |
| Q5 | $t_d(\text{SCLK-CS})$ | Delay time, sclk falling edge to cs inactive edge | $N \cdot P - 1^{(1)(3)}$ | | $N \cdot P + 2.5^{(1)(3)}$ | ns |
| Q6 | $t_d(\text{SCLK-D1})$ | Delay time, sclk falling edge to d[1] transition | -3.5 | | 7 | ns |
| Q7 | $t_{\text{ena}}(\text{CS-D1LZ})$ | Enable time, cs active edge to d[1] driven (lo-z) | $-P - 4^{(3)}$ | | $-P + 1^{(3)}$ | ns |
| Q8 | $t_{\text{dis}}(\text{CS-D1Z})$ | Disable time, cs active edge to d[1] tri-stated (hi-z) | $-P - 4^{(3)}$ | | $-P + 1^{(3)}$ | ns |
| Q9 | $t_d(\text{SCLK-D1})$ | Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only) | $-3.5 - P^{(3)}$ | | $7 - P^{(3)}$ | ns |
| Q12 | $t_{\text{su}}(\text{D-SCLK})$ | Setup time, d[3:0] valid before falling sclk edge | 7.3 | | | ns |
| Q13 | $t_{\text{h}}(\text{SCLK-D})$ | Hold time, d[3:0] valid after falling sclk edge | 1.5 | | | ns |
| Q14 | $t_{\text{su}}(\text{D-SCLK})$ | Setup time, final d[3:0] bit valid before final falling sclk edge | $7.3 - P^{(3)}$ | | | ns |
| Q15 | $t_{\text{h}}(\text{SCLK-D})$ | Hold time, final d[3:0] bit valid after final falling sclk edge | $1.5 + P^{(3)}$ | | | ns |

- (1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals $(\text{DCLK_DIV}/2) / (\text{DCLK_DIV}+1)$. For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. The HSDIVIDER on CLKOUTX2_H13 output of DPLL_PER can be used to achieve the desired clock divider ratio. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
- (2) P = SCLK period in ns.
- (3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2



SPRS85v_TIMING_OSP1_02

Figure 5-14. QSPI Read (Clock Mode 0)



SPRS85v_TIMING_OSP11_04

Figure 5-15. QSPI Write (Clock Mode 0)

5.10.10 ETM Trace Interface

Table 5-23 and assume the recommended operating conditions stated in Table 5-22.

Table 5-22. ETMTRACE Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Output Conditions | | | | | |
| C _{LOAD} | Output load capacitance | 2 | | 20 | pF |

Table 5-23. ETM TRACE Switching Characteristics

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|--|-----|-----|-----|------|
| 1 | t _{cyc(ETM)} Cycle time, TRACECLK period | 20 | | | ns |
| 2 | t _{h(ETM)} Pulse Duration, TRACECLK High | 9 | | | ns |
| 3 | t _{l(ETM)} Pulse Duration, TRACECLK Low | 9 | | | ns |
| 4 | t _{r(ETM)} Clock and data rise time | | | 3.3 | ns |
| 5 | t _{f(ETM)} Clock and data fall time | | | 3.3 | ns |
| 6 | t _{d(ETMTRAC ECLKH- ETMDATAV)} Delay time, ETM trace clock high to ETM data valid | 1 | | 7 | ns |
| 7 | t _{d(ETMTRAC ECLKL- ETMDATAV)} Delay time, ETM trace clock low to ETM data valid | 1 | | 7 | ns |

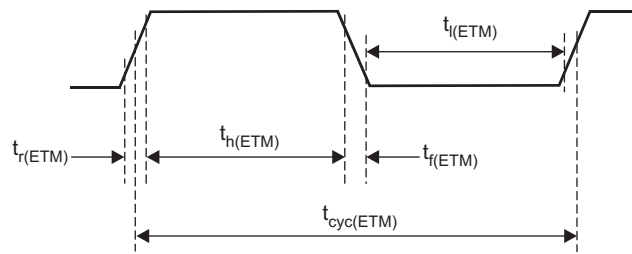


Figure 5-16. ETMTRACECLKOUT Timing

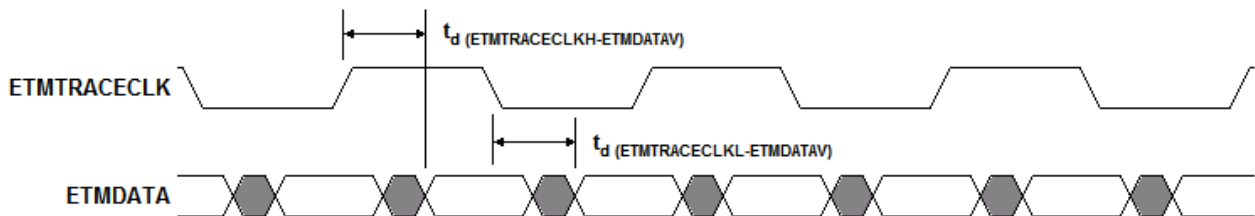


Figure 5-17. ETMDATA Timing

5.10.11 Data Modification Module (DMM)

A Data Modification Module (DMM) gives the ability to write external data into the device memory.

The DMM has the following features:

- Acts as a bus master, thus enabling direct writes to the 4GB address space without CPU intervention
- Writes to memory locations specified in the received packet (leverages packets defined by trace mode of the RAM trace port [RTP] module)
- Writes received data to consecutive addresses, which are specified by the DMM (leverages packets defined by direct data mode of RTP module)
- Configurable port width (1, 2, 4, 8, 16 pins)
- Up to 65 Mbit/s pin data rate

Table 5-24. DMM Timing Requirements

| | | MIN | TYP | MAX | UNIT |
|----------------|---|------|-----|-----|------|
| $t_{cyc(DMM)}$ | Clock period | 15.4 | | | ns |
| t_R | Clock rise time | 1 | | 3 | ns |
| t_F | Clock fall time | 1 | | 3 | ns |
| $t_{h(DMM)}$ | High pulse width | 6 | | | ns |
| $t_{l(DMM)}$ | Low pulse width | 6 | | | ns |
| $t_{ssu(DMM)}$ | SYNC active to clk falling edge setup time | 2 | | | ns |
| $t_{sh(DMM)}$ | DMM clk falling edge to SYNC deactive hold time | 3 | | | ns |
| $t_{dsu(DMM)}$ | DATA to DMM clk falling edge setup time | 2 | | | ns |
| $t_{dh(DMM)}$ | DMM clk falling edge to DATA hold time | 3 | | | ns |

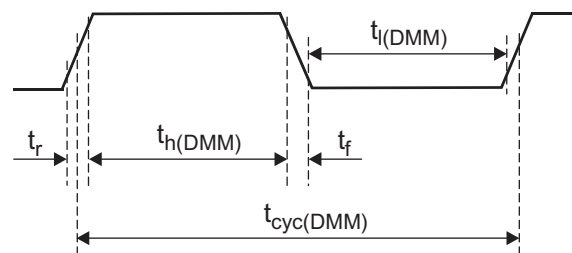


Figure 5-18. DMMCLK Timing

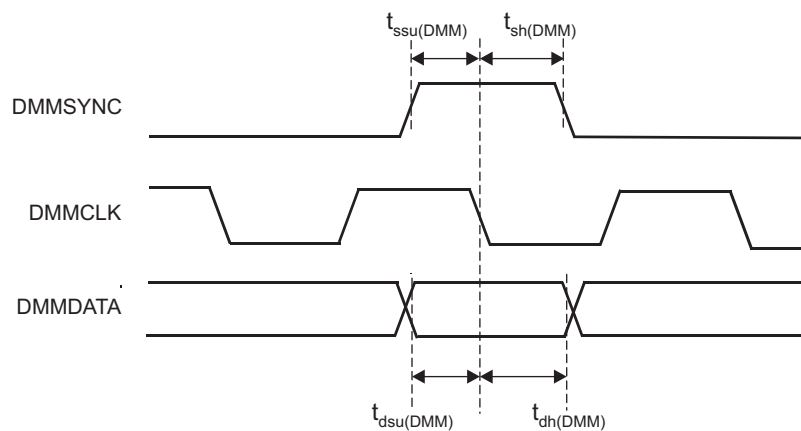


Figure 5-19. DMMDATA Timing

5.10.12 JTAG Interface

Table 5-26 and Table 5-27 assume the operating conditions stated in Table 5-25.

Table 5-25. JTAG Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

Table 5-26. Timing Requirements for IEEE 1149.1 JTAG

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|-------------------|---|-------|-----|-----|------|
| 1 | $t_c(TCK)$ | Cycle time TCK | 66.66 | | | ns |
| 1a | $t_w(TCKH)$ | Pulse duration TCK high (40% of t_c) | 26.67 | | | ns |
| 1b | $t_w(TCKL)$ | Pulse duration TCK low(40% of t_c) | 26.67 | | | ns |
| 3 | $t_{su}(TDI-TCK)$ | Input setup time TDI valid to TCK high | 2.5 | | | ns |
| | $t_{su}(TMS-TCK)$ | Input setup time TMS valid to TCK high | 2.5 | | | ns |
| 4 | $t_h(TCK-TDI)$ | Input hold time TDI valid from TCK high | 18 | | | ns |
| | $t_h(TCK-TMS)$ | Input hold time TMS valid from TCK high | 18 | | | ns |

Table 5-27. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|------------------|----------------------------------|-----|-----|-----|------|
| 2 | $t_d(TCKL-TDOV)$ | Delay time, TCK low to TDO valid | 0 | | 25 | ns |

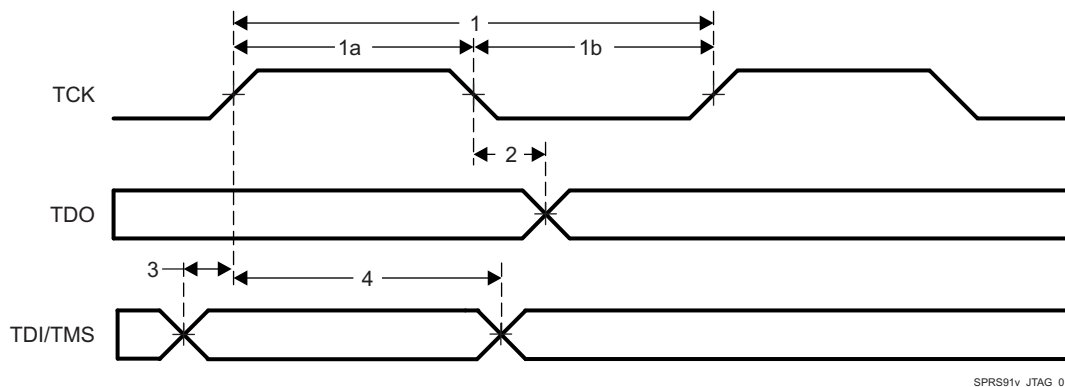


Figure 5-20. JTAG Timing

6 Detailed Description

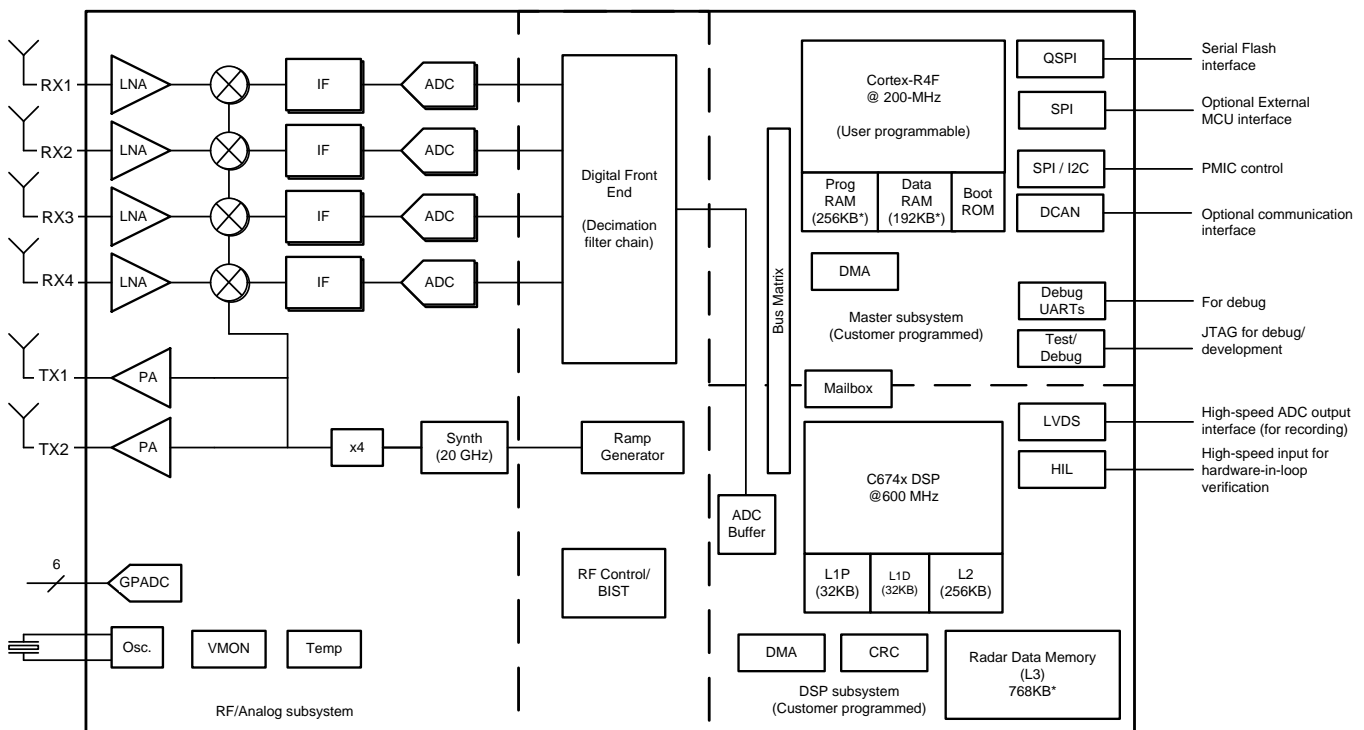
6.1 Overview

The IWR1642 device includes the entire Millimeter Wave blocks and analog baseband signal chain for two transmitters and four receivers, as well as a customer-programmable MCU and DSP. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive industrial radar sensing applications. Examples are:

- Industrial level sensing
- Industrial automation sensor fusion with radar
- Traffic intersection monitoring with radar
- Industrial radar-proximity monitoring
- People counting
- Gesturing

In terms of scalability, the IWR1642 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. The IWR1642 has an embedded DSP for signal processing, processing the radar signals for FFT, magnitude, detection and other applications.

6.2 Functional Block Diagram



* Up to 512KB of Radar Data Memory can be switched to the Master R4F if required

6.3 Subsystems

6.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The two transmit channels can be operated simultaneously. The four receive channels can be operated simultaneously.

6.3.1.1 Clock Subsystem

The IWR1642 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76- to 81-GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 6-1 describes the clock subsystem.

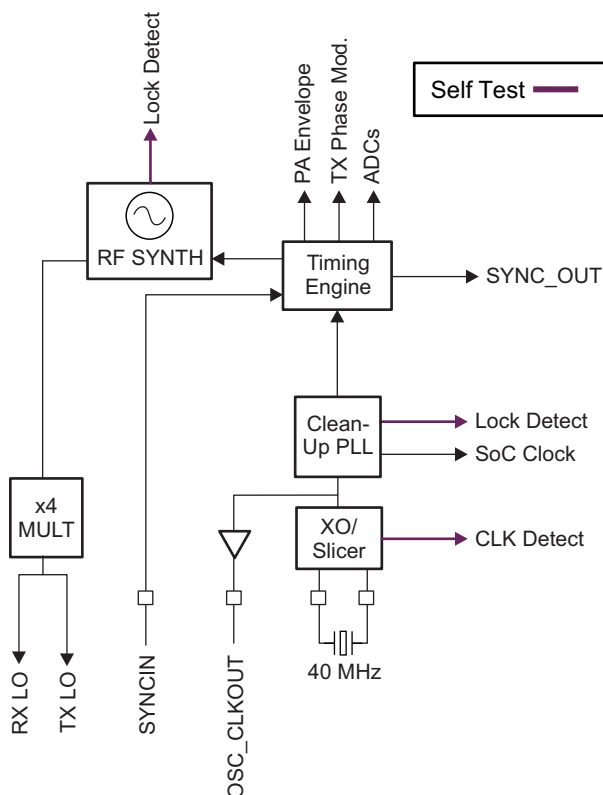


Figure 6-1. Clock Subsystem

6.3.1.2 Transmit Subsystem

The IWR1642 transmit subsystem consists of two parallel transmit chains, each with independent phase and amplitude control. The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12.5 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 6-2 describes the transmit subsystem.

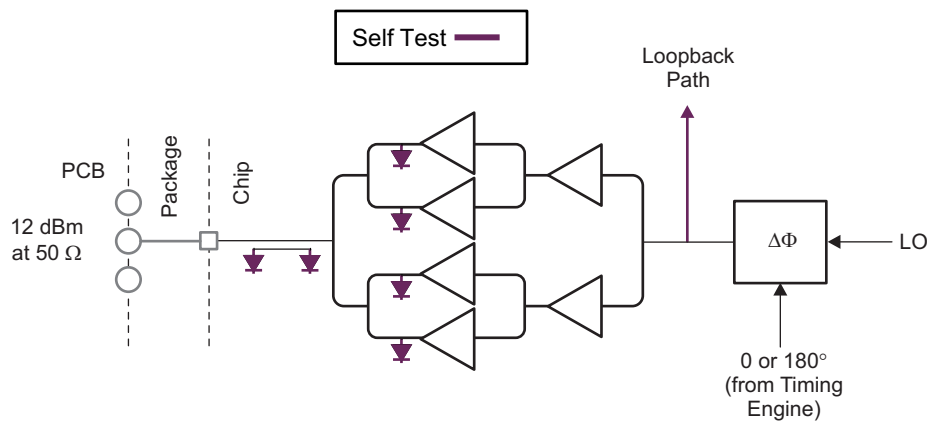


Figure 6-2. Transmit Subsystem (Per Channel)

6.3.1.3 Receive Subsystem

The IWR1642 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, A2D conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the IWR1642 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The IWR1642 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 5 MHz.

Figure 6-3 describes the receive subsystem.

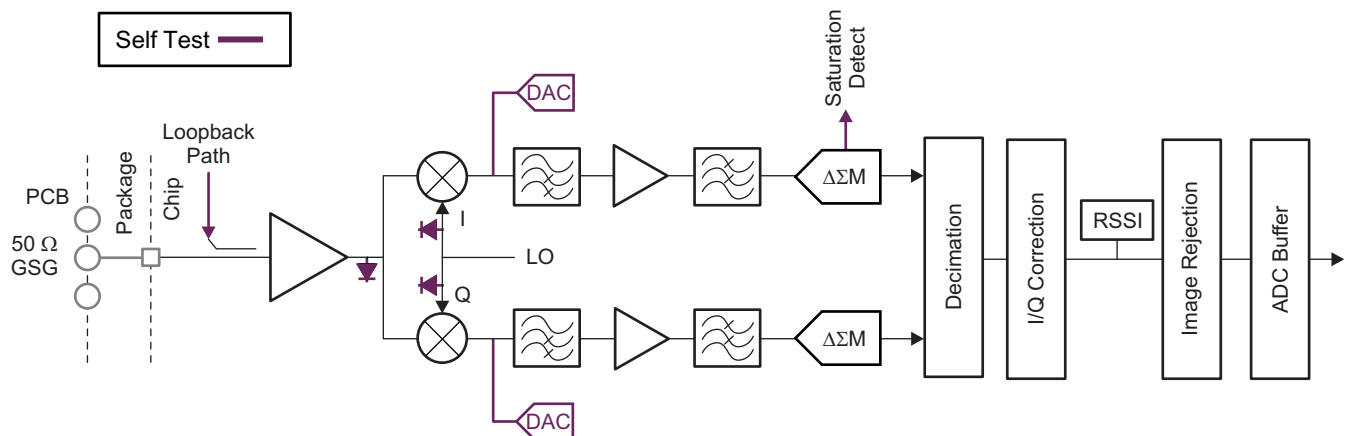
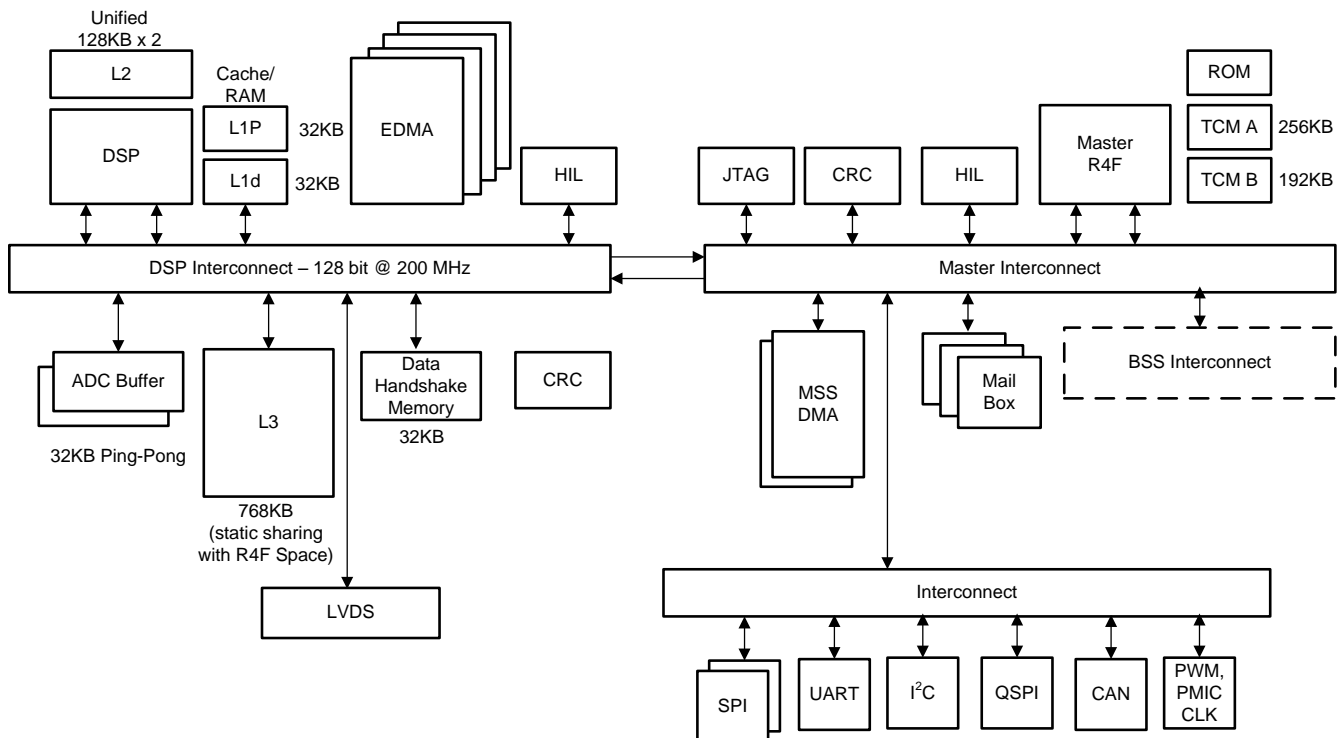


Figure 6-3. Receive Subsystem (Per Channel)

6.3.2 Processor Subsystem



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Figure 6-4. Processor Subsystem

Figure 6-4 shows the block diagram for customer programmable processor subsystems in the IWR1642 device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. Left hand side shows the DSP Subsystem which contains TI's high-performance C674x DSP, a high-bandwidth interconnect for high performance (128-bit, 200MHz) and associated peripherals – four DMAs for data transfer, LVDS interface for Measurement data output, L3 Radar data cube memory, ADC buffers, CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Master subsystem. Master subsystem as name suggests is the master of the device and controls all the device peripherals and house-keeping activities of the device. Master subsystem contains Cortex-R4F (Master R4F) processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I²C, UART, SPIs, CAN, PMIC clocking module, PWM, and others) connected to Master Interconnect through Peripheral Central Resource (PCR interconnect).

Details of the DSP CPU core can be found at <http://www.ti.com/product/TMS320C6748>.

HIL module is shown in both the subsystems and can be used to perform the radar operations feeding the captured data from outside into the device without involving the RF subsystem. HIL on master SS is for controlling the configuration and HIL on DSPSS for high speed ADC data input to the device. Both HIL modules uses the same IOs on the device, one additional IO (DMM_MUX_IN) allows selecting either of the two.

6.3.3 Host Interface

The host interface can be provided through a SPI, UART, or CAN interface. In some cases the serial interface for industrial applications is transcoded to a different serial standard.

The IWR1642 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (slave) for host control. All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host
- Host Interrupt - an indication that the mmwave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

6.3.4 Master Subsystem Cortex-R4F Memory Map

Table 6-1 shows the master subsystem, Cortex-R4F memory map.

NOTE

There are separate Cortex-R4F addresses and DMA MSS addresses for the master subsystem. See the [Technical Reference Manual](#) for a complete list.

Table 6-1. Master Subsystem, Cortex-R4F Memory Map

| NAME | FRAME ADDRESS (HEX) | | SIZE | DESCRIPTION |
|-------------------------------------|---------------------|---------------------------------|---------|--|
| | START | END | | |
| CPU Tightly-Coupled Memories | | | | |
| TCMA ROM | 0x0000_0000 | 0x0001_FFFF | 128 KiB | Program ROM |
| TCM RAM-A | 0x0020_0000 | 0x0023_FFFF (or 0x0027_FFFF) | 512 KiB | 256/512KB based on variant |
| TCM RAM-B | 0x0800_0000 | 0x0802_FFFF | 192 KB | Data RAM |
| S/W Scratch Pad Memory | | | | |
| SW_Buffer | 0x0C20_0000 | 0x0C20_1FFF | 8 KB | S/W Scratchpad memory |
| System Peripherals | | | | |
| Mail Box MSS<->RADARSS | 0xF060_1000 | 0xF060_17FF | 2 KB | RADARSS to MSS mailbox memory space |
| | 0xF060_2000 | 0xF060_27FF | | MSS to RADARSS mailbox memory space |
| | 0xF060_8000 | 0xF060_80FF | 188 B | MSS to RADARSS mailbox Configuration registers |
| | 0xF060_8060 | 0xF060_86FF | | RADARSS to MSS mailbox Configuration registers |
| Mail Box MSS<->DSPSS | 0xF060_4000 | 0xF060_47FF | 2 KB | DSPSS to MSS mailbox memory space |
| | 0xF060_5000 | 0xF060_57FF | | MSS to DSPSS mailbox memory space |
| | 0xF060_8400 | 0xF060_84FF | 188 B | MSS to DSPSS mailbox Configuration registers |
| | 0xF060_8300 | 0xF060_83FF | | DSPSS to MSS mailbox Configuration registers |
| Mail Box RADARSS<->DSPSS | 0xF060_6000 | 0xF060_67FF | 2 KB | RADARSS to DSPSS mailbox memory space |
| | 0xF060_7000 | 0xF060_7FFF | | DSPSS to RADARSS mailbox memory space |
| | 0xF060_8200 | 0xF060_82FF | 188 B | RADARSS to DSPSS mailbox Configuration registers |
| | 0xF060_8100 | 0xF060_81FF | | DSPSS to RADARSS mailbox Configuration registers |
| PRCM and Control Module | 0xFFFF_E100 | 0xFFFF_E2FF | 756 B | TOP Level Reset, Clock management registers |
| | 0xFFFF_FF00 | 0xFFFF_FFFF | 256 B | MSS Reset, Clock management registers |
| | 0xFFFF_EA00 | 0xFFFF_EBFF | 512 KB | IO Mux module registers |
| | 0xFFFF_F800 | 0xFFFF_FBFF | 352 B | General-purpose control registers |

Table 6-1. Master Subsystem, Cortex-R4F Memory Map (continued)

| NAME | FRAME ADDRESS (HEX) | | SIZE | DESCRIPTION |
|---|---------------------|--------------|--------|--|
| | START | END | | |
| GIO | 0xFFFF7_BC00 | 0xFFFF7_BDFF | 180 B | GIO module configuration registers |
| DMA-1 | 0xFFFF_F000 | 0xFFFF_F3FF | 1 KB | DMA-1 module configuration registers |
| DMA-2 | 0xFCFF_F800 | 0xFCFF_FBFF | 1 KB | DMA-2 module configuration registers |
| DMM-1 | 0xFCFF_F700 | 0xFCFF_F7FF | 472 B | DMM-1 module configuration registers |
| DMM-2 | 0xFCFF_F600 | 0xFCFF_F6FF | 472 B | DMM-2 module configuration registers |
| VIM | 0xFFFF_FD00 | 0xFFFF_FEFF | 512 B | VIM module configuration registers |
| RTI-A/WD | 0xFFFF_FC00 | 0xFFFF_FCFF | 192 B | RTI-A module configuration registers |
| RTI-B | 0xFFFF_EE00 | 0xFFFF_EEFF | 192 B | RTI-B module configuration registers |
| Serial Interfaces and Connectivity | | | | |
| QSPI | 0xC000_0000 | 0xC07F_FFFF | 8 MB | QSPI –flash memory space |
| | 0xC080_0000 | 0xC0FF_FFFF | 116 B | QSPI module configuration registers |
| MIBSPI-A | 0xFFFF7_F400 | 0xFFFF7_F5FF | 512 B | MIBSPI-A module configuration registers |
| MIBSPI-B | 0xFFFF7_F600 | 0xFFFF7_F7FF | 512 B | MIBSPI-B module configuration registers |
| SCI-A | 0xFFFF7_E500 | 0xFFFF7_E5FF | 148 B | SCI-A module configuration registers |
| SCI-B | 0xFFFF7_E700 | 0xFFFF7_E7FF | 148 B | SCI-B module configuration registers |
| CAN | 0xFFFF7_DC00 | 0xFFFF7_DDFD | 512 B | CAN module configuration registers |
| RESERVED | 0xFFFF7_C800 | 0xFFFF7_CFFF | 768 B | Reserved |
| | 0xFFFF7_A000 | 0xFFFF7_A1FF | 452 B | Reserved |
| I2C | 0xFFFF7_D400 | 0xFFFF7_D4FF | 112 B | I2C module configuration registers |
| Interconnects | | | | |
| PCR-1 | 0xFFFF7_8000 | 0xFFFF7_87FF | 1 KiB | PCR-1 interconnect configuration port |
| PCR-2 | 0xFCFF_1000 | 0xFCFF_17FF | 1 KiB | PCR-2 interconnect configuration port |
| Safety Modules | | | | |
| CRC | 0xFE00_0000 | 0xFEFF_FFFF | 16 KiB | CRC module configuration registers |
| PBIST | 0xFFFF_E400 | 0xFFFF_E5FF | 464 B | PBIST module configuration registers |
| STC | 0xFFFF_E600 | 0xFFFF_E7FF | 284 B | STC module configuration registers |
| DCC-A | 0xFFFF_EC00 | 0xFFFF_ECFF | 44 B | DCC-A module configuration registers |
| DCC-B | 0xFFFF_F400 | 0xFFFF_F4FF | 44 B | DCC-B module configuration registers |
| ESM | 0xFFFF_F500 | 0xFFFF_F5FF | 156 B | ESM module configuration registers |
| CCMR4 | 0xFFFF_F600 | 0xFFFF_F6FF | 136 B | CCMR4 module configuration registers |
| Other Subsystems | | | | |
| DSS_TPTC0 | 0x5000_0000 | 0x5000_0317 | 792 B | TPTC0 module configuration space |
| DSS_REG | 0x5000_0400 | 0x5000_075F | 864 B | DSPSS control module registers |
| DSS_TPTC1 | 0x5000_0800 | 0x5000_0B17 | 792 B | TPTC1 module configuration space |
| DSS_REG2 | 0x5000_0C00 | 0x5000_0EA3 | 676 B | DSPSS control module registers |
| DSS_TPCC0 | 0x5001_0000 | 0x5001_3FFF | 16 KB | TPCC0 module configuration space |
| DSS_RTIA/WDT | 0x5002_0000 | 0x5002_00BF | 192 B | DSS_RTIA/WDT configuration space |
| DSS_SCI | 0x5003_0000 | 0x5003_0093 | 148 B | SCI memory space |
| DSS_STC | 0x5004_0000 | 0x5004_011B | 284 B | STC module configuration space |
| DSS_CBUFF | 0x5007_0000 | 0x5007_0233 | 564 B | Common Buffer module configuration registers |
| DSS_TPTC2 | 0x5009_0000 | 0x5009_0317 | 792 B | TPTC2 module configuration space |
| DSS_TPTC3 | 0x5009_0400 | 0x5009_0717 | 792 B | TPTC3 module configuration space |
| DSS_TPCC1 | 0x500A_0000 | 0x500A_3FFF | 16 KB | TPCC1 module configuration space |
| DSS_ESM | 0x500D_0000 | 0x500D_005B | 92 B | ESM module configuration registers |
| DSS_RTIB | 0x500F_0000 | 0x500F_00BF | 192 B | RTI-B module configuration registers |

Table 6-1. Master Subsystem, Cortex-R4F Memory Map (continued)

| NAME | FRAME ADDRESS (HEX) | | SIZE | DESCRIPTION |
|---|---------------------|-------------|---------------------|--|
| | START | END | | |
| DSS_L3RAM Shared memory | 0x5100 0000 | 0x511F FFFF | 2 MB ⁽¹⁾ | L3 shared memory space |
| DSS_ADCBUF Buffer | 0x5200 0000 | 0x5200 7FFF | 32 KB | ADC buffer memory space |
| DSS_CBUFF_FIFO | 0x5202 0000 | 0x5202 3FFF | 16 KB | Common buffer FIFO space |
| DSS_HSRAM1 | 0x5208 0000 | 0x5208 7FFF | 32 KB | Handshake memory space |
| DSS_DSP_L2_UMA P1 | 0x577E 0000 | 0x577F FFFF | 128 KB | L2 RAM space |
| DSS_DSP_L2_UMA P0 | 0x5780 0000 | 0x5781 FFFF | 128 KB | L2 RAM space |
| DSS_DSP_L1P | 0x57E0 0000 | 0x57E0 7FFF | 32 KB | L1 program memory space |
| DSS_DSP_L1D | 0x57F0 0000 | 0x57F0 7FFF | 32 KB | L1 data memory space |
| Peripheral Memories (System and Nonsystem) | | | | |
| CAN RAM | 0xFF1E_0000 | 0xFF1F_FFFF | 128 KB | CAN RAM memory space |
| RESERVED | 0xFF50_0000 | 0xFF51_FFFF | 68 KB | Reserved |
| DMA1 RAM | 0xFFF8_0000 | 0xFFF8_0FFF | 4 KB | DMA1 RAM memory space |
| DMA2 RAM | 0xFCF8 1000 | 0xFCF8_0FFF | 4 KB | DMA2 RAM memory space |
| VIM RAM | 0xFFF8_2000 | 0xFFF8_2FFF | 2 KB | VIM RAM memory space |
| MIBSPIB-TX RAM | 0xFF0C_0000 | 0xFF0C_01FF | 0.5 KB | MIBSPIB-TX RAM memory space |
| MIBSPIB-RX RAM | 0xFF0C_0200 | 0xFF0C_03FF | 0.5 KB | MIBSPIB-RX RAM memory space |
| MIBSPIA-TX RAM | 0xFF0E_0000 | 0xFF0E_01FF | 0.5 KB | MIBSPIA-TX RAM memory space |
| MIBSPIA- RX RAM | 0xFF0E_0200 | 0xFF0E_03FF | 0.5 KB | MIBSPIA- RX RAM memory space |
| Debug Modules | | | | |
| Debug subsystem | 0xFFA0_0000 | 0xFFAF_FFFF | 244 KB | Debug subsystem memory space and registers |

(1) 768 KB memory within 2 MB memory space

6.3.5 DSP Subsystem Memory Map

Table 6-2 shows the DSP C674x memory map.

Table 6-2. DSP C674x Memory Map

| Name | Frame Address (Hex) | | Size | Description |
|---------------------|---------------------|-------------|---------|----------------------------------|
| | Start | End | | |
| DSP Memories | | | | |
| DSP_L1D | 0x00F0_0000 | 0x00F0_7FFF | 32 KiB | L1 data memory space |
| DSP_L1P | 0x00E0_0000 | 0x00E0_7FFF | 32 KiB | L1 program memory space |
| DSP_L2_UMAP0 | 0x0080_0000 | 0x0081_FFFF | 128 KiB | L2 RAM space |
| DSP_L2_UMAP1 | 0x007E_0000 | 0x007F_FFFF | 128 KiB | L2 RAM space |
| EDMA | | | | |
| TPCC0 | 0x0201_0000 | 0x0201_3FFF | 16 KiB | TPCC0 module configuration space |
| TPCC1 | 0x020A_0000 | 0x020A_3FFF | 16 KiB | TPCC1 module configuration space |
| TPTC0 | 0x0200 0000 | 0x0200 03FF | 1 KiB | TPTC0 module configuration space |
| TPTC1 | 0x0200 0800 | 0x0200 0BFF | 1 KiB | TPTC1 module configuration space |
| TPTC2 | 0x0209_0000 | 0x0209_03FF | 1 KiB | TPTC2 module configuration space |

Table 6-2. DSP C674x Memory Map (continued)

| Name | Frame Address (Hex) | | Size | Description |
|-----------------------------|---------------------|-------------|---------------------|--|
| | Start | End | | |
| TPTC3 | 0x0209_0400 | 0x0209_07FF | 1 KiB | TPTC3 module configuration space |
| Control Registers | | | | |
| DSS_REG | 0x0200_0400 | 0x0200_07FF | 864 B | DSPSS control module registers |
| DSS_REG2 | 0x0200_0C00 | 0x0200_0FFF | 624 B | DSPSS control module registers |
| System Memories | | | | |
| ADC Buffer | 0x2100_0000 | 0x2100_7FFC | 32 KiB | ADC buffer memory space |
| CBUFF-FIFO | 0x2102_0000 | 0x2102_3FFC | 16 KiB | Common buffer FIFO space |
| L3-Shared memory | 0x2000_0000 | 0x201F_FFFF | 2 MB ⁽¹⁾ | L3 shared memory space |
| HS-RAM | 0x2108_0000 | 0x2108_7FFC | 32 KiB | Handshake memory space |
| System Peripherals | | | | |
| RTI-AWD | 0x0202_0000 | 0x0202_00FF | 192 B | RTI-A module configuration registers |
| RTI-B | 0x020F_0000 | 0x020F_00FF | 192 B | RTI-B module configuration registers |
| CBUFF | 0x0207_0000 | 0x0207_03FF | 564 B | Common Buffer module Configuration registers |
| Mail Box MSS<->RADARSS | 0x5060_1000 | 0x5060_17FF | 2 KiB | RADARSS to MSS mailbox memory space |
| | 0x5060_2000 | 0x5060_27FF | | MSS to RADARSS mailbox memory space |
| | 0x0460_8000 | 0x0460_80FF | 188 B | MSS to RADARSS mailbox Configuration registers |
| | 0x0460_8060 | 0x0460_86FF | | RADARSS to MSS mailbox Configuration registers |
| Mail Box MSS<->DSPSS | 0x5060_4000 | 0x5060_47FF | 2 KiB | DSPSS to MSS mailbox memory space |
| | 0x5060_5000 | 0x5060_57FF | | MSS to DSPSS mailbox memory space |
| | 0x0460_8400 | 0x0460_84FF | 188 B | MSS to DSPSS mailbox Configuration registers |
| | 0x0460_8300 | 0x0460_83FF | | DSPSS to MSS mailbox Configuration registers |
| Mail Box RADARSS<->DSPSS | 0x5060_6000 | 0x5060_67FF | 2 KiB | RADARSS to DSPSS mailbox memory space |
| | 0x5060_7000 | 0x5060_77FF | | DSPSS to RADARSS mailbox memory space |
| | 0x0460_8200 | 0x0460_82FF | 188 B | RADARSS to DSPSS mailbox Configuration registers |
| | 0x0460_8100 | 0x0460_81FF | | DSPSS to RADARSS mailbox Configuration registers |
| Safety Modules | | | | |
| ESM | 0x020D_0000 | | 92 B | ESM module Configuration registers |
| CRC | 0x2200_0000 | 0x2200_03FF | 1 KiB | CRC module Configuration registers |

(1) 768 KB memory within 2 MB memory space

Table 6-2. DSP C674x Memory Map (continued)

| Name | Frame Address (Hex) | | Size | Description |
|------------------------------|---------------------|-------------|-------|------------------------------------|
| | Start | End | | |
| STC | 0x0204_0000 | 0x0204_01FF | 284 B | STC module Configuration registers |
| Nonsystem Peripherals | | | | |
| SCI | 0x0203_0000 | 0x0203_00FF | 148 B | SCI module Configuration registers |

6.4 Other Subsystems

6.4.1 ADC Channels (Service) for User Application

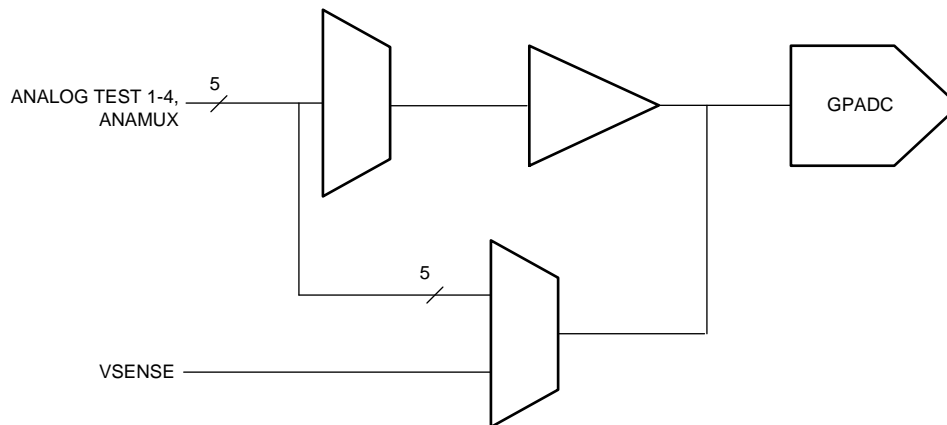
The IWR1642 device includes provision for an ADC service for user application, where the

GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on the Master R4.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).

**Figure 6-5. ADC Path****Table 6-3. GP-ADC Parameter**

over Tjunction temperature range (unless otherwise noted)

| PARAMETER | TYP | UNIT |
|------------------------------------|---------|------|
| ADC supply | 1.8 | V |
| ADC unbuffered input voltage range | 0 – 1.8 | V |

Table 6-3. GP-ADC Parameter (continued)

over Tjunction temperature range (unless otherwise noted)

| PARAMETER | TYP | UNIT |
|---|-----------|------|
| ADC buffered input voltage range ⁽¹⁾ | 0.4 – 1.3 | V |
| ADC resolution | 10 | bits |
| ADC offset error | ±5 | LSB |
| ADC gain error | ±5 | LSB |
| ADC DNL | -1/+2.5 | LSB |
| ADC INL | ±2.5 | LSB |
| ADC sample rate ⁽²⁾ | 625 | Ksps |
| ADC sampling time ⁽²⁾ | 400 | ns |
| ADC internal cap | 10 | pF |
| ADC buffer input capacitance | 2 | pF |
| ADC input leakage current | 3 | uA |

(1) Outside of given range, the buffer output will become nonlinear.

(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

7 Monitoring and Diagnostics

7.1 Monitoring and Diagnostic Mechanisms

Below is the list given for the main monitoring and diagnostic mechanisms available in the IWR1642.

Table 7-1. Monitoring and Diagnostic Mechanisms for IWR1642

| S No | Feature | Description |
|------|----------------------|--|
| 1 | Temperature Sensors | IWR1642 architecture supports various temperature sensors all across the device (next to power hungry modules such as PAs, DSP etc) which is monitored during the inter-frame period. ⁽¹⁾ |
| 2 | RX saturation detect | Provision to detect ADC saturation due to excessive incoming signal level and/or interference. |

(1) Monitoring is done by the TI's code running on BIST R4F. There are two modes in which it could be configured to report the temperature sensed via API by customer application.

- Report the temperature sensed after every N frames
- Report the condition once the temperature crosses programmed threshold.

It is completely up to customer SW to decide on the appropriate action based on the message from BIST R4F via Mailbox.

7.1.1 Error Signaling Module

When a diagnostic detects a fault, the error must be indicated. IWR1642 architecture provides aggregation of fault indication from internal diagnostic mechanisms using a peripheral logic known as the error signaling module (ESM). The ESM provides mechanisms to classify faults by severity and allows programmable error response. Below is the high level block diagram for ESM module.

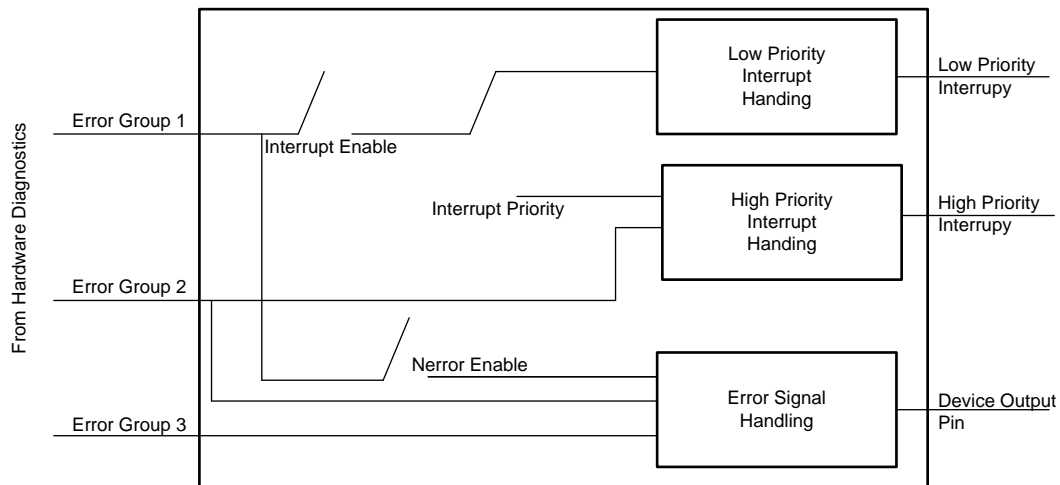


Figure 7-1. ESM Module Diagram

8 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Key device features driving the following applications are:

- Integration of Radar Front End and Programmable MCU
- Flexible boot modes: Autonomous Application boot using a serial flash or external boot over SPI.

The IWR1642 can be a radar sensor, or can be combined with an MSP432, or for LVDS processing with a LVDS to DSP subsystem for more advanced applications. Some applications are:

- Liquid and solid level sensing for process sensors or industrial automation
- Industrial proximity sensing, non contact sensing for security, traffic monitoring, and industrial transportation
- Sensor fusion of camera and radar instruments for security, factory automation, robotics
- Sensor fusion with multiple camera and radar instruments for object identification, manipulation, and flight avoidance for security, robotics, material handling or drone devices
- People counting
- Gesturing
- Motion detection

8.2 Reference Schematic

The reference schematic and power supply information can be found in the [IWR1642 EVM Documentation](#).

8.3 Layout

8.3.1 *Layout Guidelines*

General layout guidelines can be found in the [IWR1642 EVM Documentation](#) and [IWR1642 Checklist for Schematic Review, Layout Review, Bringup/Wakeup](#).

8.3.2 *Layout Example*

The IWR1642 EVM, RF layout can be found in the [IWR1642BOOST Layout and Design Files](#), and [IWR1642BOOST Schematics, Assembly Files, and BOM](#).

8.3.3 *Stackup Details*

Layout Stackup details can be found in the [IWR1642BOOST Layout and Design Files](#).

There are specific RF guidelines for the RF Tx and Rx. There are additional layout guidelines for other sections in the [IWR1642 Checklist for Schematic Review, Layout Review, Bringup/Wakeup](#).

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *IWR1642*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161), the temperature range (for example, blank is the default commercial temperature range). [Figure 9-1](#) provides a legend for reading the complete device name for any *IWR1642* device.

For orderable part numbers of *IWR1642* devices in the ABL0161 package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [IWR1642 Device Errata](#).

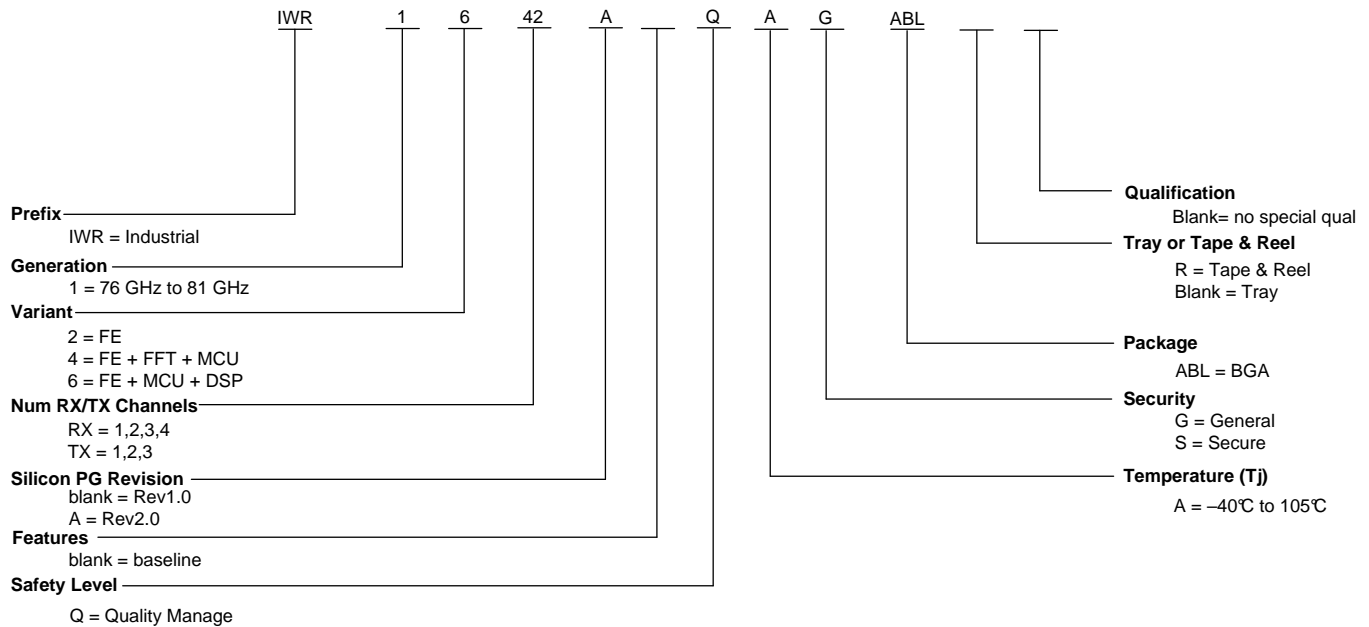


Figure 9-1. Device Nomenclature

9.2 Tools and Software

Models

IWR1642 BSDL Model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

IWR1642 IBIS Model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

IWR1642 Checklist for Schematic Review, Layout Review, Bringup/Wakeup A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

9.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (IWR1642). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

IWR1642 Device Errata Describes known advisories, limitations, and cautions on silicon and provides workarounds.

9.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

9.5 Trademarks

E2E is a trademark of Texas Instruments.

ARM, Cortex are registered trademarks of ARM Limited.

All other trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

9.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

CAUTION

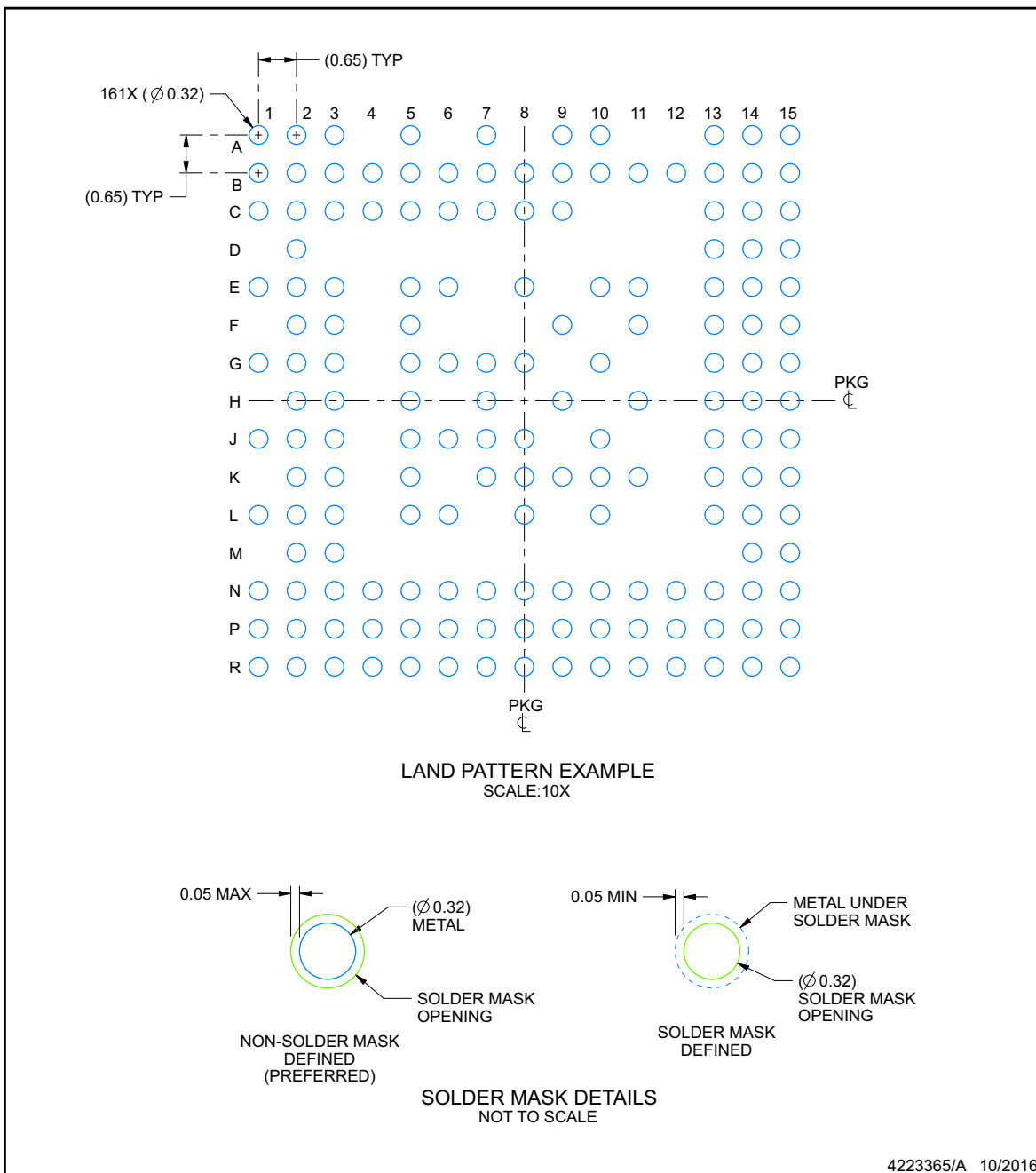
The following package information is subject to change without notice.

EXAMPLE BOARD LAYOUT

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

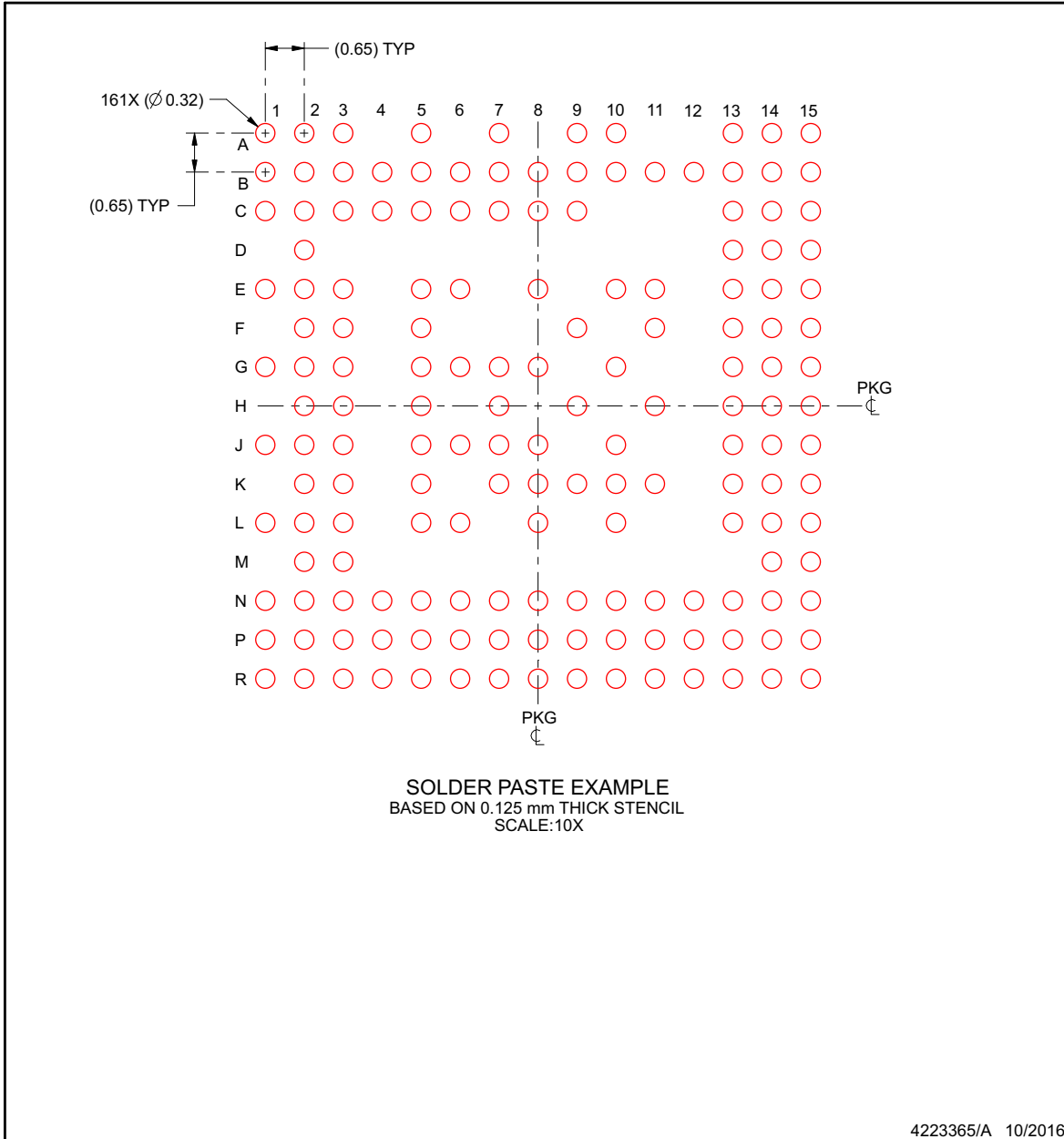
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ABL0161B

FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| IWR1642AQAGABL | ACTIVE | FC/CSP | ABL | 161 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | IWR1642 QG | Samples |
| IWR1642AQAGABLR | ACTIVE | FC/CSP | ABL | 161 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | IWR1642 QG | Samples |
| IWR1642AQASABL | ACTIVE | FC/CSP | ABL | 161 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | IWR1642 QS | Samples |
| IWR1642AQASABLR | ACTIVE | FC/CSP | ABL | 161 | | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 105 | IWR1642 QS | Samples |
| XI1642QGABL | ACTIVE | FC/CSP | ABL | 161 | 1 | TBD | Call TI | Call TI | -40 to 105 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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