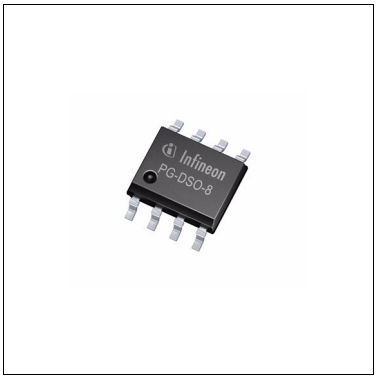
Smart high-side NMOS-power switch

ITS4060S-SJ-N

RoHS



Features

- CMOS compatible input
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized Electromagnetic Compatibility (EMC)
- Overload protection
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of Vbb protection
- Electrostatic Discharge Protection (ESD)
- Green Product (RoHS compliant)

Applications

- All types of resistive, inductive and capacitive loads
- Power switch for 12V and 24V DC applications with CMOS compatible control interface
- Driver for electromagnetic relays
- Power management for high-side-switching with low current consumption in OFF-mode

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC.

Description

The ITS4060S-SJ-N is a protected single channel smart high-side NMOS power switch in a PG-DSO-8 package with charge pump and CMOS compatible input. The device is monolithically integrated in Smart technology.

Table 1 Product summary

Parameter	Symbol	Values
Overvoltage protection	V_{SAZmin}	41 V
Operating voltage range	V_S	$5 < V_S < 34V$
On-state resistance	R_{DSON}	typ. 50 mΩ
Nominal load current	$I_{L(nom)}$	2.6 A
Operating temperature range	T_j	-40°C to 125°C
Stand-by current	I_{SSTB}	15 µA

Type	Package	Marking
ITS4060S-SJ-N	PG-DSO-8	I060SN

Table of Contents

1 Block diagram and terms

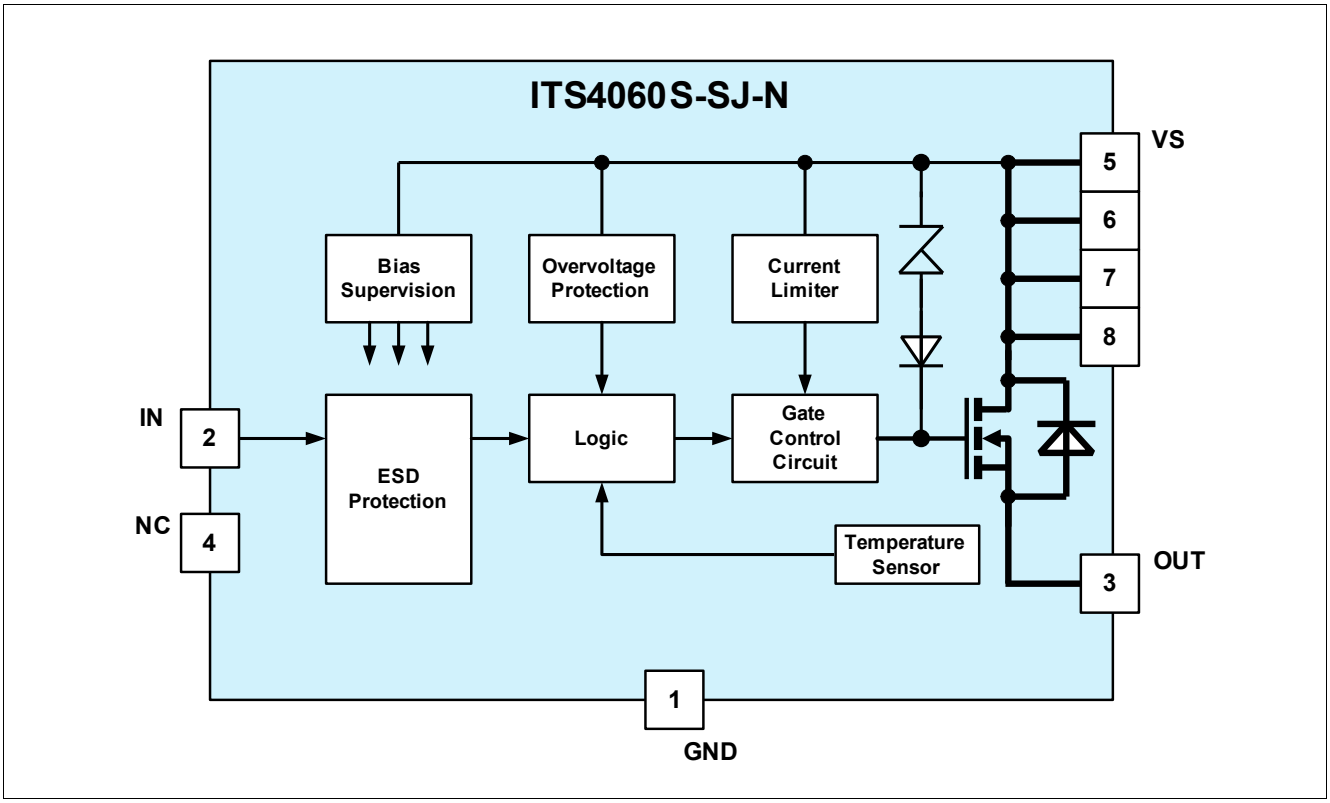


Figure 1 Block diagram

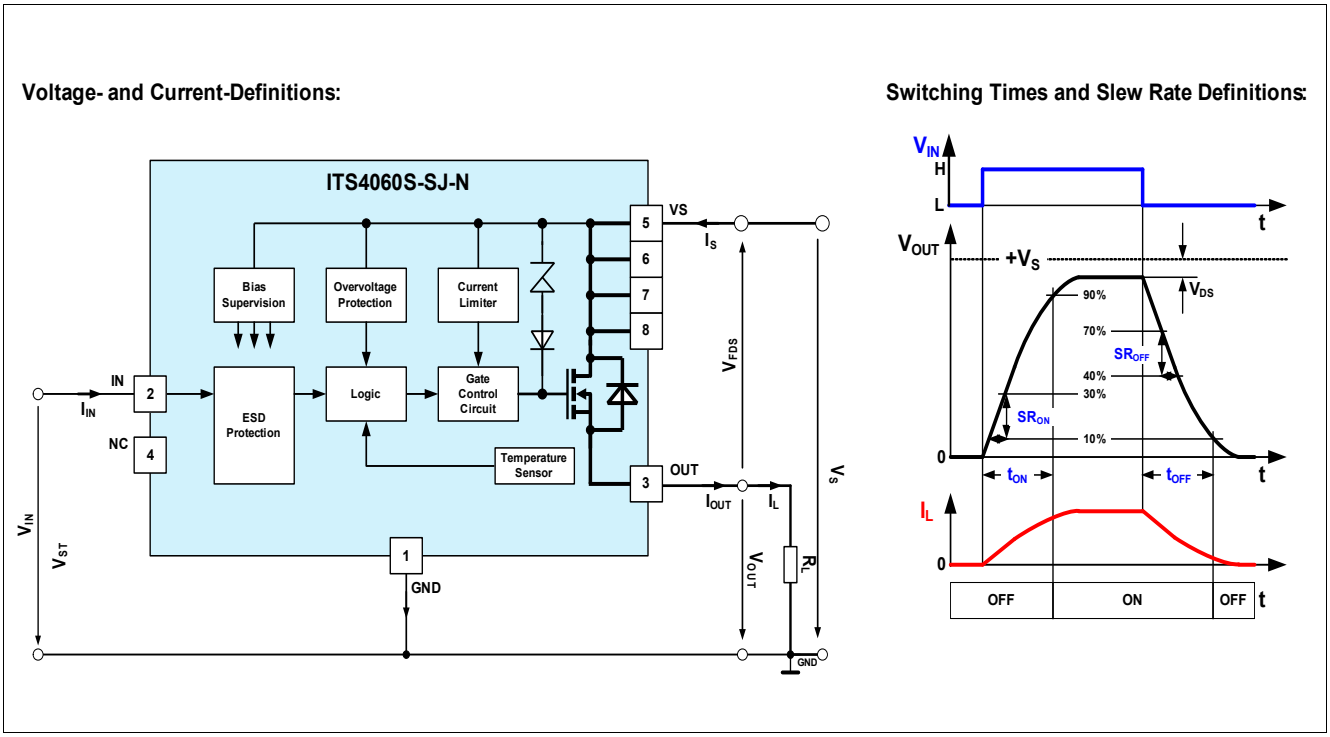


Figure 2 Terms - parameter definition

2 Pin configuration

2.1 Pin assignment

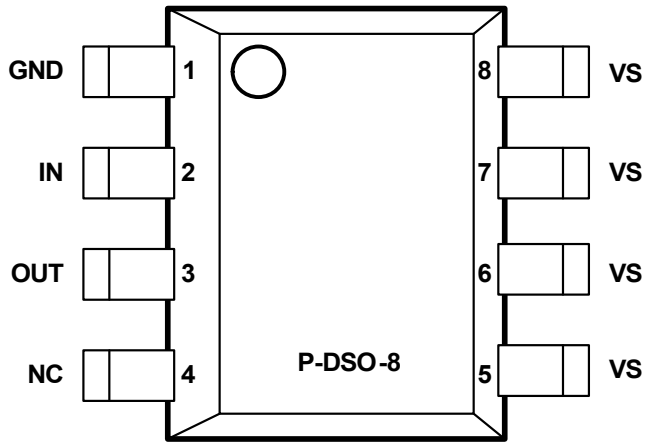


Figure 3 Pin configuration top view, PG-DSO-8

2.2 Pin definitions and functions

Pin	Symbol	Function
1	GND	**Logic ground**
2	IN	**Input, controls the power switch; the powerswitch is ON when high**
3	OUT	Output to the load
4	NC	**Not connected**
5, 6, 7, 8	VS	**Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance)**

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings [1] at T_j = 25°C unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage VS							
Voltage	V_S	–	–	40	V	–	4.1.1
Voltage for short circuit protection	V_{SSC}	–	–	36	V	-40°C < T_j < 150°C	4.1.2
Output stage OUT							
Output current; (short circuit current see electrical characteristics)	I_{OUT}	–	–	self limited	A	–	4.1.3
Input IN							
Voltage	V_{IN}	-10	–	16	V	–	4.1.4
Current	I_{IN}	-5	–	5	mA	–	4.1.5
Temperatures							
Junction temperature	T_j	-40	–	125	°C	–	4.1.6
Storage temperature	T_{stg}	-55	–	125	°C	–	4.1.7
Power dissipation							
Ta = 25 °C[2]	P_{tot}	–	–	1.5	W	–	4.1.8
Inductive load switch-off energy dissipation							
Tj = 125 °C; V_S=13.5V; IL= 1.5A[3]	E_{AS}	–	–	900	mJ	single pulse	4.1.9
ESD Susceptibility							
ESD susceptibility (input pin IN)	V_{ESD}	-1	–	1	kV	HBM[4]	4.1.10
ESD susceptibility (output pin OUT)	V_{ESD}	-6	–	6	kV	HBM[4]	4.1.12
ESD susceptibility (all other pins)	V_{ESD}	-4	–	4	kV	HBM[4]	4.1.11

1) Not subject to production test, specified by design
2) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70mm thick) copper area for Vbb connection. PCB is vertical without blown air
3) Not subject to production test, specified by design
4) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_S	5	–	34	V	V_S increasing	4.2.1

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance - unction to pin5	$R_{thj\text{-}pin5}$	–	26.7	–	K/W	–	4.3.1
Thermal resistance - junction to ambient - 1s0p, minimal footprint	R_{thJA_1s0p}	–	140.1	–	K/W	2)	4.3.2
Thermal resistance - junction to ambient - 1s0p, 300mm^2	$R_{thJA\_1s0p\_300mm}$	–	85.8	–	K/W	3)	4.3.3
Thermal resistance - junction to ambient - 1s0p, 600mm^2	$R_{thJA\_1s0p\_600mm}$	–	74.7	–	K/W	4)	4.3.4
Thermal resistance - junction to ambient - 2s2p	R_{thJA_2s2p}	–	78.2	–	K/W	5)	4.3.5
Thermal resistance - junction to ambient with thermal vias - 2s2p	R_{thJA_2s2p}	–	76.6	–	K/W	6)	4.3.6

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm^2; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

4) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm^2; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

6)Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu. The diameter of the two vias are equal 0.3mm and have a plating of 25um with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.

4 Electrical characteristics

Table 5 **V_S=13.5V; Tj = -40°C to 125°C; all voltages with respect to ground. Currents flowing into the device unless otherwise specified in chapter "Block diagram and terms". Typical values at V_s = 13.5V, T_j = 25°C**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Powerstage							
NMOS ON resistance	R_{DSON}	–	50	60	mΩ	I_{OUT}= 2A;T_j = 25°C; 9V < V_S < 34V; V_{IN}= 5V	5.0.1
NMOS ON resistance	R_{DSON}	–	95	120	mΩ	I_{OUT}= 2A;T_j = 125°C; 9V < V_S < 34V; V_{IN}= 5V	5.0.2
Nominal load current; device on PCB [1]	I_{LNOM}	2.6	3.1	–	A	T_{pin5} = 85°C	5.0.3
Timings of power stages[2]							
Turn ON time (to 90% of V_{out}); L to H transition of V_{IN}	t_{ON}	–	90	180	µs	V_S=13.5V; R_L = 47Ω	5.0.4
Turn OFF time (to 10% of V_{out}); H to L transition of V_{IN}	t_{OFF}	–	110	230	µs	V_S=13.5V; R_L = 47Ω	5.0.5
ON-slew rate; $\Delta V_{OUT}/\Delta t$ (10 to 30% of V_{out}); L to H transition of V_{IN}	SR_{ON}	–	0.7	1.5	V / µs	V_S=13.5V; R_L = 47Ω	5.0.6
OFF-slew rate; $\Delta V_{OUT}/\Delta t$ (70 to 40% of V_{out}); H to L transition of V_{IN}	SR_{OFF}	–	0.7	1.5	V / µs	V_S=13.5V; R_L = 47Ω	5.0.7
Under voltage lockout (charge pump start-stop-restart)							
Supply undervoltage; charge pump stop voltage	V_{SUV}	–	–	5.5	V	V_S decreasing	5.0.8
Supply startup voltage; Charge pump restart voltage	V_{SSU}	–	4.0	5.5	V	V_S increasing	5.0.9
Current consumption							
Operating current	I_{GND}	–	0.8	1.5	mA	V_{IN}= 5V	5.0.10
Standby current	I_{SSTB}	–	–	10	µA	V_{IN}= 0V; V_{OUT}= 0V -40°C < T_j < 85°C	5.0.11
Standby current	I_{SSTB}	–	–	15	µA	V_{IN}= 0V; V_{OUT}= 0V T_j = 125°C	5.0.12
Output leakage current	I_{OUTLK}	–	–	5	µA	V_{IN}= 0V; V_{OUT}= 0V	5.0.13
Protection functions [3]							
Initial peak short circuit current limit	I_{LSCP}	–	–	28	A	T_j = -40°C; V_S = 20V V_{IN} = 5.0V; t_m =150µs	5.0.14

Electrical characteristics

Table 5 **V_S=13.5V; Tj = -40°C to 125°C; all voltages with respect to ground. Currents flowing into the device unless otherwise specified in chapter "Block diagram and terms". Typical values at V_s = 13.5V, T_j = 25°C**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Initial peak short circuit current limit	I_{LSCP}	–	17	–	A	T_j = 25°C; V_S = 20V V_{IN} = 5.0V; t_m =150µs	5.0.15
Initial peak short circuit current limit	I_{LSCP}	9	–	–	A	T_j =125°C; V_S = 20V V_{IN} = 5.0V; t_m =150µs	5.0.16
Repetitive short circuit current limit $T_j = T_{jTrip}$; see timing diagrams	I_{LSCR}	–	12	–	A	V_{IN} = 5.0V	5.0.17
Output clamp at $V_{OUT} = V_S - V_{DSCL}$ (inductive load switch off)	V_{DSCL}	41	47	–	V	I_S = 4mA	5.0.18
Overvoltage protection $V_{OUT} = V_S - V_{ONCL}$	V_{SAZ}	41	–	–	V	I_S = 4mA	5.0.19
Thermal overload trip temperature	T_{jTrip}	150	–	–	°C	–	5.0.20
Thermal hysteresis	T_{HYS}	–	10	–	K	–	5.0.21
Reverse battery[4]							
Continuous reverse battery voltage	V_{SREV}	- 32	–	–	V	–	5.0.22
Forward voltage of the drain-source reverse diode	V_{FDS}	–	600	–	mV	I_{FDS} = 200mA; V_{IN}= 0V; T_j = 125°C	5.0.23
Input interface; pin IN							
Input turn-ON voltage (logic input high-level)	V_{INON}	2.2	–	–	V	–	5.0.24
Input turn-OFF voltage (logic input low-level)	V_{INOFF}	–	–	0.8	V	–	5.0.25
Input threshold hysteresis	V_{INHYS}	–	0.3	–	V	–	5.0.26
Off state input current	I_{INOFF}	1	–	30	µA	V_{IN} = 0.7V	5.0.27
On state input current	I_{INON}	1	–	30	µA	V_{IN} = 5.0V	5.0.28
Input resistance	R_{IN}	1.5	3.5	5.0	kΩ	–	5.0.29

1) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm² (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position without blown air.

2) Timing values only with high slewrate input signal; otherwise slower.

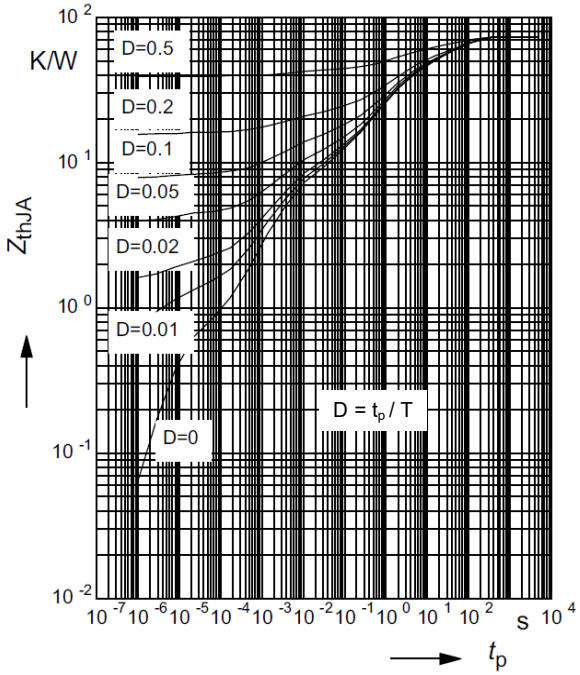
3) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4) Requires a 150 Ω resistor in GND connection. The reverse load current trough the intrinsic drain-source diode of the power-MOS has to be limited by the connected load. Power dissipation is higher compared to normal operation due to the voltage drop across the drain-source diode. The temperature protection is not functional during reverse current operation! Input current has to be limited (see max ratings).

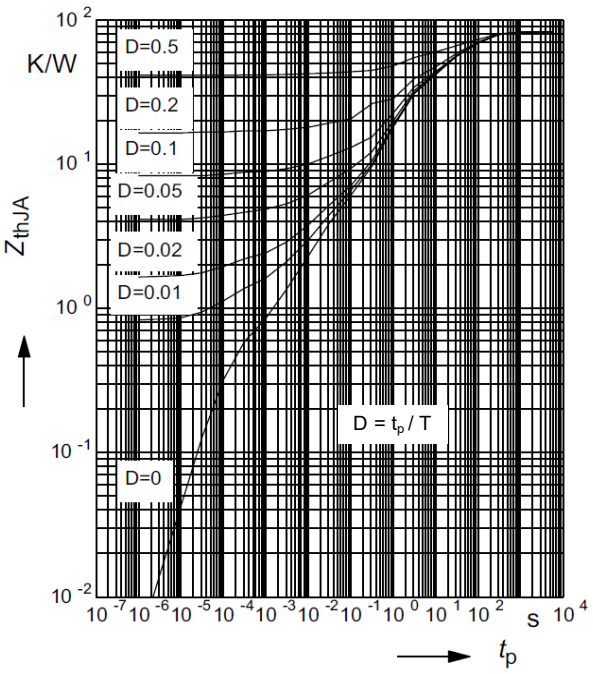
5 Typical performance graphs

Typical characteristics

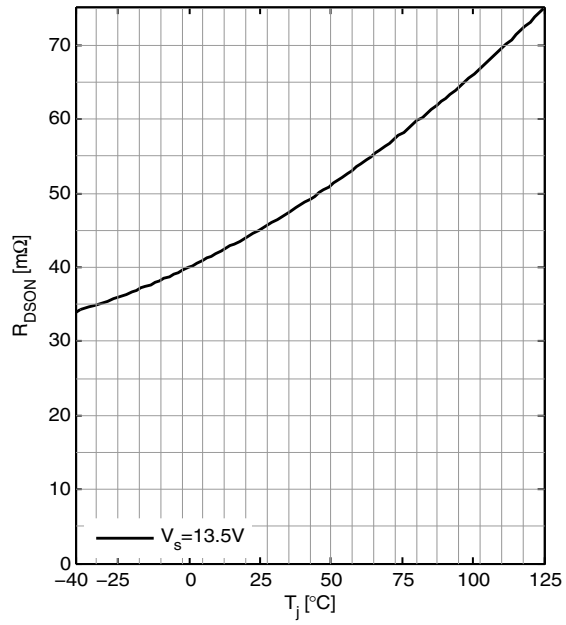
Transient thermal impedance Z_{thJA} versus pulse time t_p @ 6cm² heatsink area



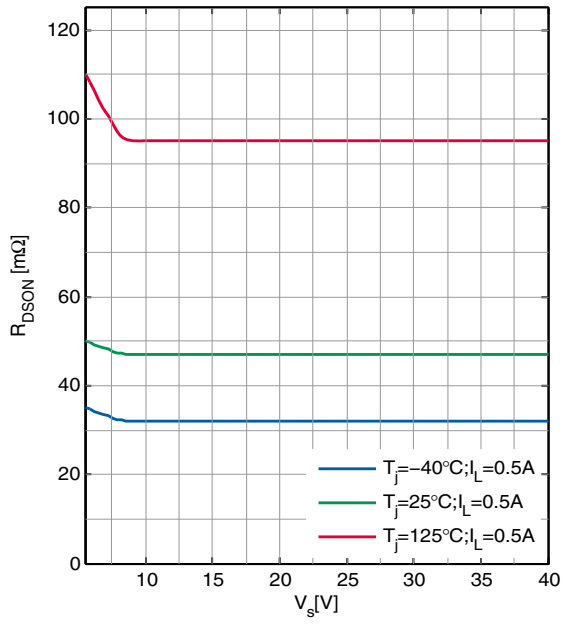
Transient thermal impedance Z_{thJA} versus pulse time t_p @ min. footprint



On-resistance R_{DSON} versus junction temperature T_j



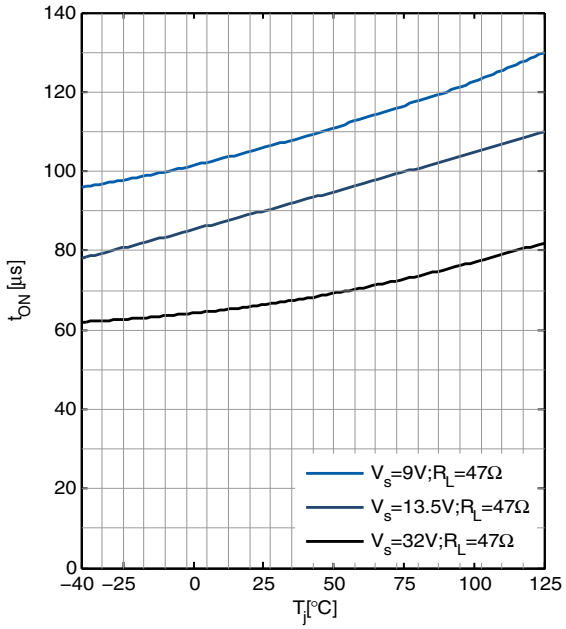
On-resistance R_{DSON} versus supply voltage V_S



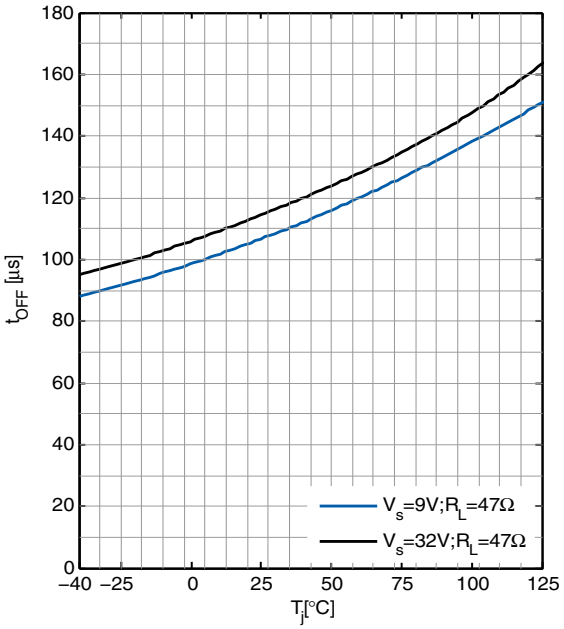
Typical performance graphs

Typical characteristics

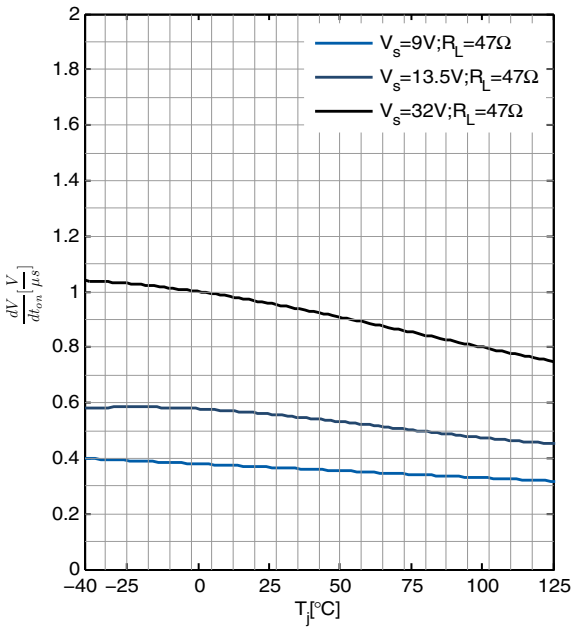
Switch ON time t_{ON} versus junction temperature T_j



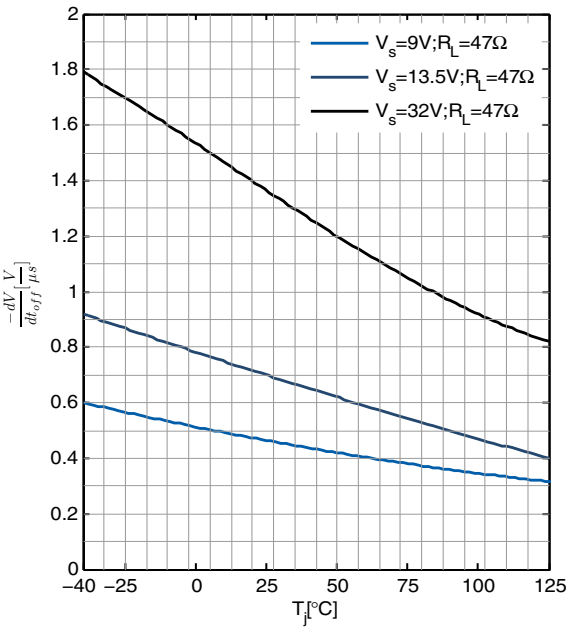
Switch OFF time t_{OFF} versus junction temperature T_j



ON slewrate SR_{ON} versus junction temperature T_j



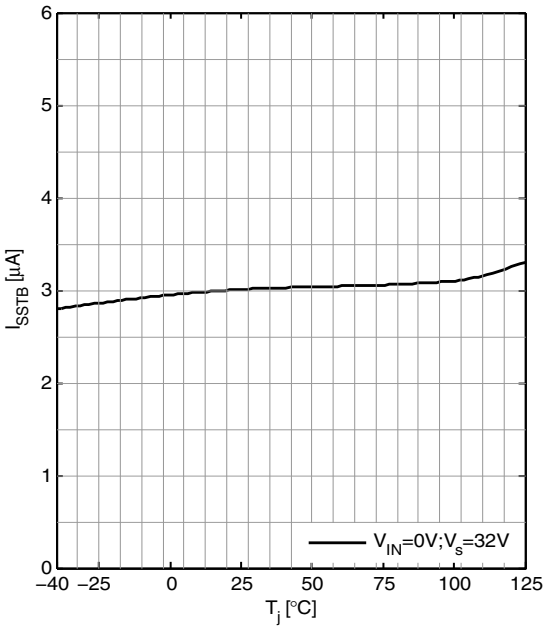
OFF slewrate SR_{OFF} versus junction temperature T_j



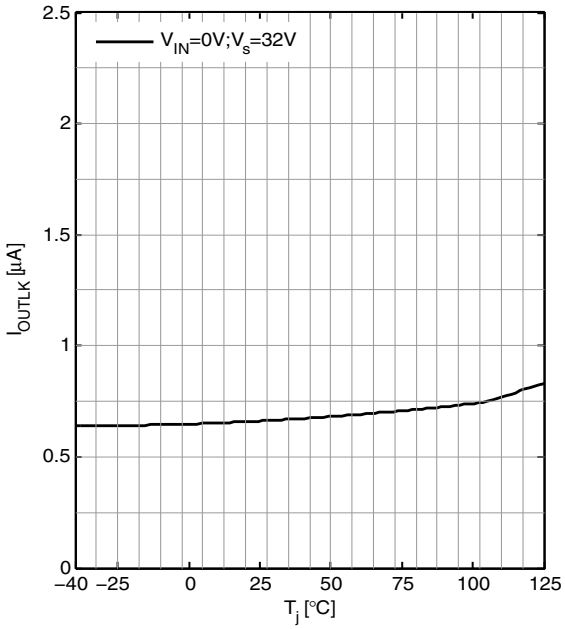
Typical performance graphs

Typical characteristics

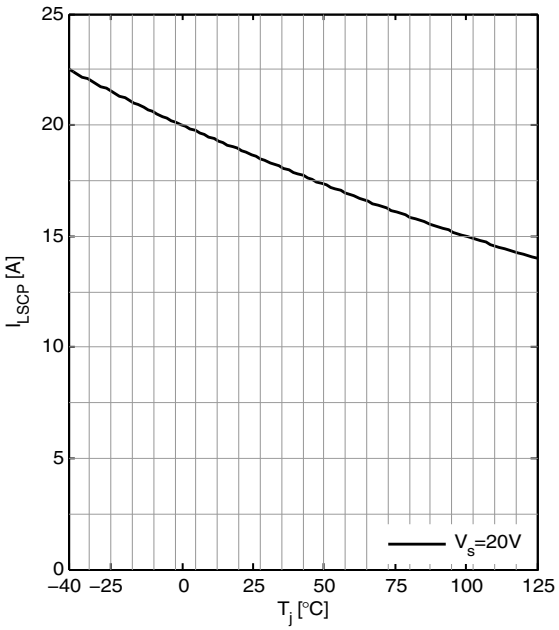
Standby current I_{SSTB} versus junction temperature T_j



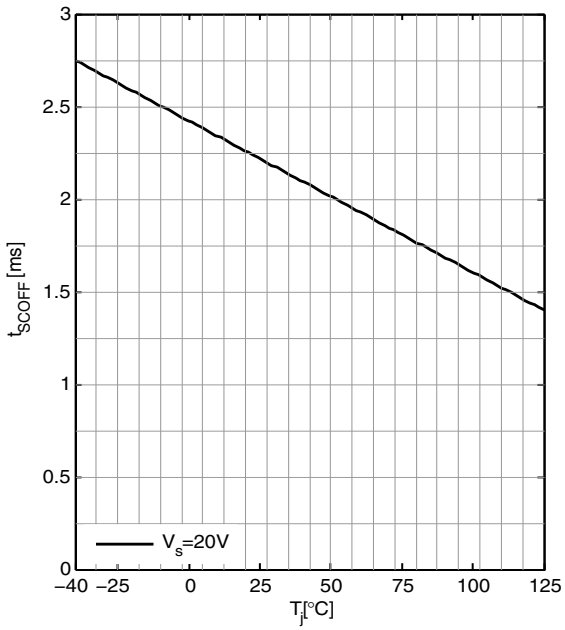
Output leakage current I_{OUTLK} versus junction temperature T_j



Initial peak short circuit current limit I_{LSCP} versus junction temperature T_j



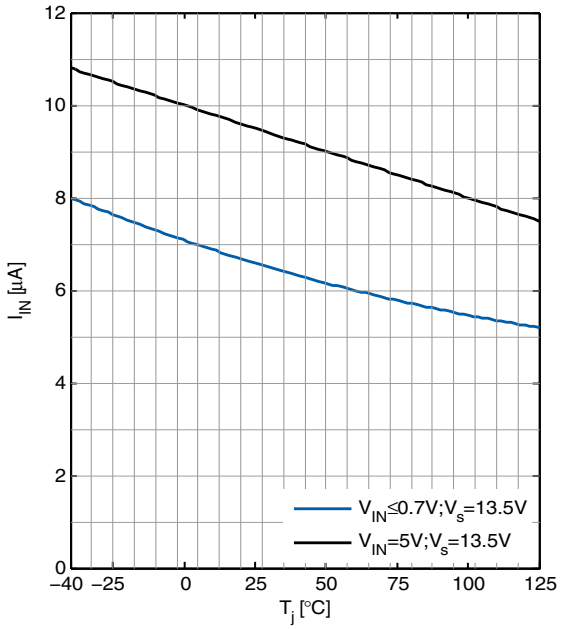
Initial short circuit shutdown time t_{SCOFF} versus junction temperature T_j



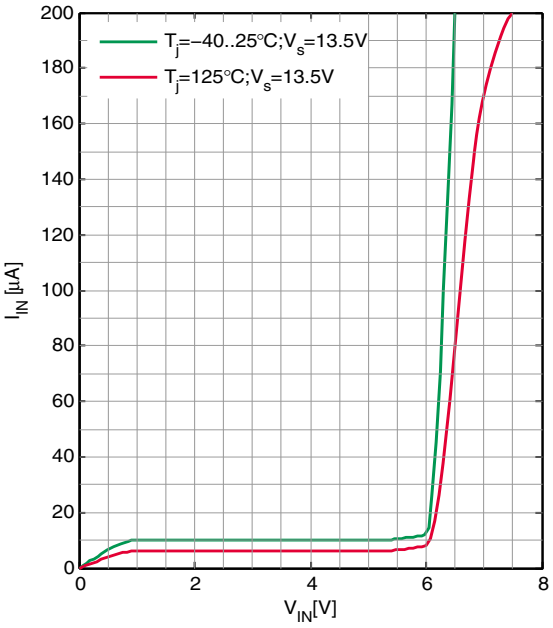
Typical performance graphs

Typical characteristics

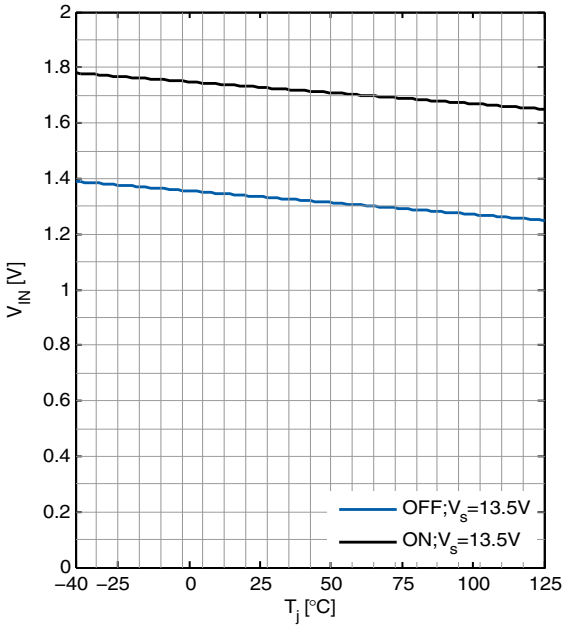
Input current consumption I_{IN} versus junction temperature T_j



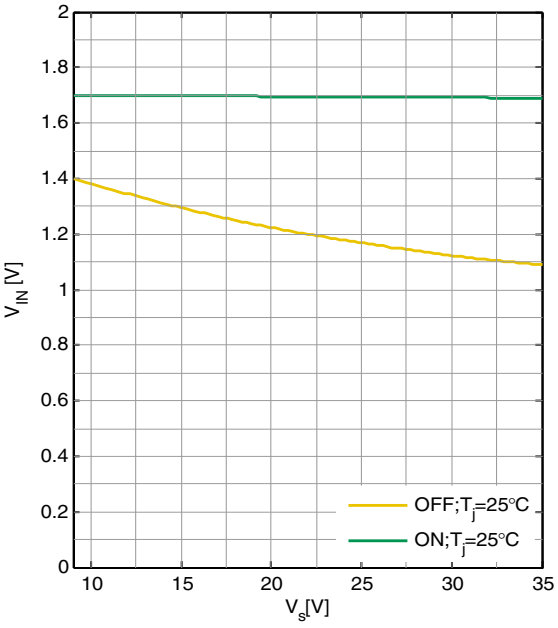
Input current consumption I_{IN} versus input voltage V_{IN}



Input threshold voltage $V_{INH,L}$ versus junction temperature T_j



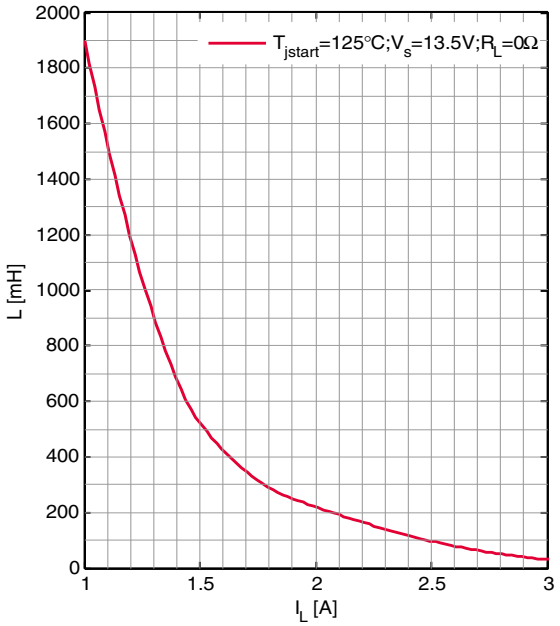
Input threshold voltage $V_{INH,L}$ versus supply voltage V_S



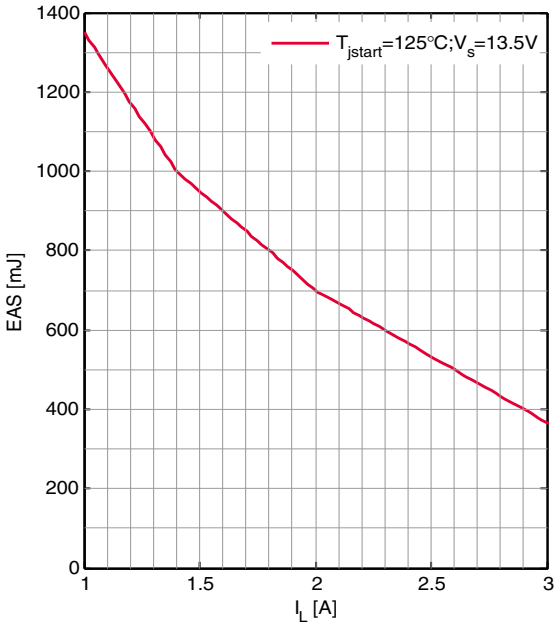
Typical performance graphs

Typical characteristics

Max. allowable load inductance *L* versus load current I_L



Max. allowable inductive single pulse switch-off energy E_{AS} versus load current I_L



6 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

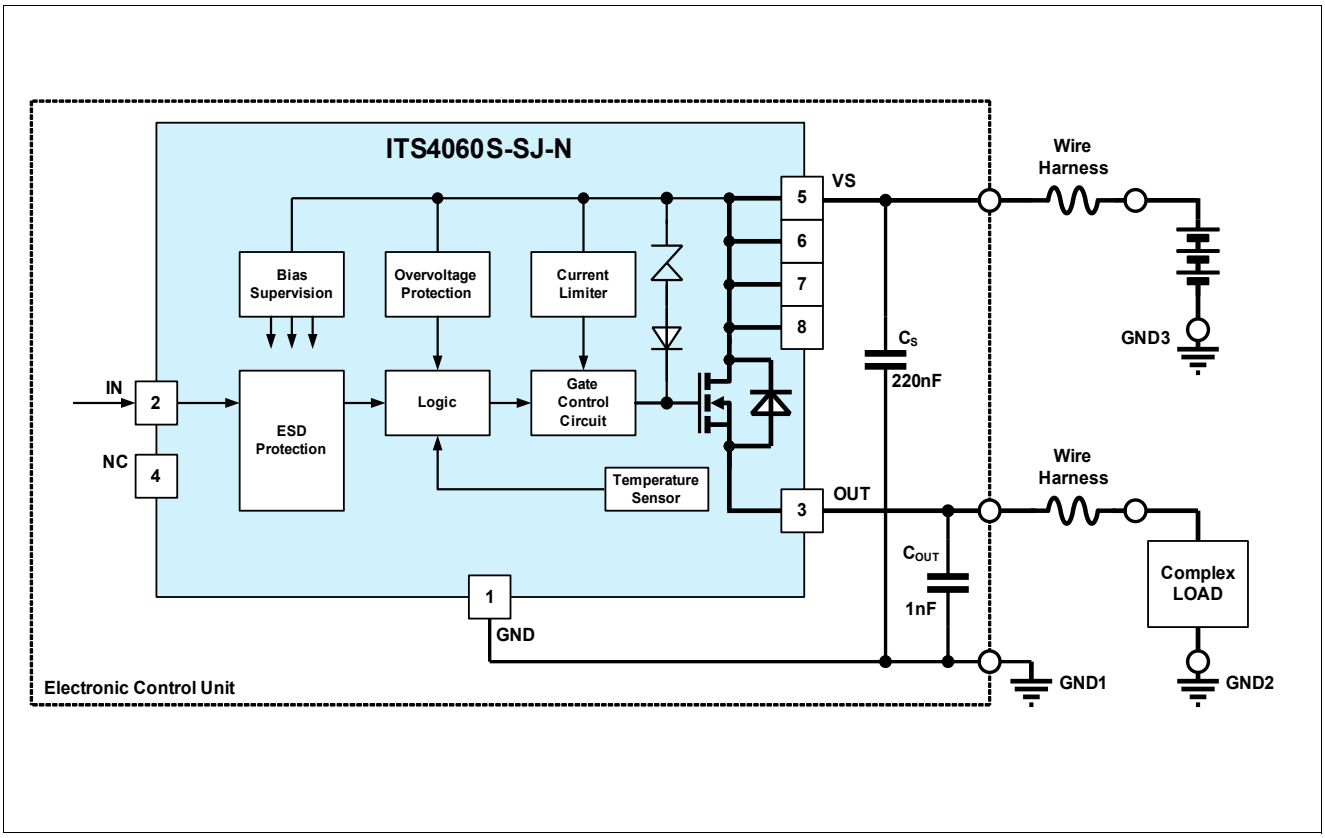


Figure 4 Application diagram

The ITS4060S-SJ-N can be connected directly to a supply network. It is recommended to place a ceramic capacitor (e.g. C_S = 220nF) between supply and GND of the ECU to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS4060S-SJ-N can be switched on and off with standard logic ground related logic signal at pin IN.

In standby mode (IN=L) the ITS4060S-SJ-N is deactivated with very low current consumption.

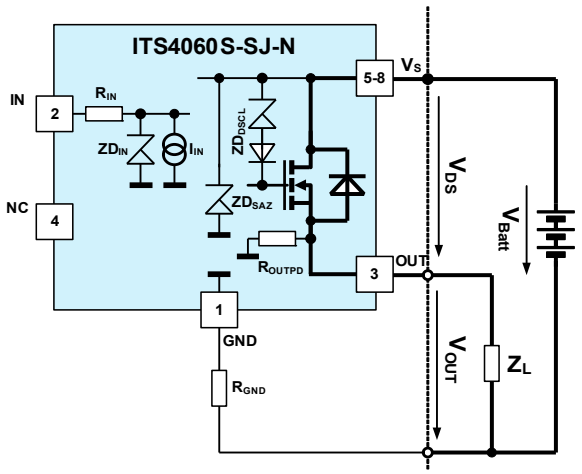
The output voltage slope is controlled during on and off transition to minimize emissions. Only a small ceramic capacitor COUT=1nF is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behavior of the ITS4060S-SJ-N is shown. For further details please refer to application notes on the Infineon homepage.

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

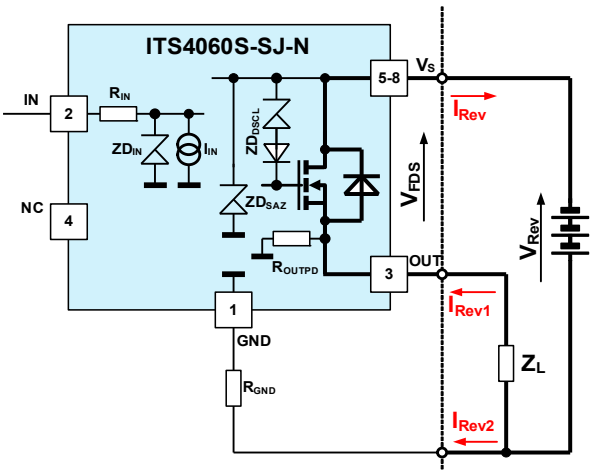
6.1 Special feature description

Supply over voltage:



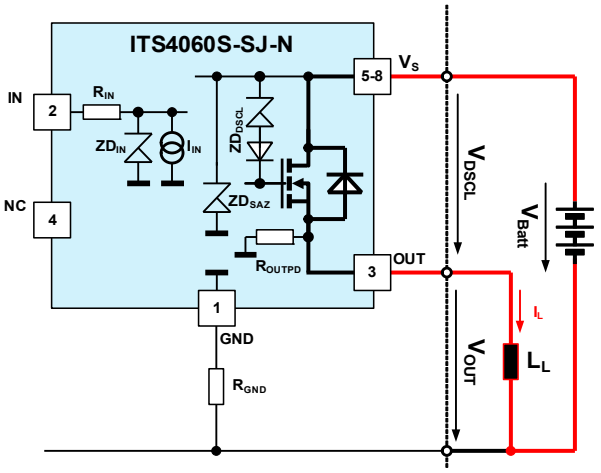
If over-voltage is applied to the V_S-Pin:
Voltage is limited to V_{ZDSAZ}; current can be calculated:
$I_{ZDSAZ} = (V_S - V_{ZDSAZ}) / R_{GND}$
A typical value for RGND is 150Ω.
In case of ESD pulse on the input pin there is in both polarities a peak current $I_{INpeak} \sim V_{ESD} / R_{IN}$

Supply reverse voltage:



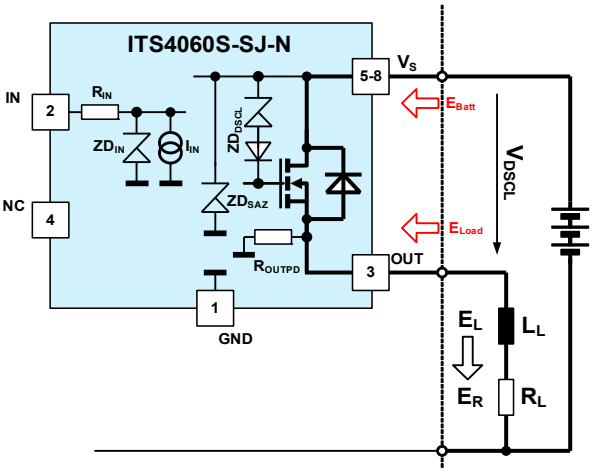
If reverse voltage is applied to the device:
1.) Current via load resistance RL:
$I_{Rev1} = (V_{Rev} - V_{FDS}) / R_L$
2.) Current via Input pin IN and dignostic pin ST:
$I_{Rev2} = I_{ST} + I_{IN} \sim (V_{Rev} - V_{CC}) / R_{IN} + (V_{Rev} - V_{CC}) / R_{ST1,2}$
Current I_{ST} must be limited with the extrernal series resistor R_{STS}. Both currents will sum up to:
$I_{Rev} = I_{Rev1} + I_{Rev2}$

Drain-Source power stage clamper V_{DSCL}:



When an inductive load is switched off a current path must be established until the current is sloped down to zero (all energy removed from the inductive load). For that purpose the series combination Z_{DSCL} is connected between Gate and Drain of the power DMOS acting as an active clamp.
When the device is switched off, the voltage at OUT turns negative until V_{DSCL} is reached.
The voltage on the inductive load is the difference between V_{DSCL} and V_S.

Energy calculation:



Energy stored in the load inductance is given by:
$E_L = I_L^2 * L/2$
While demagnetizing the load inductance the energy dissipated by the Power-DMOS is:
$E_{AS} = E_S + E_L - E_R$

With an approximate solution for R_L =0Ω:
$E_{AS} = ½ * L * I_L^2 * \{(1 - V_S / (V_S - V_{DSCL})\}$

Figure 5 Special feature description

6.2 Typical application waveforms

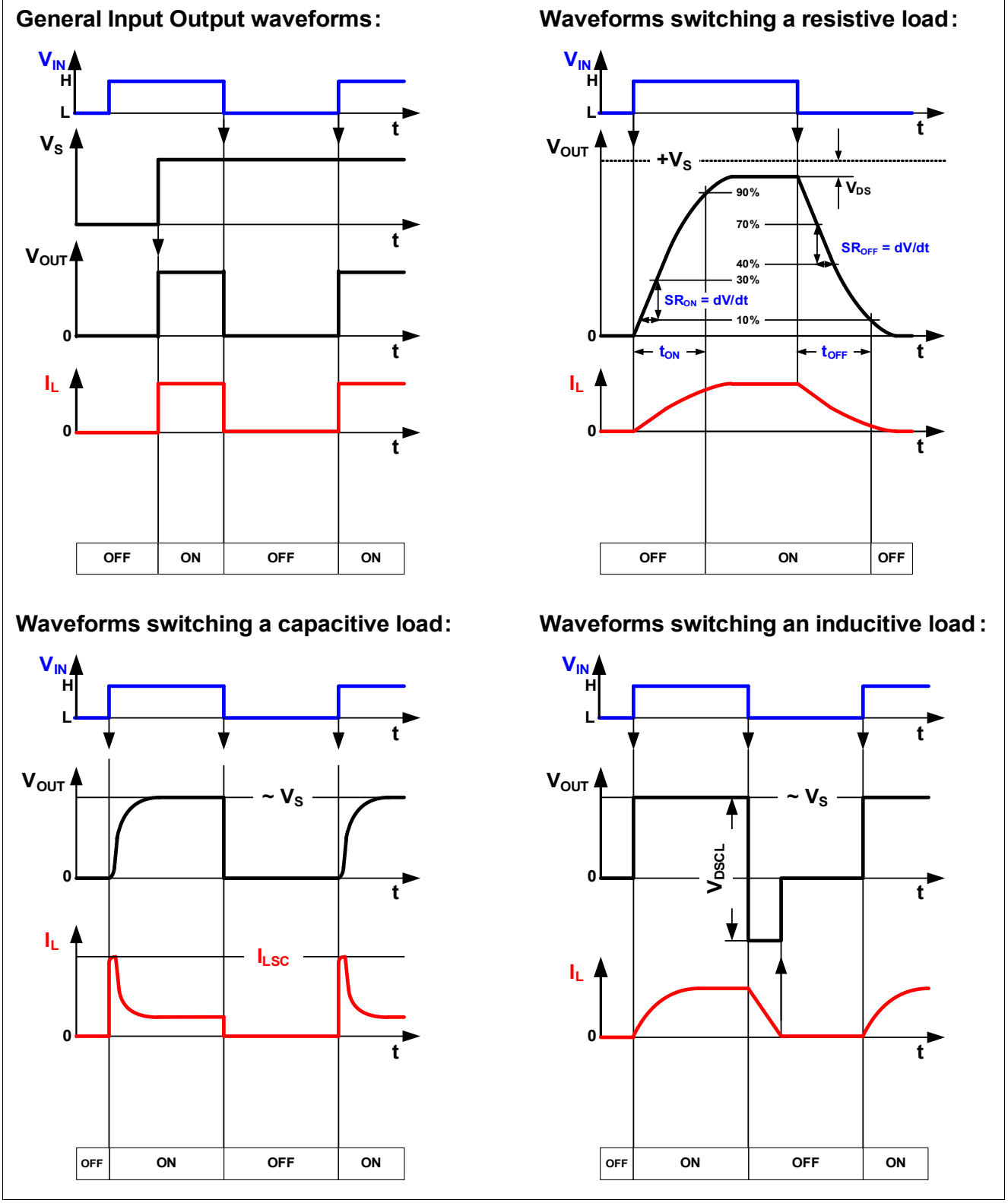


Figure 6 Typical application waveforms of the ITS4060S-SJ-N

6.3 Protection behavior

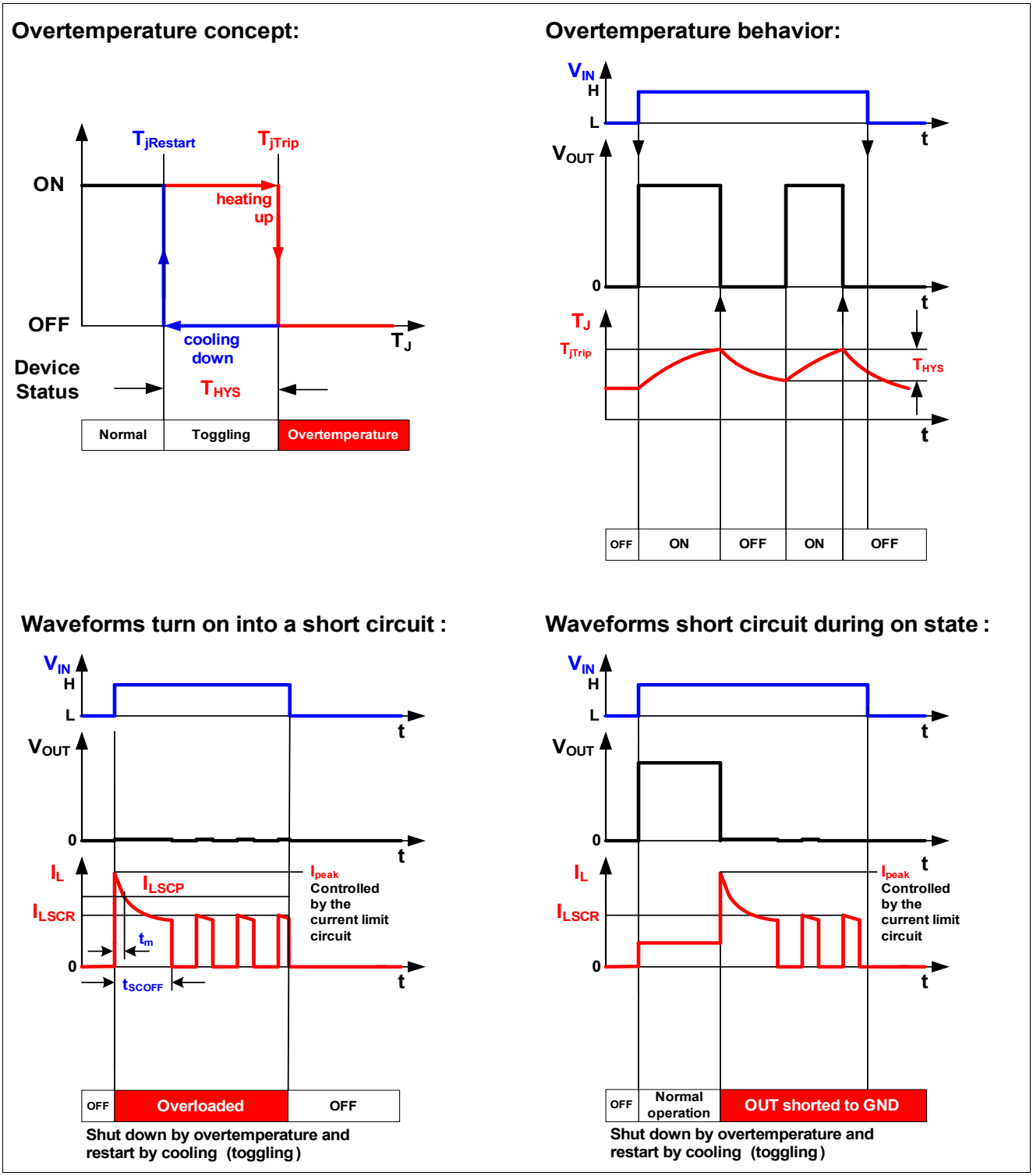


Figure 7 Protective behavior of the ITS4060S-SJ-N

7 Package information

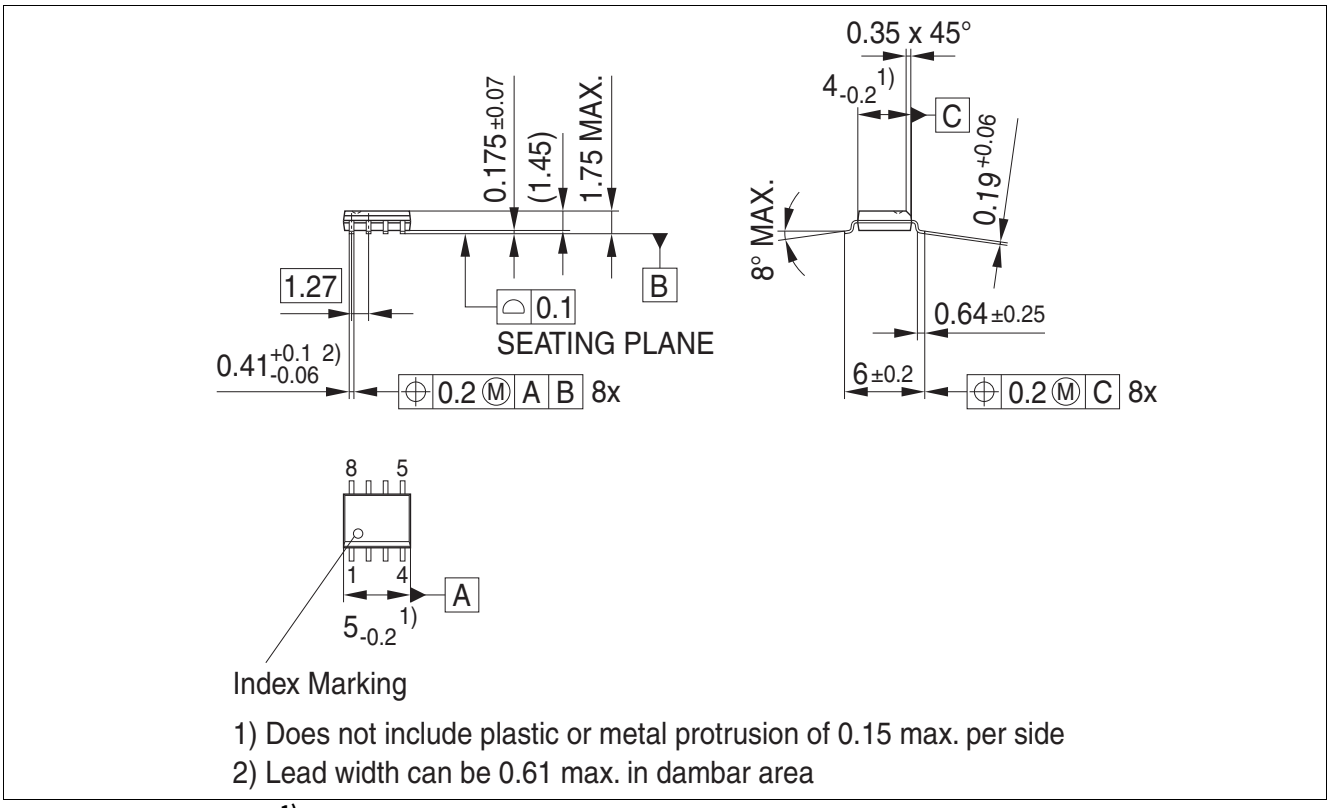


Figure 8 PG-DSO-8[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

8 Revision history

Revision	Date	Changes
1.10	2019-07-25	Datasheet updated: - ESD ratings for HBM updated according ANSI/ESDA/JEDEC JS-001 - Editorial changes
1.0	12-09-01	Datasheet release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-07-25
Published by
Infineon Technologies AG
81726 Munich, Germany

© 2019 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about any aspect of this document?
Email: erratum@infineon.com
Z8F51106907

IMPORTANT NOTICE
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").
With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.
In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.
The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.