

DirectFET® N-Channel Power MOSFET

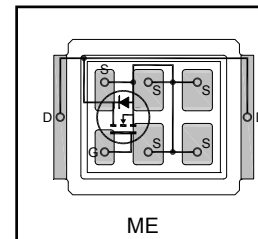
**Application**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

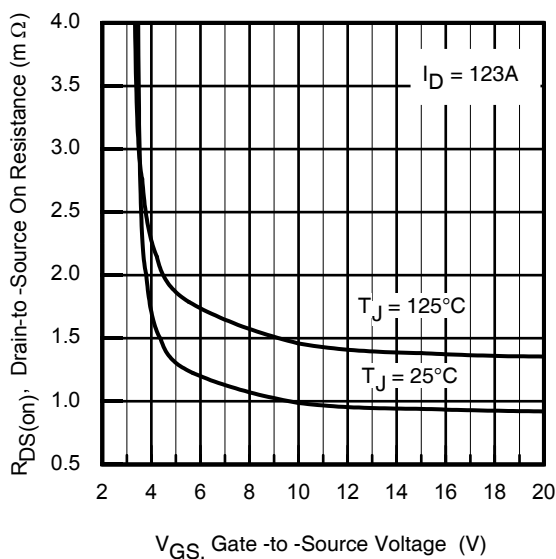
**Benefits**

- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead-Free, RoHS Compliant

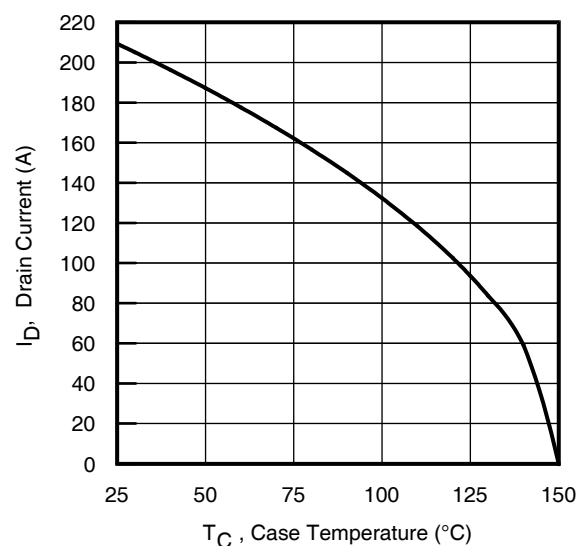
<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b> <b>max</b> <b>@ V<sub>GS</sub> = 10V</b>	<b>1.0mΩ</b>
	<b>1.25mΩ</b>
<b>R<sub>DS(on)</sub> typ.</b> <b>max</b> <b>@ V<sub>GS</sub> = 4.5V</b>	<b>1.5mΩ</b>
	<b>2.0mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>209A</b>



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRL7486MPbF	DirectFET® ME	Tape and Reel	4800	IRL7486MTRPbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	209	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	132	
$I_{DM}$	Pulsed Drain Current ①	836	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	104	W
	Linear Derating Factor	0.83	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	80	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	190	
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ④	111	
$I_{AR}$	Avalanche Current ①	See Fig.15,16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

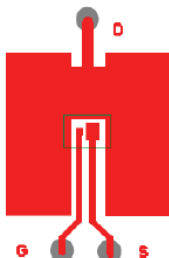
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ❶	—	60	°C/W
$R_{\theta JA}$	Junction-to-Ambient ❷	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ❸	20	—	
$R_{\theta JC}$	Junction-to-Case ❹⑦	—	1.2	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	0.75	—	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

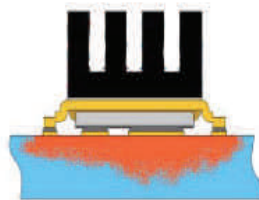
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	35	—	mV/°C	Reference to $25^\circ\text{C}$ , $I_D = 1.0\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.0	1.25	mΩ	$V_{GS} = 10\text{V}$ , $I_D = 123\text{A}$ ④
		—	1.5	2.0		$V_{GS} = 4.5\text{V}$ , $I_D = 62\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.8	2.5	V	$V_{DS} = V_{GS}$ , $I_D = 150\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Internal Gate Resistance	—	0.97	—	Ω	

**Notes:**

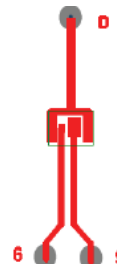
- ❶ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ❷ Used double sided cooling , mounting pad with large heatsink.
- ❸ TC measured with thermocouple mounted to top (Drain) of part.



❶ Surface mounted on 1 in. square Cu board (still air).



❷ Mounted to a PCB with small clip heatsink (still air)

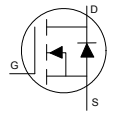


❸ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

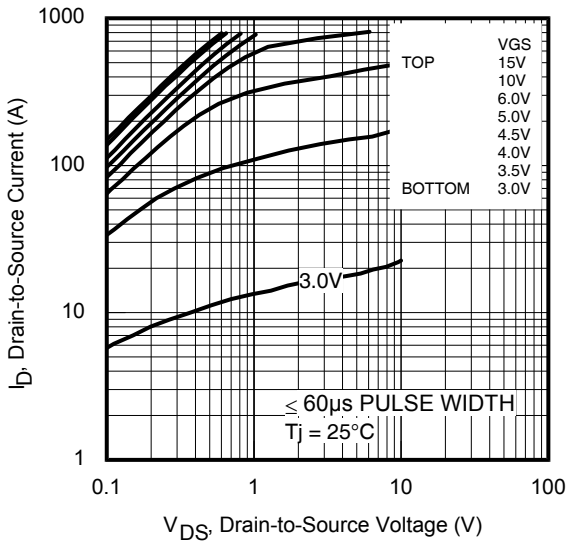
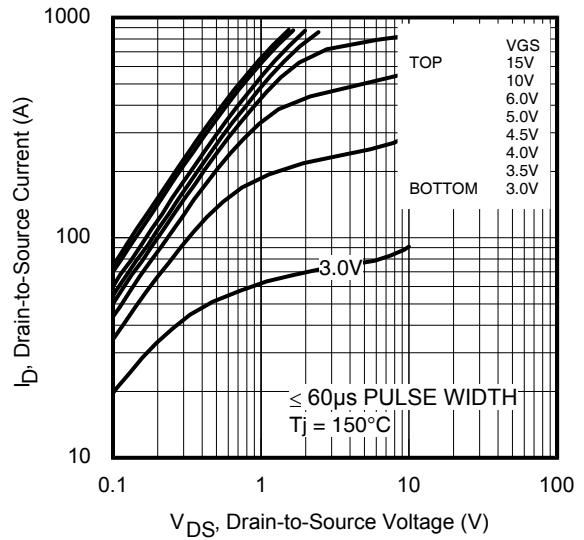
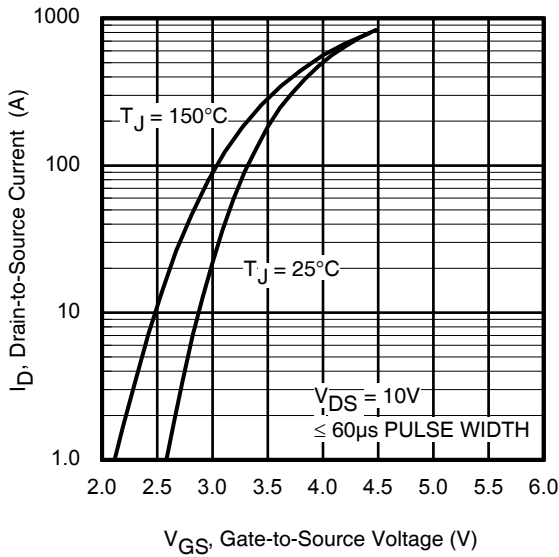
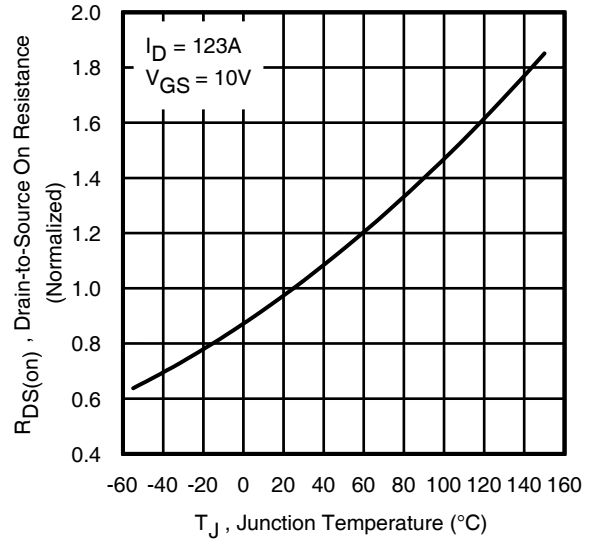
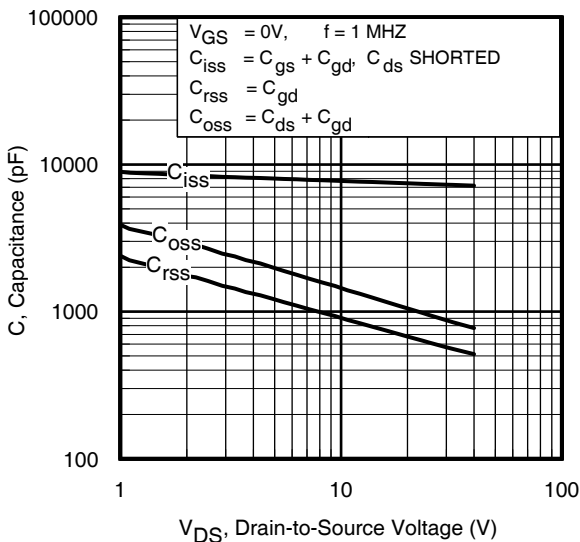
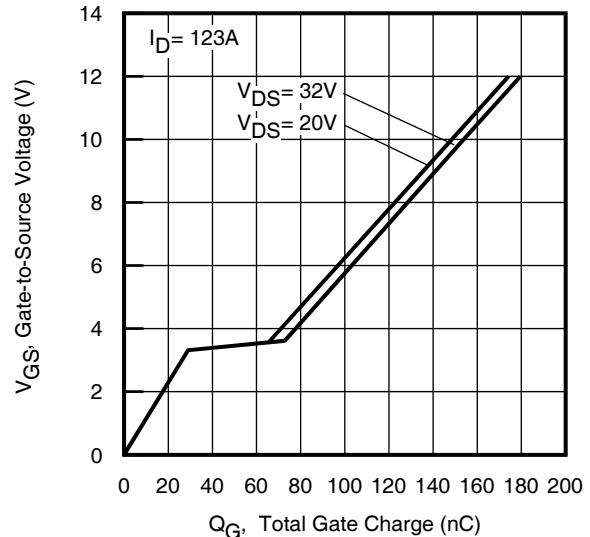
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	427	—	—	S	$V_{DS} = 10\text{V}$ , $I_D = 123\text{A}$
$Q_g$	Total Gate Charge	—	76	111	nC	$I_D = 123\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	27	—		$V_{DS} = 20\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	33	—		$V_{GS} = 4.5\text{V}$ ④
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	41	—		$I_D = 123\text{A}$ , $V_{DS} = 0\text{V}$ , $V_{GS} = 10\text{V}$
$t_{d(on)}$	Turn-On Delay Time	—	35	—	ns	$V_{DD} = 20\text{V}$
$t_r$	Rise Time	—	110	—		$I_D = 30\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	54	—		$R_G = 2.7\Omega$
$t_f$	Fall Time	—	47	—		$V_{GS} = 4.5\text{V}$ ④
$C_{iss}$	Input Capacitance	—	6904	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	939	—		$V_{DS} = 25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	607	—		$f = 1.0\text{MHz}$
$C_{oss}$ eff. (ER)	Effective Output Capacitance (Energy Related)	—	1150	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $32\text{V}$ ⑥
$C_{oss}$ eff. (TR)	Effective Output Capacitance (Time Related)	—	1376	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $32\text{V}$ ⑤

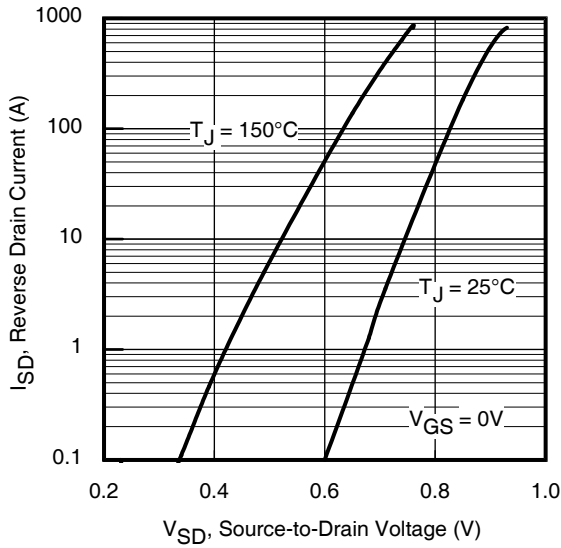
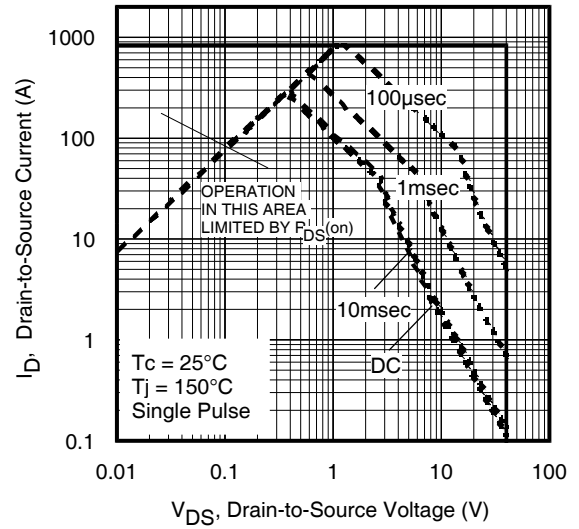
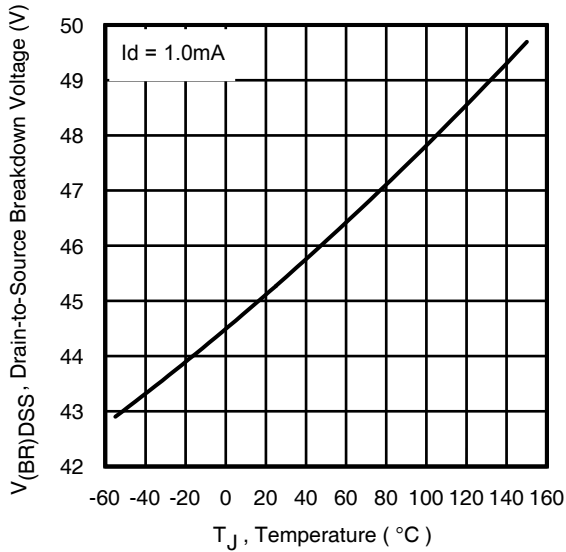
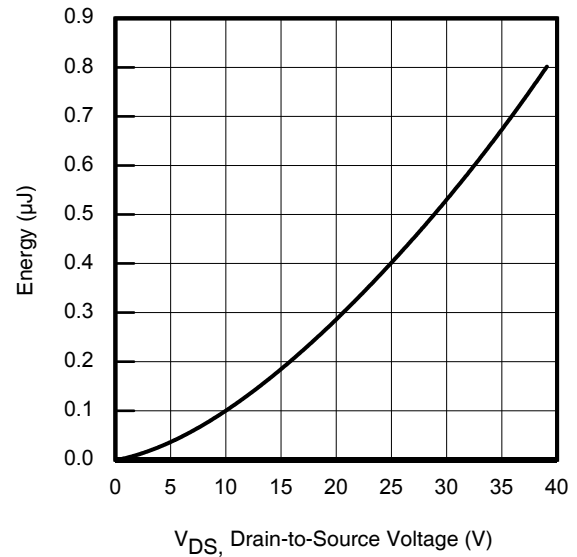
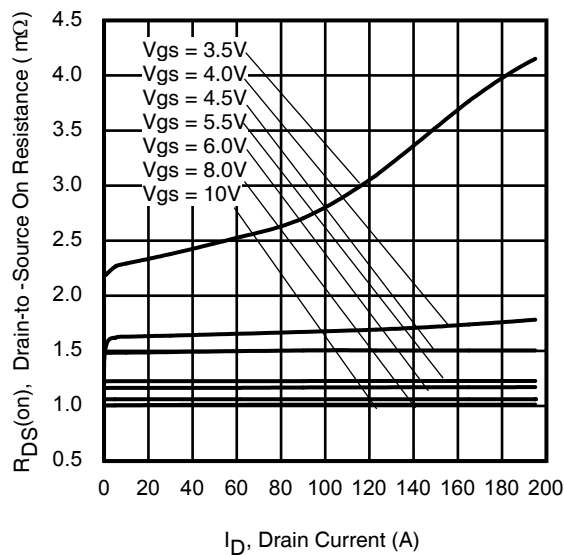
**Diode Characteristics**

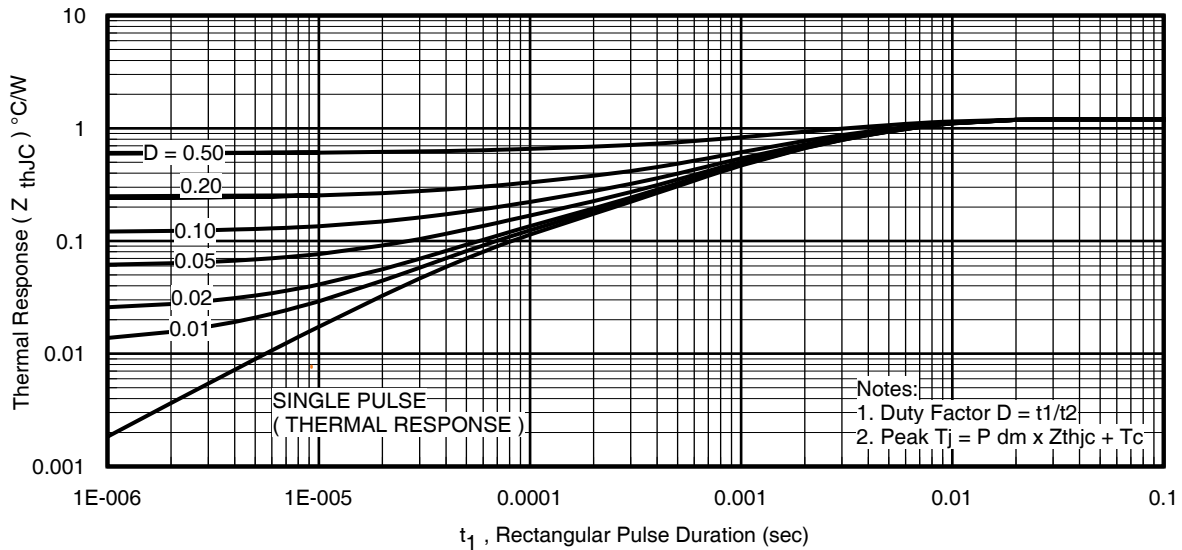
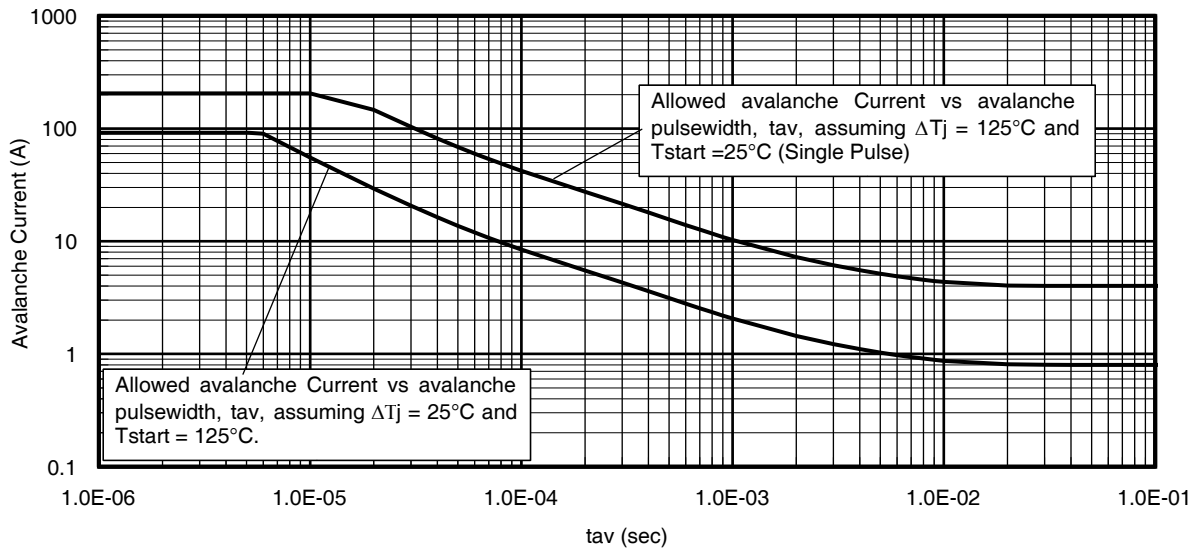
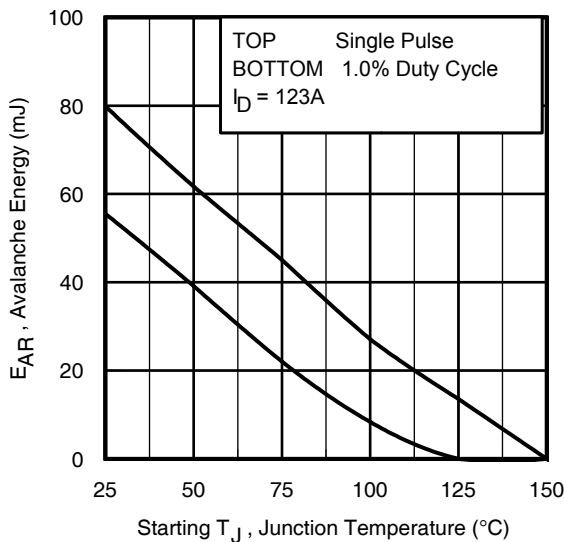
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	104	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	836		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = 123\text{A}$ , $V_{GS} = 0\text{V}$ ④
dv/dt	Peak Diode Recovery ③	—	3.6	—	V/ns	$T_J = 150^\circ\text{C}$ , $I_S = 123\text{A}$ , $V_{DS} = 40\text{V}$
$t_{rr}$	Reverse Recovery Time	—	43	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 34\text{V}$ , $T_J = 125^\circ\text{C}$ $I_F = 123\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	55	—		nC
$I_{RRM}$	Reverse Recovery Current	—	2.1	—	A	

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.011\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 123\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 123\text{A}$ ,  $di/dt \leq 1056\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.011\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 123\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑨ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.0\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 20\text{A}$ ,  $V_{GS} = 10\text{V}$ .


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current


**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).

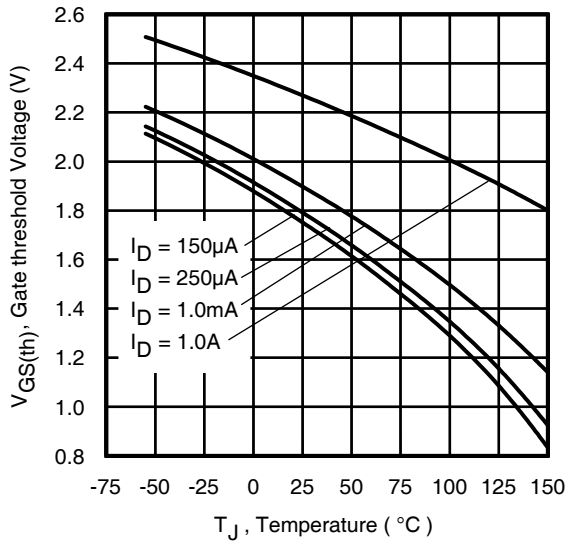
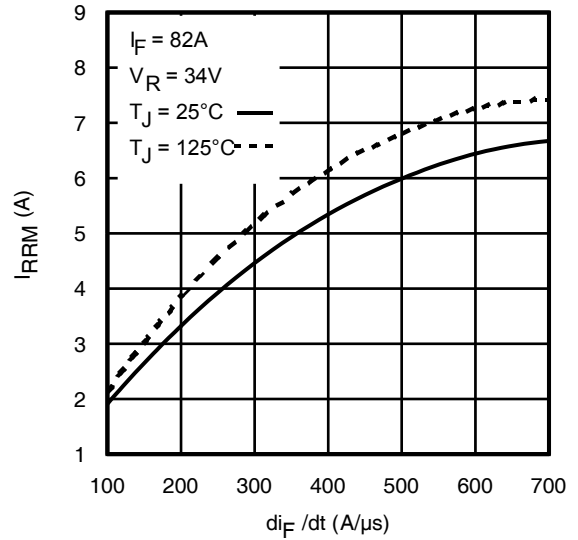
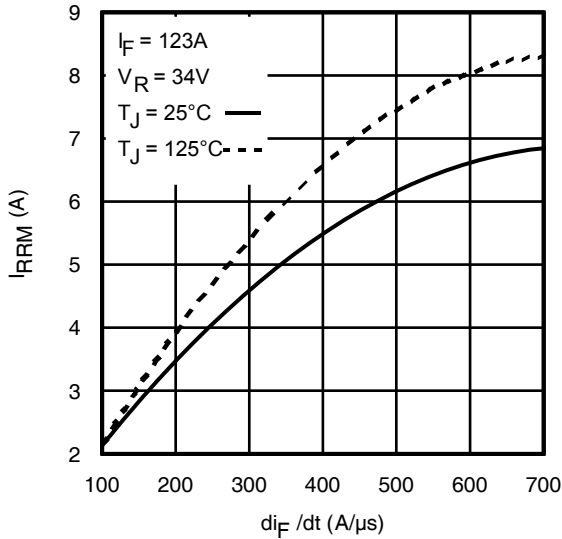
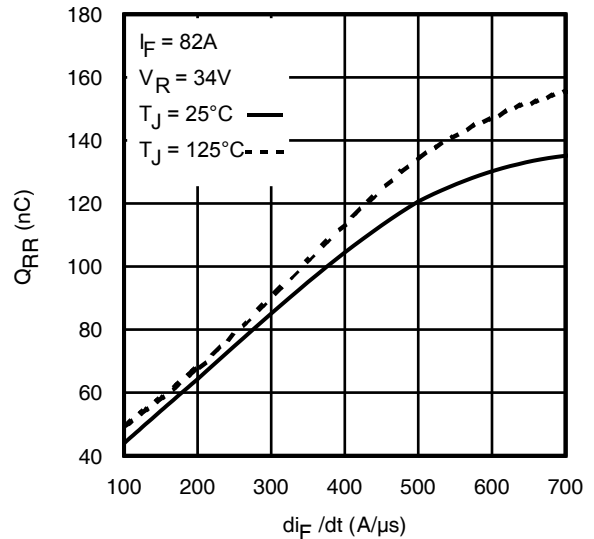
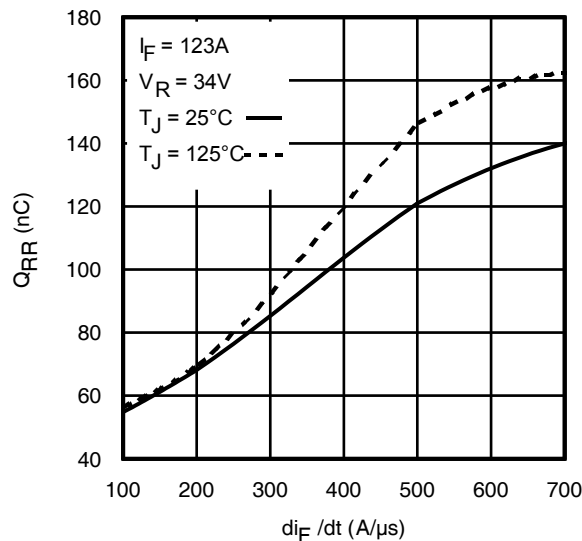
 $t_{av}$  = Average time in avalanche.

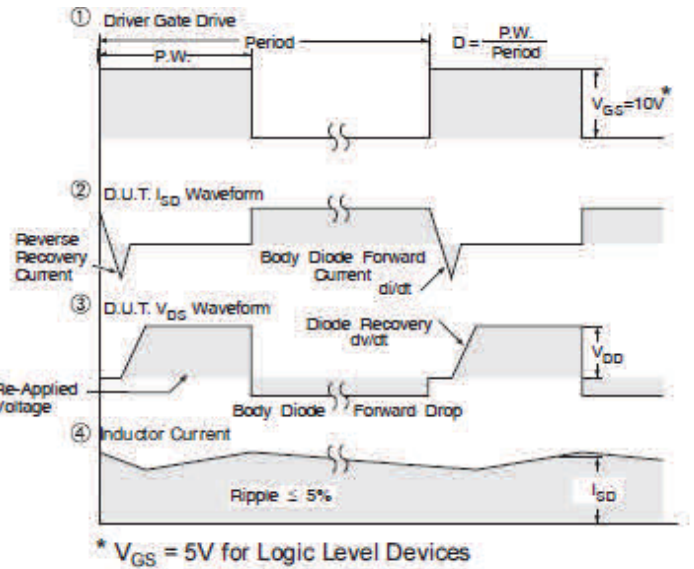
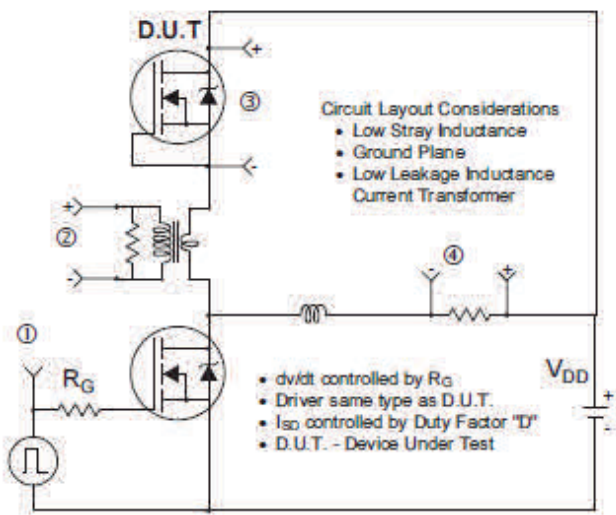
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$ 
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

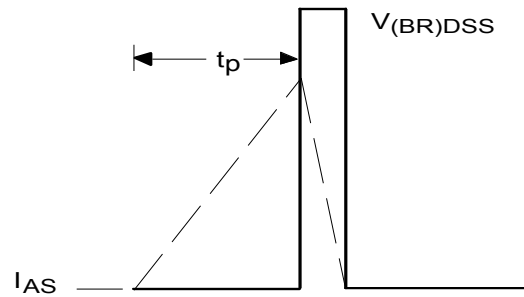
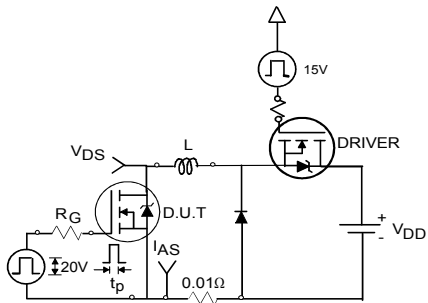
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig 17. Threshold Voltage vs. Temperature**

**Fig 18. Typical Recovery Current vs. dif/dt**

**Fig 19. Typical Recovery Current vs. dif/dt**

**Fig 20. Typical Stored Charge vs. dif/dt**

**Fig 21. Typical Stored Charge vs. dif/dt**

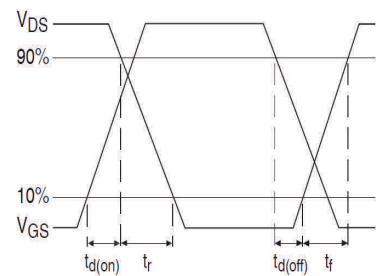
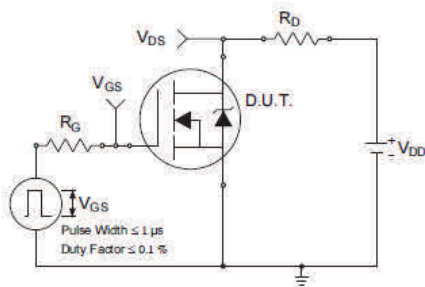


**Fig 22.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



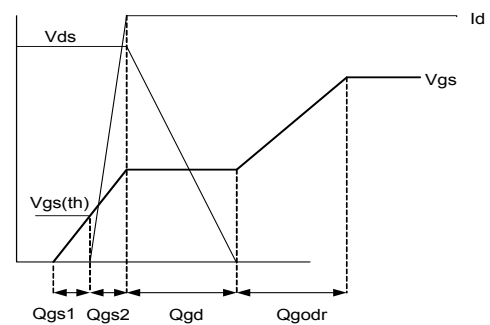
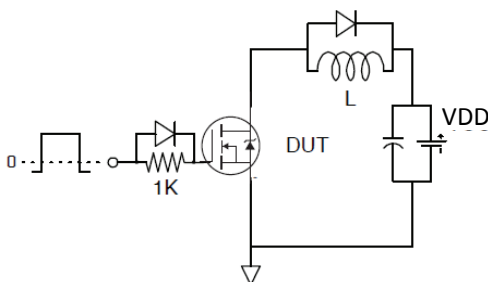
**Fig 23a.** Unclamped Inductive Test Circuit

**Fig 23b.** Unclamped Inductive Waveforms



**Fig 24a.** Switching Time Test Circuit

**Fig 24b.** Switching Time Waveforms



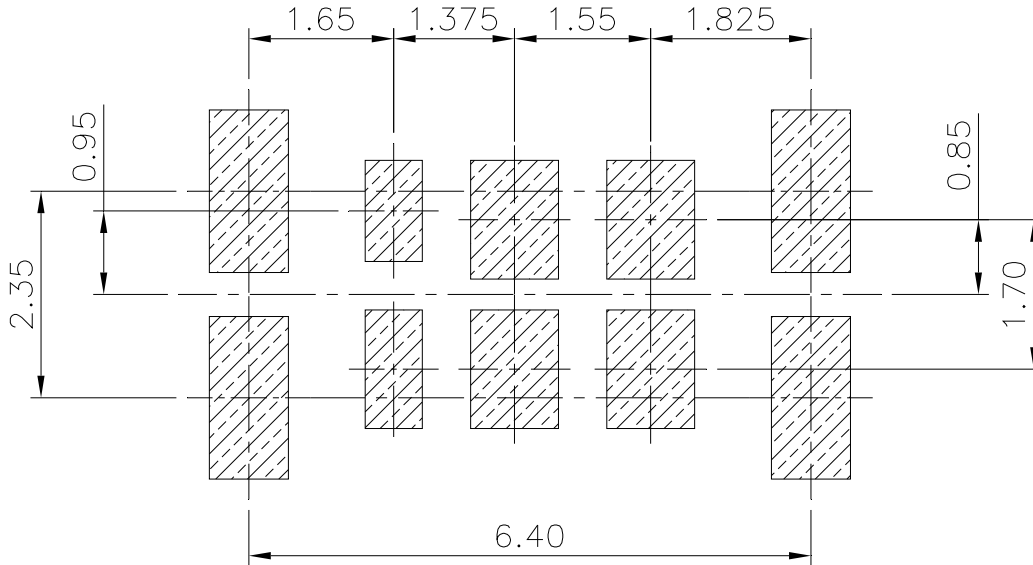
**Fig 25a.** Gate Charge Test Circuit

**Fig 25b.** Gate Charge Waveform

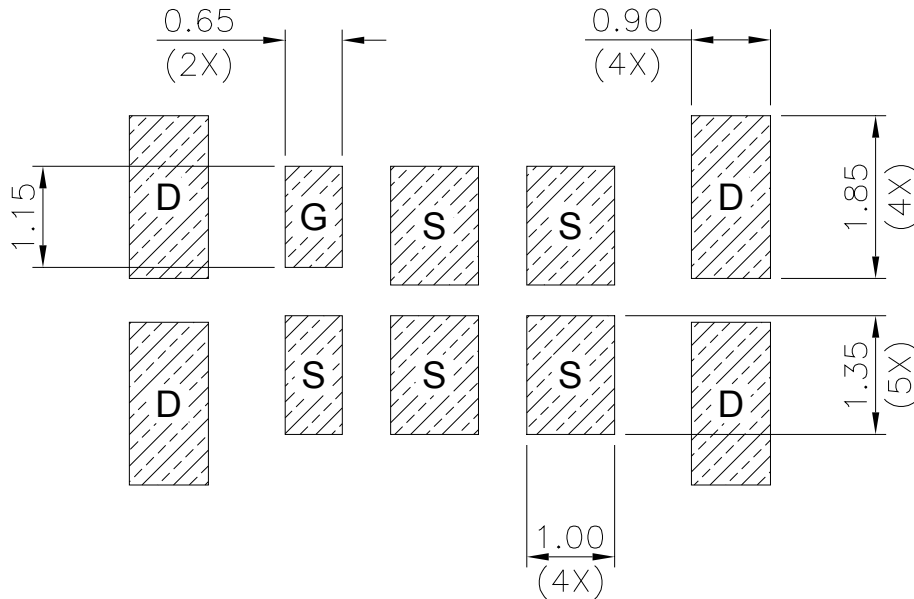


**DirectFET® Board Footprint, ME Outline**
**(Medium Size Can, E-Designation)**

Please see DirectFET® application note AN-1035 for all details regarding the assembly of DirectFET®. This includes all recommendations for stencil and substrate designs.



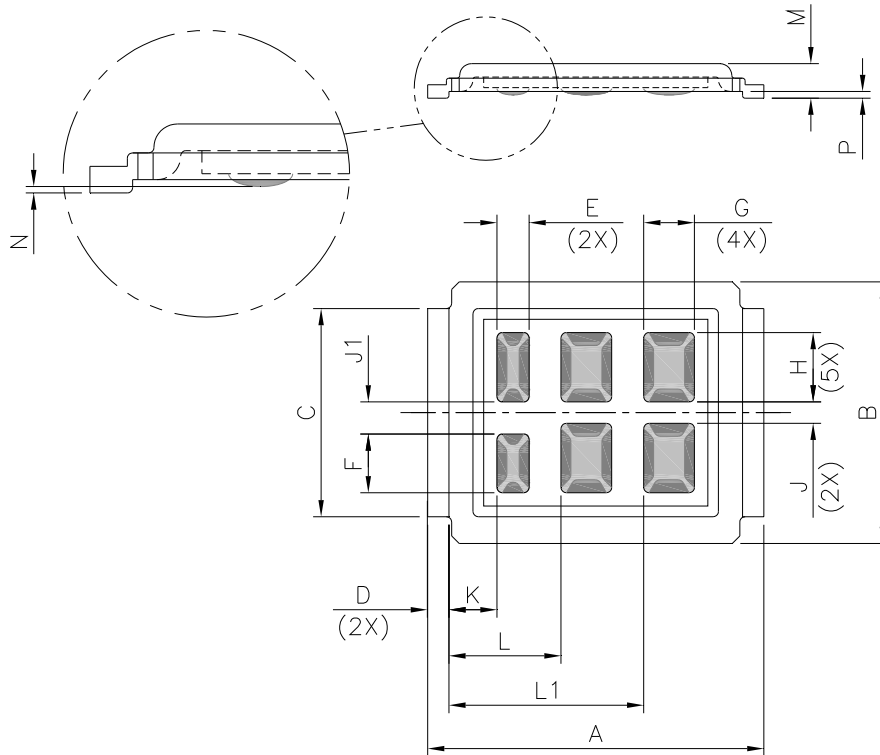
G = GATE  
D = DRAIN  
S = SOURCE



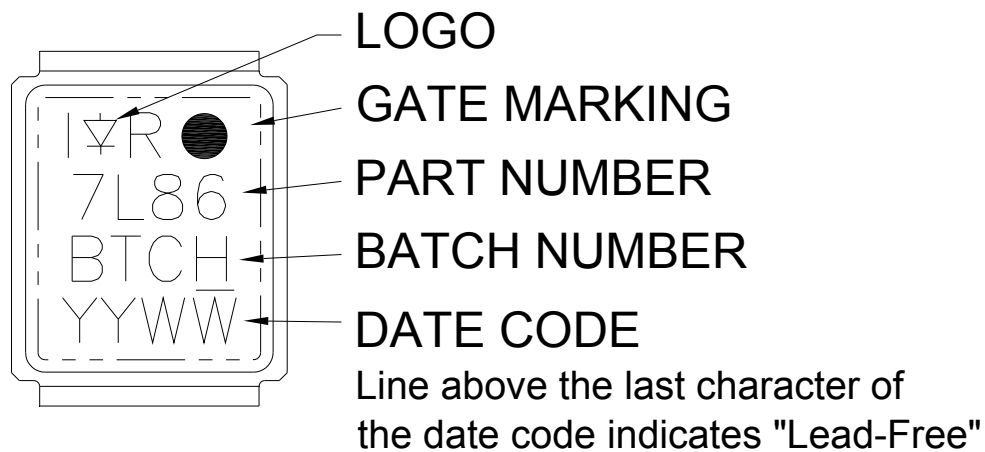
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**DirectFET® Outline Dimension, ME Outline**
**(Medium Size Can, E-Designation)**

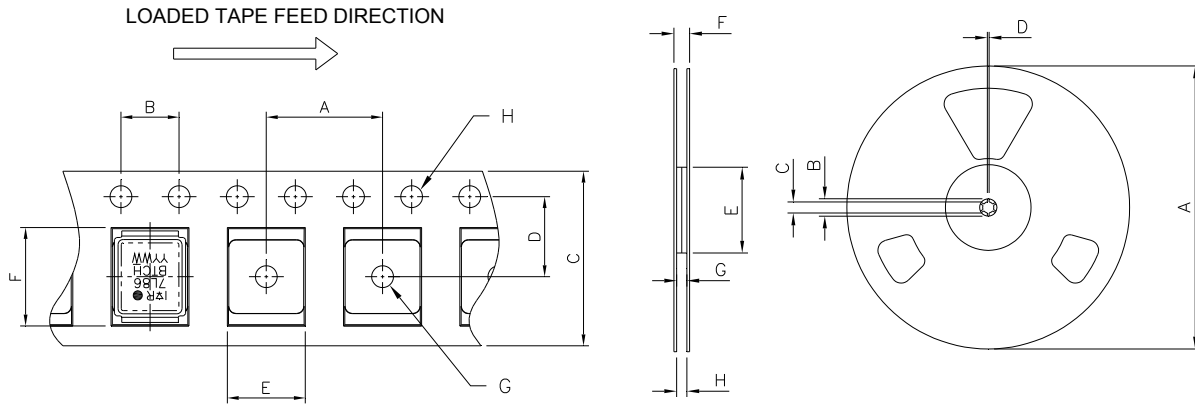
Please see DirectFET® application note AN-1035 for all details regarding the assembly of DirectFET®. This includes all recommendations for stencil and substrate designs.



CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	1.08	1.12	0.043	0.044
G	0.93	0.97	0.037	0.038
H	1.28	1.32	0.050	0.052
J	0.38	0.42	0.015	0.017
J1	0.58	0.62	0.023	0.024
K	0.88	0.92	0.035	0.036
L	2.08	2.12	0.082	0.083
L1	3.63	3.67	0.143	0.144
M	0.59	0.70	0.023	0.028
N	0.02	0.08	0.0008	0.003
P	0.08	0.17	0.003	0.007

**DirectFET® Part Marking**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**DirectFET® Tape & Reel Dimension (Showing component orientation).**


NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

 NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. Ordered as IRL7486MTRPbF.

REEL DIMENSIONS				
STANDARD OPTION (QTY 4800)				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

 Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
**Qualification Information†**

<b>Qualification Level</b>	Industrial * (per JEDEC JESD47F†† guidelines)	
<b>Moisture Sensitivity Level</b>	DFET 1.5	MSL1 (per JEDEC J-STD-020D††)
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

\* Industrial qualification standards except autoclave test conditions.

**Revision History**

Date	Comments
05/14/2015	• Updated registered trademark from DirectFET™ to DirectFET® on page 1,9 and 10.