

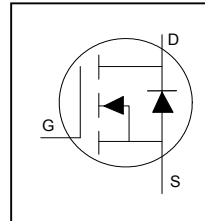
**Application**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

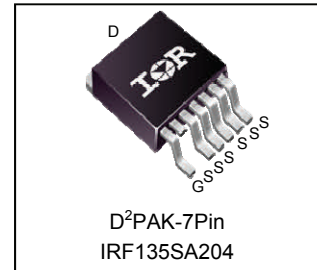
**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET

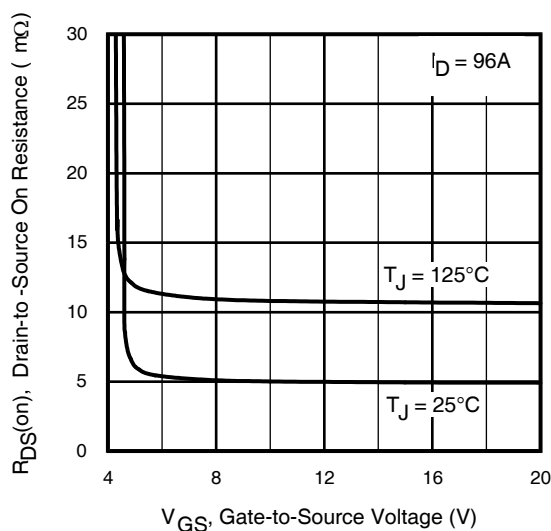


<b>V<sub>DSS</sub></b>	<b>135V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>4.7mΩ</b>
	<b>max</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>160A</b>

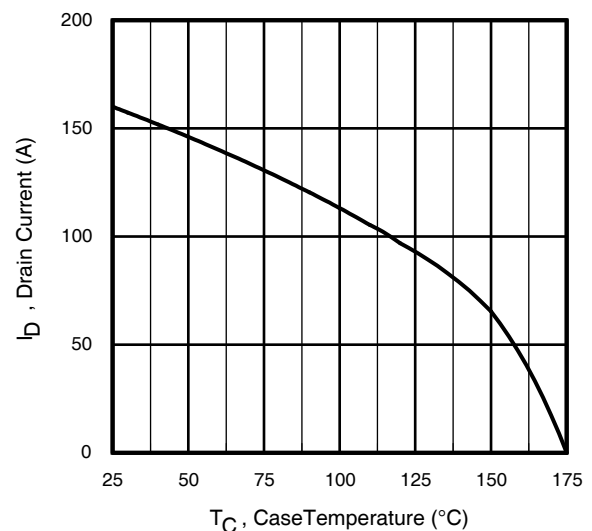


<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF135SA204	D <sup>2</sup> PAK-7Pin	Tape and Reel	800	IRF135SA204



**Fig 1.** Typical On- Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	160	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	113	
$I_{DM}$	Pulsed Drain Current ①	608	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	500	W
	Linear Derating Factor	3.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	670	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	1280	
$I_{AR}$	Avalanche Current ④	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	0.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	135	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.14	—	V/°C	Reference to $25^\circ\text{C}, I_D = 5\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.7	5.9	mΩ	$V_{GS} = 10\text{V}, I_D = 96\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 135\text{V}, V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 135\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.2	—	Ω	


**Notes:**

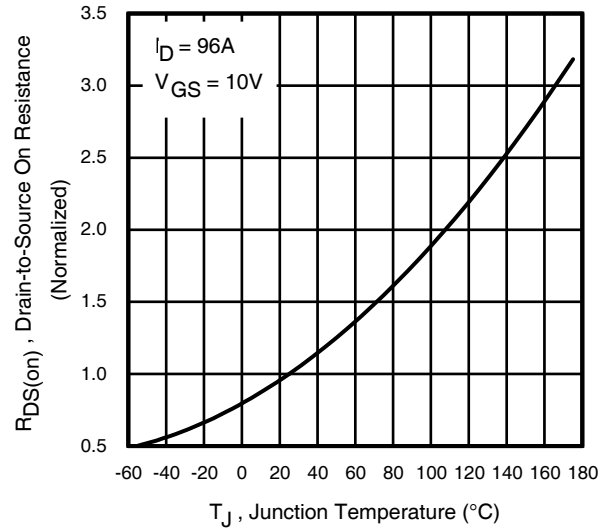
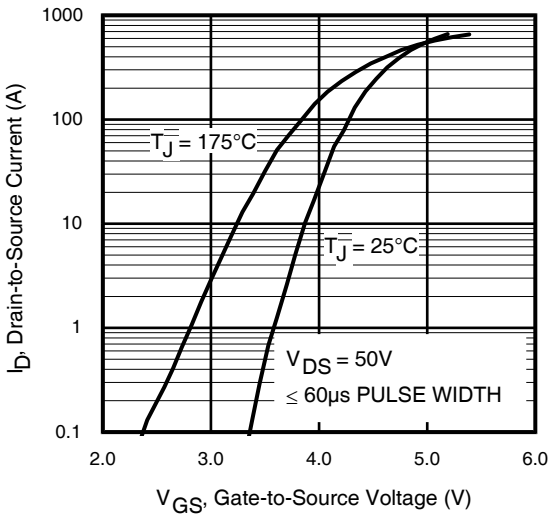
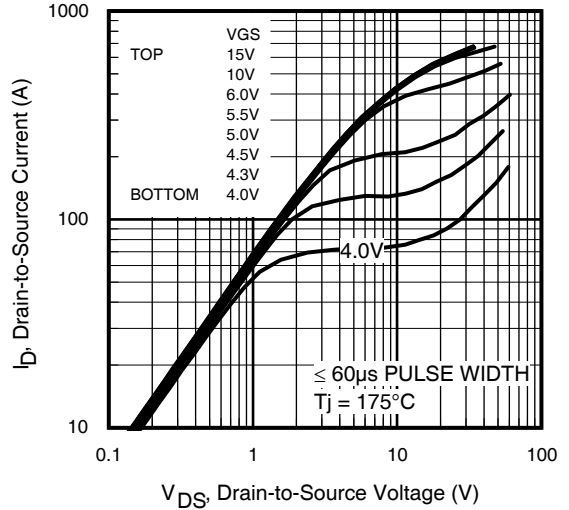
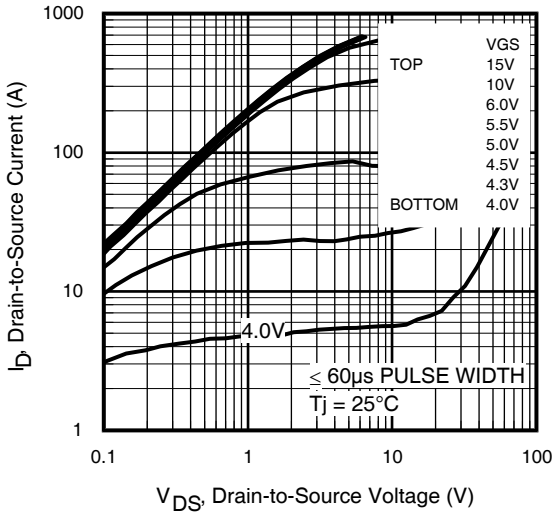
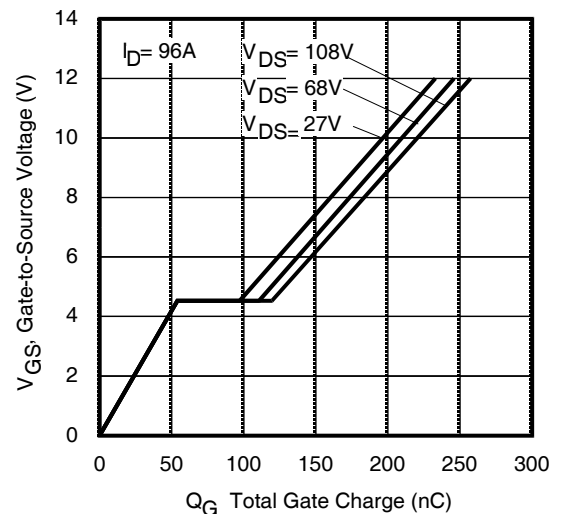
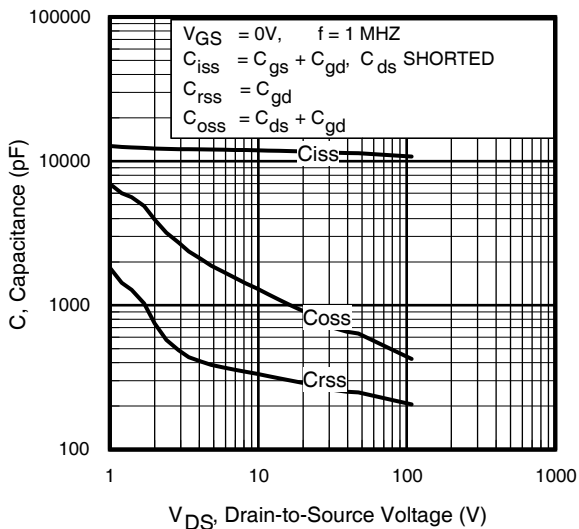
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 146\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 96\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 96\text{A}$ ,  $di/dt \leq 2200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:  
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑨ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.0\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 49\text{A}$ ,  $V_{GS} = 10\text{V}$ .

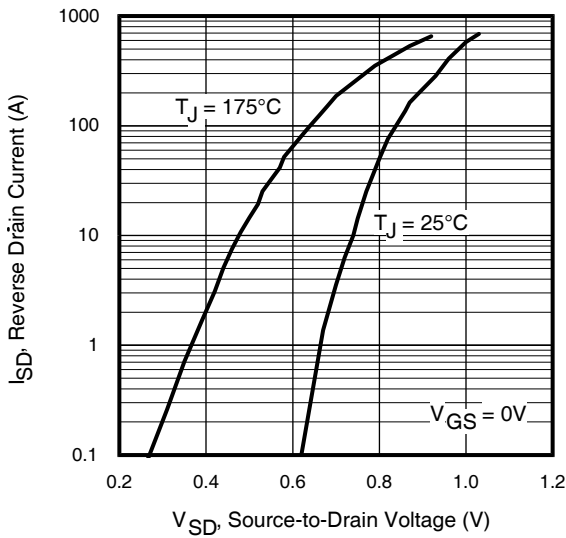
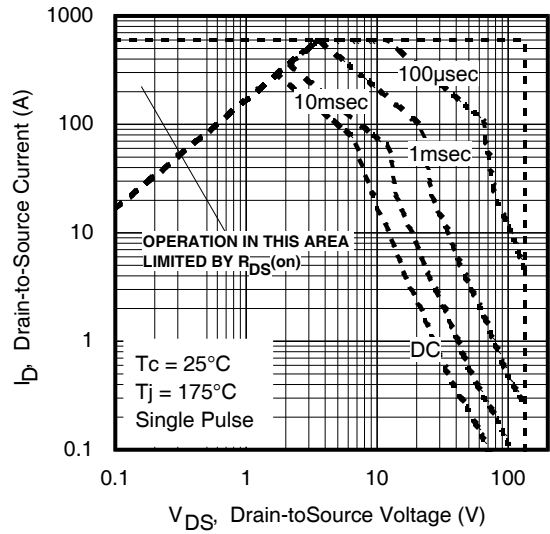
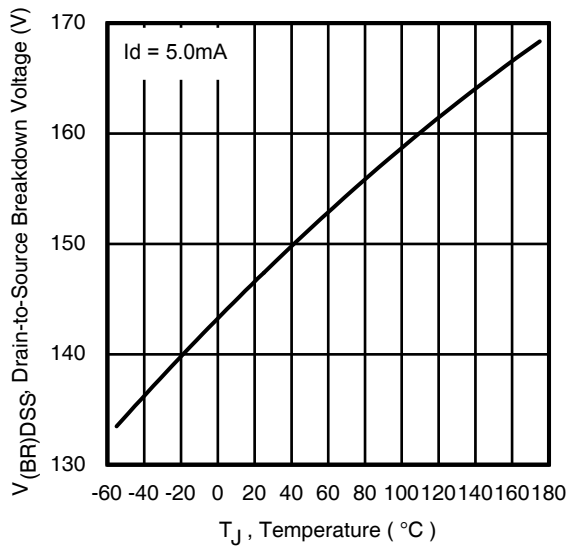
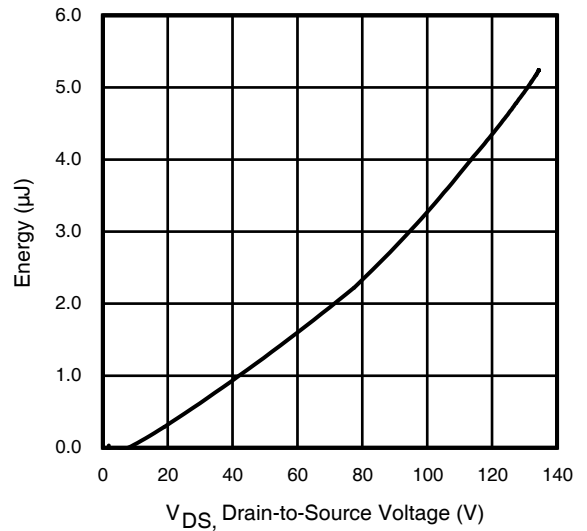
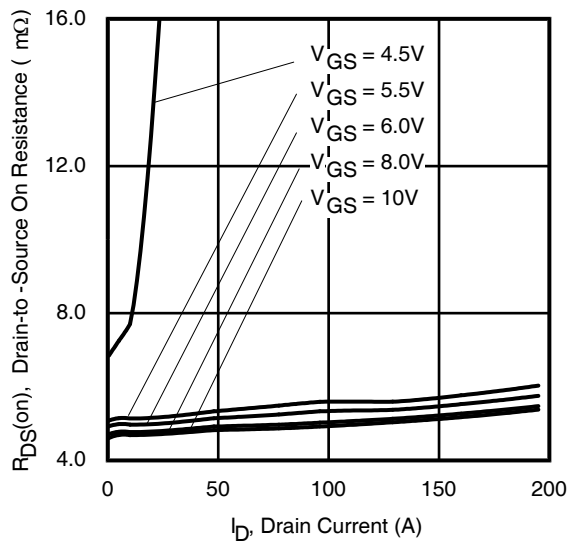
**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

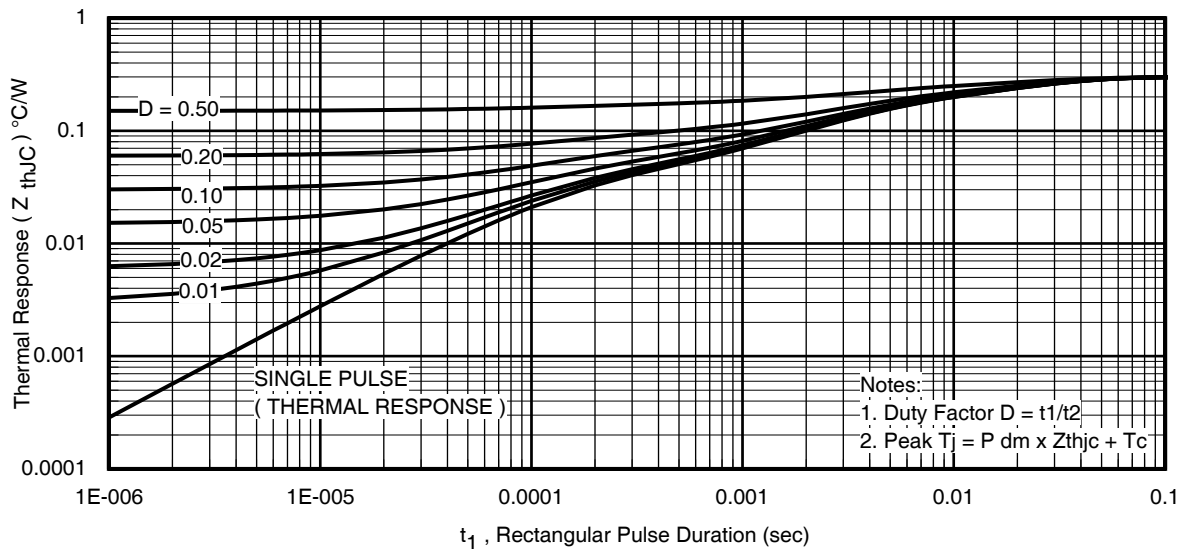
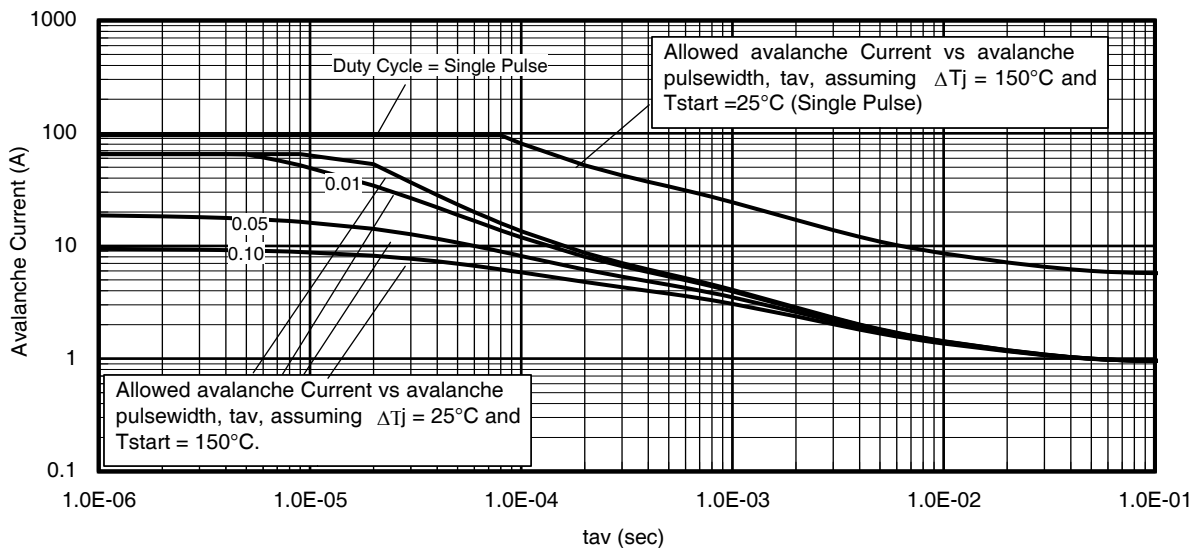
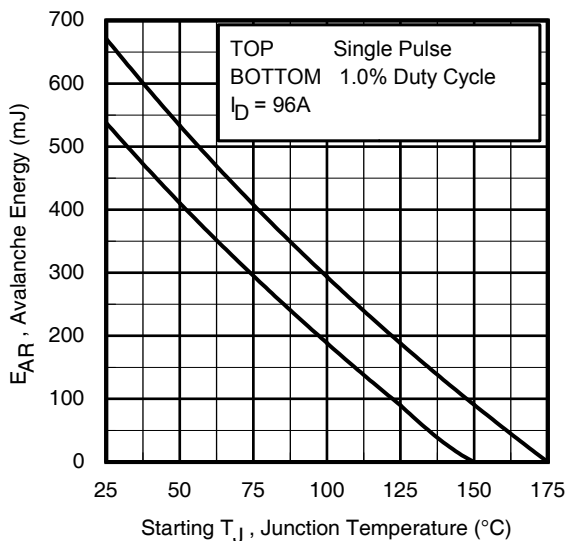
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	270	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 96A
Q <sub>g</sub>	Total Gate Charge	—	210	315	nC	I <sub>D</sub> = 96A V <sub>DS</sub> = 68V V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	54	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	57	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	153	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	20	—	ns	V <sub>DD</sub> = 81V I <sub>D</sub> = 96A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V④
t <sub>r</sub>	Rise Time	—	56	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	140	—		
t <sub>f</sub>	Fall Time	—	56	—		
C <sub>iss</sub>	Input Capacitance	—	11690	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz, See Fig.7 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 108V⑥ V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 108V⑤
C <sub>oss</sub>	Output Capacitance	—	650	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	290	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	630	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	845	—		

**Diode Characteristics**

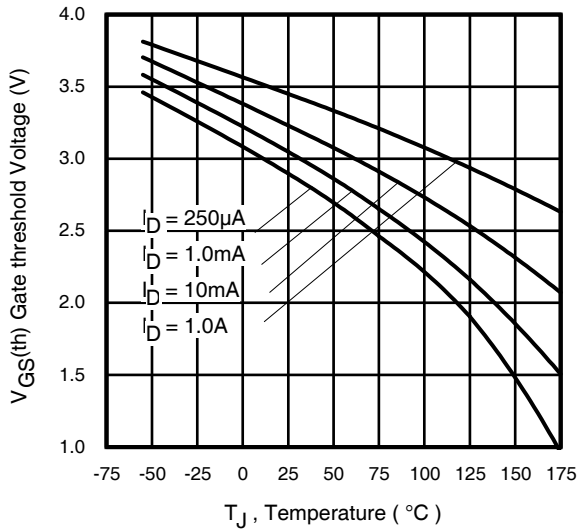
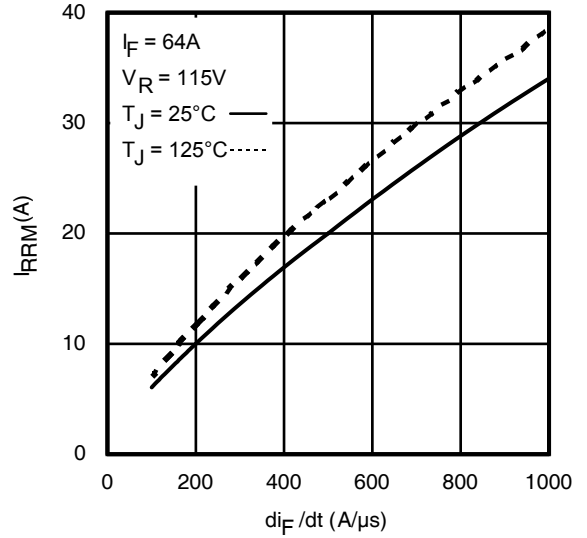
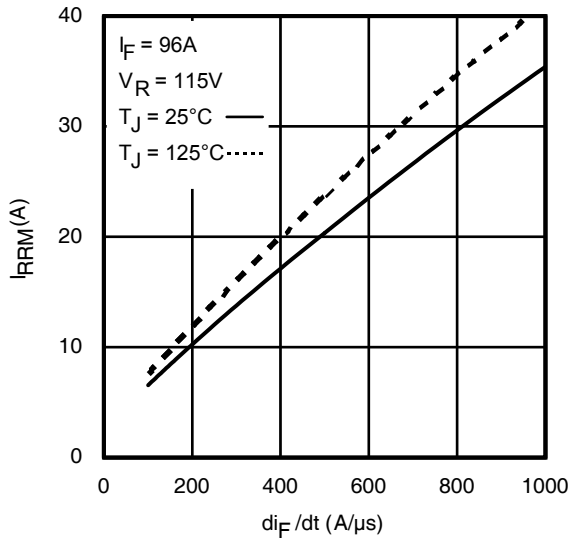
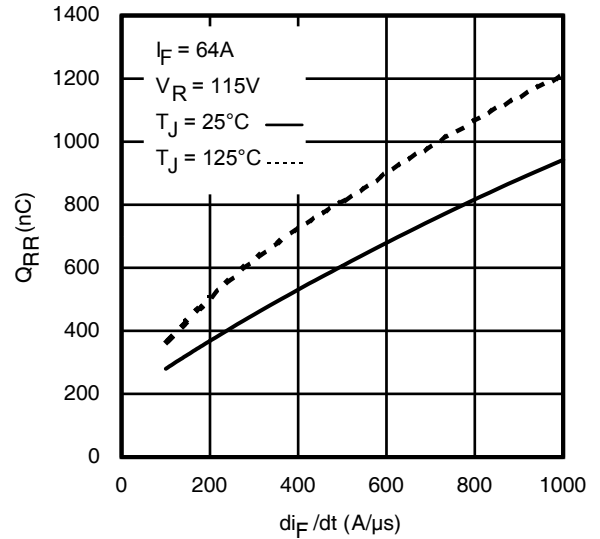
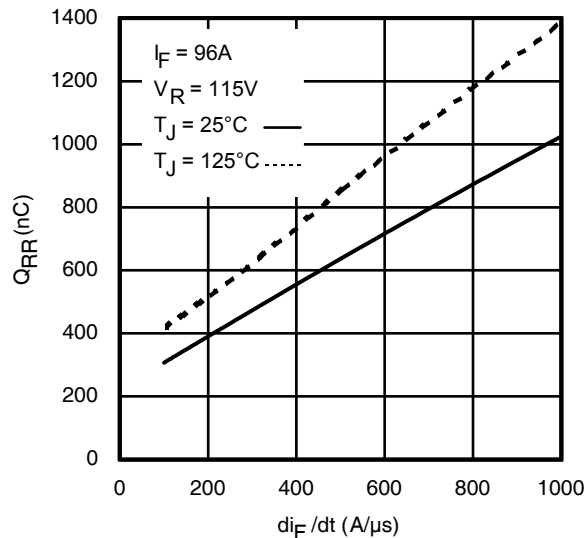
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	160	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	608		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 96A, V <sub>GS</sub> = 0V ④
dv/dt	Peak Diode Recovery dv/dt③	—	22	—	V/ns	T <sub>J</sub> = 175°C, I <sub>S</sub> = 96A, V <sub>DS</sub> = 135V
t <sub>rr</sub>	Reverse Recovery Time	—	85	—	ns	T <sub>J</sub> = 25°C V <sub>DD</sub> = 115V T <sub>J</sub> = 125°C I <sub>F</sub> = 96A,
		—	98	—		
Q <sub>rr</sub>	Reverse Recovery Charge	—	315	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs ④ T <sub>J</sub> = 125°C
		—	430	—		
I <sub>RRM</sub>	Reverse Recovery Current	—	6.6	—	A	T <sub>J</sub> = 25°C

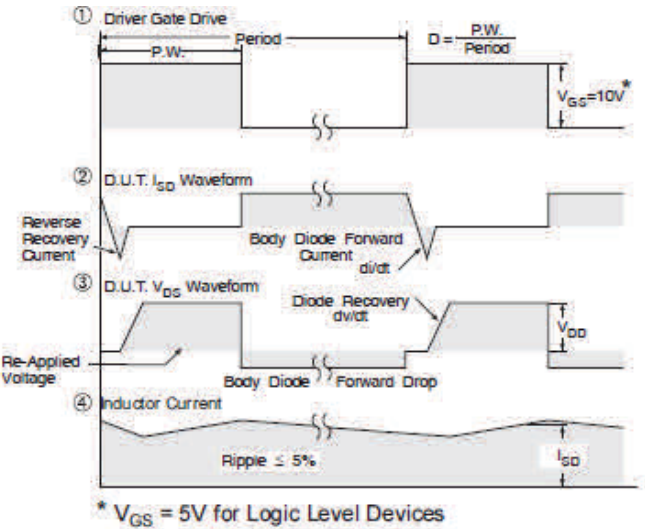
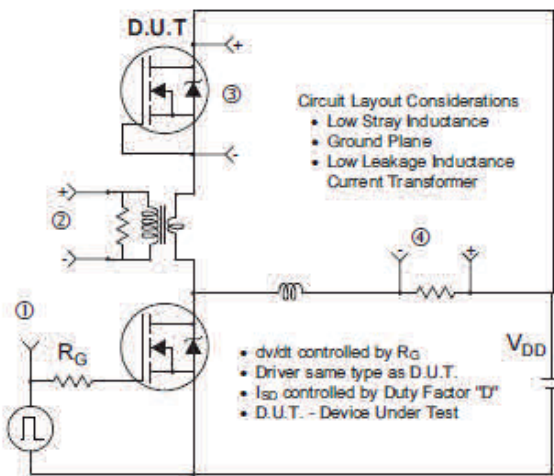

**Fig 5. Typical Transfer Characteristics**
**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**
**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{OSS}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current

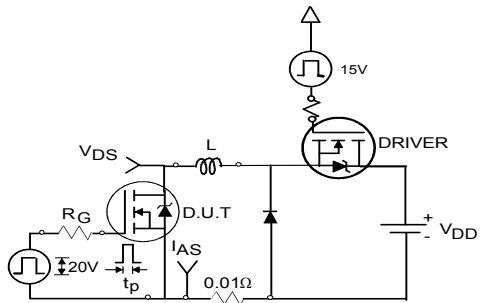

**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves, Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 14)  
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

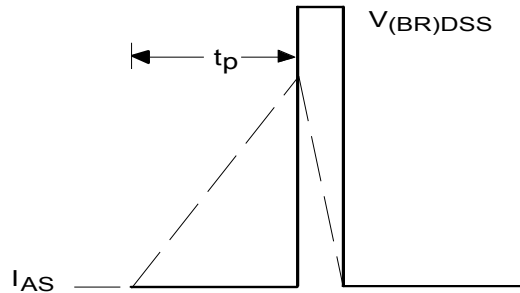

**Fig 17. Threshold Voltage vs. Temperature**

**Fig 18. Typical Recovery Current vs.  $di_F/dt$** 

**Fig 19. Typical Recovery Current vs.  $di_F/dt$** 

**Fig 20. Typical Stored Charge vs.  $di_F/dt$** 

**Fig 21. Typical Stored Charge vs.  $di_F/dt$**



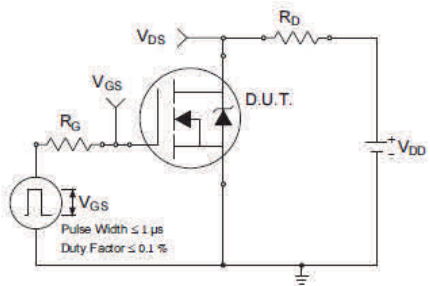
**Fig 22.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs



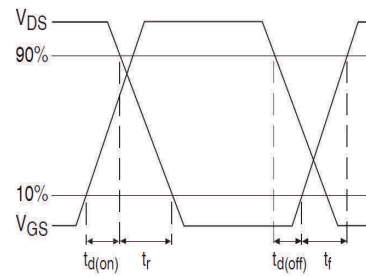
**Fig 23a.** Unclamped Inductive Test Circuit



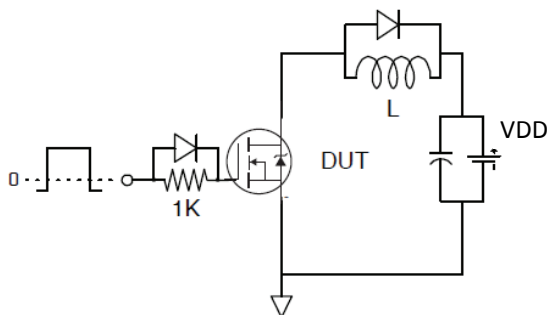
**Fig 23b.** Unclamped Inductive Waveforms



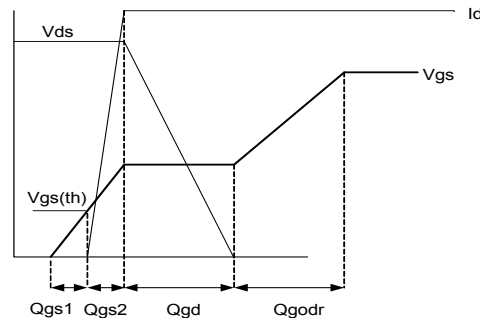
**Fig 24a.** Switching Time Test Circuit



**Fig 24b.** Switching Time Waveforms

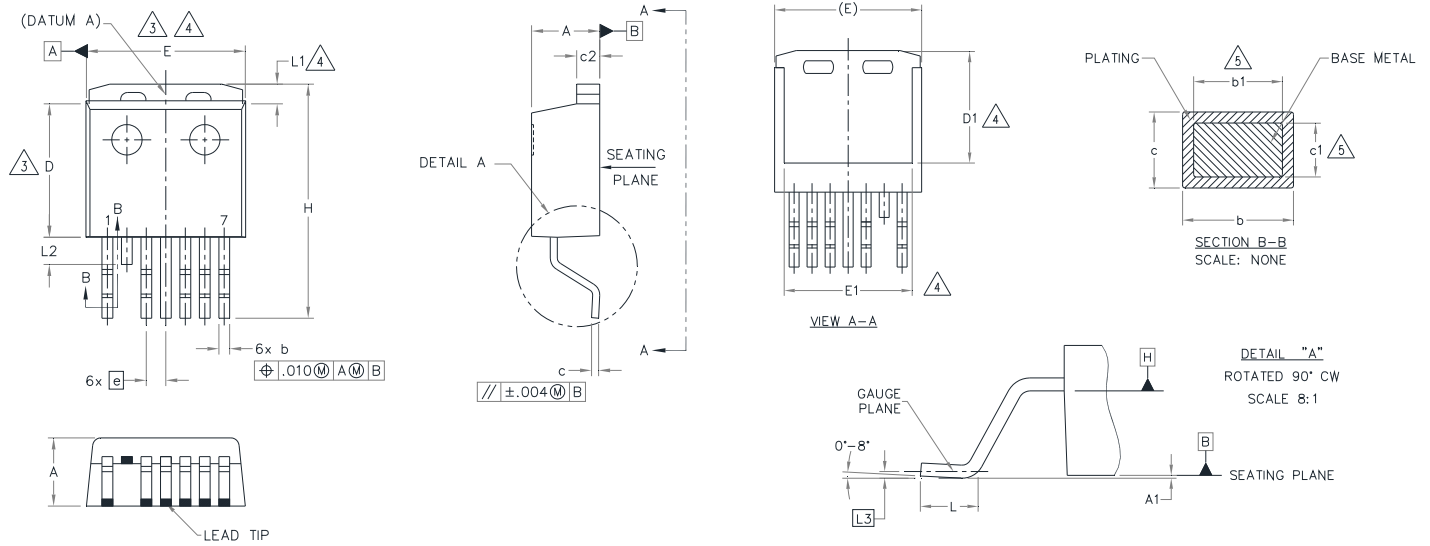


**Fig 25a.** Gate Charge Test Circuit



**Fig 25b.** Gate Charge Waveform



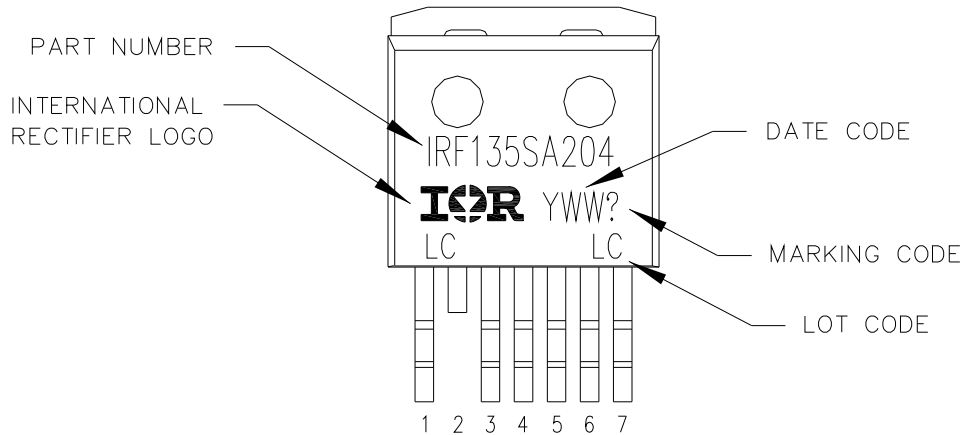
**D<sup>2</sup>PAK-7Pin Package Outline (Dimensions are shown in millimeters (inches))**


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	8.00	9.00	.315	.354	
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

**NOTES:**

- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.** DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- 4.** THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- 5.** DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- CONTROLLING DIMENSION: INCH.
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB, EXCEPT FOR DIMS. E, E1 & D1.

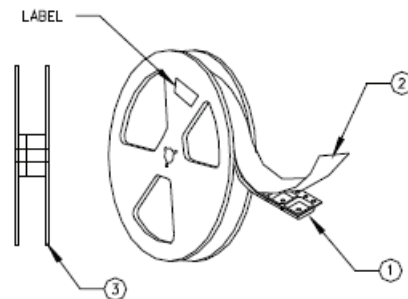
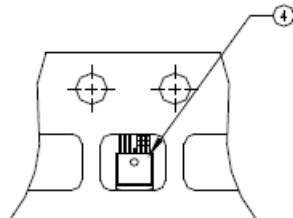
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak-7Pin Part Marking Information**

**D<sup>2</sup>PAK-7Pin Tape and Reel**
**NOTES, TAPE & REEL, LABELLING:**
**1. TAPE AND REEL**

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

**2. LABELLING (REEL AND SHIPPING BAG).**

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	D <sup>2</sup> PAK-7Pin	MSL1
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

<b>Date</b>	<b>Comments</b>
05/12/2017	<ul style="list-style-type: none"> <li>• Corrected package picture added "s" on pin number 2 - page 1.</li> <li>• Changed datasheet with Infineon logo - all pages.</li> <li>• Added disclaimer on last page</li> </ul>

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