

## MOSFET

### 950V CoolMOS™ P7 SJ Power Device

The latest 950V CoolMOS™ P7 series sets a new benchmark in 950V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

#### Features

- Best-in-class FOM  $R_{DS(on)} * E_{oss}$ ; reduced  $Q_g$ ,  $C_{iss}$ , and  $C_{oss}$
- Best-in-class SOT-223  $R_{DS(on)}$
- Best-in-class  $V_{(GS)th}$  of 3V and smallest  $V_{(GS)th}$  variation of  $\pm 0.5V$
- Integrated Zener Diode ESD protection
- Best-in-class CoolMOS™ quality and reliability
- Fully optimized portfolio

#### Benefits

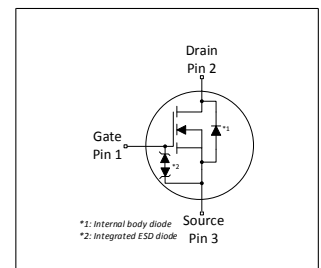
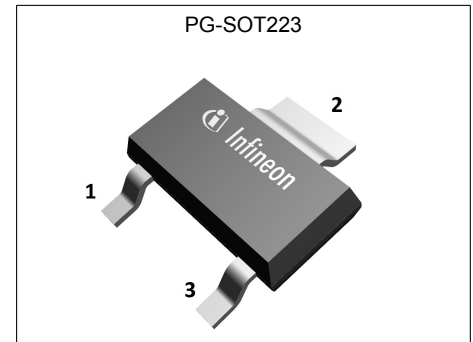
- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

#### Potential applications

Recommended for flyback topologies for LED Lighting, low power Chargers and Adapters, Smart Meter, AUX power and Industrial power. Also suitable for PFC stage in Consumer and Solar applications.

**Product Validation:** Fully qualified acc. JEDEC for Industrial Applications

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_J=25^{\circ}C$	950	V
$R_{DS(on),max}$	2	$\Omega$
$Q_{g,typ}$	10	nC
$I_D$	4	A
$E_{oss} @ 500V$	0.9	$\mu J$
$V_{GS(th),typ}$	3	V
ESD class (HBM)	2	-

Type / Ordering Code	Package	Marking	Related Links
IPN95R2K0P7	PG-SOT223	95R2K0	see Appendix A

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	4
Electrical characteristics .....	5
Electrical characteristics diagrams .....	7
Test Circuits .....	11
Package Outlines .....	12
Appendix A .....	13
Revision History .....	14
Trademarks .....	14
Disclaimer .....	14

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	4 2.4	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	10	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	6	mJ	$I_D=0.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.08	mJ	$I_D=0.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Application (Flyback) relevant avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	2.0	-	A	measured with standard leakage inductance of transformer of $10\mu\text{H}$
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{Hz}$ )
Power dissipation	$P_{tot}$	-	-	7	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	$I_S$	-	-	1.1	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	10	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>4)</sup>	dv/dt	-	-	1	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 0.8\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>F</sub> /dt	-	-	50	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 0.8\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.5$ ; IPAK equivalent.

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> For further explanation please read AN - CoolMOS™ 700V P7 & 950V P7

<sup>4)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	18.29	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	160	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	75	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	950	-	-	V	$V_{GS}=0\text{V}$ , $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	$V_{DS}=V_{GS}$ , $I_D=0.08\text{mA}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=950\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $V_{DS}=950\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	1000	nA	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.71 3.817	2	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=1.7\text{A}$ , $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$ , $I_D=1.7\text{A}$ , $T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	1	-	$\Omega$	$f=250\text{kHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	330	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	5	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	8	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	81	-	pF	$I_D=\text{constant}$ , $V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=1.7\text{A}$ , $R_G=23.1\Omega$ ; see table 9
Rise time	$t_r$	-	13	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=1.7\text{A}$ , $R_G=23.1\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	41	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=1.7\text{A}$ , $R_G=23.1\Omega$ ; see table 9
Fall time	$t_f$	-	18	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=1.7\text{A}$ , $R_G=23.1\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	2	-	nC	$V_{DD}=760\text{V}$ , $I_D=1.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	3	-	nC	$V_{DD}=760\text{V}$ , $I_D=1.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	10	-	nC	$V_{DD}=760\text{V}$ , $I_D=1.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=760\text{V}$ , $I_D=1.7\text{A}$ , $V_{GS}=0$ to $10\text{V}$

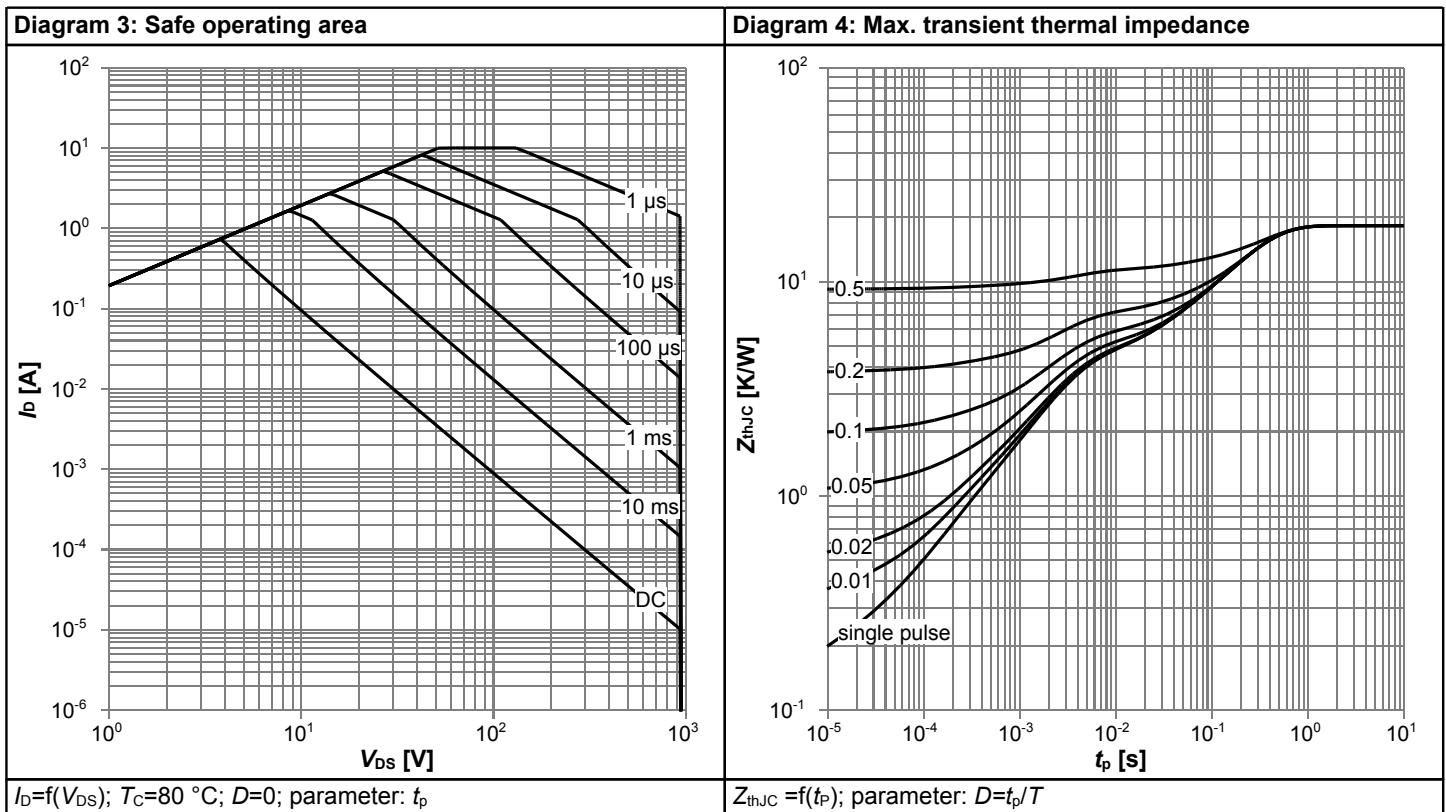
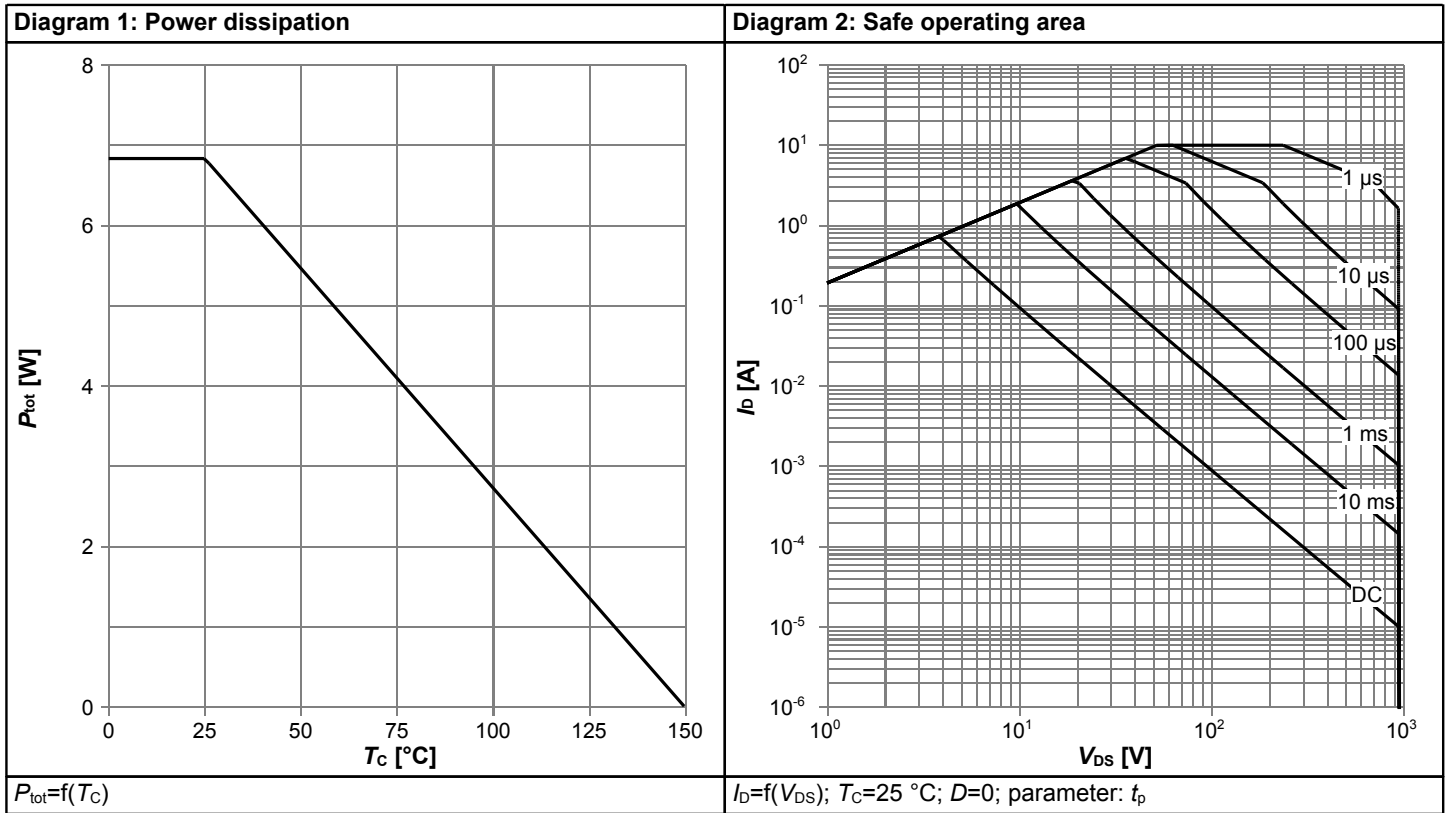
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

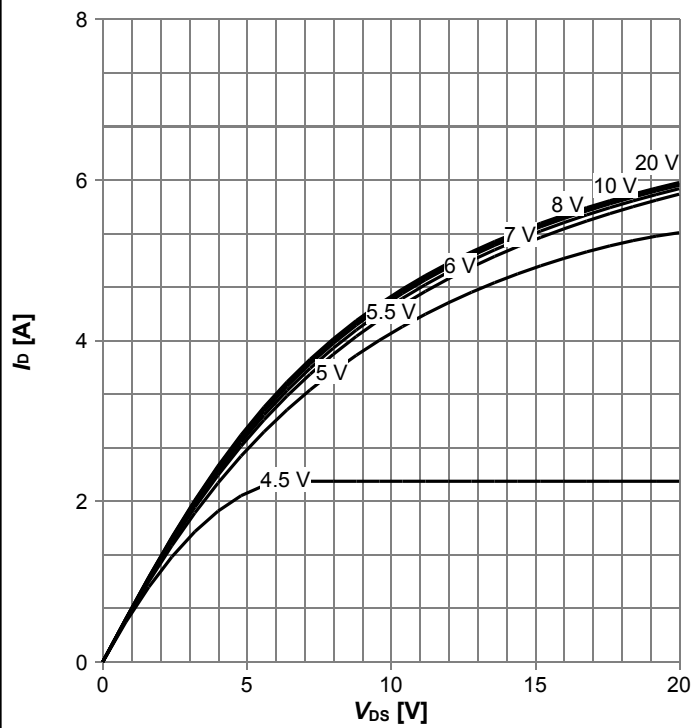
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=1.7A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	337	-	ns	$V_R=400V, I_F=0.8A, di_F/dt=50A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	2	-	$\mu C$	$V_R=400V, I_F=0.8A, di_F/dt=50A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	9	-	A	$V_R=400V, I_F=0.8A, di_F/dt=50A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

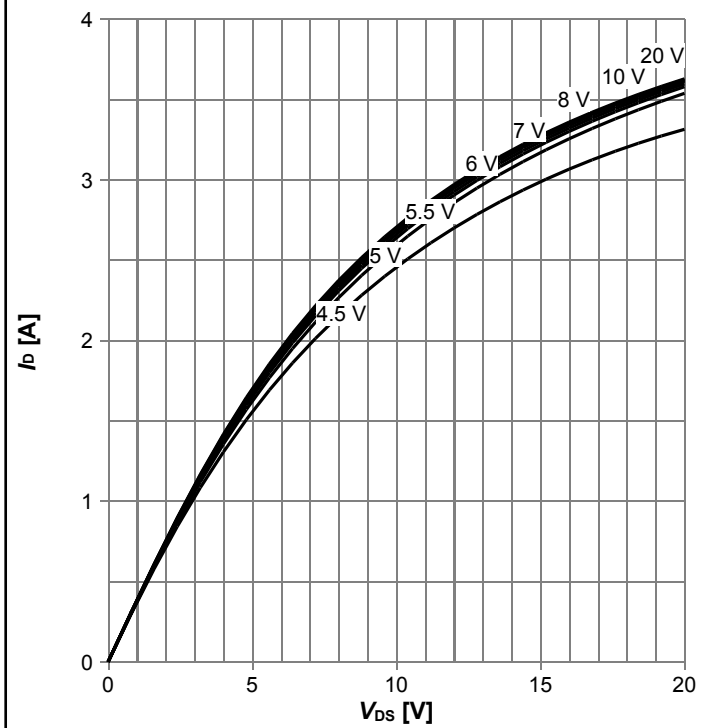


**Diagram 5: Typ. output characteristics**



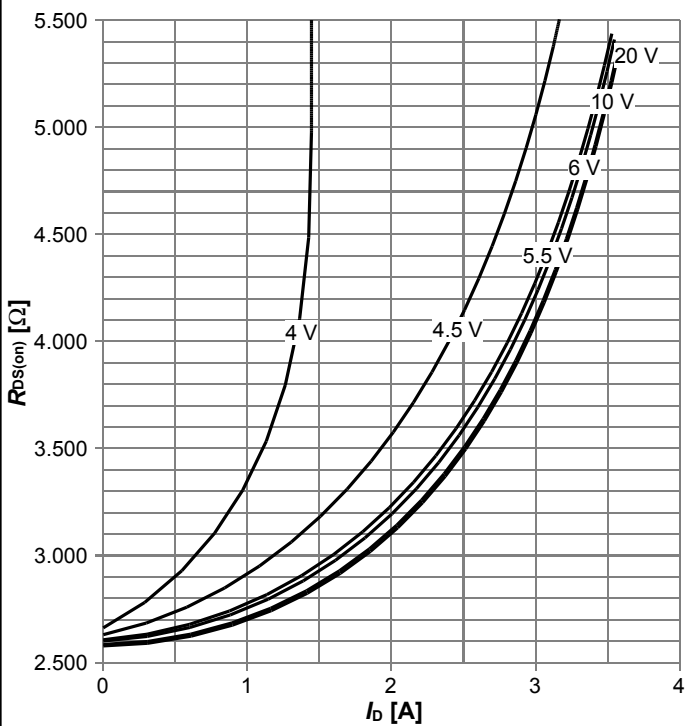
$I_D=f(V_{DS}); T_j=25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. output characteristics**



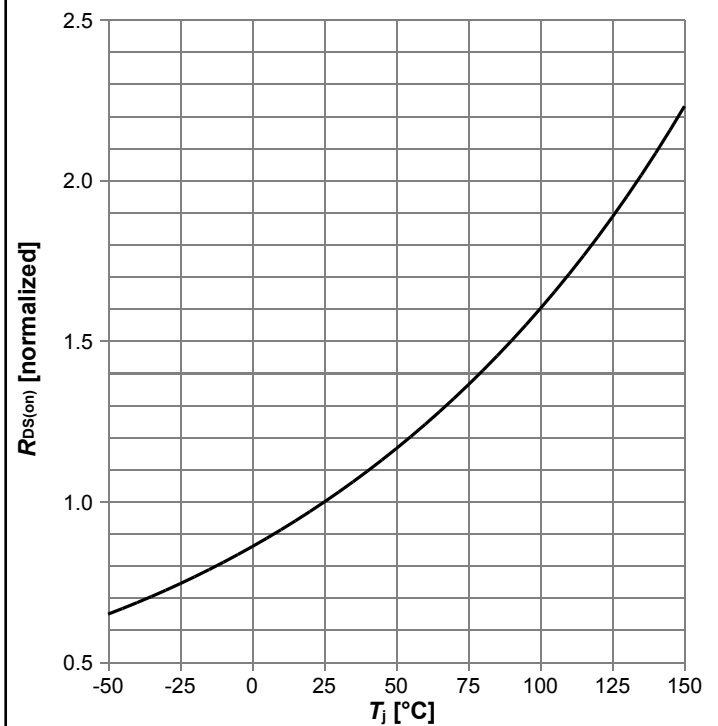
$I_D=f(V_{DS}); T_j=125\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)}=f(I_D); T_j=125\text{ °C};$  parameter:  $V_{GS}$

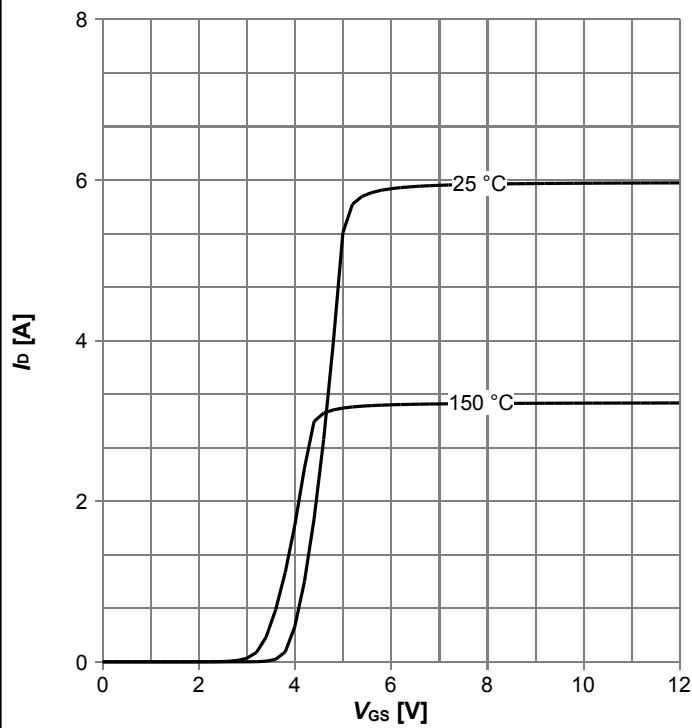
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)}=f(T_j); I_D=1.7\text{ A}; V_{GS}=10\text{ V}$

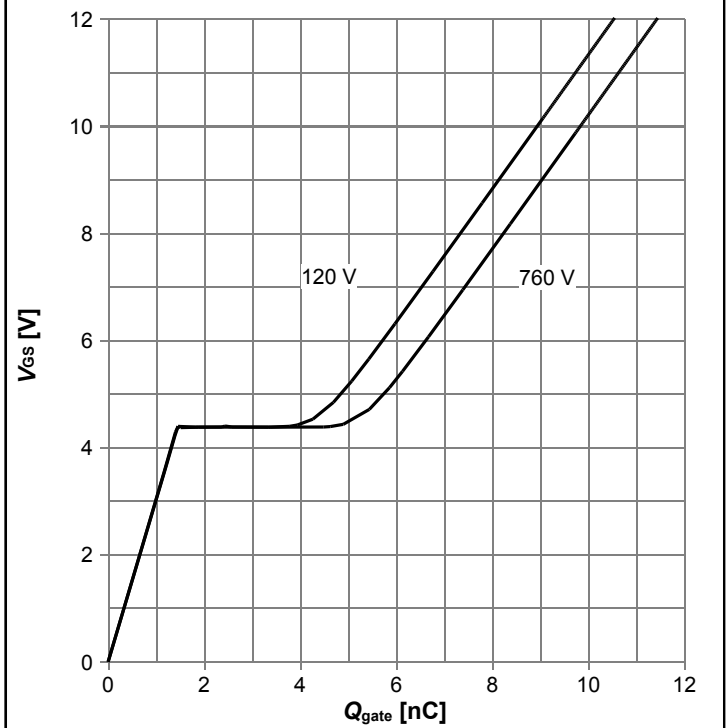


Diagram 9: Typ. transfer characteristics



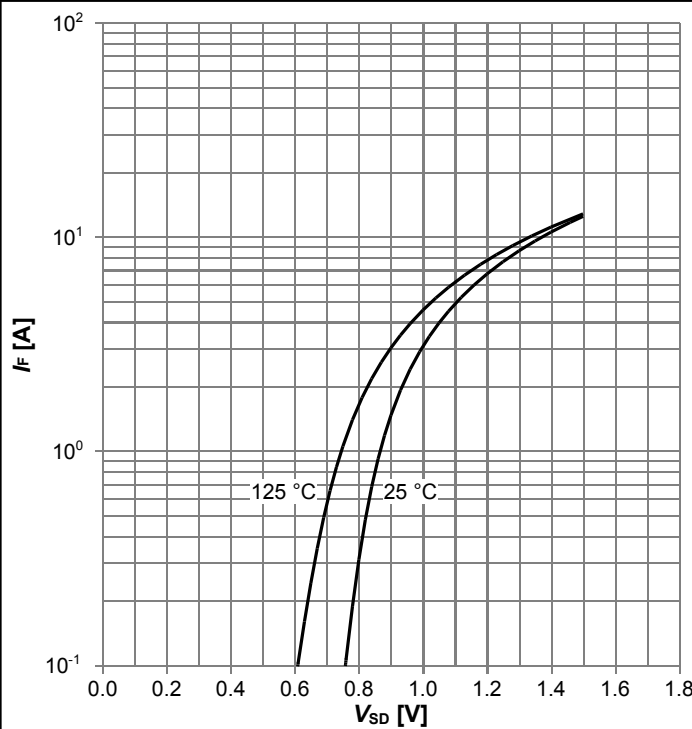
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



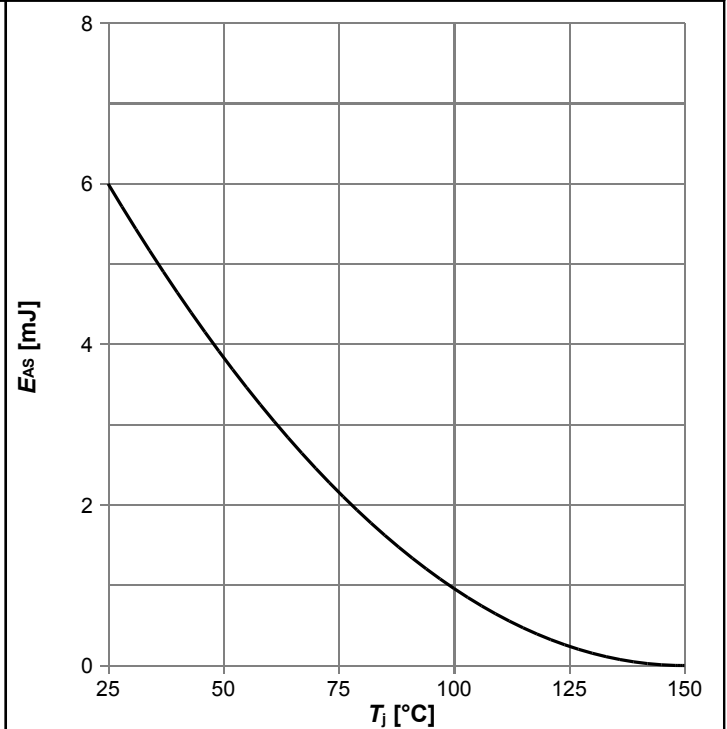
$V_{GS}=f(Q_{gate}); I_D=1.7 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



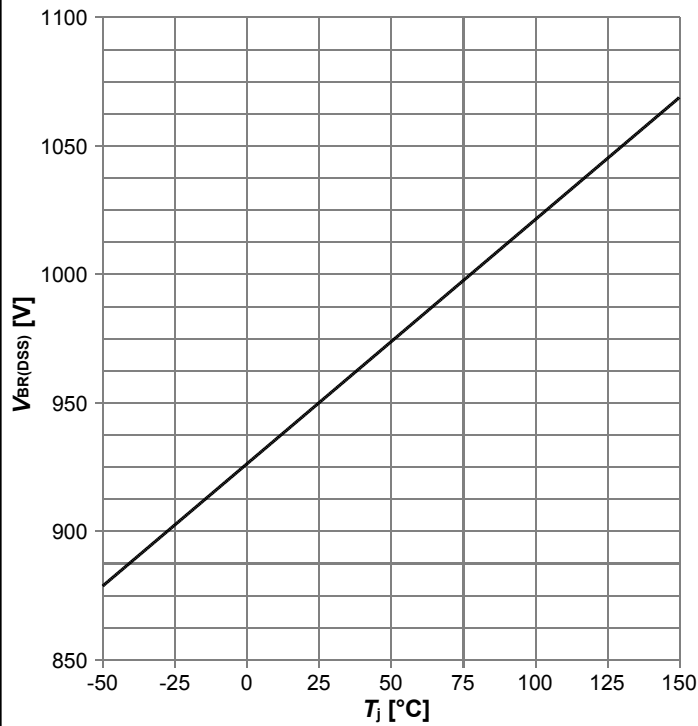
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



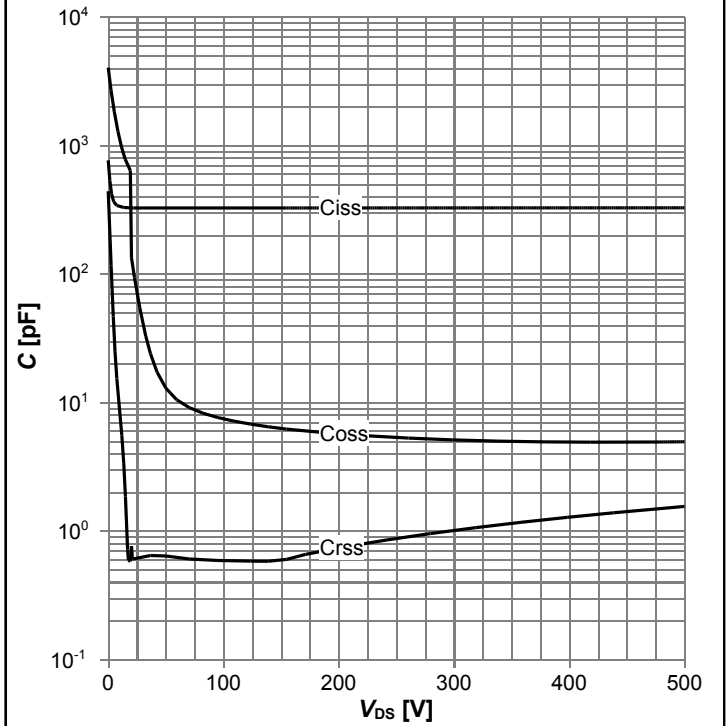
$E_{AS}=f(T_j); I_D=0.4 \text{ A}; V_{DD}=50 \text{ V}$

**Diagram 13: Drain-source breakdown voltage**



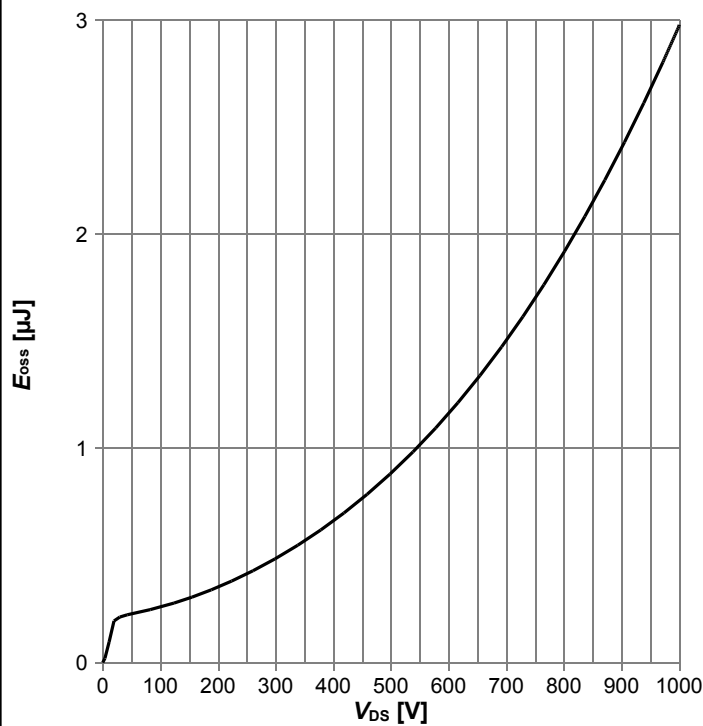
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

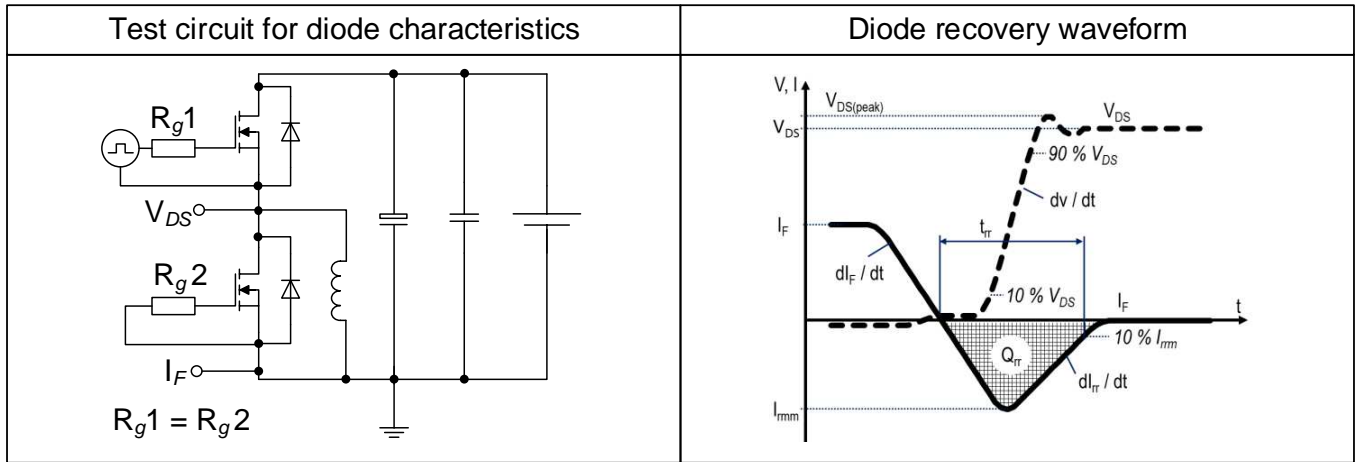
**Diagram 15: Typ. Coss stored energy**



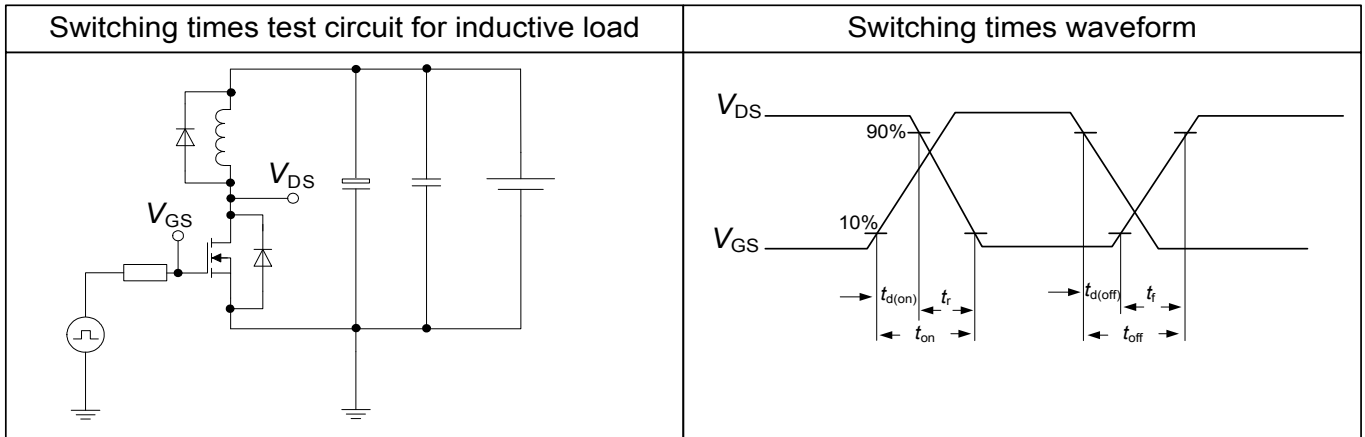
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

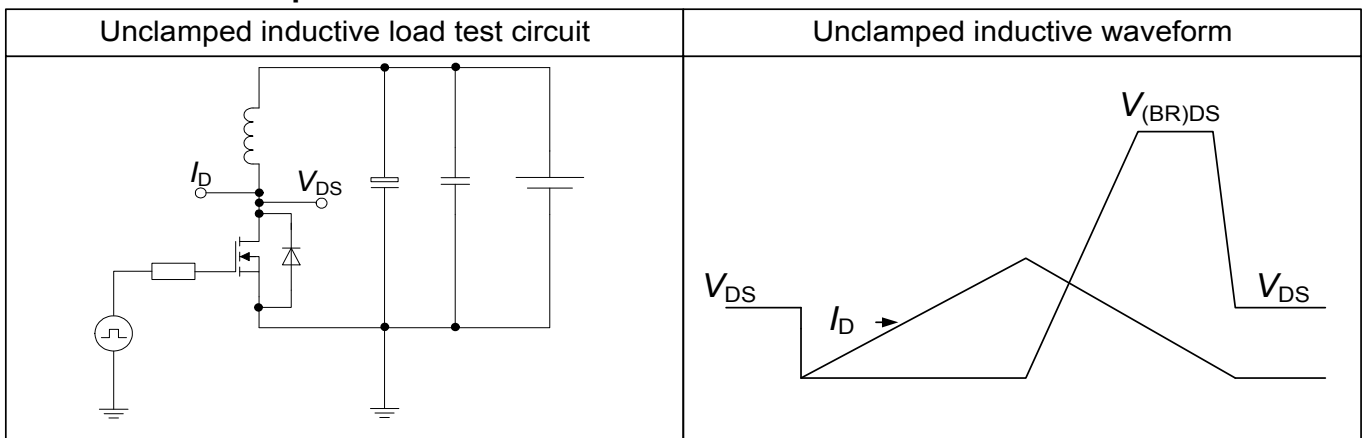
**Table 8 Diode characteristics**



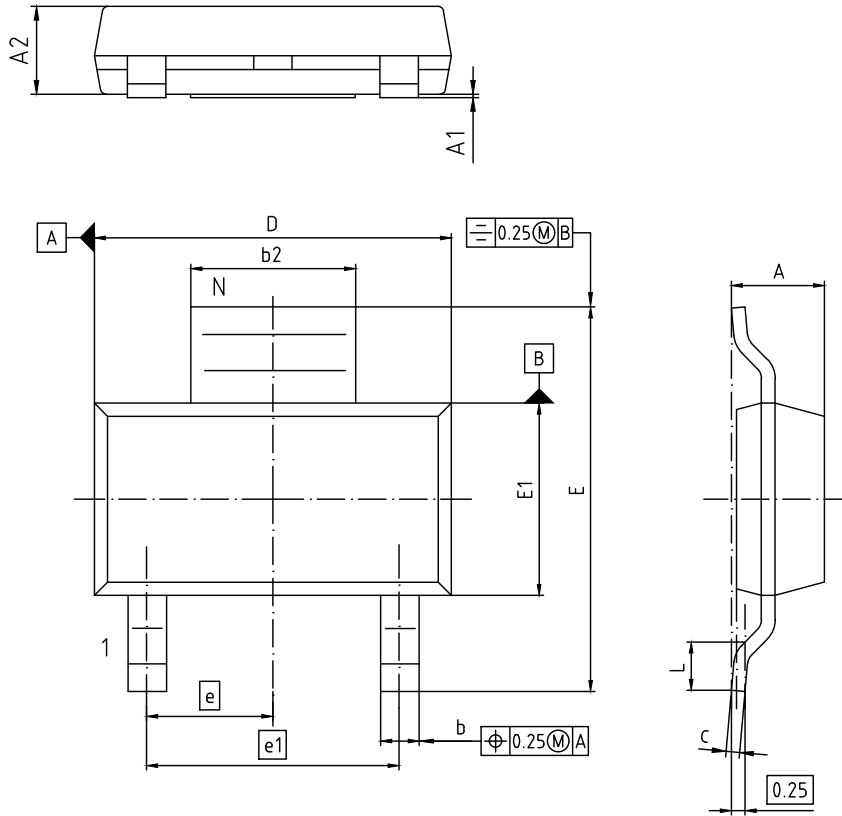
**Table 9 Switching times**



**Table 10 Unclamped inductive load**



## 6 Package Outlines



NOTES:  
1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

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Figure 1 Outline PG-SOT223, dimensions in mm/inches

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS P7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS P7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS P7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPN95R2K0P7

**Revision: 2018-06-01, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-06-01	Release of final version

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