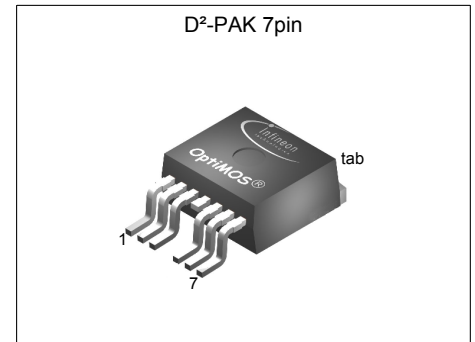


# MOSFET

## OptiMOS™ 5 Linear FET, 100 V

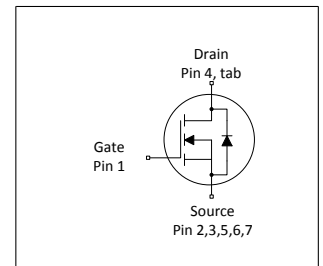
### Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance  $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	100	V
$R_{DS(on),max}$	1.7	m $\Omega$
$I_D$ (silicon limited)	314	A
$I_D$ (package limited)	180	A
$I_{pulse}$ ( $V_{DS}=56$ V, $t_p=10$ ms)	10.2	A



Type / Ordering Code	Package	Marking	Related Links
IPB017N10N5LF	PG-TO 263-7	017N10LF	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	180	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ , $R_{thJA}=40\text{ K/W}^{(1)}$
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	-	-	720	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>(3)</sup>	$E_{AS}$	-	-	979	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	313	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.25	0.4	K/W	-
Device on PCB, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>(1)</sup>	$R_{thJA}$	-	-	40	K/W	-

<sup>(1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>(2)</sup> See Diagram 3 for more detailed information

<sup>(3)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3.3	4.1	V	$V_{DS}=V_{GS}$ , $I_D=270\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	1 10	10 100	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	2 -2	5 -5	$\mu\text{A}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$ $V_{GS}=-10\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.5	1.7	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	44	66	$\Omega$	-
Transconductance	$g_{fs}$	32	63	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=100\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	650	840	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	1900	2500	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	25	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.7\text{ }\Omega$
Rise time	$t_r$	-	28	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.7\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	128	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.7\text{ }\Omega$
Fall time	$t_f$	-	82	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.7\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	4.4	-	nC	$V_{DD}=50\text{ V}$ , $I_D=180\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	141	-	nC	$V_{DD}=50\text{ V}$ , $I_D=180\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	195	-	nC	$V_{DD}=50\text{ V}$ , $I_D=180\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	7.1	-	V	$V_{DD}=50\text{ V}$ , $I_D=180\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	209	-	nC	$V_{DD}=50\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	180	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	720	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.86	1.2	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	62	-	ns	$V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	113	-	nC	$V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

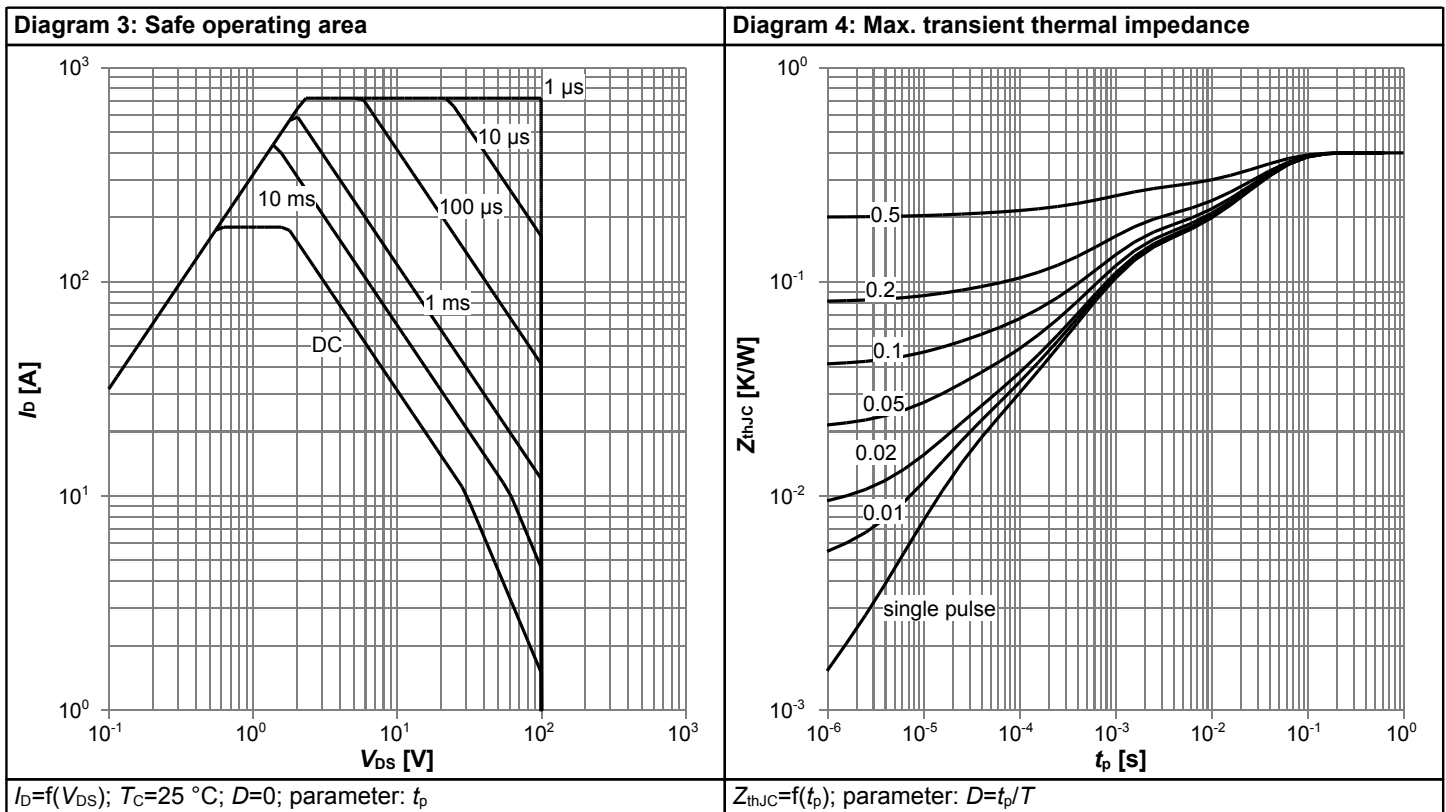
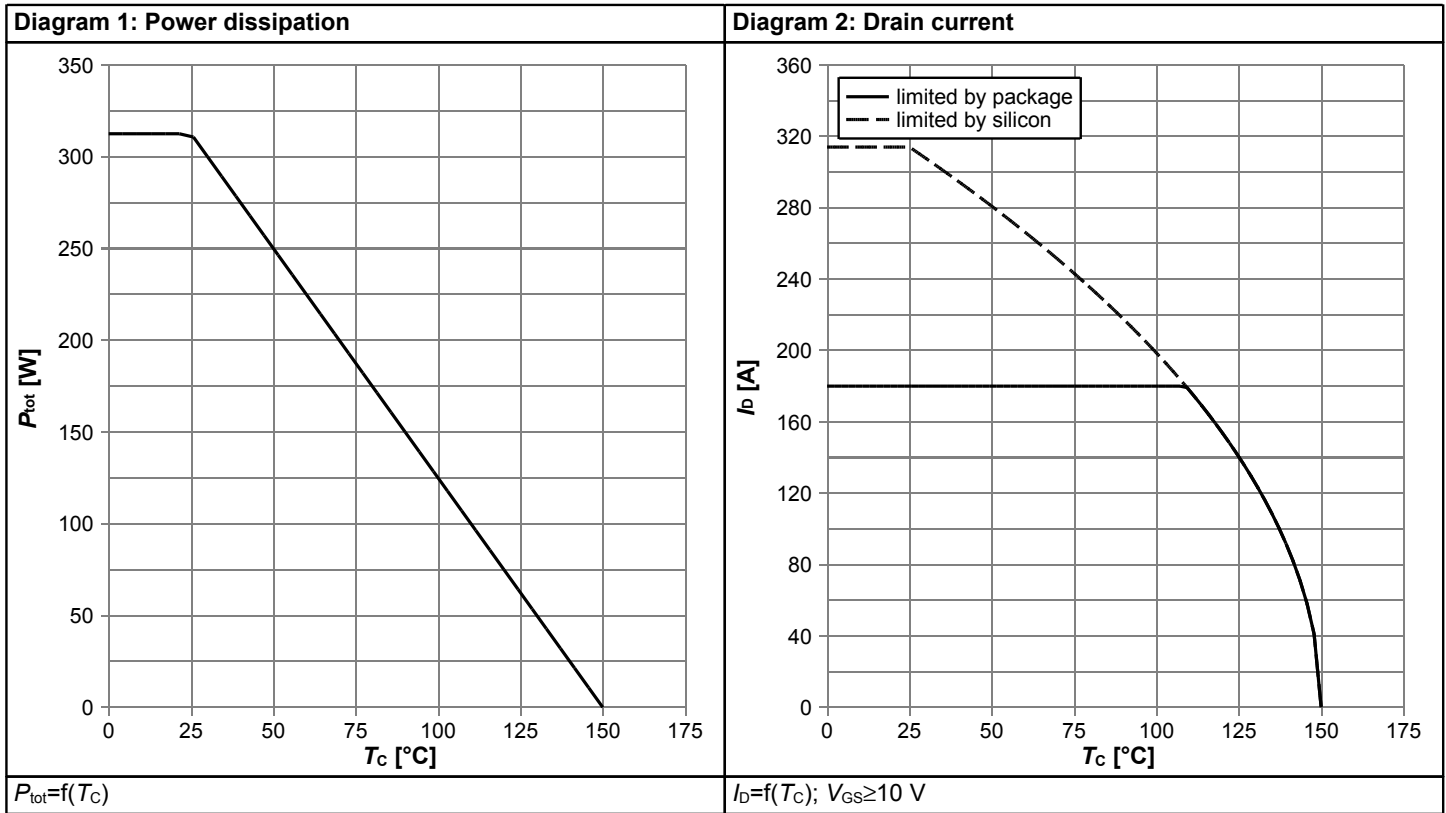
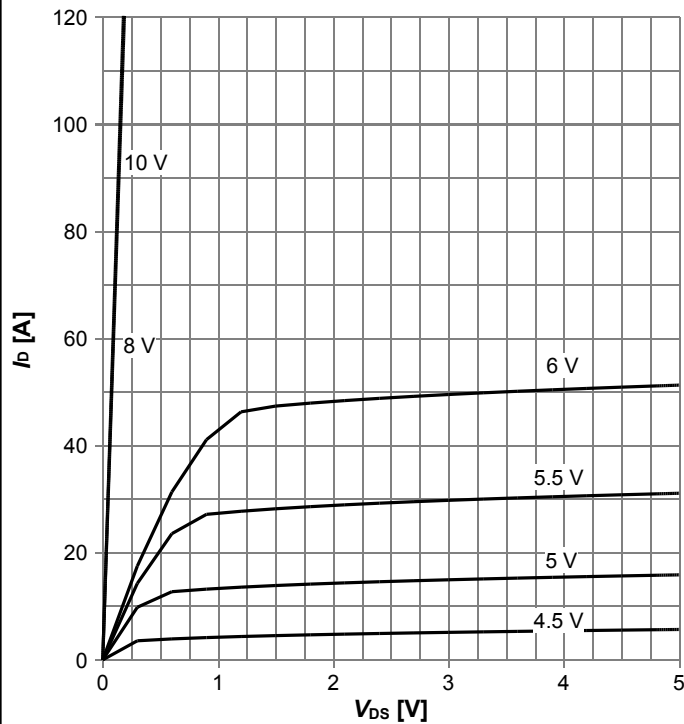
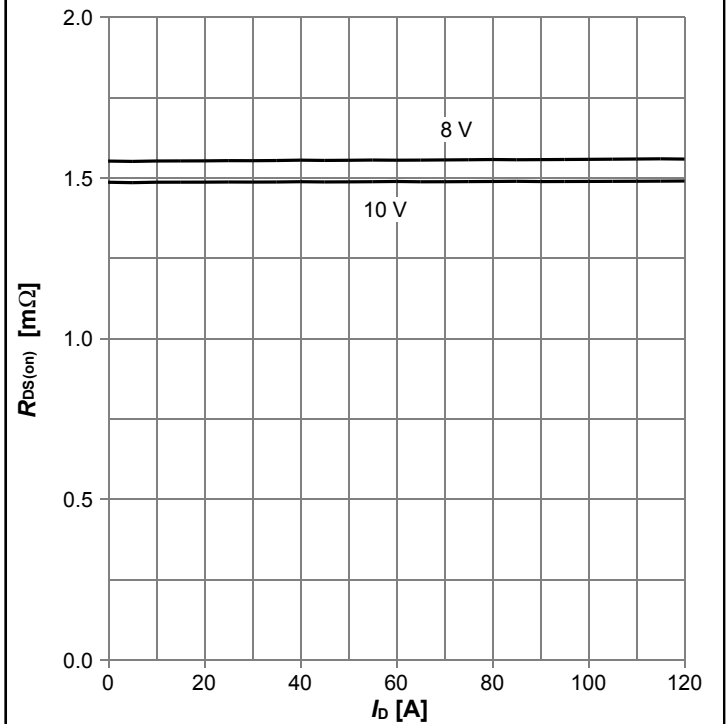


Diagram 5: Typ. output characteristics



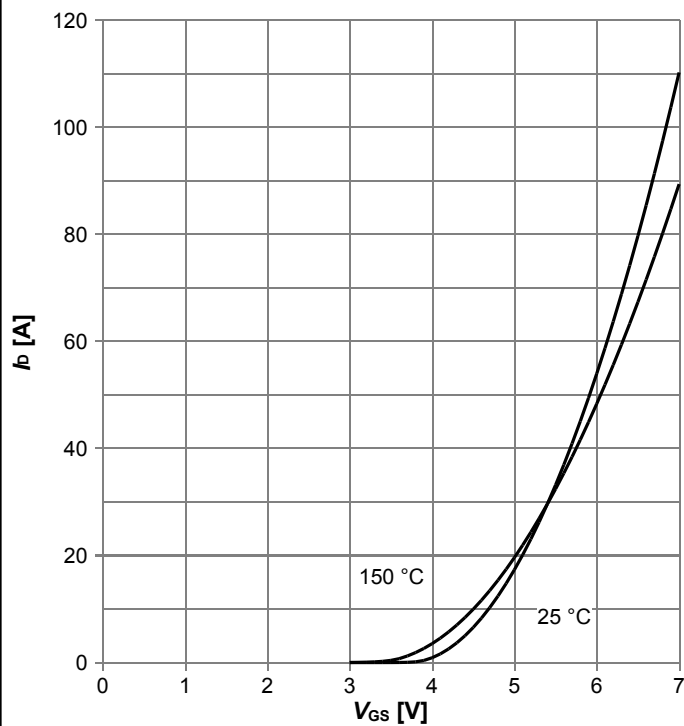
$I_D = f(V_{DS}); T_j = 25\text{ °C}, t_p = 30\text{ }\mu\text{s};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



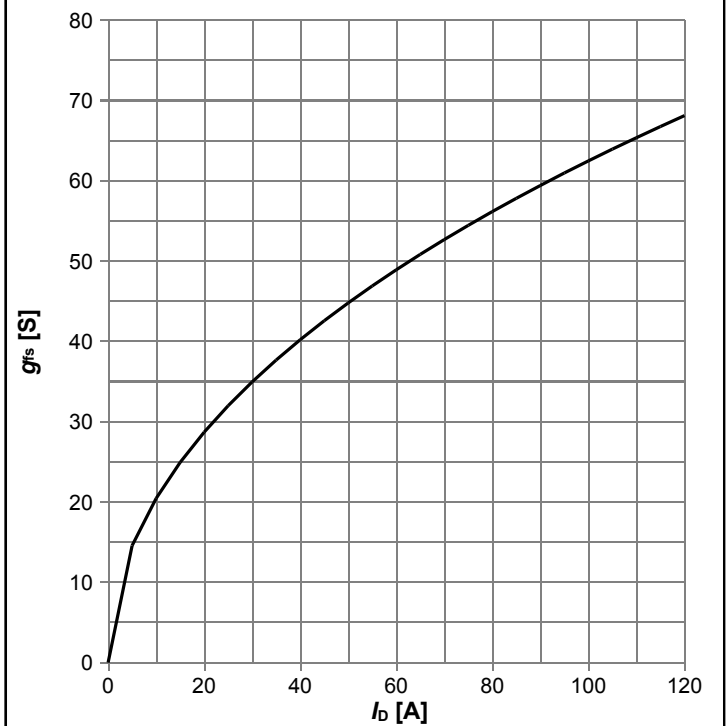
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



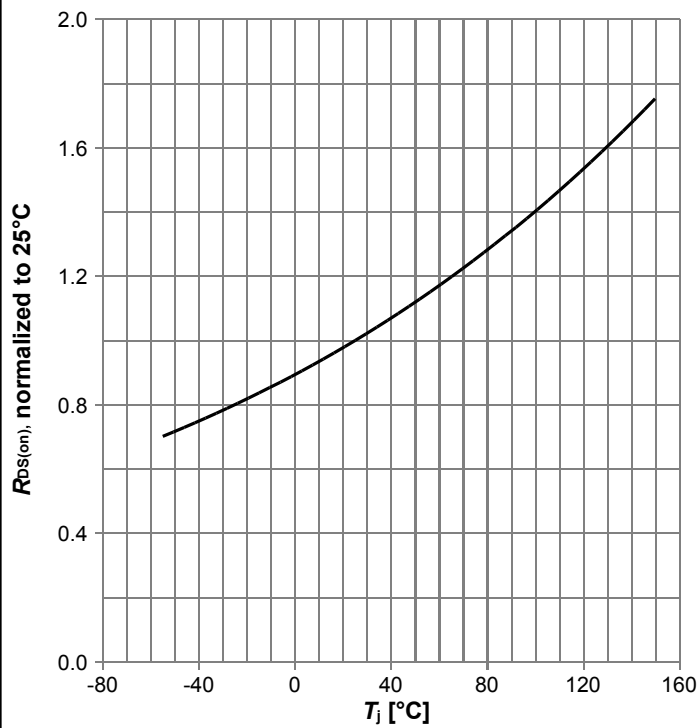
$I_D = f(V_{GS}); V_{DS} = 10\text{ V};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



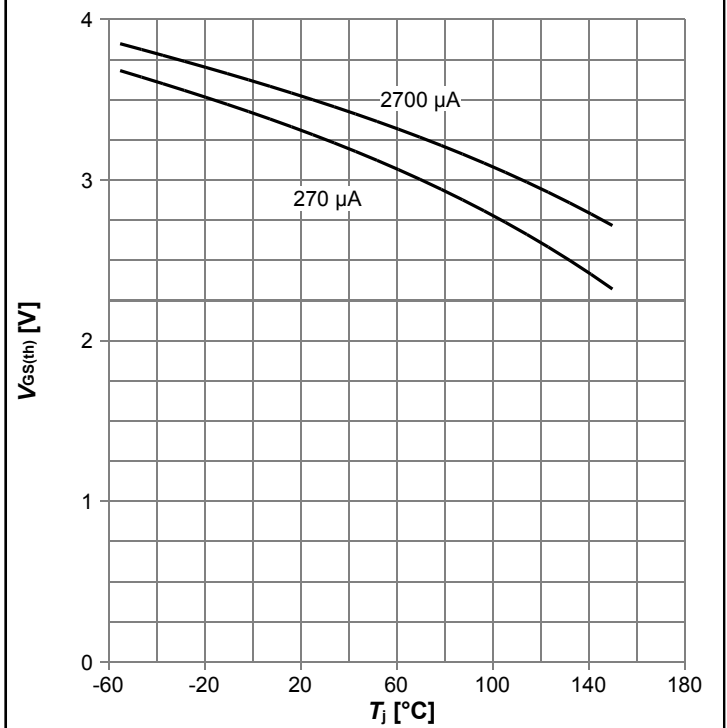
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Normalized drain-source on-state resistance



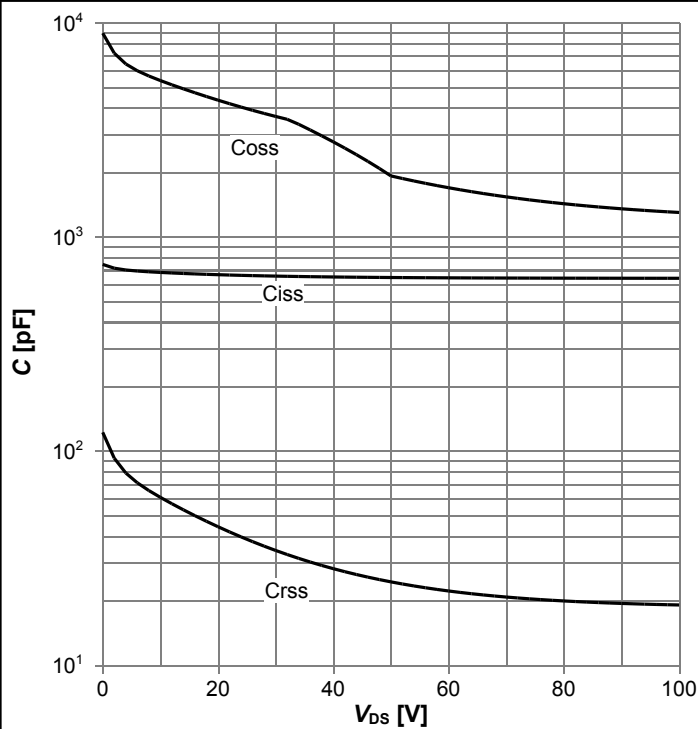
$R_{DS(on)}=f(T_j)$ ;  $I_D=100$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



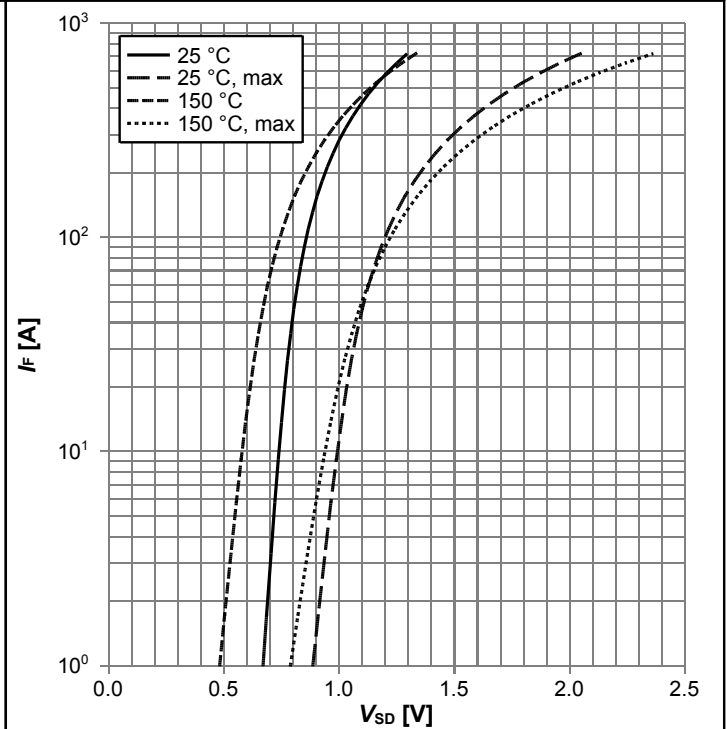
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

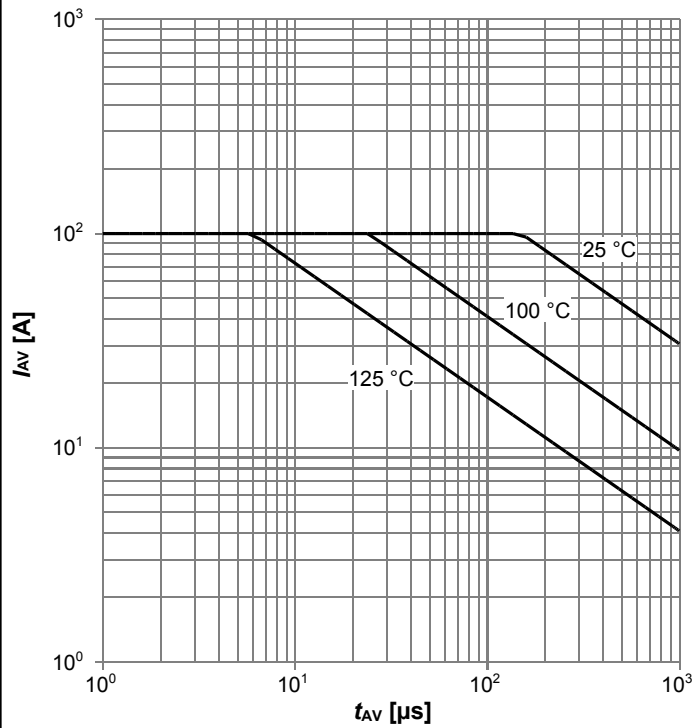
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

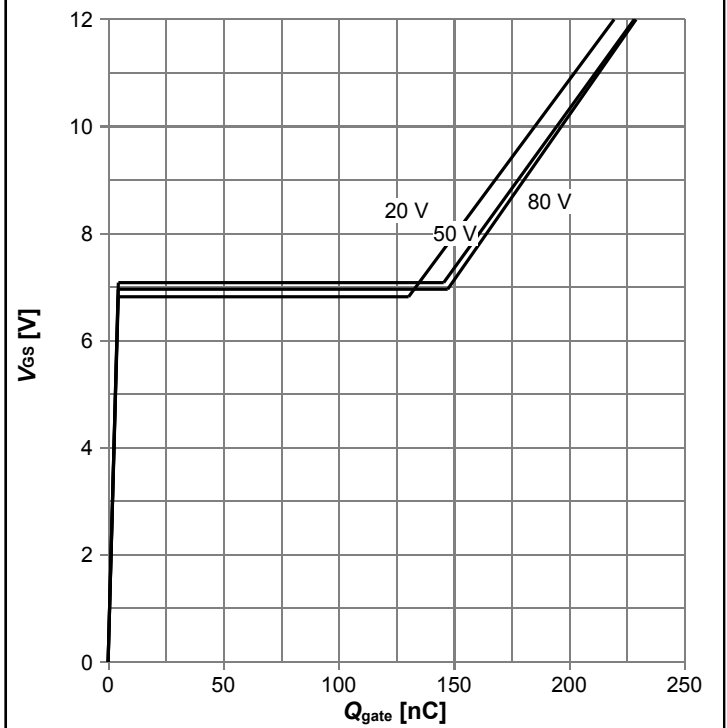


**Diagram 13: Avalanche characteristics**



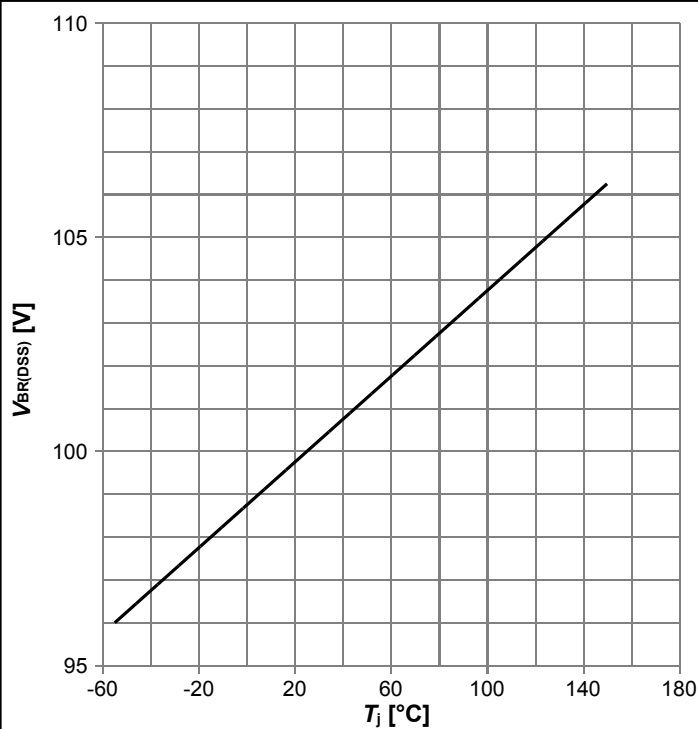
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



$V_{GS}=f(Q_{gate}); I_D=180 \text{ A}$  pulsed, resistive load; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

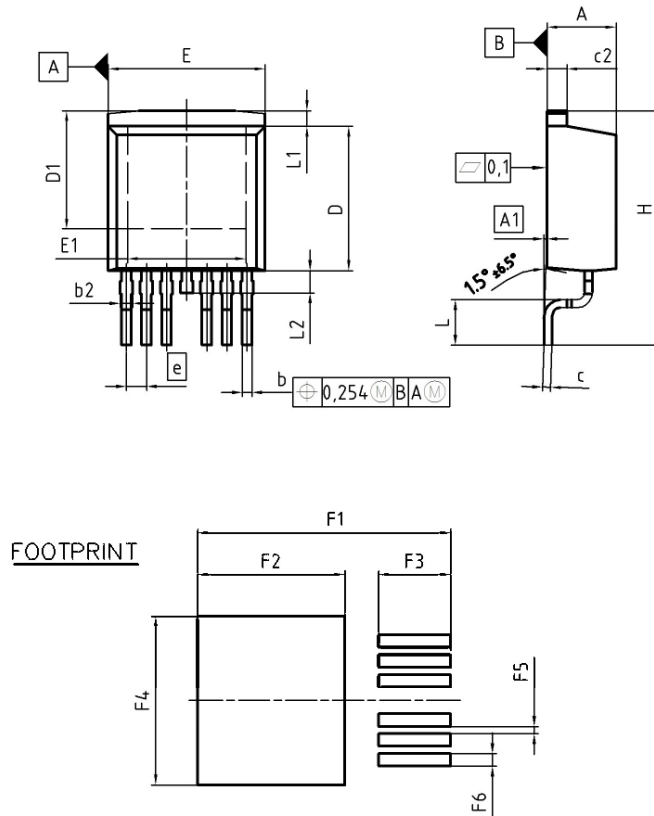


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



## 5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.50	0.70	0.020	0.028
b2	0.50	1.00	0.020	0.039
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	6.90	7.90	0.272	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	1.27		0.050	
N	6		6	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	0.37	0.57	0.015	0.022
F6	0.70	0.90	0.028	0.035

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REVISION  
01

Figure 1 Outline PG-TO 263-7, dimensions in mm/inches

## Revision History

IPB017N10N5LF

**Revision: 2017-02-16, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-12-15	Release of final version
2.1	2017-02-16	Update technology heading

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