INA818 35-µV Offset, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier

1 Features

- Low offset voltage: 10 µV (typ), 35 µV (max)
- Gain drift: 5 ppm/°C (G = 1), 35 ppm/°C (G > 1) (max)
- Noise: 8 nV/√Hz
- Bandwidth: 2 MHz (G = 1), 270 kHz (G = 100)
- Stable with 1-nF capacitive loads
- Inputs protected up to ±60 V
- Common-mode rejection: 110 dB, G = 10 (min)
- Power supply rejection: 100 dB, G = 1 (min)
- Supply current: 385 µA (max)
- Supply voltage range:
  - Single supply: 4.5 V to 36 V
  - Dual supply: ±2.25 V to ±18 V
- Specified temperature: –40°C to +125°C
- Package: 8-Pin SOIC

2 Applications

- Industrial process control
- Circuit breakers
- Battery testers
- ECG amplifiers
- Power automation
- Medical instrumentation
- Portable instrumentation

3 Description

The INA818 is a high-precision instrumentation amplifier that offers low power consumption and operates over a very wide single-supply or dual-supply range. A single external resistor sets any gain from 1 to 1000. The device offers high precision as a result of super-beta input transistors, which provide exceptionally low input offset voltage, offset voltage drift, input bias current, input voltage, and current noise. Additional circuitry protects the inputs against overvoltage up to ±60 V.

The INA818 is optimized to provide a high common-mode rejection ratio. At G = 1, the common-mode rejection ratio exceeds 90 dB across the full input common-mode range. The device is designed for low-voltage operation from a 4.5-V single supply, as well as dual supplies up to ±18 V.

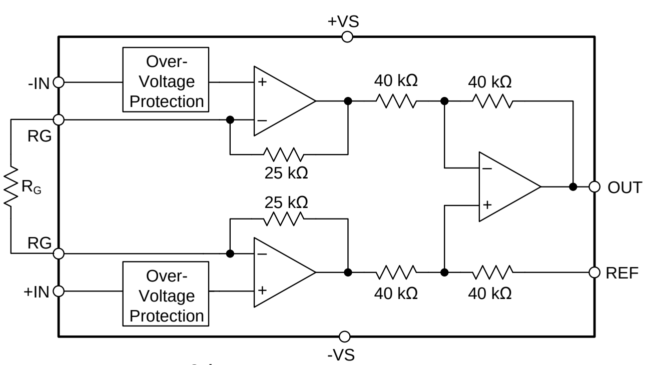
The INA818 is available in an 8-pin SOIC package and is specified over the –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA818	SOIC (8)	4.90 mm × 3.91 mm

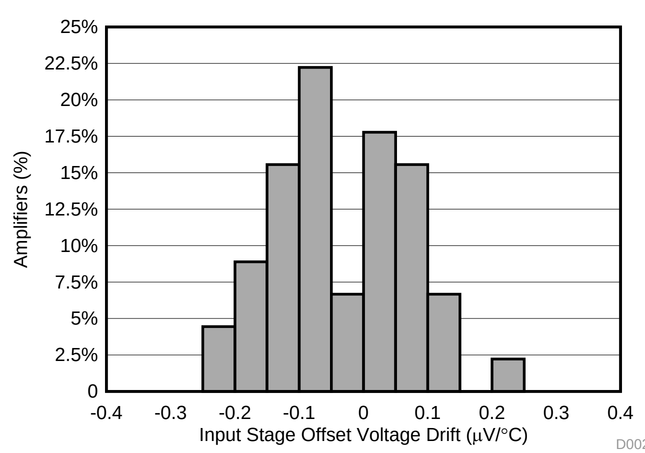
(1) For all available packages, see the package option addendum at the end of the data sheet.

INA818 Simplified Internal Schematic



$$G = 1 + \frac{50\ k\Omega}{R_G} \qquad V_O = G(V_{+IN} - V_{-IN}) + V_{REF}$$

Typical Distribution of Input Stage Offset Voltage Drift



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4 Revision History

DATE	REVISION	NOTES
April 2019	*	Initial release.

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5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA819	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	2, 3
INA821	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-µV Offset, 0.5 µV/°C V_{OS} Drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} Drift, 1.8-V to 5-V, RRO, 50-µA I_Q, Chopper-Stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion	G = 0.2 V/V	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

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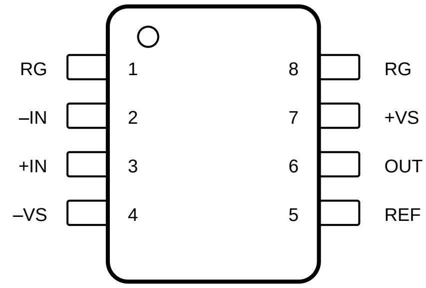
6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	2	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
OUT	6	O	Output
REF	5	I	Reference input. This pin must be driven by a low-impedance source.
RG	1, 8	—	Gain setting pin. Place a gain resistor between pin 1 and pin 8.
–VS	4	—	Negative supply
+VS	7	—	Positive supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage dual supply, V_S = (V+) – (V–)		±20	V
Supply voltage single supply, V_S = (V+) – (V–)		40, (single supply)	V
Signal input pins	–60	60	V
VREF pin	–20	20	V
Signal output pins maximum voltage	$(-V_S) - 0.5$	$(+V_S) + 0.5$	V
Signal output pins maximum current	-50	50	mA
Output short-circuit(2)	Continuous		
Operating Temperature, T_A	–50	150	°C
Junction Temperature, T_J		175	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S	Single-supply	4.5	36	V
	Dual-supply	±2.25	±18	
Specified temperature	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA818 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{OSI}	Input stage offset voltage(1)(2)			10	35	µV
		T_A = –40°C to 125°C(3)			75	µV
		drift vs temperature, T_A = –40°C to 125°C			0.4	µV/°C
V_{OSO}	Output stage offset voltage(1)(2)			50	300	µV
		T_A = –40°C to 125°C(3)			800	µV
		drift vs temperature, T_A = –40°C to 125°C			5	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI	110	120		dB
		G = 10, RTI	114	130		
		G = 100, RTI	130	135		
		G = 1000, RTI	136	140		
z_{id}	Differential impedance			100 || 1		GΩ || pF
z_{ic}	Common-mode impedance			100 || 4		GΩ || pF
	RFI filter, –3-dB frequency			32		MHz
V_{CM}	Operating input range(4)		(V–) + 2		(V+) – 2	V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C	See Figure 49 to Figure 52			
	Input overvoltage range	T_A = –40°C to 125°C(3)			±60	V
CMRR	Common-mode rejection ratio	At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1	90	105		dB
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 10	110	125		
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 100	130	145		
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1000	140	150		
BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		0.15	0.5	nA
		T_A = –40°C to 125°C			2	
I_{OS}	Input offset current	V_{CM} = V_S / 2		0.15	0.5	nA
		T_A = –40°C to 125°C			2	
NOISE VOLTAGE						
e_{NI}	Input stage voltage noise(5)	f = 1 kHz, G = 100, R_S = 0 Ω		8		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		0.19		$µV_{PP}$
e_{NO}	Output stage voltage noise(5)	f = 1 kHz, R_S = 0 Ω		80		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω		2.6		$µV_{PP}$
I_n	Noise current	f = 1 kHz		130		fA/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100		4.7		pA_{PP}
GAIN						
	Gain equation			1 + (50 kΩ / R_G)		V/V
G	Gain		1		1000	V/V
GE	Gain error	G = 1, V_O = ±10 V		±0.005%	±0.025%	
		G = 10, V_O = ±10 V		±0.025%	±0.15%	
		G = 100, V_O = ±10 V		±0.025%	±0.15%	
		G = 1000, V_O = ±10 V		±0.05%		
	Gain error drift(6)	G = 1, T_A = –40°C to 125°C, V_O = ±10 V			±5	ppm/°C
		G > 1, T_A = –40°C to 125°C, V_O = ±10 V			±35	

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$
(3) Specified by characterization.
(4) Input voltage range of the INA818 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves Figure 49 through Figure 52 for more information.
(5) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$
(6) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain nonlinearity	G = 1 to 10, V_O = –10 V to 10 V, R_L = 10 kΩ		1	10	ppm
		G = 100, V_O = –10 V to 10 V, R_L = 10 kΩ			15	
		G = 1000, V_O = –10 V to 10 V, R_L = 10 kΩ		10		
		G = 1 to 100, V_O = –10 V to 10 V, R_L = 2 kΩ		30		
OUTPUT						
	Voltage swing		(V–) + 0.15		(V+) – 0.15	V
	Load capacitance stability			1000		pF
Z_O	Closed-loop output impedance	f = 10 kHz		5.0		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±20		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		2.0		MHz
		G = 10		890		kHz
		G = 100		270		
		G = 1000		30		
SR	Slew rate	G = 1, V_O = ±10 V		0.9		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 10 V		12		µs
		0.01%, G = 1000, V_{STEP} = 10 V		40		
		0.001%, G = 1 to 100, V_{STEP} = 10 V		16		
		0.001%, G = 1000, V_{STEP} = 10 V		60		
REFERENCE INPUT						
R_{IN}	Input impedance			40		kΩ
	Voltage range		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
I_Q	Quiescent current	V_{IN} = 0 V		350	385	µA
		V_{IN} = 0 V, T_A = –40°C to 125°C			520	

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7.6 Typical Characteristics: Table of Graphs

Table 1. Table of Graphs

DESCRIPTION	FIGURE
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Output Stage Offset Voltage vs Temperature	Figure 6
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Small-Signal Response G = 100	Figure 43
Small-Signal Response G = 1000	Figure 44
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Typical Characteristics: Table of Graphs (continued)

Table 1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Differential-Mode EMI Rejection Ratio	Figure 47
Common-Mode EMI Rejection Ratio	Figure 48
Input Common-Mode Voltage vs Output Voltage G = 1, V_S = 5 V	Figure 49
Input Common-Mode Voltage vs Output Voltage G = 100, V_S = 5 V	Figure 50
Input Common-Mode Voltage vs Output Voltage V_S =±5 V	Figure 51
Input Common-Mode Voltage vs Output Voltage V_S =±15 V	Figure 52

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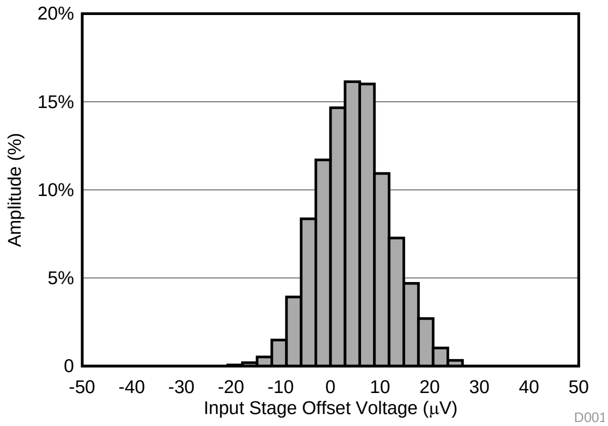
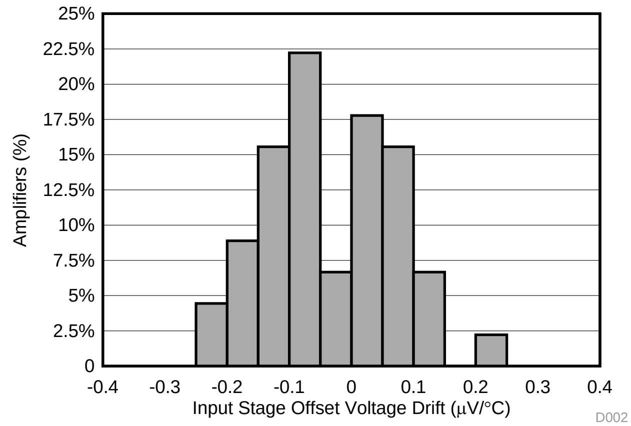
7.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



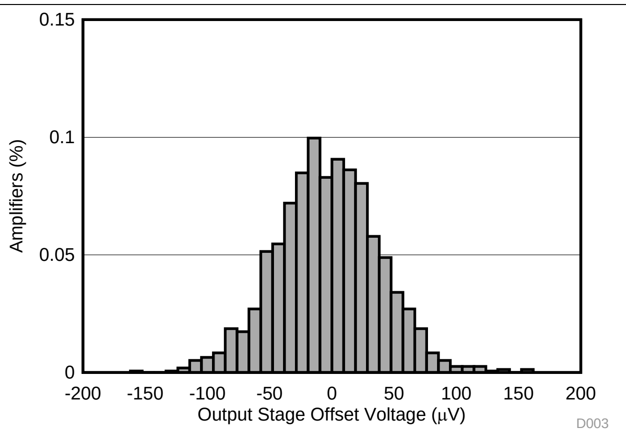
N = 1555 Mean = 4.71 μV Std. Dev. = 7.12 μV

Figure 1. Typical Distribution of Input Stage Offset Voltage



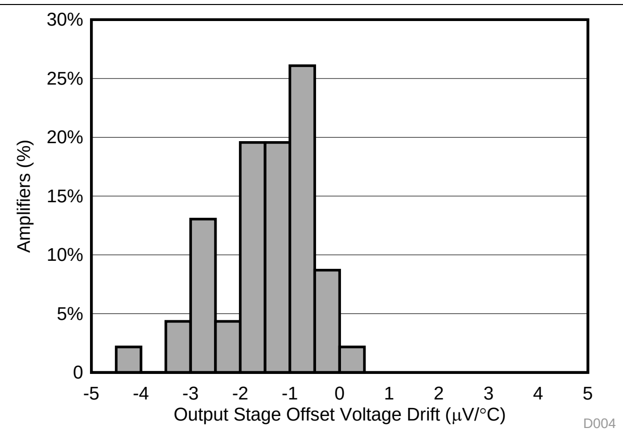
N = 45 Mean = 0.0357 μV/°C Std. Dev. = 0.099 μV/°C

Figure 2. Typical Distribution of Input Stage Offset Voltage Drift



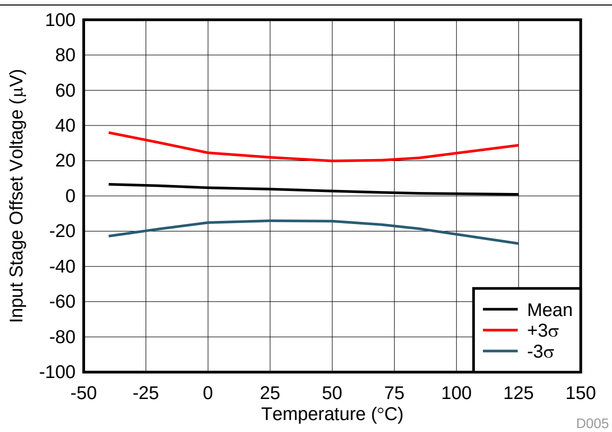
N = 1555 Mean = –3.18 μV Std. Dev. = 41.26 μV

Figure 3. Typical Distribution of Output Stage Offset Voltage



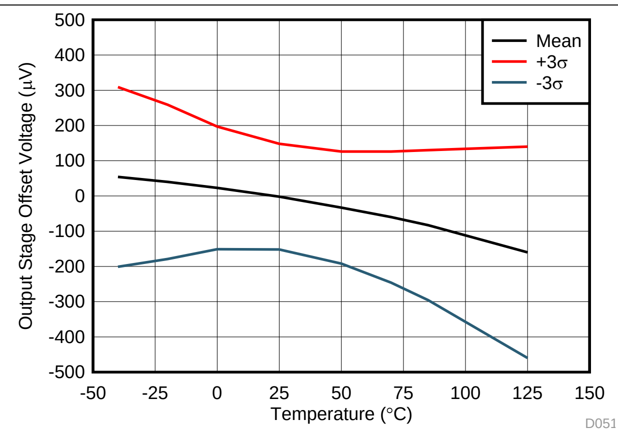
N = 45 Mean = –1.49 μV/°C Std. Dev. = 0.89 μV/°C

Figure 4. Typical Distribution of Output Stage Offset Voltage Drift



45 units, 1 wafer lot

Figure 5. Input Stage Offset Voltage vs Temperature

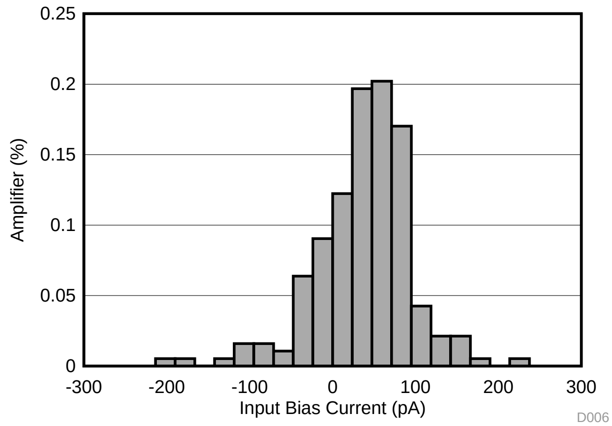


45 units, 1 wafer lots

Figure 6. Output Stage Offset Voltage vs Temperature

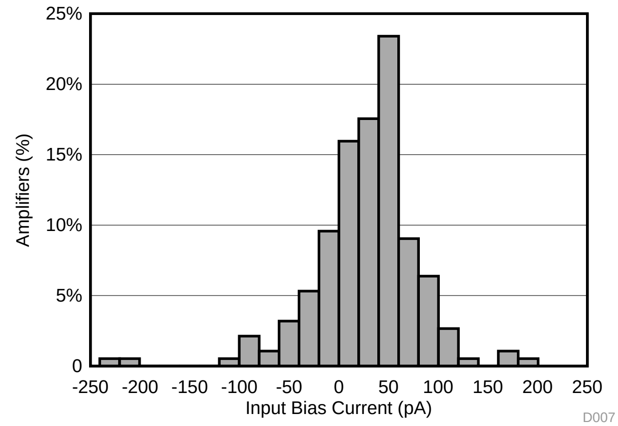
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



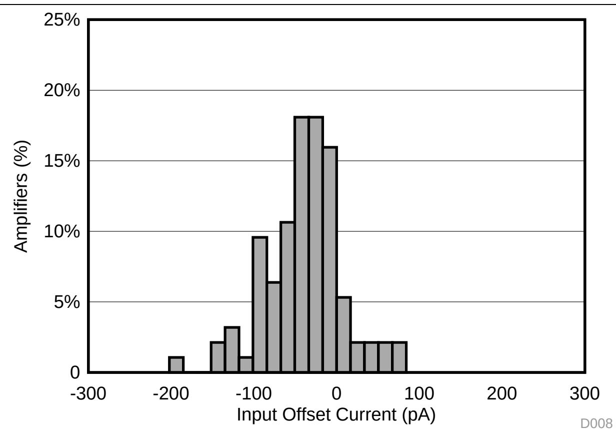
N = 94 Mean = 37.13 pA Std. Dev. = 57.65 pA
T_A = 25°C

Figure 7. Typical Distribution of Input Bias Current



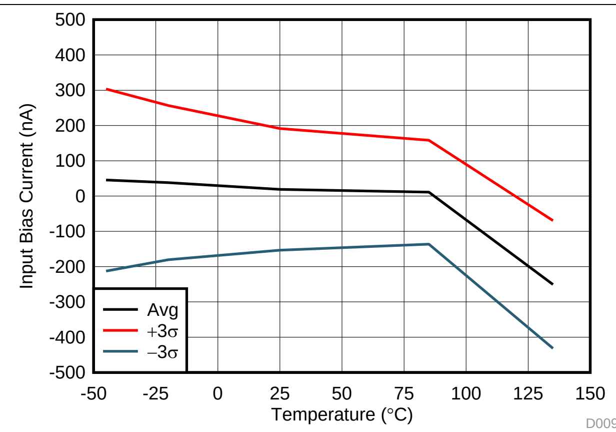
N = 94 Mean = –27.65 pA Std. Dev. = 52.58 pA
T_A = 90°C

Figure 8. Typical Distribution of Input Bias Current



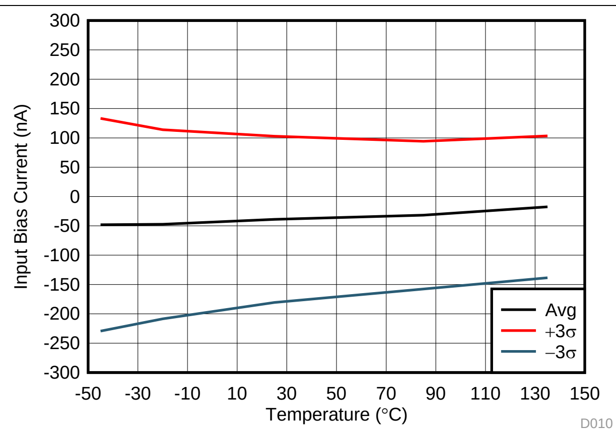
N = 94 Mean = –38.82 pA Std. Dev. = 47.24 pA

Figure 9. Typical Distribution of Input Offset Current



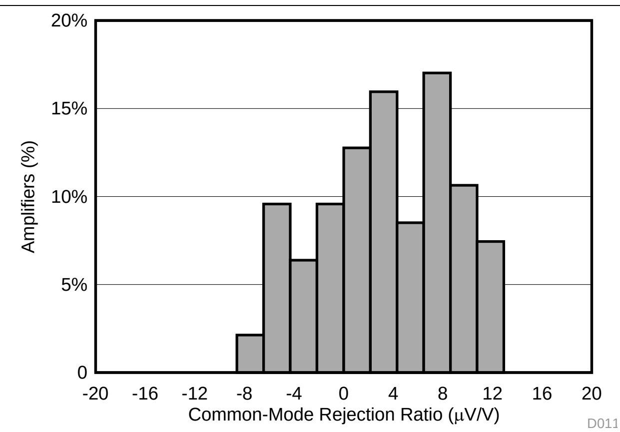
N = 94 G = 1

Figure 10. Input Bias Current vs Temperature



N = 94 G = 1

Figure 11. Input Offset Current vs Temperature



N = 94 Mean = 3.23 µV/V Std. Dev. = 5.38 µV/V
G = 1

Figure 12. Typical CMRR Distribution

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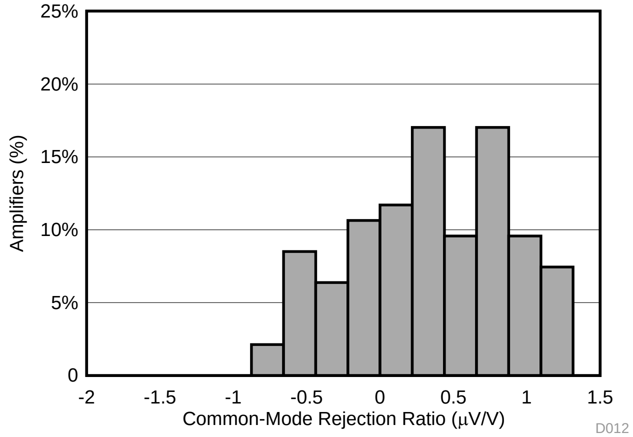
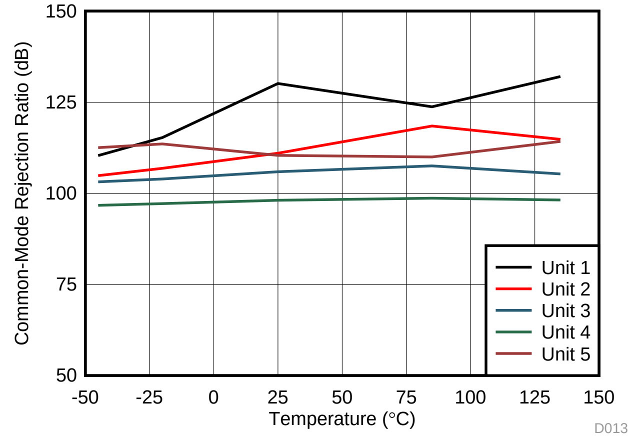
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



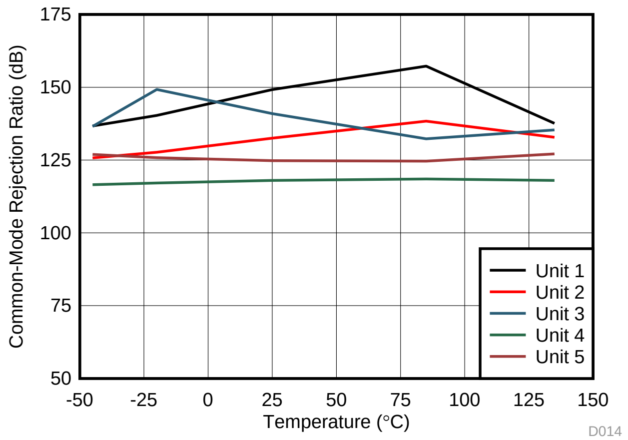
N = 94 Mean = 0.34 µV/V Std. Dev. = 0.54 µV/V
G = 10

Figure 13. Typical CMRR Distribution



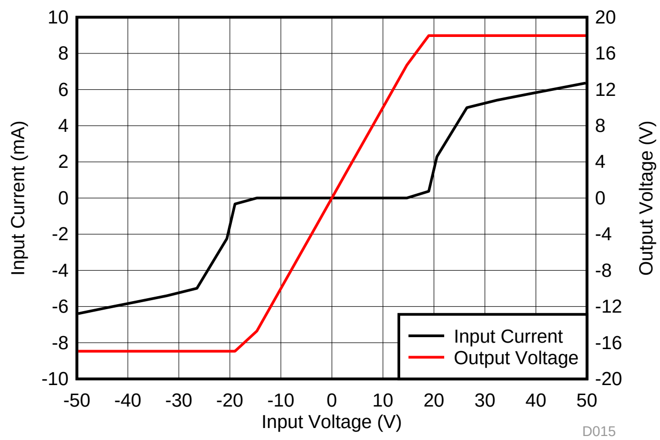
5 typical units G = 1

Figure 14. CMRR vs Temperature



5 typical units G = 10

Figure 15. CMRR vs Temperature



V_S = 36 V

Figure 16. Input Current vs Input Overvoltage

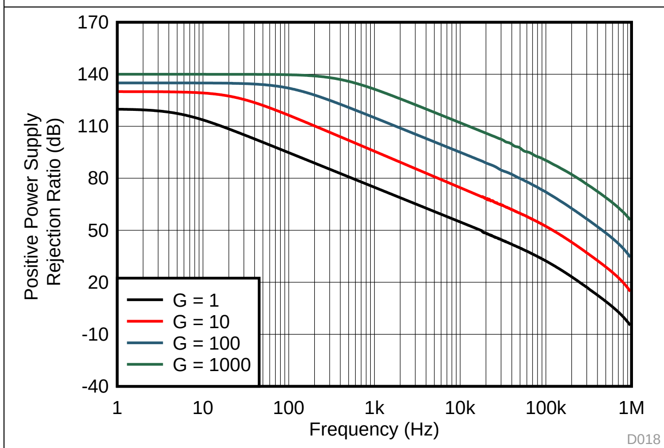


Figure 17. Positive PSRR vs Frequency (RTI)

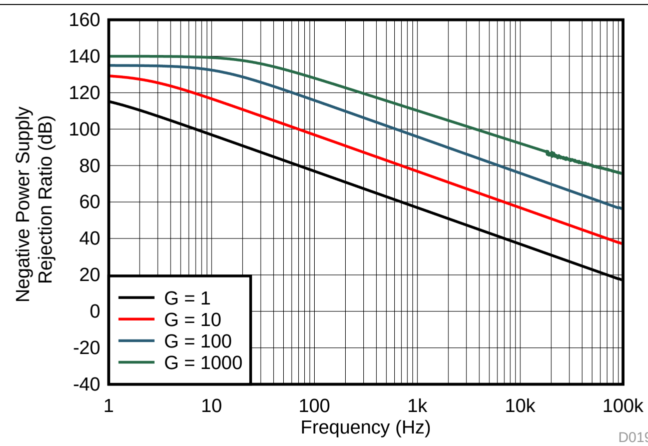


Figure 18. Negative PSRR vs Frequency (RTI)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

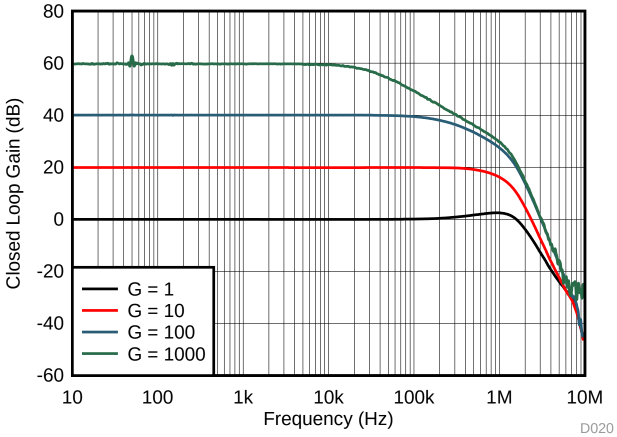


Figure 19. Gain vs Frequency

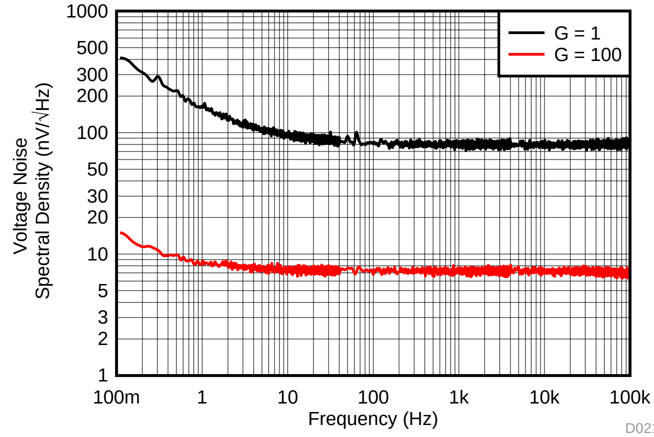


Figure 20. Voltage Noise Spectral Density vs Frequency (RTI)

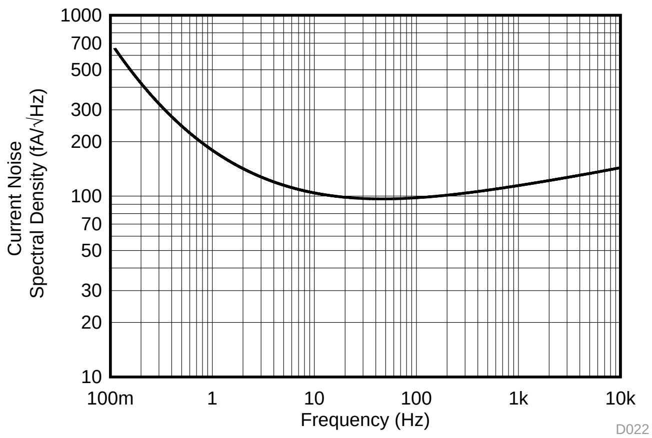


Figure 21. Current Noise Spectral Density vs Frequency (RTI)

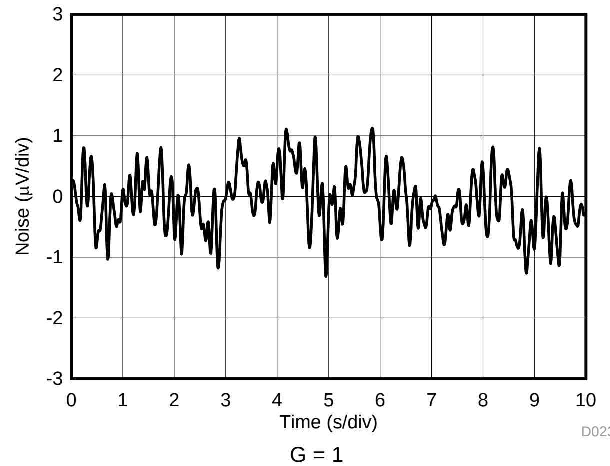


Figure 22. 0.1-Hz to 10-Hz RTI Voltage Noise

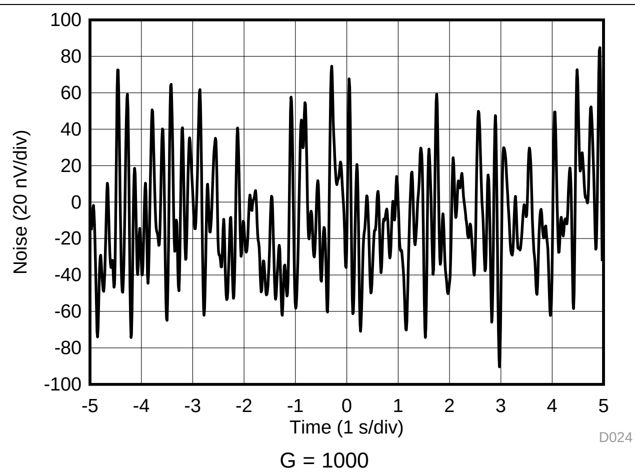


Figure 23. 0.1-Hz to 10-Hz RTI Voltage Noise

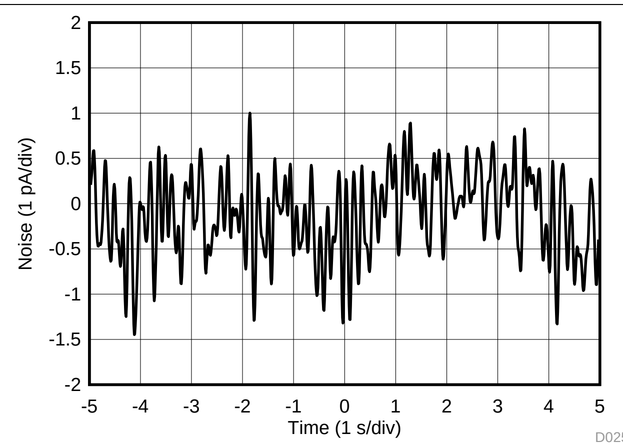
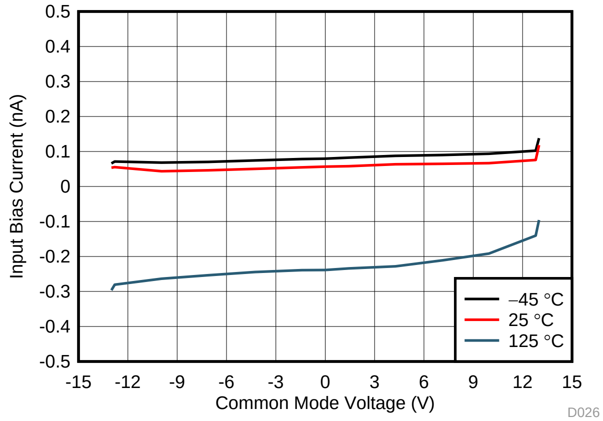


Figure 24. 0.1-Hz to 10-Hz RTI Current Noise

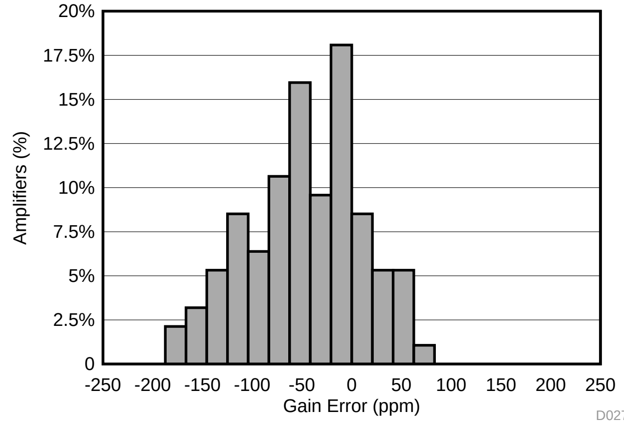
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



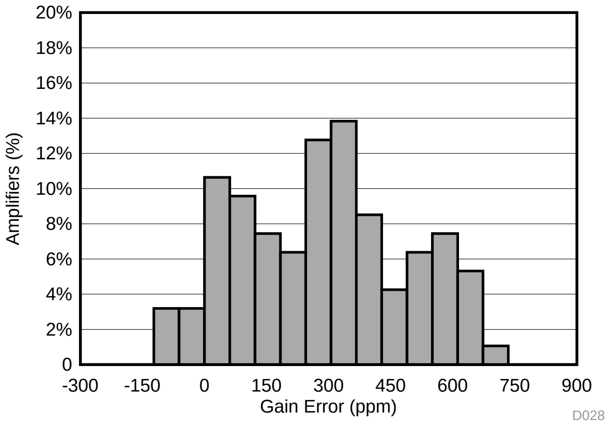
V_S = ±15 V

Figure 25. Input Bias Current vs Common-Mode Voltage



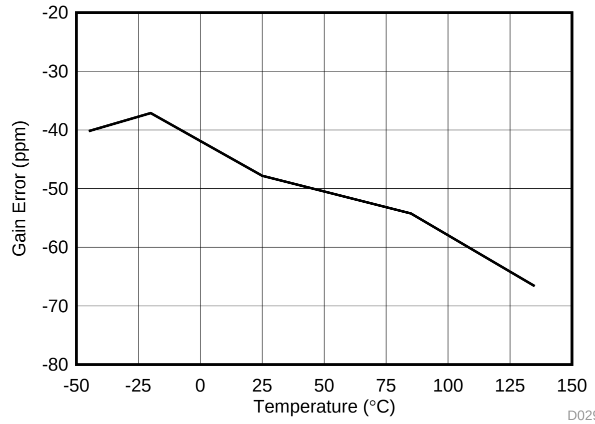
N = 94 Mean = –48 ppm Std. Dev. = 58 ppm
G = 1

Figure 26. Typical Distribution of Gain Error G = 1



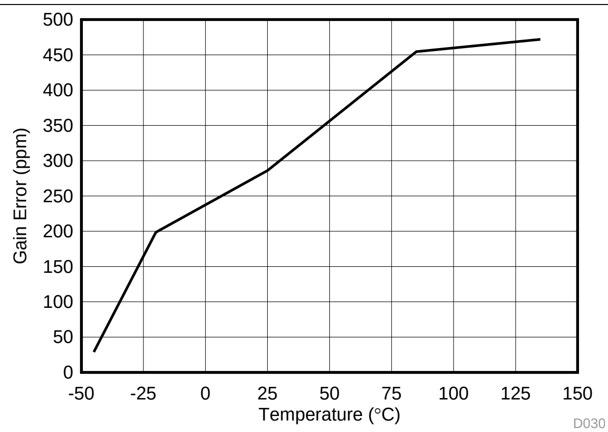
N = 94 Mean = 286 ppm Std. Dev. = 204 ppm
G = 10

Figure 27. Typical Distribution of Gain Error G = 10



G = 1

Figure 28. Gain Error vs Temperature



G = 10

Figure 29. Gain Error vs Temperature

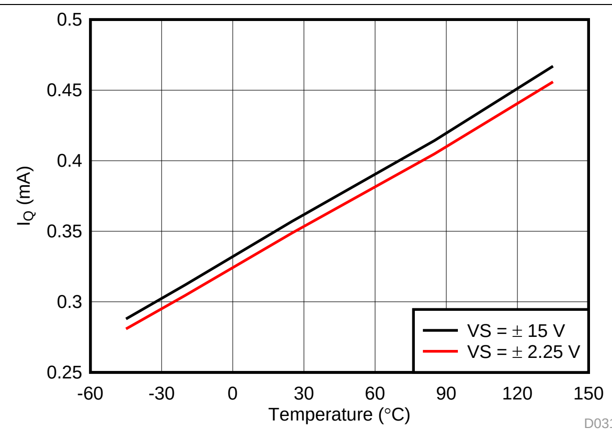
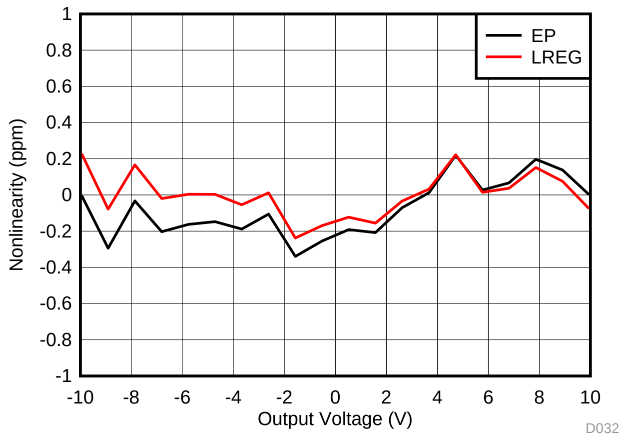


Figure 30. Supply Current vs Temperature

ADVANCE INFORMATION

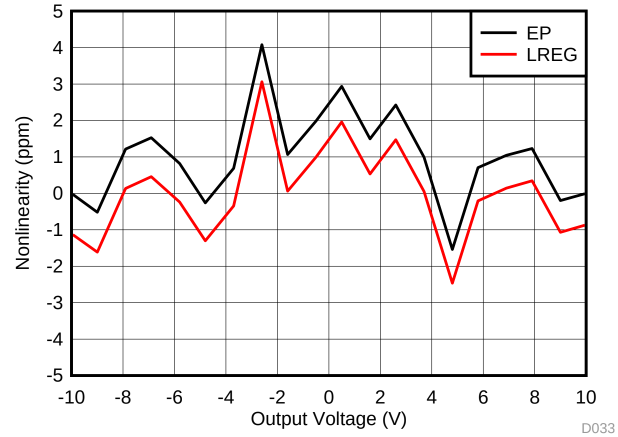
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 1

Figure 31. Gain Nonlinearity



G = 10

Figure 32. Gain Nonlinearity

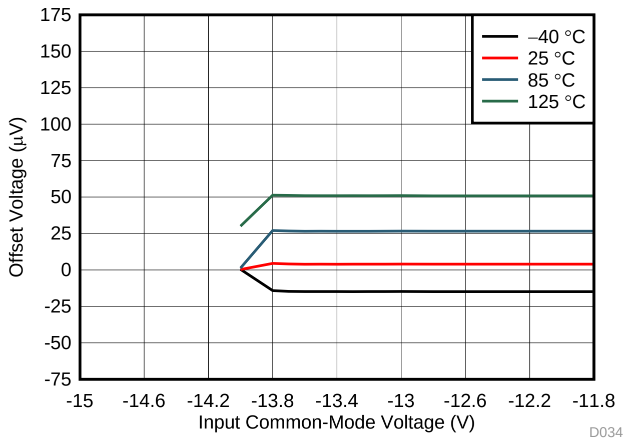


Figure 33. Offset Voltage vs Negative Common-Mode Voltage

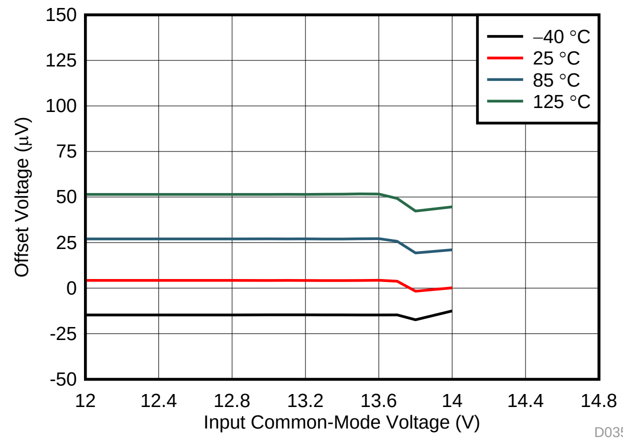


Figure 34. Offset Voltage vs Positive Common-Mode Voltage

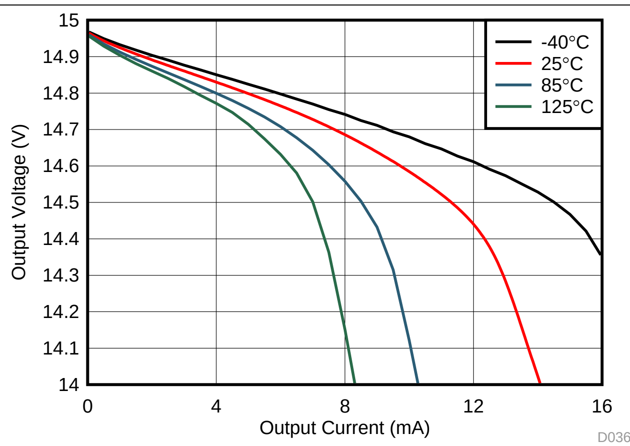


Figure 35. Positive Output Voltage Swing vs Output Current

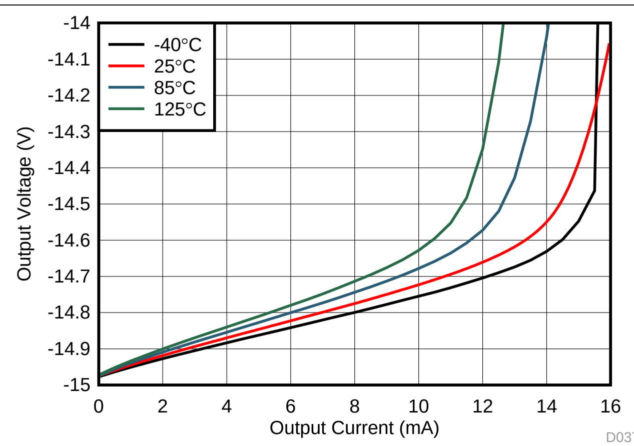


Figure 36. Negative Output Voltage Swing vs Output Current

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Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

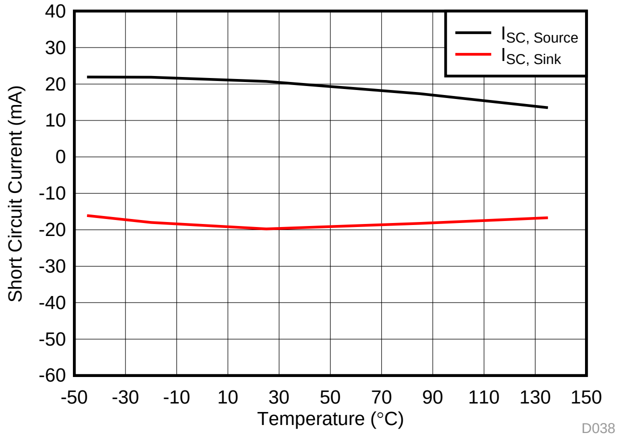


Figure 37. Short Circuit Current vs Temperature

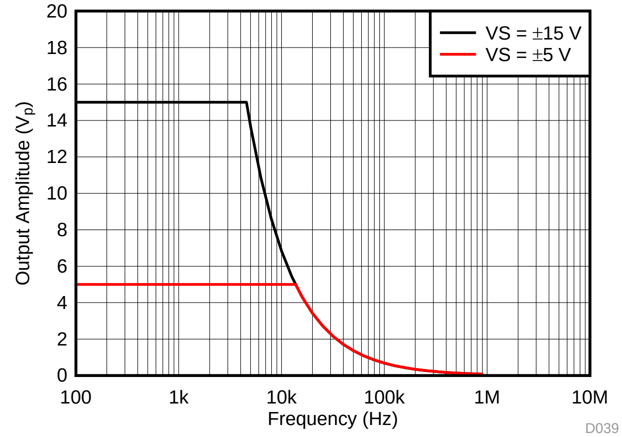
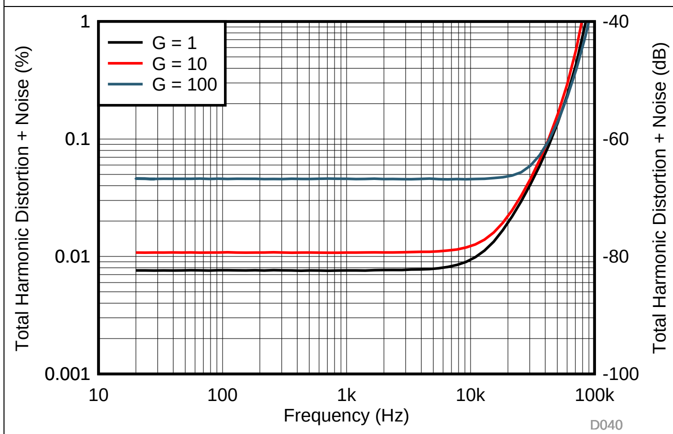


Figure 38. Large-Signal Frequency Response



500-kHz measurement bandwidth

1-V_{RMS} output voltage 100-kΩ load

Figure 39. THD+N vs Frequency

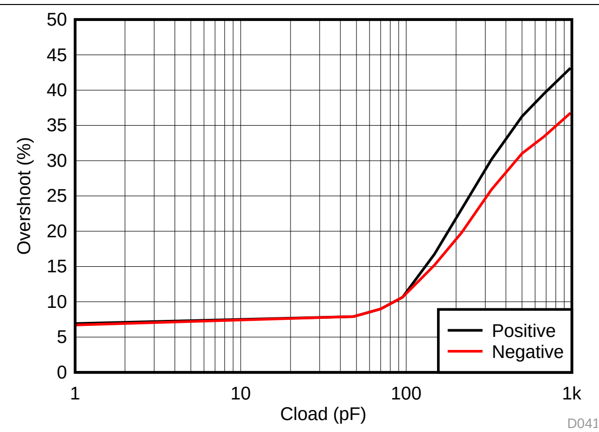
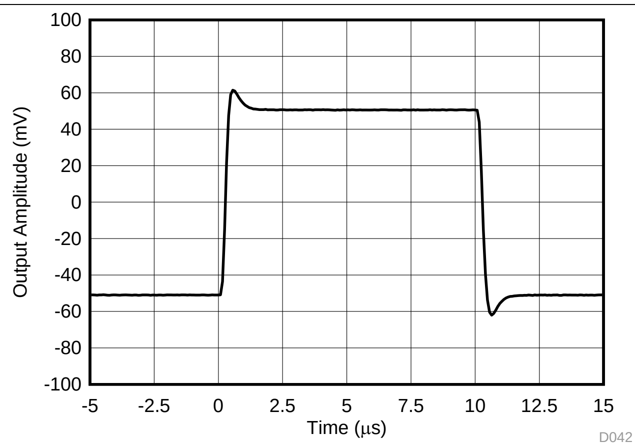
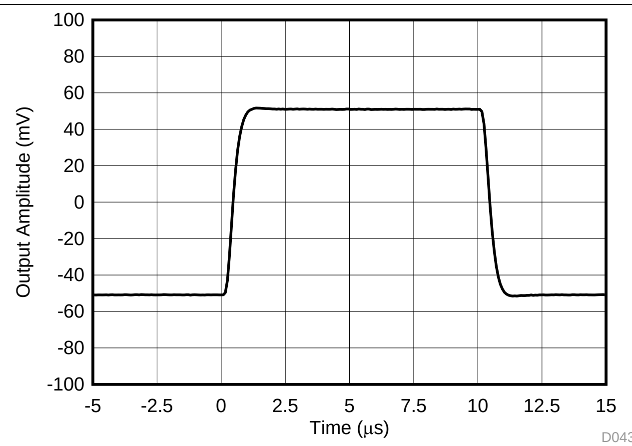


Figure 40. Overshoot vs Capacitive Loads



G = 1 R_L = 10 kΩ C_L = 100 pF

Figure 41. Small-Signal Response



G = 10 R_L = 10 kΩ C_L = 100 pF

Figure 42. Small-Signal Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

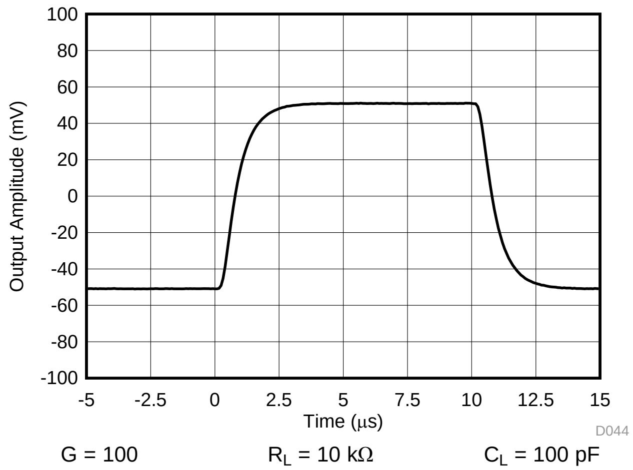


Figure 43. Small-Signal Response

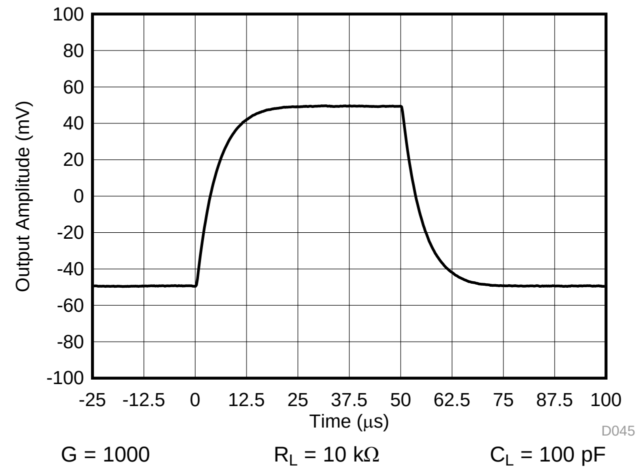


Figure 44. Small-Signal Response

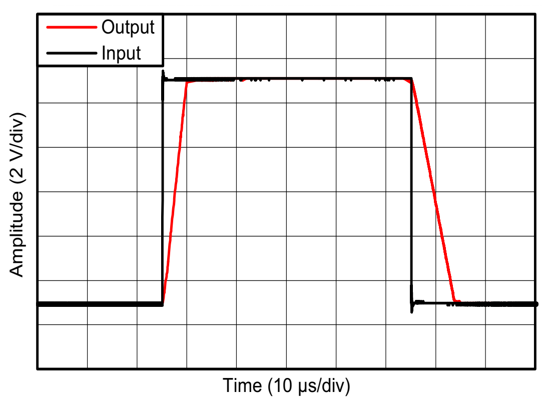


Figure 45. Large Signal Step Response

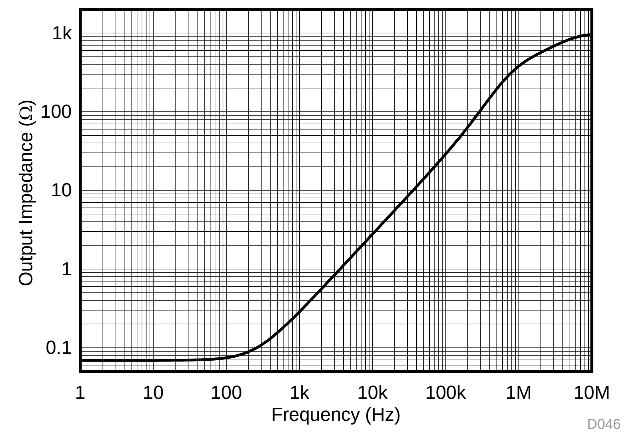


Figure 46. Closed-Loop Output Impedance

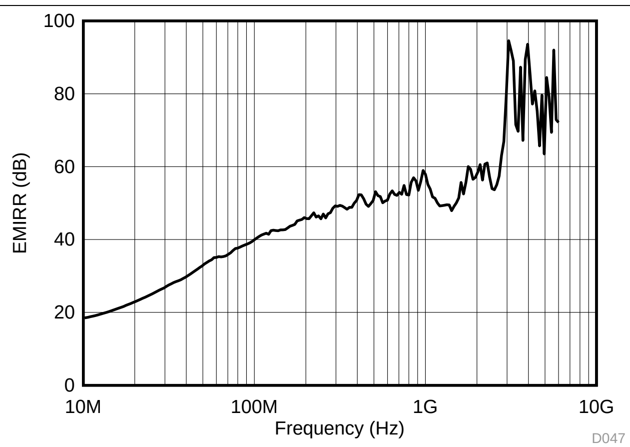


Figure 47. Differential-Mode EMI Rejection Ratio

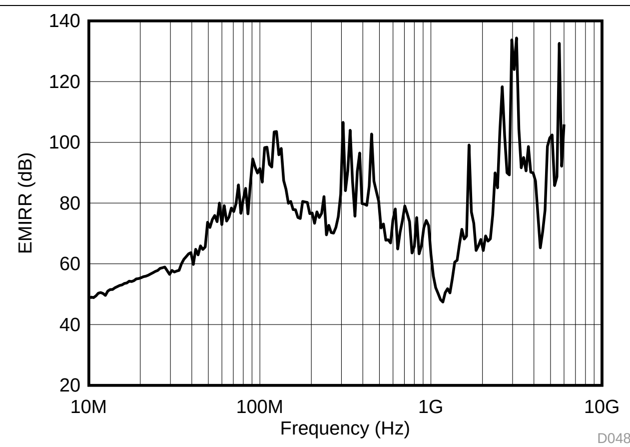
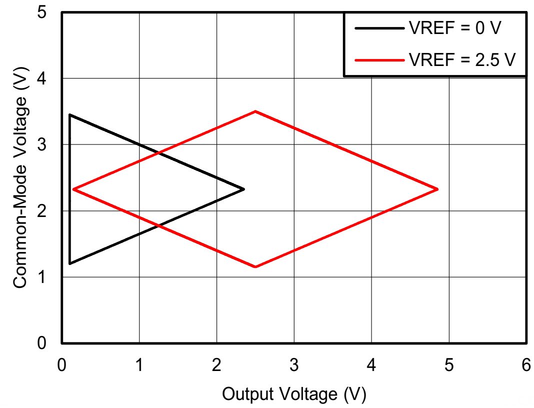


Figure 48. Common-Mode EMI Rejection Ratio

ADVANCE INFORMATION

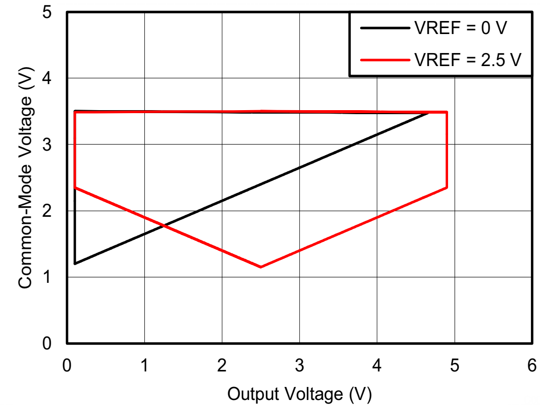
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



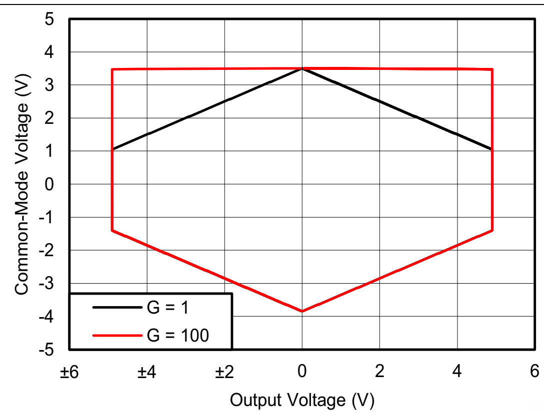
V_S = 5 V G = 1

Figure 49. Input Common-Mode Voltage vs Output Voltage



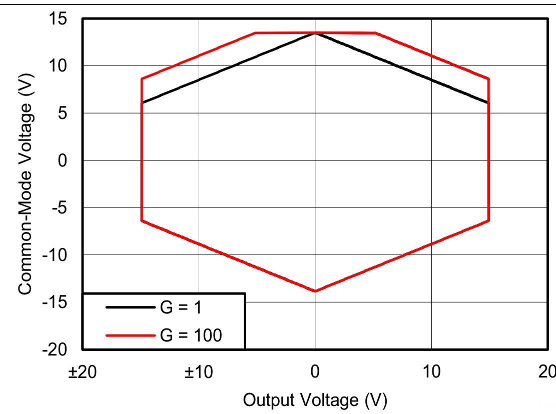
V_S = 5 V G = 100

Figure 50. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

Figure 51. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

Figure 52. Input Common-Mode Voltage vs Output Voltage

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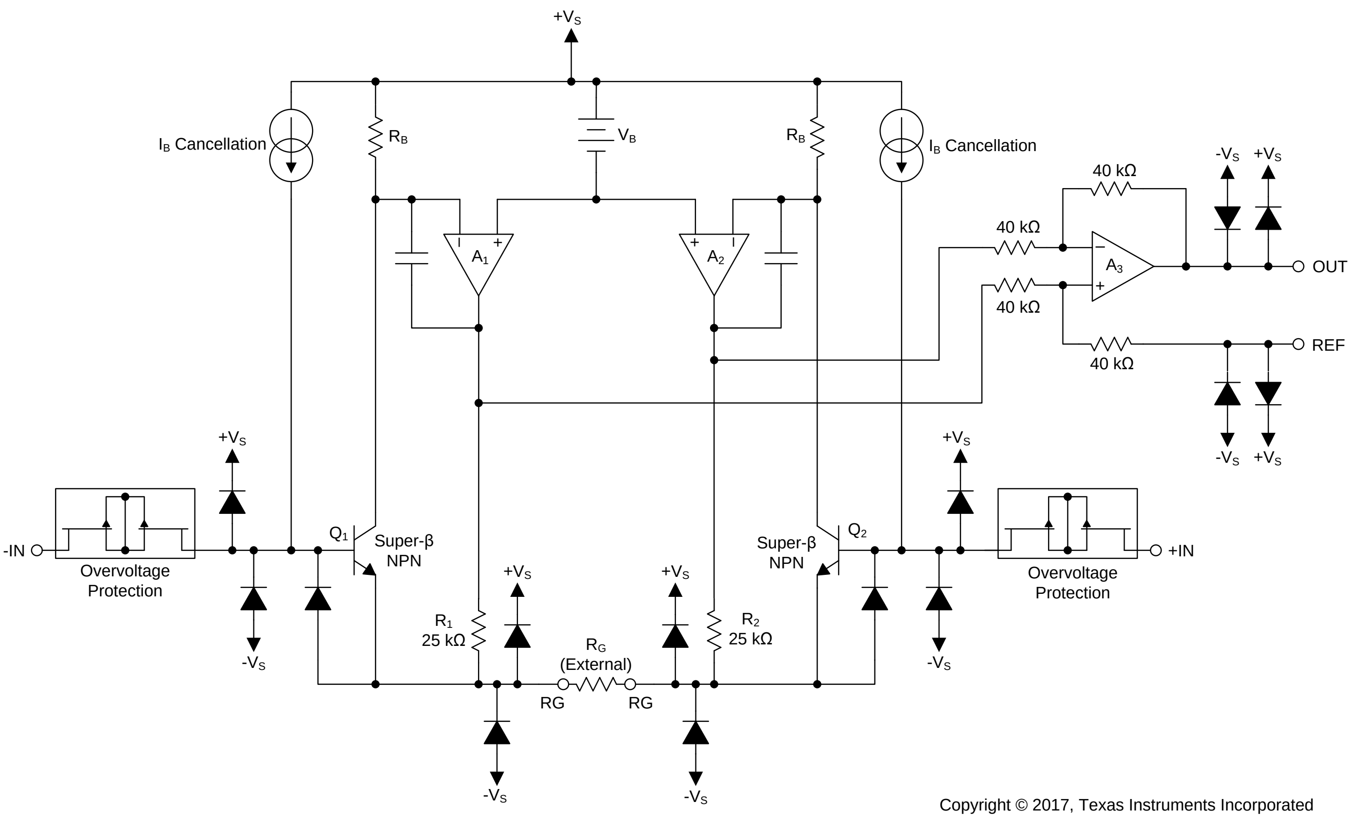
8 Detailed Description

8.1 Overview

The INA818 is a monolithic, precision instrumentation amplifier incorporating a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by transistors Q_1 and Q_2 and is forced across resistor R_G, which causes a signal current to flow through resistors R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Setting the Gain

Figure 53 shows that the gain of the INA818 is set by a single external resistor (R_G) connected between the RG pins (pins 1 and 8).

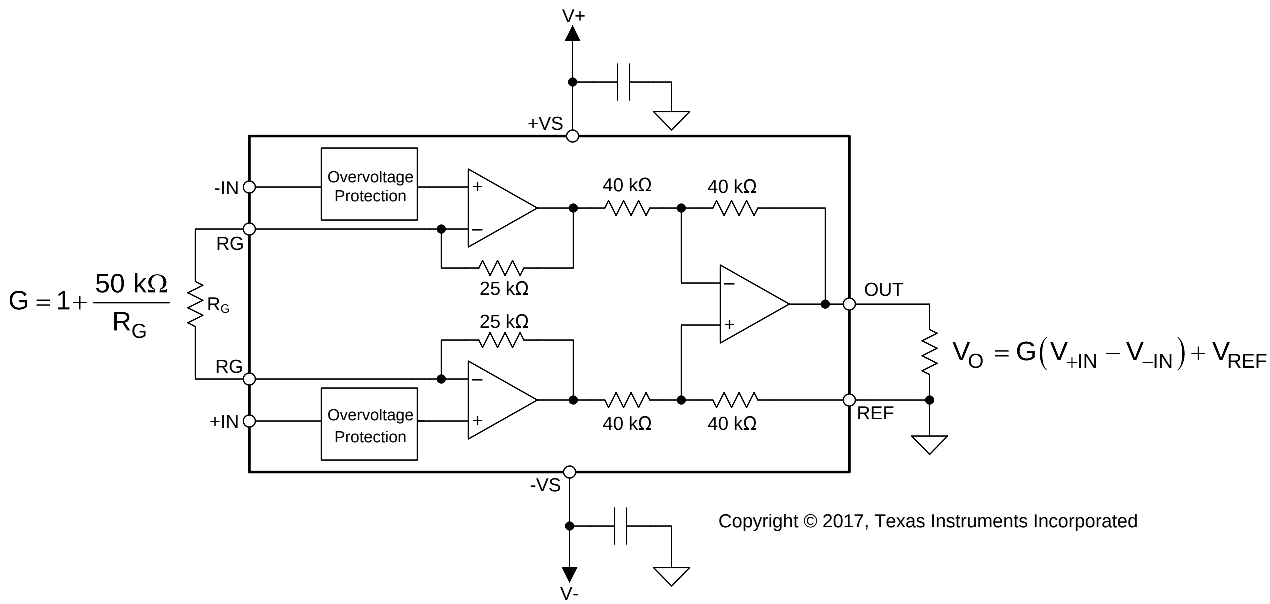

Figure 53. Simplified Diagram of the INA818 With Gain and Output Equations

The value of R_G is selected according to Equation 1:

$$G = 1 + \frac{50\ k\Omega}{R_G} \quad (1)$$

Table 2 lists several commonly-used gains and resistor values. The 50-kΩ term in Equation 1 comes from the sum of the two internal 25-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA818. As shown in Figure 53 and explained in more details in the *Layout* section, make sure to connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground that are placed as close to the device as possible.

Table 2. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50 k	49.9 k
5	12.5 k	12.4 k
10	5.556 k	5.49 k
20	2.632 k	2.61 k
50	1.02 k	1.02 k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9

8.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is determined from Equation 1.

The best gain drift of 5 ppm/℃ (maximum) is achieved when the INA818 uses G = 1 without R_G connected. In this case, gain drift is limited by the mismatch of the temperature coefficient of the integrated 40-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor (R_G.) The low temperature coefficient of the internal feedback resistors improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on the R_G pins maintains optimal CMRR over frequency.

8.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA818 to reject EMI. The offset resulting from an input EMI signal is calculated using Equation 2:

$$\Delta V_{OS} = \left(\frac{V_{RF\_PEAK}^{\,2}}{100\ mV_P} \right) \cdot 10^{-\left(\frac{EMIRR\ (dB)}{20} \right)}$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal. (2)

Figure 54 and Figure 55 show the INA818 EMIRR graphs for differential and common-mode EMI rejection across this frequency range. Table 3 lists the EMIRR values for the INA818 at frequencies commonly encountered in real-world applications. Applications listed in Table 3 are centered on or operated near the frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system. Incorporating known good practices, such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing may also be required.

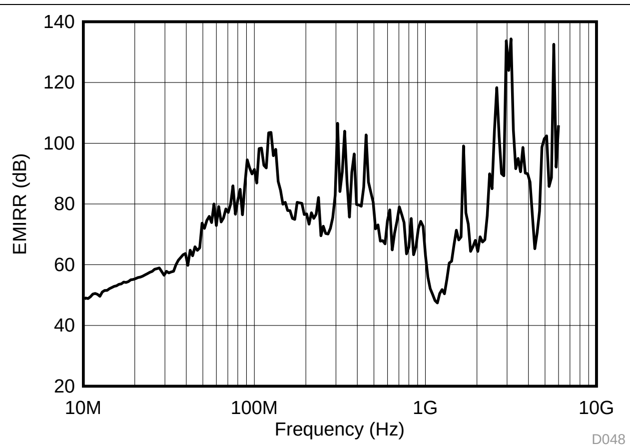

Figure 54. Common-Mode EMIRR Testing

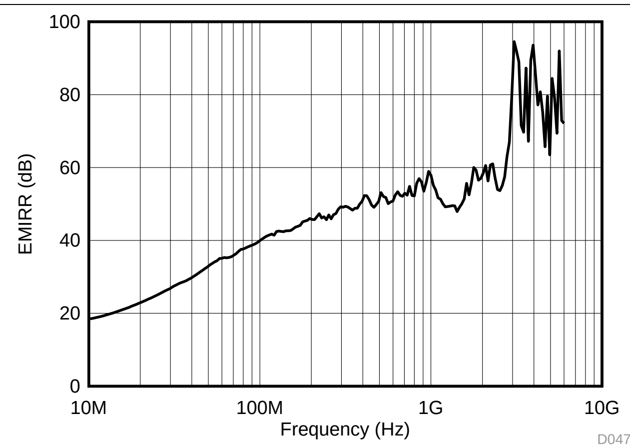

Figure 55. Differential Mode EMIRR Testing

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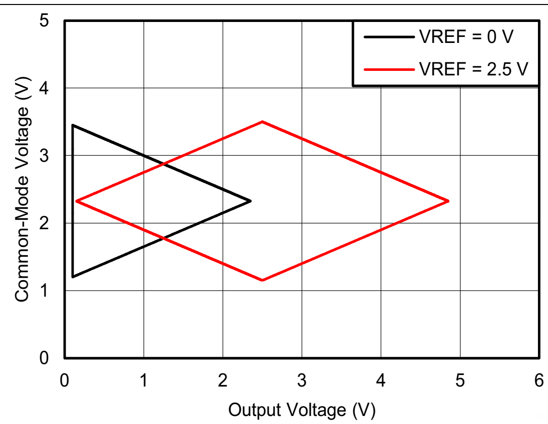
Table 3. INA818 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	52 dB	80 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	55 dB	71 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	58 dB	73 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	59 dB	95 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78 dB	96 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	70 dB	100 dB

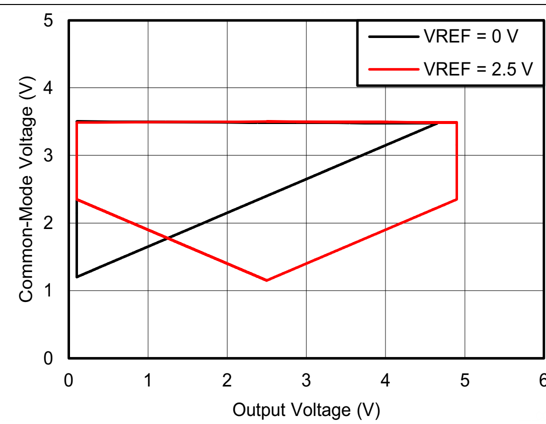
8.3.3 Input Common-Mode Range

The linear input voltage range of the INA818 input circuitry extends within 1.5 V (typical) of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in Figure 56, Figure 51, and Figure 52. The common-mode range for other operating conditions is best calculated using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers*.



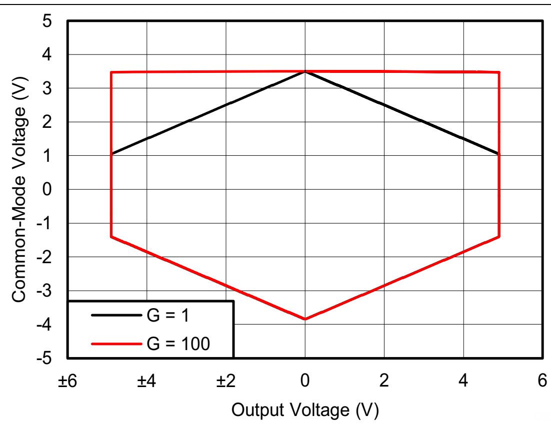
V_S = 5 V G = 1

Figure 56. Input Common-Mode Voltage vs Output Voltage



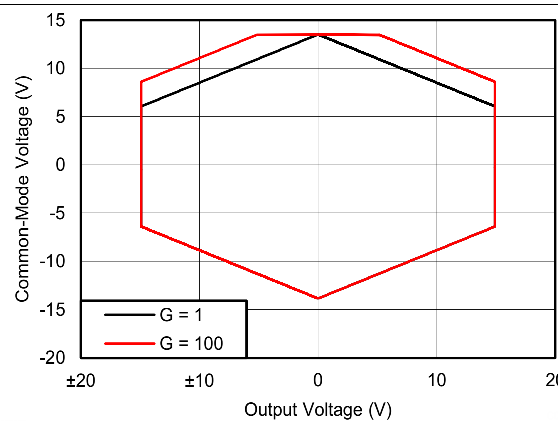
V_S = 5 V G = 100

Figure 57. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

Figure 58. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

Figure 59. Input Common-Mode Voltage vs Output Voltage

8.3.4 Input Protection

The inputs of the INA818 device are individually protected for voltages up to ±60 V. For example, a condition of –60 V on one input and +60 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

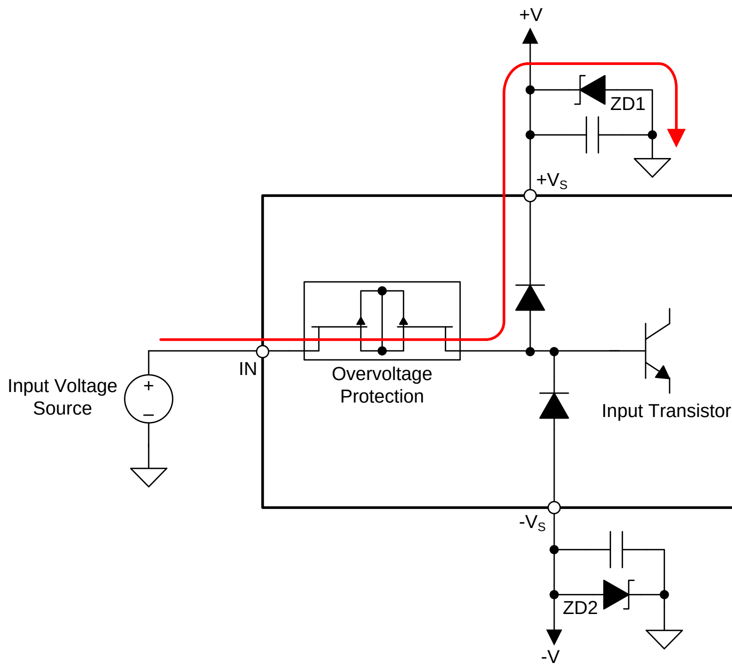


Figure 60. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see Figure 60. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in Figure 60) must be placed on the power supplies to provide a current pathway to ground. Figure 61 shows the input current for input voltages from –50 V to +50 V when the INA818 is powered by ±15-V supplies.

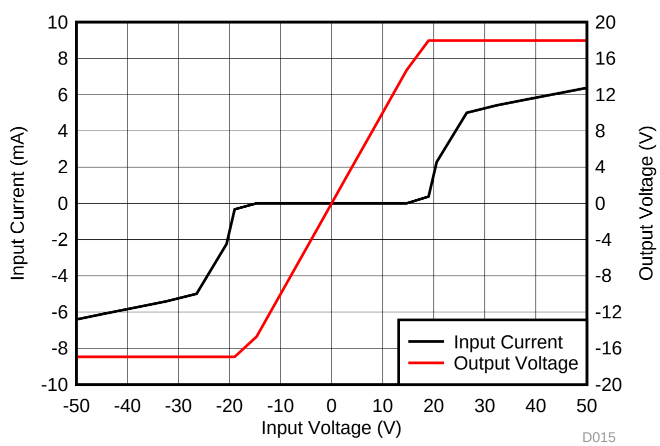


Figure 61. Input Current vs Input Overvoltage

8.3.5 Operating Voltage

The INA818 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in *Typical Characteristics* .

8.3.6 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimize these errors by choosing high-precision components, such as the INA818, that have improved specifications in critical areas that impact the precision of the overall system. Figure 62 shows an example application.

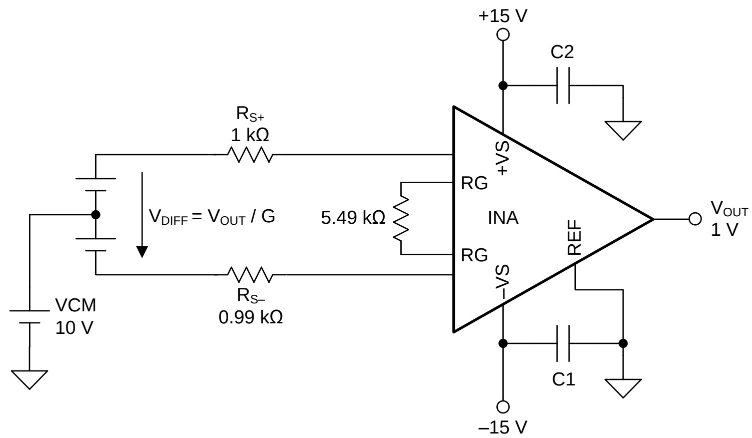


Figure 62. Example Application With G = 10 V/V and 1-V Output Voltage

Resistor-adjustable devices (such as the INA818) show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V), the gain error becomes a significant error source because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA818 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). Table 5 summarizes the major error sources in common INA applications and compares the three cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor) and G = 100 (511-Ω external resistor). All calculations are assuming an output voltage of V_{OUT} = 1 V. Thus, the input signal V_{DIFF} (given by V_{DIFF}= V_{OUT} / G) exhibits smaller and smaller amplitudes with increasing gain G. V_{DIFF} = 1 mV at G = 1000 in this example. All calculations refer the error to the input for easy comparison and system evaluation. As Table 5 shows, errors generated by the input stage (such as input offset voltage) are more dominant at higher gain, while the effects of output stage are suppressed because they are divided by the gain when referring them back to the input. The gain error and gain drift error are much more significant for gains greater than 1 because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. In most applications, static errors (absolute accuracy errors) can readily be removed during calibration in production, while the drift errors are the key factors limiting overall system performance.

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Table 4. System Specifications for Error Calculation

QUANTITY	VALUE	UNIT
V_{OUT}	1	V
VCM	10	V
VS	1	V
R_{S+}	1000	Ω
R_{S-}	999	Ω
RG tolerance	0.01	%
RG drift	10	ppm/°C
Temperature range upper limit	105	°C

Table 5. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA818 VALUES				
		SPECIFICATION	UNIT	G = 1 ERROR (ppm)	G = 100 ERROR (ppm)	G = 1000 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C						
Input offset voltage	V_{OSI} / V_{DIFF}	35	µV	35	350	3500
Output offset voltage	$V_{OSO} / (G \times V_{DIFF})$	300	µV	300	300	300
Input offset current	$I_{OS} \times \text{maximum} (R_{S+}, R_{S-}) / V_{DIFF}$	0.5	nA	1	5	50
CMRR (min)	$V_{CM} / (10^{CMRR/20} \times V_{DIFF})$	90 (G = 1), 110 (G = 10), 130 (G = 100)	dB	316	316	316
PSRR (min)	$(V_{CC} - V_S) / (10^{PSRR/20} \times V_{DIFF})$	110 (G = 1), 114 (G = 10), 130 (G = 100)	dB	3	20	32
Gain error from INA (max)	$GE(\%) \times 10^4$	0.02 (G = 1), 0.15 (G = 10, 100)	%	200	1500	1500
Gain error from external resistor RG (max)	$GE(\%) \times 10^4$	0.01	%	100	100	100
Total absolute accuracy error (ppm) at 25°C, worst case	sum of all errors	—	—	955	2591	5798
Total absolute accuracy error (ppm) at 25°C, average	rms sum of all errors	—	—	491	1604	3835
DRIFT TO 105°C						
Gain drift from INA (max)	$GTC \times (T_A - 25)$	5 (G = 1), 35 (G = 10, 100)	ppm/°C	400	2800	2800
Gain drift from external resistor RG (max)	$GTC \times (T_A - 25)$	10	ppm/°C	800	800	800
Input offset voltage drift (max)	$(V_{OSI\_TC} / V_{DIFF}) \times (T_A - 25)$	0.4	µV/°C	32	320	3200
Output offset voltage drift	$[V_{OSO\_TC} / (G \times V_{DIFF})] \times (T_A - 25)$	5	µV/°C	400	400	400
Offset current drift	$I_{OS\_TC} \times \text{maximum} (R_{S+}, R_{S-}) \times (T_A - 25) / V_{DIFF}$	20	pA/°C	2	16	160
Total drift error to 105°C (ppm), worst case	sum of all errors	—	—	1634	4336	7360
Total drift error to 105°C (ppm), typical	rms sum of all errors	—	—	980	2957	4348
RESOLUTION						
Gain nonlinearity		10 (G = 1, 10), 15 (G = 100)	ppm of FS	10	10	15
Voltage noise (at 1 kHz)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left[\frac{e_{NO}}{G}\right]^2} \times \frac{6}{V_{DIFF}}$	e_{NI} = 8, e_{NO} = 90	μV_{PP}	1204	1070	3941
Current noise (at 1kHz)	$I_N \times \text{maximum} (R_{S+}, R_{S-}) \times \sqrt{BW} / V_{DIFF}$	0.13	pA/√Hz	0.3	2	11
Total resolution error (ppm), worst case	sum of all errors	—	—	1214	1080	3956
Total resolution error (ppm), typical	rms sum of all errors	—	—	1204	1070	3941
TOTAL ERROR						
Total error (ppm), worst case	sum of all errors	—	—	3802	8007	17113
Total error (ppm), typical	rms sum of all errors	—	—	1628	3530	7010

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8.4 Device Functional Modes

The INA818 has a single functional mode and operates when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA818 is 36 V (±18 V.)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reference Pin

The output voltage of the INA818 is developed with respect to the voltage on the reference pin, REF. In dual-supply operation, REF (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA818 drives a single-supply ADC.

The voltage source applied to the reference pin must have a low output impedance. As shown in Figure 63, any resistance at the reference pin (shown as R_{REF} in Figure 63) is in series with an internal 40-kΩ resistor.

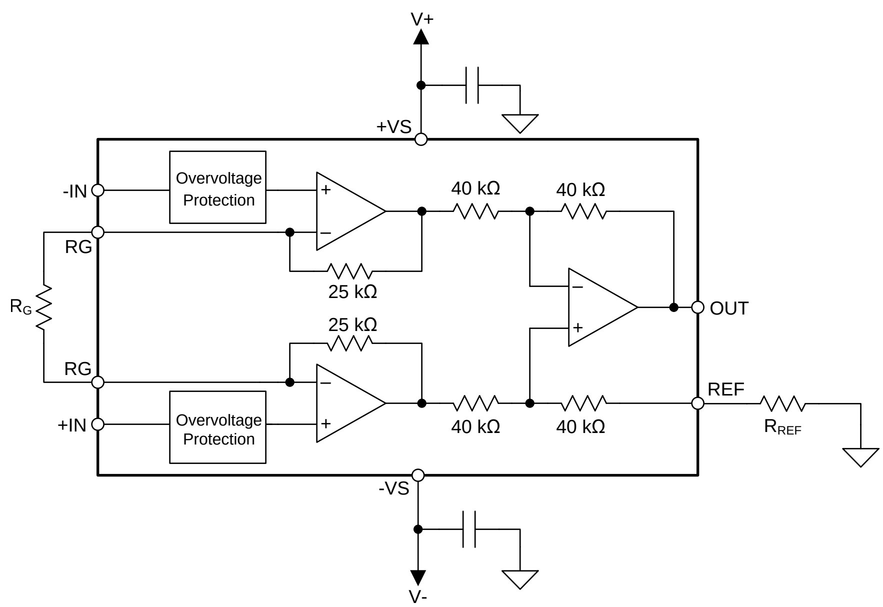

Figure 63. Parasitic Resistance Shown at the Reference Pin

Application Information (continued)

The parasitic resistance at the reference pin (R_{REF}) creates an imbalance in the four resistors of the internal difference amplifier, which degrades the common-mode rejection ratio (CMRR). Figure 64 shows the degradation in CMRR of the INA818 as a result of increased resistance at the reference pin. For the best performance, keep the source impedance to the REF pin (R_{REF}) below 5 Ω.

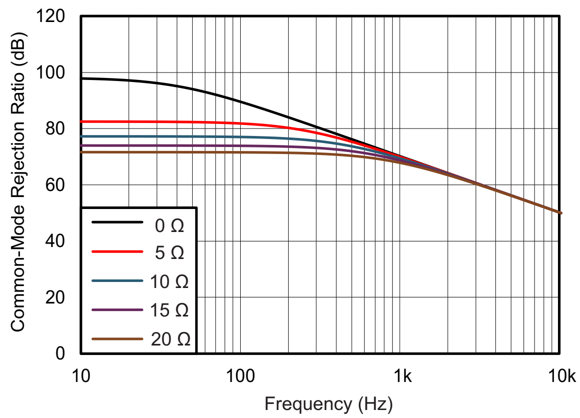

Figure 64. The Effect of Increasing Resistance at the Reference Pin

Voltage-reference devices are a suitable option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as Figure 65 shows, in order to avoid CMRR degradation.

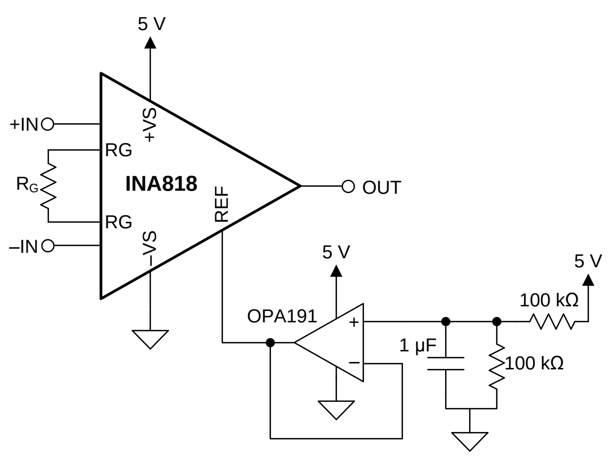

Figure 65. Using an Op Amp to Buffer Reference Voltages

ADVANCE INFORMATION

Application Information (continued)

9.1.2 Input Bias Current Return Path

The input impedance of the INA818 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for input bias current. Figure 66 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA818, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can connect to one input (as shown in the thermocouple example in Figure 66). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

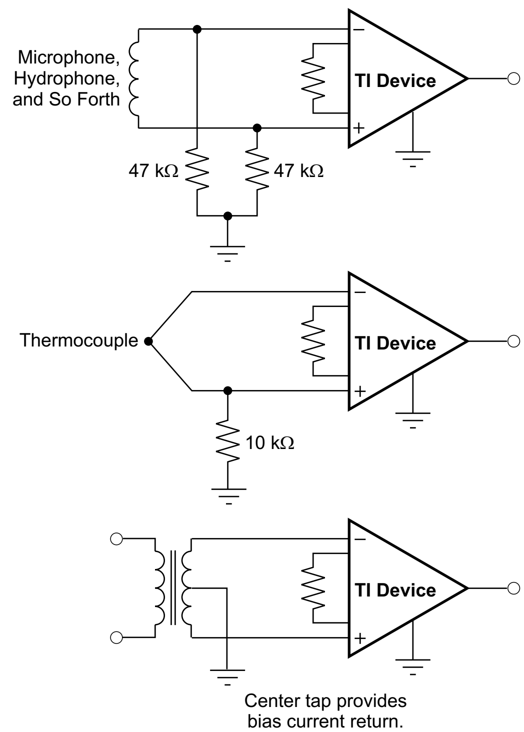

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Figure 66. Providing an Input Common-Mode Current Path

9.2 Typical Applications

9.2.1 Three-Pin Programmable Logic Controller (PLC)

Figure 67 shows a three-pin programmable-logic controller (PLC) design for the INA818. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

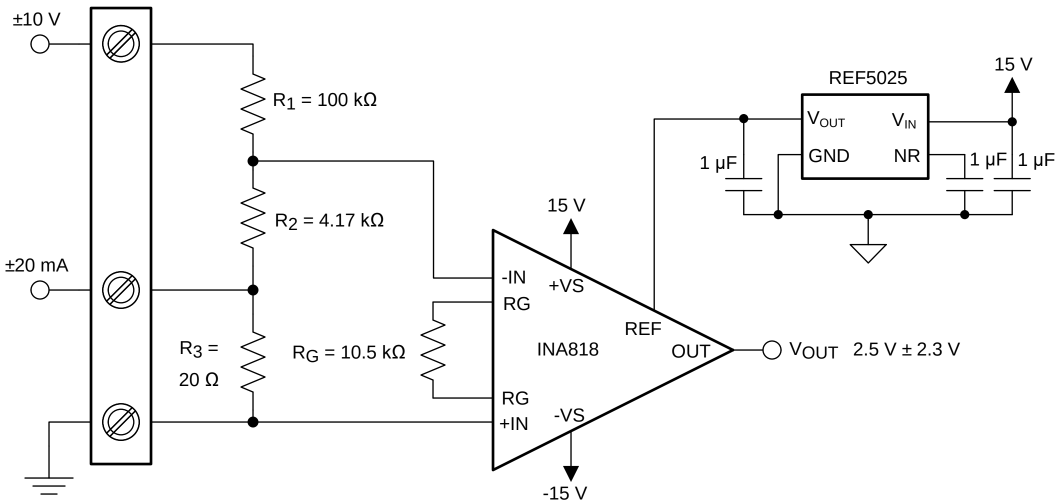

Figure 67. PLC Input (±10 V, 4 mA to 20 mA)

9.2.1.1 Design Requirements

For this application, the design requirements are as follows:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20-mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

9.2.1.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in Figure 67: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, Equation 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \quad (3)$$

where

- G represents the gain of the instrumentation amplifier
- V_D represents the differential voltage at the INA818 inputs
- V_{REF} is the voltage at the INA818 REF pin
- I_{IN} is the input current

Equation 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \quad (4)$$

where

- V_{IN} is the input voltage

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Typical Applications (continued)

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Use Equation 5 to calculate R_2 given V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ \text{k}\Omega \quad (5)$$

The value obtained from Equation 5 is not a standard 0.1% value, so 4.17 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

Use Equation 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ \text{V} - 2.5\ \text{V}}{400\ \text{mV}} = 5.75\ \frac{\text{V}}{\text{V}} \quad (6)$$

Equation 7 calculates the gain-setting resistor value using the INA818 gain equation, Equation 1.

$$R_G = \frac{50\ \text{k}\Omega}{G - 1} = \frac{50\ \text{k}\Omega}{5.75 - 1} = 10.5\ \text{k}\Omega \quad (7)$$

10.5 kΩ is a standard 0.1% resistor value that can be used in this design.

9.2.1.3 Application Curves

Figure 68 and Figure 69 show typical characteristic curves for the circuit in Figure 67.

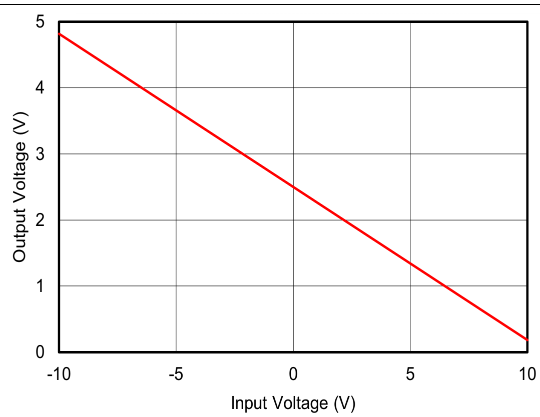

Figure 68. PLC Output Voltage vs Input Voltage

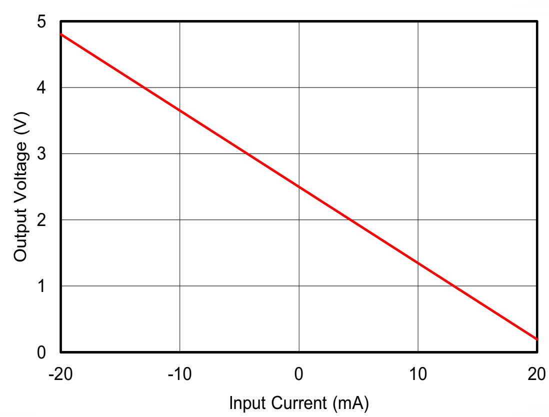

Figure 69. PLC Output Voltage vs Input Current

Typical Applications (continued)

9.2.2 Resistance Temperature Detector Interface

Figure 70 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 V to 5 V. The linearization technique employed is described in the *Analog linearization of resistance temperature detectors* analog application journal. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.

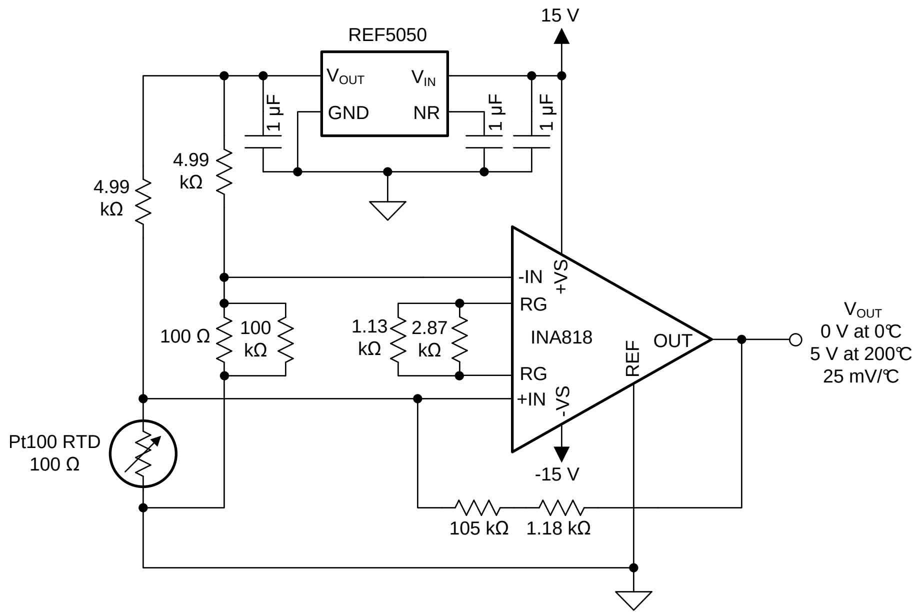

Figure 70. A 3-Wire Interface for RTDs With Analog Linearization

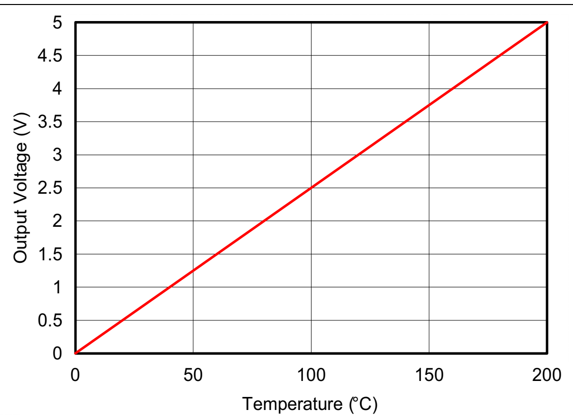

Figure 71. Transfer Function of a 3-Wire RTD Interface

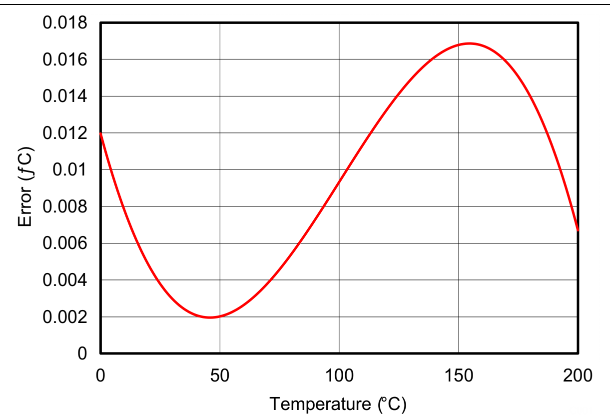

Figure 72. Temperature Error Over the Full Temperature Range

10 Power Supply Recommendations

The nominal performance of the INA818 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device can also be operated using power supplies from ±2.25 V (4.5 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in the *Typical Characteristics* section.

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 73, keeping R_G close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

11.2 Layout Example

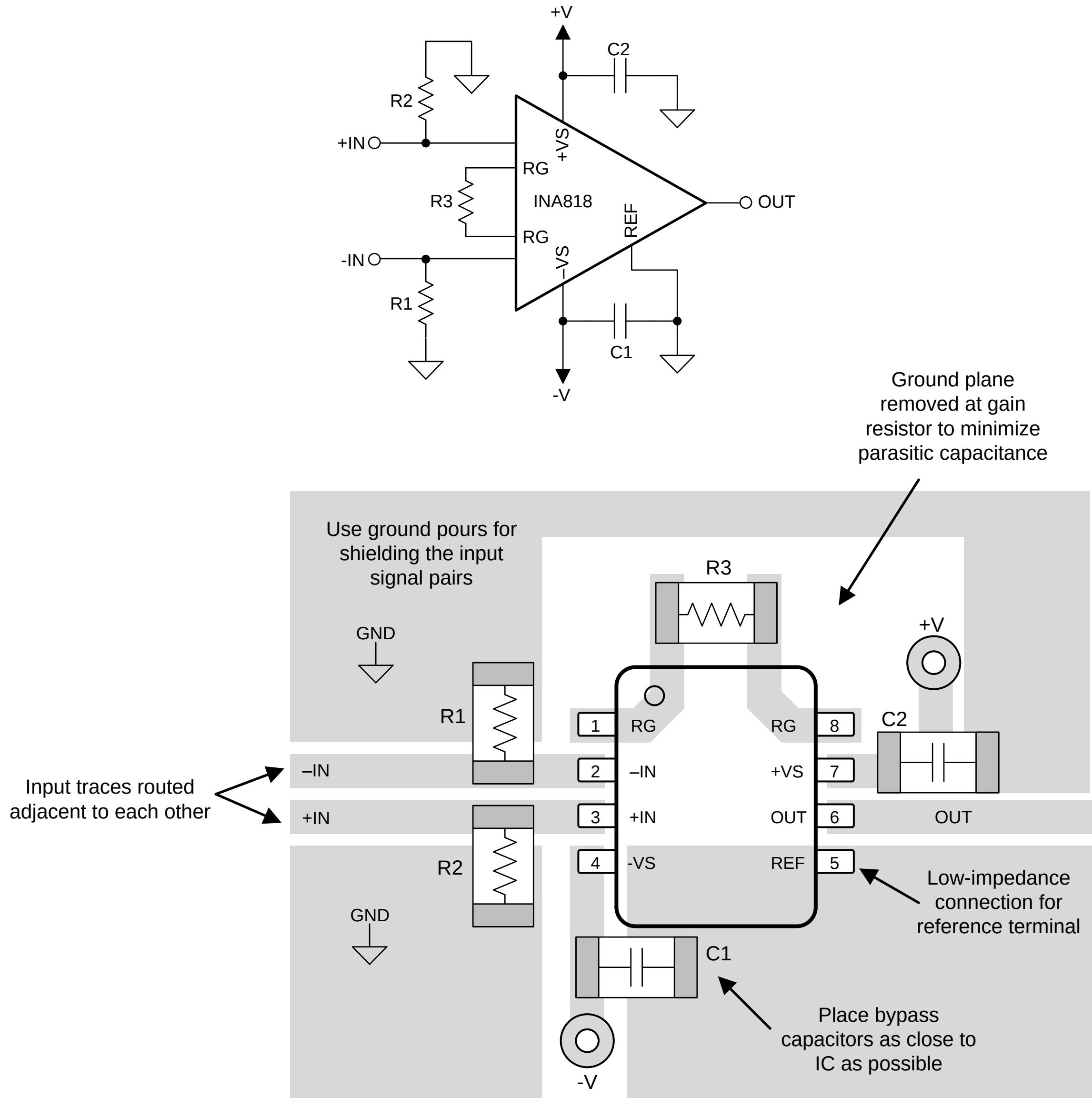

Figure 73. Example Schematic and Associated PCB Layout

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Universal Instrumentation Amplifier EVM* user's guide
- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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Bluetooth is a registered trademark of Bluetooth SIG, Inc.
PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA818ID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		
INA818IDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		
XINA818ID	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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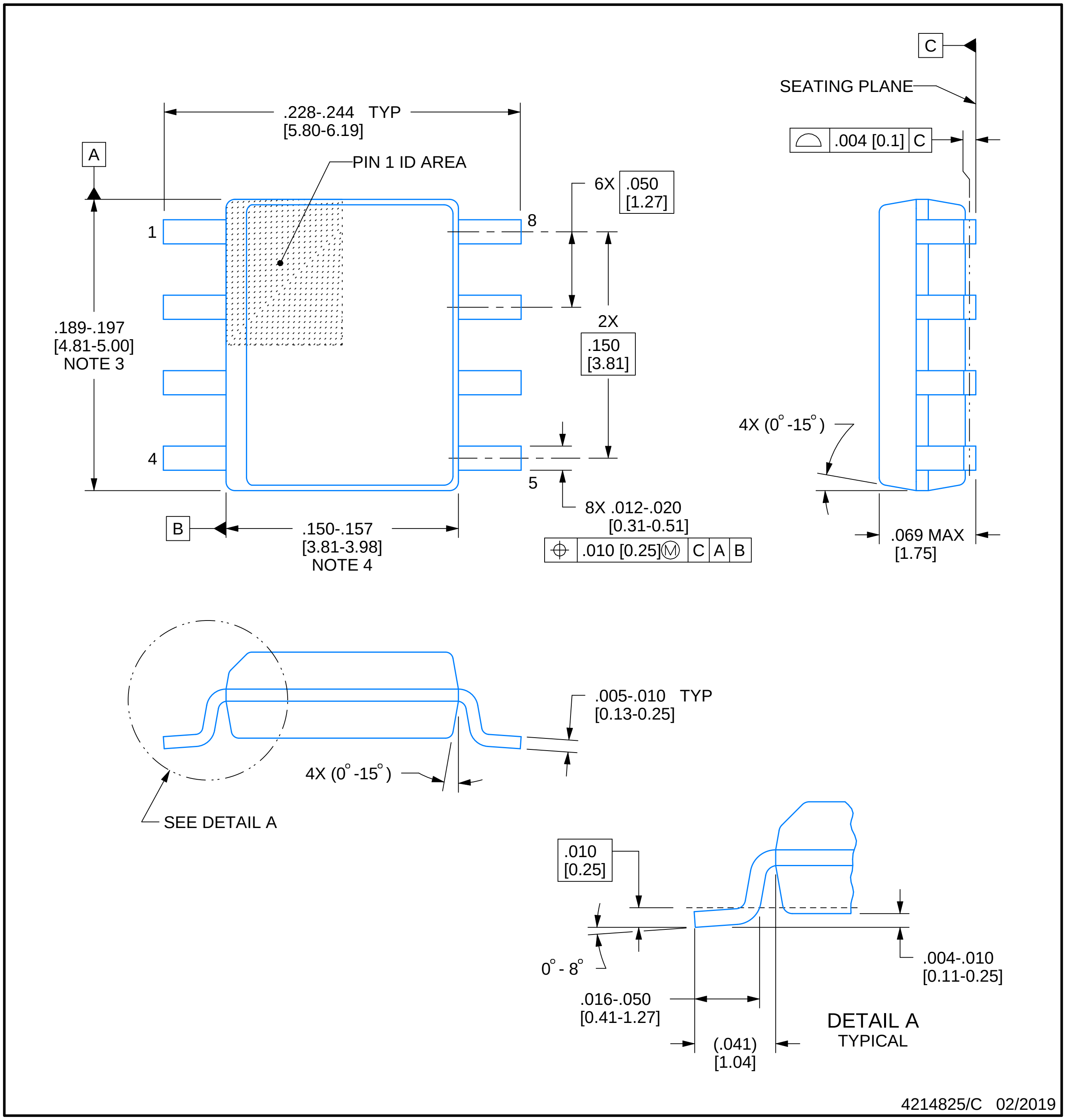
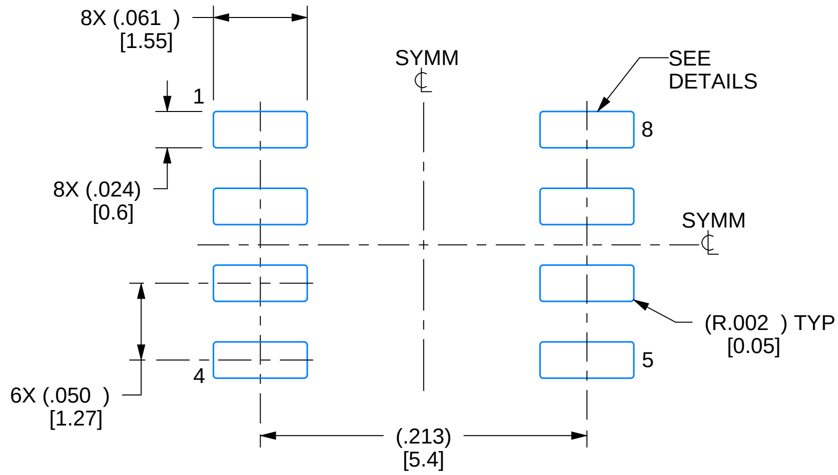
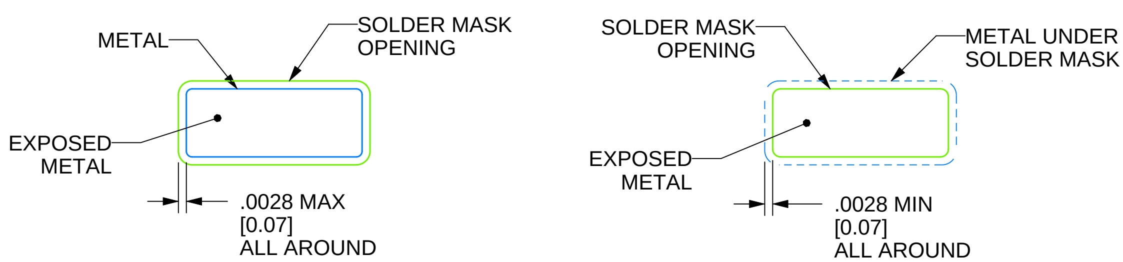


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

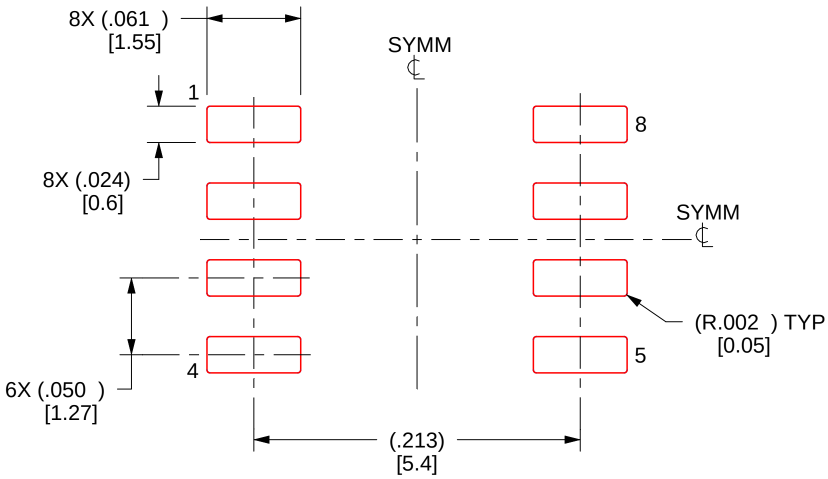
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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