

Control Integrated Power System (CIPOS™)

IKCM15L60GD

Datasheet



Table of Contents

CIPOS Control Integrated Power System 3

Features 3

Target Applications 3

Description 3

System Configuration 3

Pin Configuration 4

Internal Electrical Schematic 4

Pin Assignment 5

Pin Description 5

 HIN(U,V,W) and LIN(U,V,W) (Low side and high side control pins, Pin 7 - 12) 5

 VFO (Fault-output and NTC, Pin 14) 6

 ITRIP (Over current detection function, Pin 15) 6

 VDD, VSS (Low side control supply and reference, Pin 13, 16) 6

 VB(U,V,W) and VS(U,V,W) (High side supplies, Pin 1 - 6) 6

 NW, NV, NU (Low side emitter, Pin 17 - 19) 6

 W, V, U (High side emitter and low side collector, Pin 20 - 22) 6

 P (Positive bus input voltage, Pin 23) 6

Absolute Maximum Ratings 7

Module Section 7

Inverter Section 7

Control Section 7

Recommended Operation Conditions 8

Static Parameters 9

Dynamic Parameters 10

Bootstrap Parameters 10

Thermistor 11

Mechanical Characteristics and Ratings 11

Circuit of a Typical Application 12

Switching Times Definition 12

Electrical characteristic 13

Package Outline 14

CIPOS

Control Integrated Power System

Dual In-Line Intelligent Power Module

3Φ-bridge 600V / 15A

Features

Fully isolated Dual In-Line molded module

- TrenchStop® IGBTs
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11V for signal transmission at VBS=15V
- Integrated bootstrap functionality
- Over current shutdown
- Temperature monitor
- Under-voltage lockout at all channels
- Low side emitter pins accessible for all phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection
- Lead-free terminal plating; RoHS compliant
- Very low thermal resistance due to DCB

Target Applications

- Home appliances
- Low power motor drives

Description

The CIPOS module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

It is designed to control three phase AC motors and permanent magnet motors in variable speed drives for applications like an air conditioning, a refrigerator and a washing machine. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection.

TrenchStop® IGBTs and anti parallel diodes are combined with an optimized SOI gate driver for excellent electrical performance.

System Configuration

- 3 half bridges with TrenchStop® IGBTs and anti parallel diodes
- 3Φ SOI gate driver
- Thermistor
- Pin-to- heatsink creepage distance typ. 1.6mm

Pin Configuration

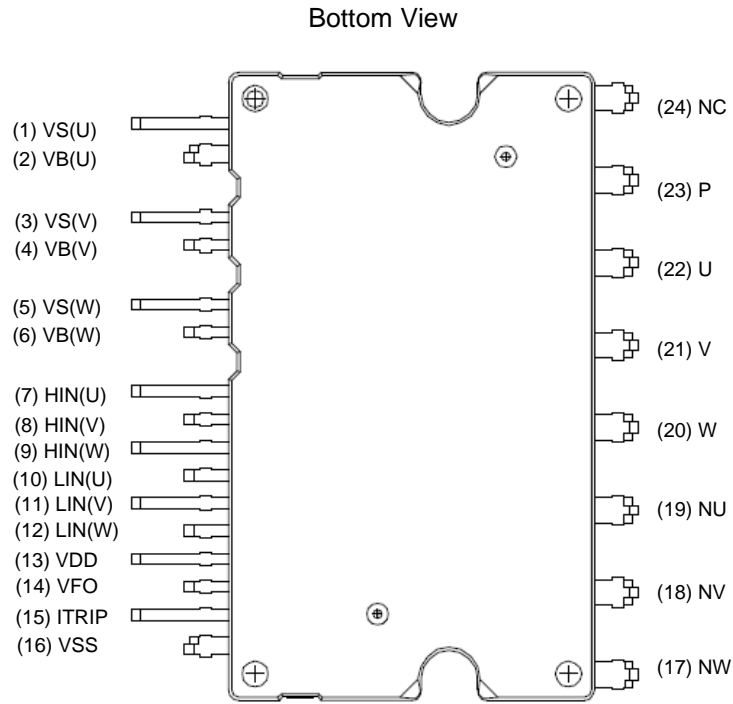


Figure 1: Pin configuration

Internal Electrical Schematic

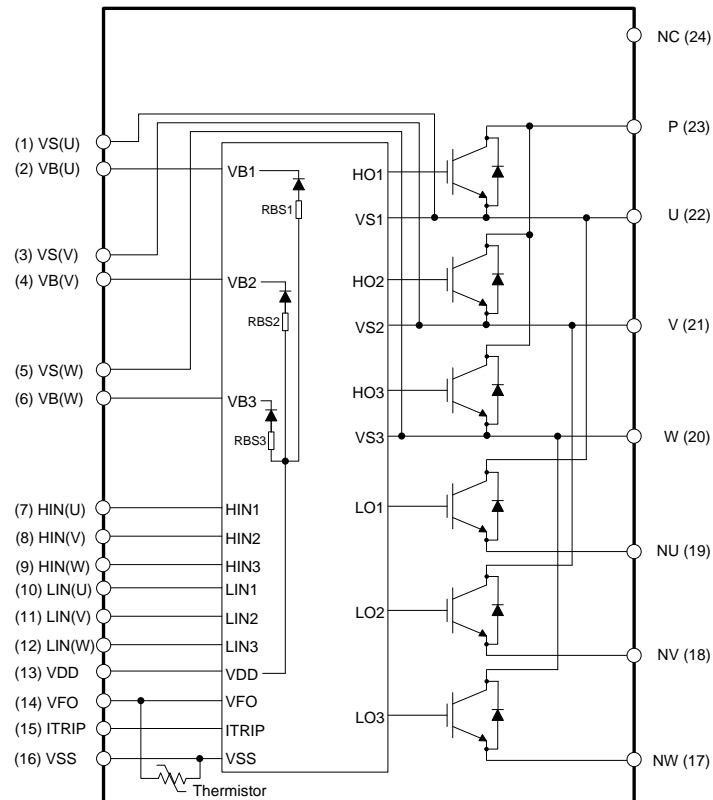


Figure 2: Internal schematic

Pin Assignment

Pin Number	Pin Name	Pin Description
1	VS(U)	U-phase high side floating IC supply offset voltage
2	VB(U)	U-phase high side floating IC supply voltage
3	VS(V)	V-phase high side floating IC supply offset voltage
4	VB(V)	V-phase high side floating IC supply voltage
5	VS(W)	W-phase high side floating IC supply offset voltage
6	VB(W)	W-phase high side floating IC supply voltage
7	HIN(U)	U-phase high side gate driver input
8	HIN(V)	V-phase high side gate driver input
9	HIN(W)	W-phase high side gate driver input
10	LIN(U)	U-phase low side gate driver input
11	LIN(V)	V-phase low side gate driver input
12	LIN(W)	W-phase low side gate driver input
13	VDD	Low side control supply
14	VFO	Fault output / Temperature monitor
15	ITRIP	Over current shutdown input
16	VSS	Low side control negative supply
17	NW	W-phase low side emitter
18	NV	V-phase low side emitter
19	NU	U-phase low side emitter
20	W	Motor W-phase output
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No Connection

Pin Description

HIN(U,V,W) and LIN(U,V,W) (Low side and high side control pins, Pin 7 - 12)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 5kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN} . The filter acts according to Figure 4.

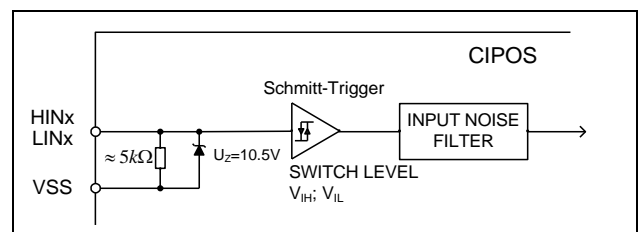


Figure 3: Input pin structure

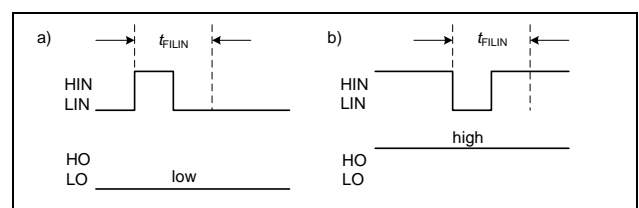


Figure 4: Input filter timing diagram

It is recommended for proper work of CIPOS not to provide input pulse-width lower than 1us.

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 380ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

VFO (Fault-output and NTC, Pin 14)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP. A pull-up resistor is externally required to bias the NTC.

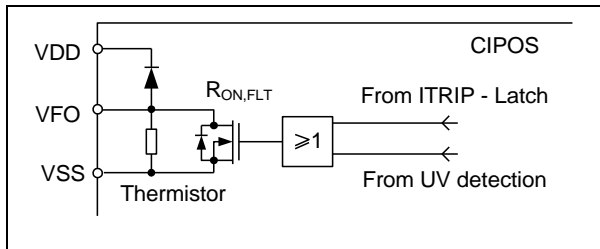


Figure 5: Internal circuit at pin VFO

The same pin provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5V ensures, that the resulting voltage can be directly connected to the microcontroller.

ITRIP (Over current detection function, Pin 15)

CIPOS provides an over current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ. 0.47V) is referenced to VSS ground. A input noise filter (typ: $t_{TRIPMIN} = 530ns$) prevents the driver to detect false over-current events.

Over current detection generates a shut down of all outputs of the gate driver after the shutdown propagation delay of typically 1000ns. The fault-clear time is set to typical 65us.

VDD, VSS (Low side control supply and reference, Pin 13, 16)

VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 12.1V$ is present.

The IC shuts down all the gate drivers' power outputs, when the VDD supply voltage is below

$V_{DDUV-} = 10.4V$. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB(U,V,W) and VS(U,V,W) (High side supplies, Pin 1 - 6)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 12.1V$ and a falling threshold of $V_{BSUV-} = 10.4V$.

VS(U,V,W) provide a high robustness against negative voltage in respect of VSS of -50V transiently. This ensures very stable designs even under rough conditions.

NW, NV, NU (Low side emitter, Pin 17 - 19)

The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

W, V, U (High side emitter and low side collector, Pin 20 - 22)

These pins are motor U, V, W input pins

P (Positive bus input voltage, Pin 23)

The high sides of IGBT are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

Absolute Maximum Ratings

($V_{DD} = 15V$ and $T_C = 25^\circ C$, if not stated otherwise)

Module Section

Description	Condition	Symbol	Value		Unit
			min	max	
Storage temperature range		T_{stg}	-40	125	$^\circ C$
Insulation test voltage	RMS, $f = 60Hz$, $t = 1min$	V_{ISOL}	2000	-	V
Operating case temperature range	Refer to Figure 6	T_C	-40	100	$^\circ C$

Inverter Section

Description	Condition	Symbol	Value		Unit
			min	max	
Max. blocking voltage	$I_C = 250\mu A$	V_{CES}	600	-	V
DC link supply voltage of P-N	Applied between P-N	V_{PN}	-	450	V
DC link supply voltage (surge) of P-N	Applied between P-N	$V_{PN(surge)}$	-	500	V
Output current	$T_C = 25^\circ C, T_J < 150^\circ C$ $T_C = 80^\circ C, T_J < 150^\circ C$	I_C	-20 -15	20 15	A
Maximum peak output current	less than 1ms	I_C	-40	40	A
Short circuit withstand time ¹	$V_{DC} \leq 400V, T_J = 150^\circ C$	t_{SC}	-	5	μs
Power dissipation per IGBT		P_{tot}	-	58.6	W
Operating junction temperature range		T_J	-40	150	$^\circ C$
Single IGBT thermal resistance, junction-case		R_{thJC}	-	2.13	K/W
Single diode thermal resistance, junction-case		R_{thJCD}	-	3.42	K/W

Control Section

Description	Condition	Symbol	Value		Unit
			min	max	
Module supply voltage		V_{DD}	-1	20	V
High side floating supply voltage (VB vs. VS)		V_{BS}	-1	20	V
Input voltage	LIN, HIN, ITRIP	V_{IN} V_{ITRIP}	-1 -1	10	V
Switching frequency		f_{PWM}	-	20	kHz

¹ Allowed number of short circuits: <1000; time between short circuits: > 1s.

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		min	typ	max	
DC link supply voltage of P-N	V_{PN}	0	-	400	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	13.5	-	18.5	V
Low side supply voltage	V_{DD}	14.5	16	18.5	V
Control supply variation	ΔV_{BS}	-1	-	1	V/ μ s
	ΔV_{DD}	-1	-	1	
Logic input voltages LIN,HIN,ITRIP	V_{IN}	0	-	5	V
	V_{ITRIP}	0	-	5	
Between VSS - N (including surge)	V_{SS}	-5	-	5	V

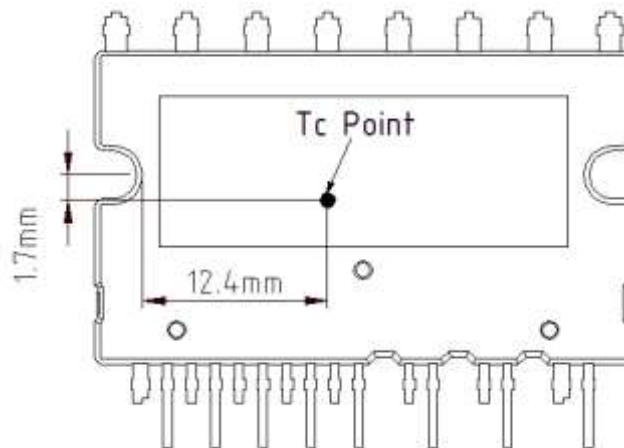


Figure 6: T_c measurement point¹

¹Any measurement except for the specified point in figure 6 is not relevant for the temperature verification and brings wrong or different information.

Static Parameters

($V_{DD} = 15V$ and $T_C = 25^\circ C$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Collector-Emitter saturation voltage	$I_{out} = 10A, T_J = 25^\circ C$ $150^\circ C$	$V_{CE(sat)}$	- -	1.55 1.85	2.1 -	V
Emitter-Collector forward voltage	$I_{out} = -10A, T_J = 25^\circ C$ $150^\circ C$	V_F	- -	1.75 1.8	2.45 -	V
Collector-Emitter leakage current	$V_{CE} = 600V$	I_{CES}	-	-	1	mA
Logic "1" input voltage (LIN,HIN)		V_{IH}	-	2.1	2.5	V
Logic "0" input voltage (LIN,HIN)		V_{IL}	0.7	0.9	-	V
ITRIP positive going threshold		$V_{IT,TH+}$	400	470	540	mV
ITRIP input hysteresis		$V_{IT,HYS}$	40	70	-	mV
V_{DD} and V_{BS} supply under voltage positive going threshold		V_{DDUV+} V_{BSUV+}	10.8	12.1	13.0	V
V_{DD} and V_{BS} supply under voltage negative going threshold		V_{DDUV-} V_{BSUV-}	9.5	10.4	11.2	V
V_{DD} and V_{BS} supply under voltage lockout hysteresis		V_{DDUVH} V_{BSUVH}	1.0	1.7	-	V
Quiescent V_{Bx} supply current (V_{Bx} only)	$H_{IN} = 0V$	I_{QBS}	-	300	500	μA
Quiescent VDD supply current (VDD only)	$L_{IN} = 0V, H_{INX} = 5V$	I_{QDD}	-	370	900	μA
Input bias current	$V_{IN} = 5V$	I_{IN+}	-	1	1.5	mA
Input bias current	$V_{IN} = 0V$	I_{IN-}	-	2	-	μA
ITRIP input bias current	$V_{ITRIP} = 5V$	I_{ITRIP+}	-	65	150	μA
VFO input bias current	$V_{FO} = 5V, V_{ITRIP} = 0V$	I_{FO}	-	60	-	μA
VFO output voltage	$I_{FO} = 10mA, V_{ITRIP} = 1V$	V_{FO}	-	0.5	-	V

Dynamic Parameters

($V_{DD} = 15V$ and $T_C = 25^\circ C$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Turn-on propagation delay time	$V_{LIN,HIN} = 5V,$ $I_{out} = 10A,$ $V_{DC} = 300V$	t_{on}	-	680	-	ns
Turn-on rise time		t_r	-	30	-	ns
Turn-on switching time		$t_{c(on)}$	-	220	-	ns
Reverse recovery time		t_{rr}	-	60	-	ns
Turn-off propagation delay time	$V_{LIN,HIN} = 0V,$ $I_{out} = 10A,$ $V_{DC} = 300V$	t_{off}	-	950	-	ns
Turn-off fall time		t_f	-	55	-	ns
Turn-off switching time		$t_{c(off)}$	-	120	-	ns
Short circuit propagation delay time	From $V_{IT,TH+}$ to 10% I_{SC}	t_{SCP}	-	1250	-	ns
Input filter time ITRIP	$V_{ITRIP} = 1V$	$t_{ITRIPmin}$	-	530	-	ns
Input filter time at LIN, HIN for turn on and off	$V_{LIN,HIN} = 0V \text{ \& } 5V$	t_{FILIN}	-	290	-	ns
Fault clear time after ITRIP-fault	$V_{ITRIP} = 1V$	t_{FLTCLR}	40	65	200	μs
Deadtime between low side and high side		DT_{PWM}	1.5	-	-	μs
Deadtime of gate drive circuit		DT_{IC}	-	380	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	$V_{DC} = 300V, T_J = 25^\circ C$ $I_C = 10A \quad 150^\circ C$	E_{on}	-	400	-	μJ
			-	490	-	
IGBT turn-off energy	$V_{DC} = 300V, T_J = 25^\circ C$ $I_C = 10A \quad 150^\circ C$	E_{off}	-	190	-	μJ
			-	290	-	
Diode recovery energy	$V_{DC} = 300V, T_J = 25^\circ C$ $I_C = 10A \quad 150^\circ C$	E_{rec}	-	55	-	μJ
			-	70	-	

Bootstrap Parameters

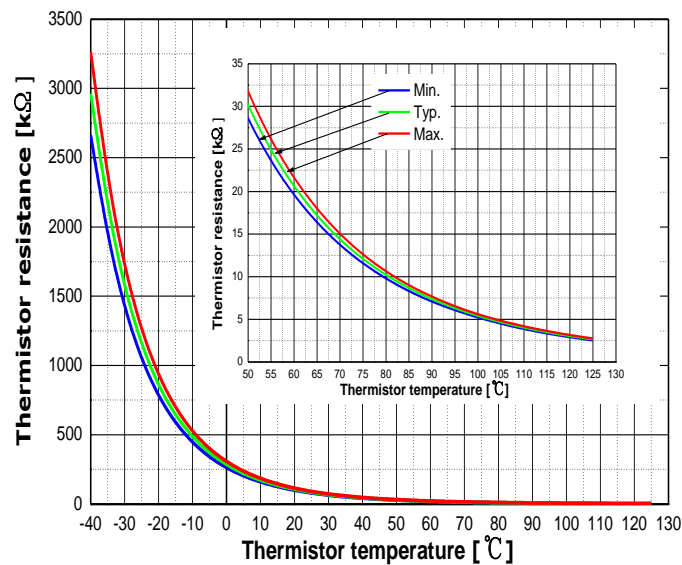
($T_C = 25^\circ C$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Repetitive peak reverse voltage		V_{RRM}	600			V
Bootstrap resistance of U-phase ¹	$VS2 \text{ or } VS3 = 300V, T_J = 25^\circ C$	R_{BS1}	-	35	-	Ω
	$VS2 \text{ and } VS3 = 0V, T_J = 25^\circ C$		-	40	-	
	$VS2 \text{ or } VS3 = 300V, T_J = 125^\circ C$		-	50	-	
	$VS2 \text{ and } VS3 = 0V, T_J = 125^\circ C$		-	65	-	
Reverse recovery time	$I_F = 0.6A, di/dt=80A/\mu s$	t_{rr_BS}	-	50	-	ns
Forward voltage drop	$I_F = 20mA, VS2 \text{ and } VS3 = 0V$	V_{F_BS}	-	2.6	-	V

¹ R_{BS2} and R_{BS3} have same values to R_{BS1} .

Thermistor

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Resistor	$T_{NTC} = 25^{\circ}C$	R_{NTC}	-	85	-	k Ω
B-constant of NTC (Negative temperature coefficient)		B(25/100)	-	4092	-	K



T [°C]	Rmin. [k Ω]	Rtyp. [k Ω]	Rmax. [k Ω]
50	28.400	29.972	31.545
60	19.517	20.515	21.514
70	13.670	14.315	14.960
80	9.745	10.169	10.593
90	7.062	7.345	7.628
100	5.199	5.388	5.576
110	3.856	4.009	4.163
120	2.900	3.024	3.149
125	2.527	2.639	2.751

Figure 7: Thermistor resistance – temperature curve and table
(For more information, please refer to the application note ‘AN CIPOS-mini 1 Technical description’)

Mechanical Characteristics and Ratings

Description	Condition	Value			Unit
		min	typ	max	
Mounting torque	M3 screw and washer	0.49	-	0.78	Nm
Flatness	Refer to Figure 7	-50	-	100	μ m
Weight		-	6.58	-	g

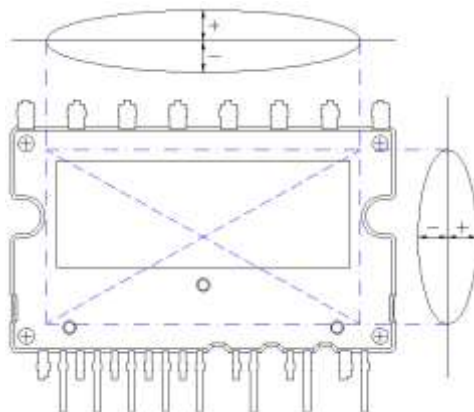


Figure 8: Flatness measurement position

Circuit of a Typical Application

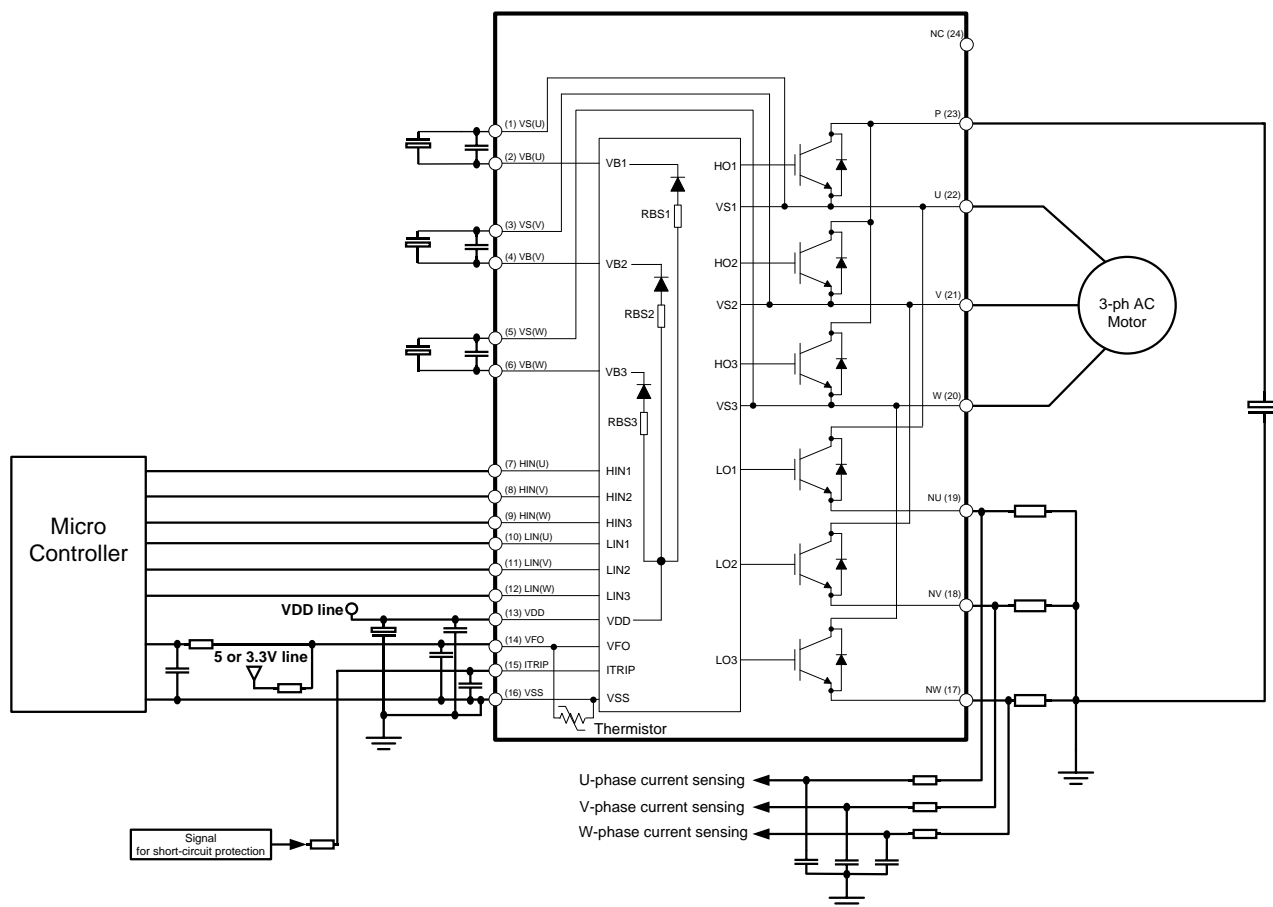


Figure 9: Application circuit

Switching Times Definition

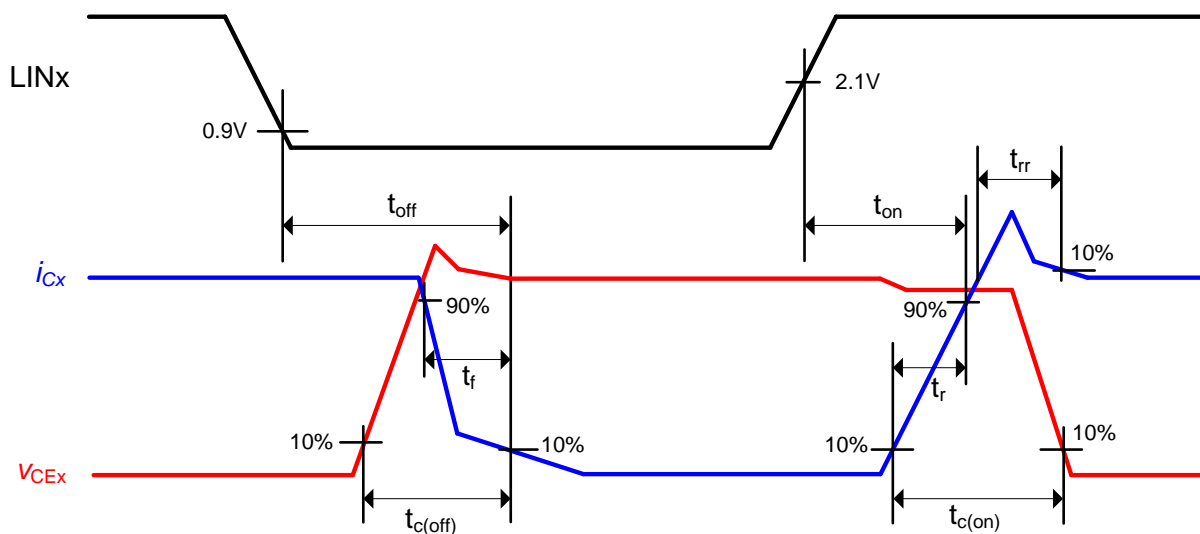
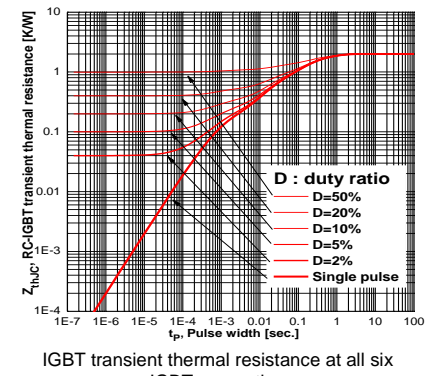
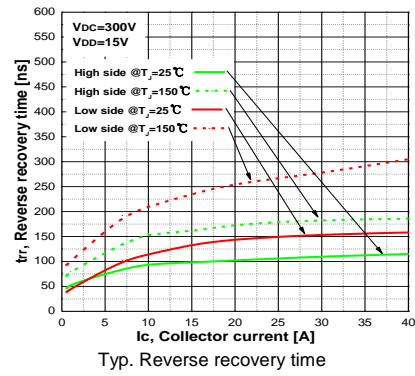
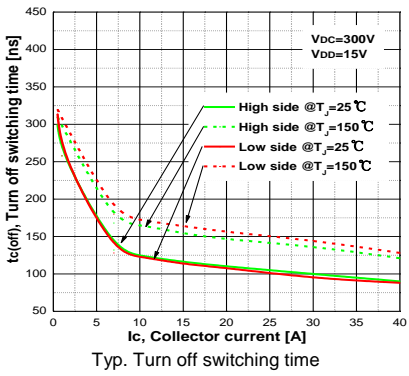
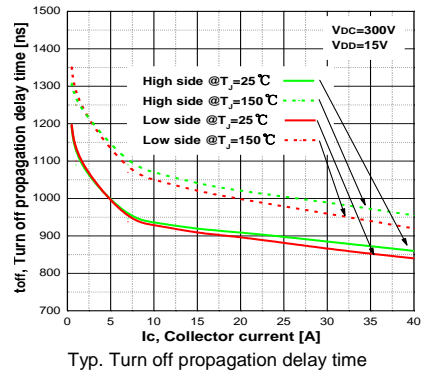
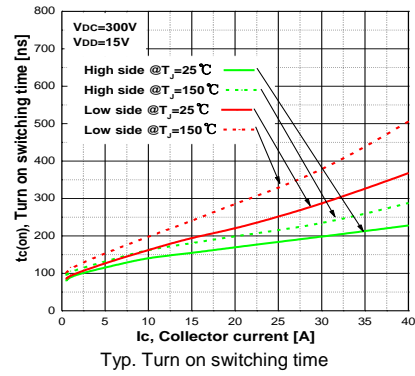
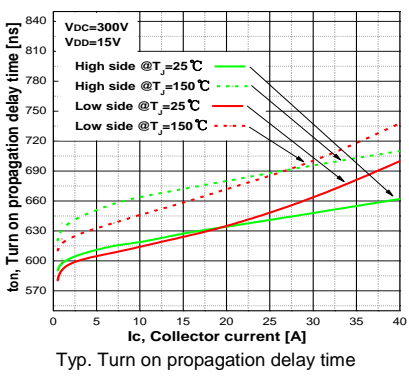
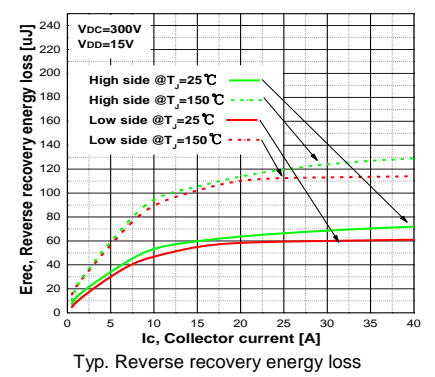
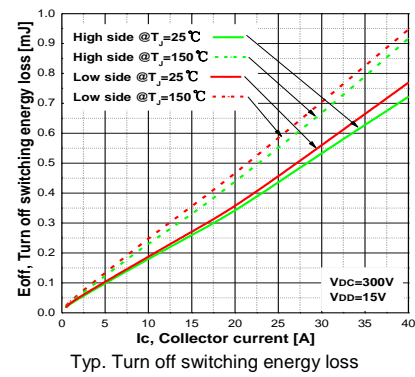
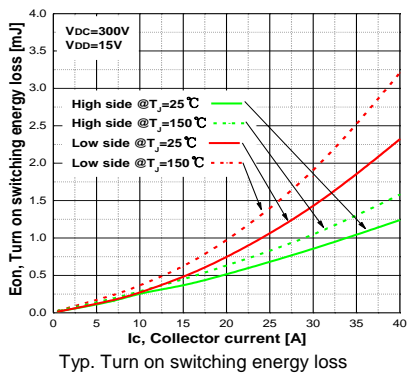
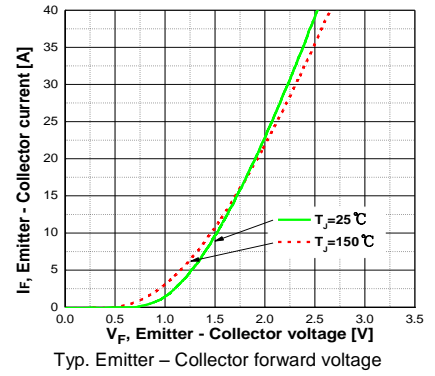
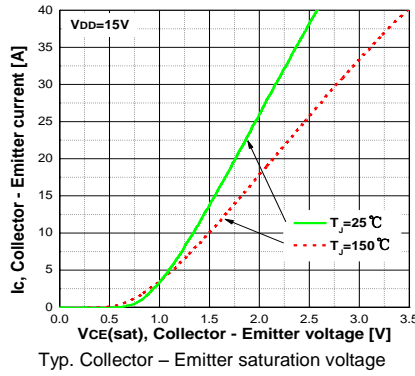
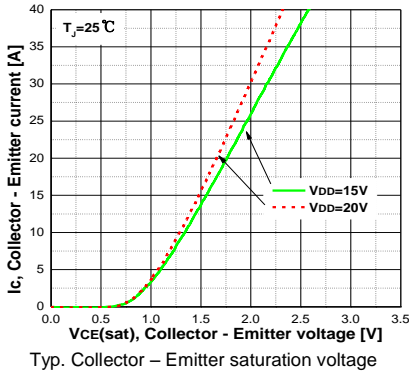
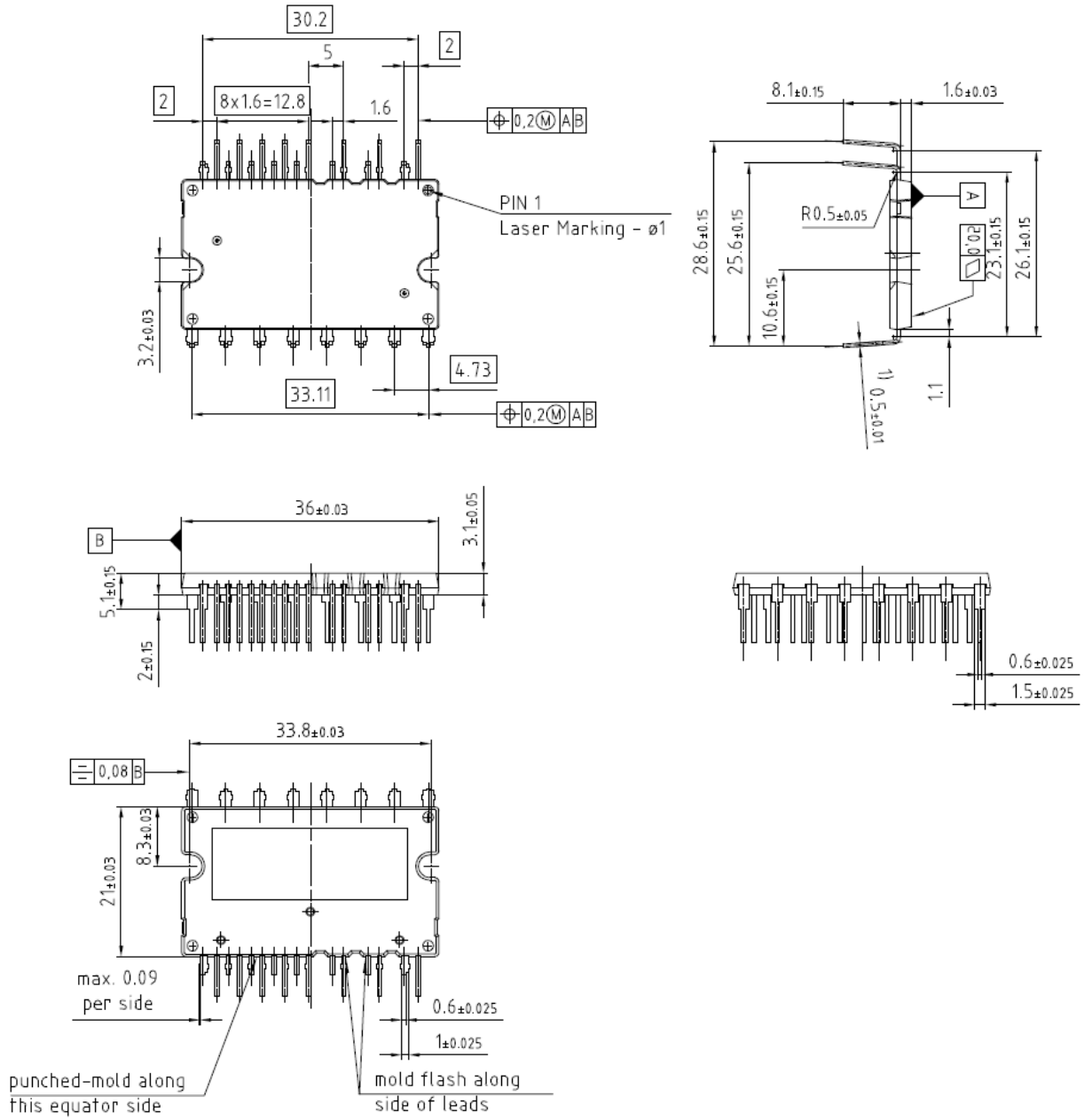


Figure 10: Switching times definition

Electrical characteristic



Package Outline



Revision History

Major changes since the last revision

Page or Reference	Description of change

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBLADE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SiL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. ANSI™ of American National Standards Institute. AUTOSAR™ of AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. HYPERTERMINAL™ of Hilgraeve Incorporated. MCS™ of Intel Corp. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ of Openwave Systems Inc. RED HAT™ of Red Hat, Inc. RFMD™ of RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex.

Last Trademarks Update 2014-07-17

www.infineon.com

Edition 2014-06-01
Published by
Infineon Technologies AG
81726 München, Germany

© Infineon Technologies AG 2015.
All Rights Reserved.

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffungsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.