

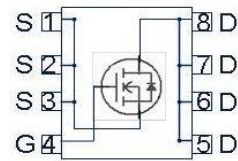
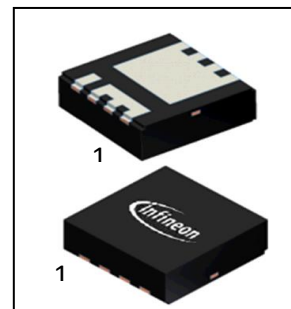
OptiMOS™ -5 Power-Transistor

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	13	mΩ
I_D	40	A

Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

PG-TSDSON-8-33


Type	Package	Marking
IAUZ40N10S5N130	PG-TSDSON-8-33	5N1N130

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾²⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{V}$	40	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{V}$	35	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=20\text{A}$	60	mJ
Avalanche current, single pulse	I_{AS}	-	22	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$ $T_J=175\text{ °C}$	68	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.2	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm ² cooling area ³⁾	-	-	62	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=27\mu A$	2.2	3.0	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6V, I_D=10A$	-	14	17	$m\Omega$
		$V_{GS}=10V, I_D=20A$	-	10.8	13	
Gate resistance ²⁾	R_G		-	1.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$	-	1173	1525	pF
Output capacitance	C_{oss}		-	197	256	
Reverse transfer capacitance	C_{rss}		-	11	17	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V,$ $I_D=40A, R_G=3.5\Omega$	-	4	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	6	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=50V, I_D=20A,$ $V_{GS}=0 \text{ to } 10V$	-	5.5	7.2	nC
Gate to drain charge	Q_{gd}		-	3.7	6.0	
Gate charge total	Q_g		-	17	24	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	40	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	160	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=20A,$ $T_j=25^\circ C$	-	0.9	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40V, I_F=40A,$ $di_F/dt=100A/\mu s$	-	40	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	39	-	nC

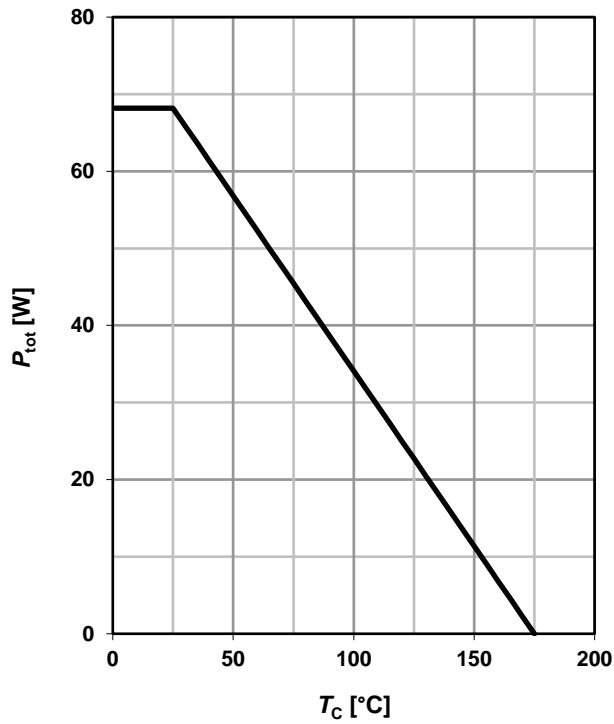
¹⁾ Current is limited by package; with an $R_{thJC} = 2.2K/W$ the chip is able to carry 50A at 25°C.

²⁾ The parameter is not subject to production test- verified by design/characterization.

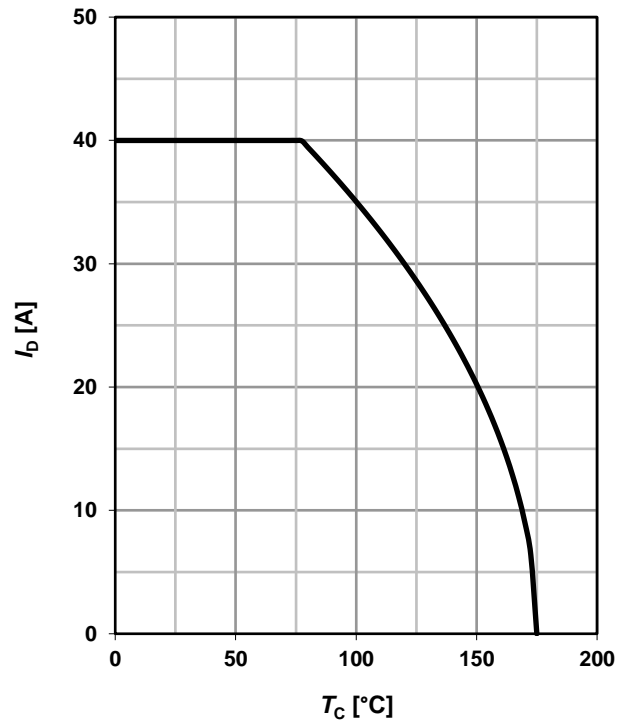
³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

1 Power dissipation

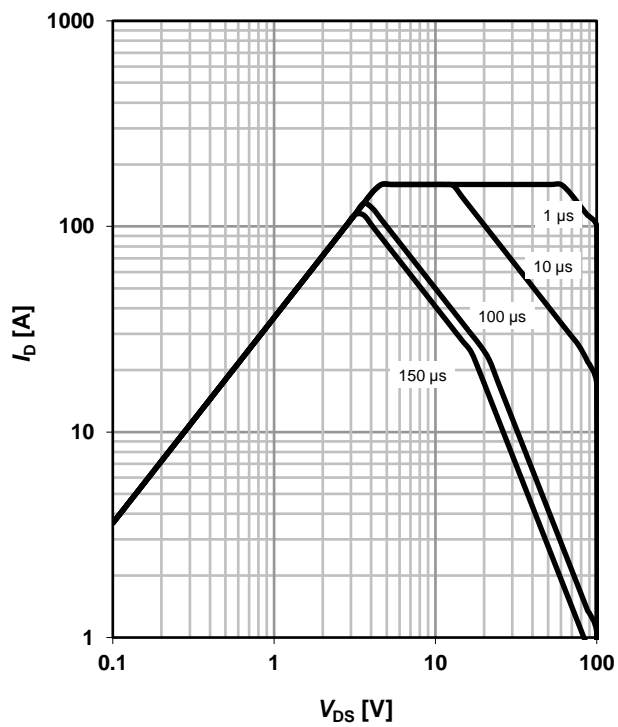
$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


2 Drain current

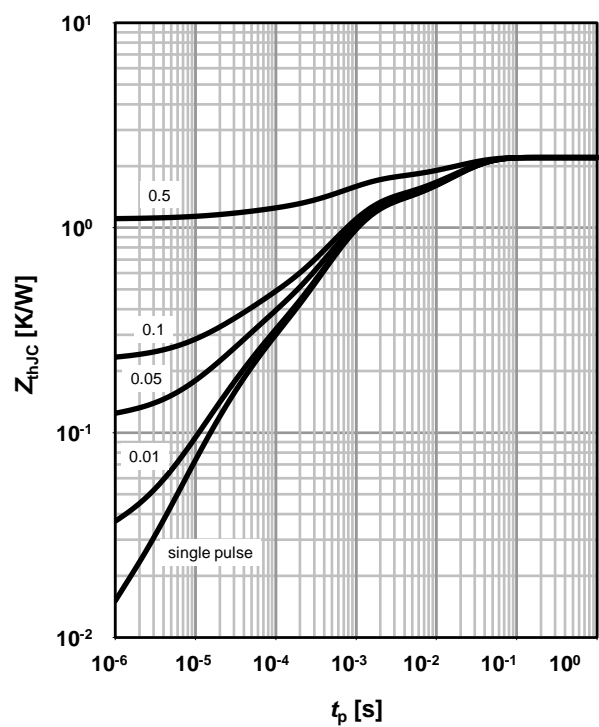
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


3 Safe operating area

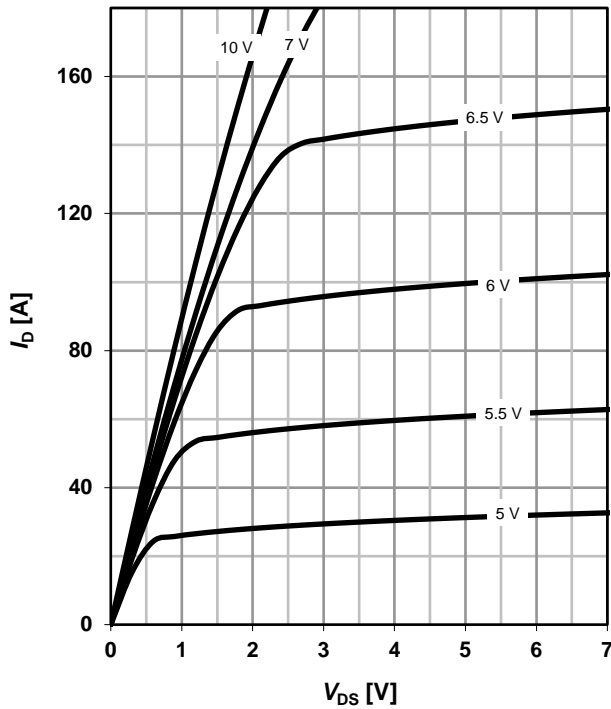
$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

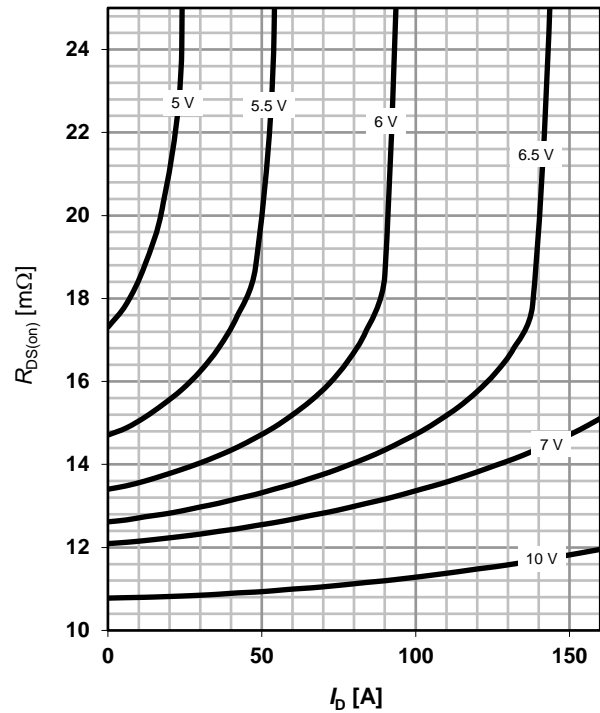
 parameter: t_p

4 Max. transient thermal impedance

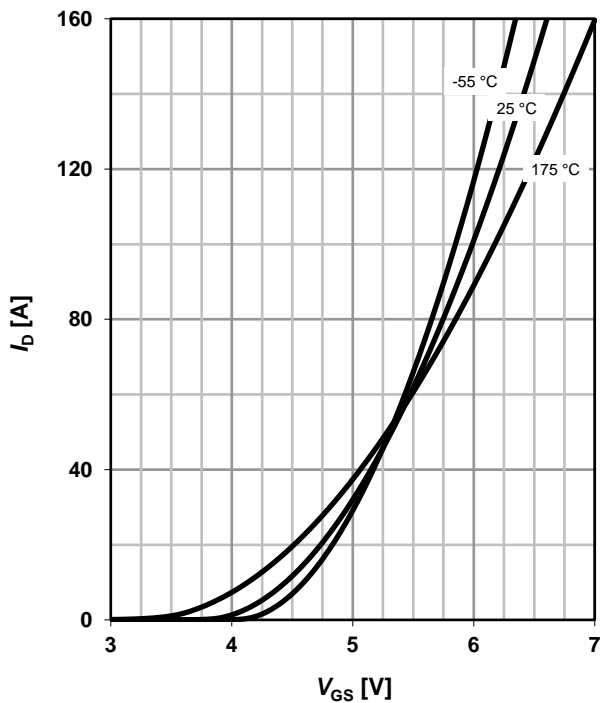
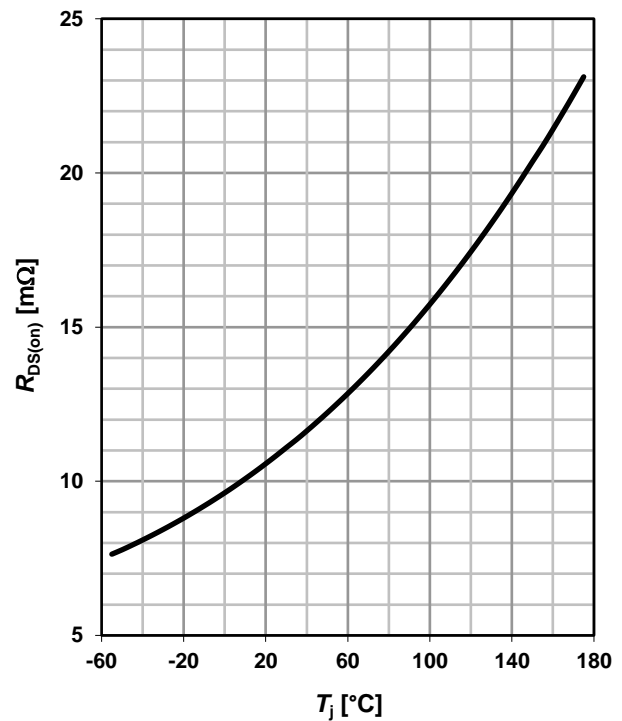
$$Z_{\text{thJC}} = f(t_p)$$

 parameter: $D = t_p/T$


5 Typ. output characteristics
 $I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

 parameter: V_{GS}

6 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

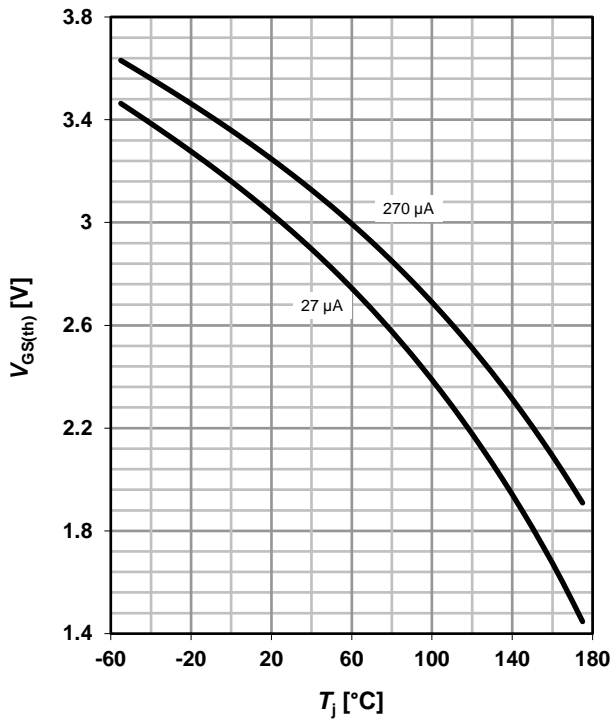
 parameter: V_{GS}

7 Typ. transfer characteristics
 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

 parameter: T_j

8 Typ. drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 20\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

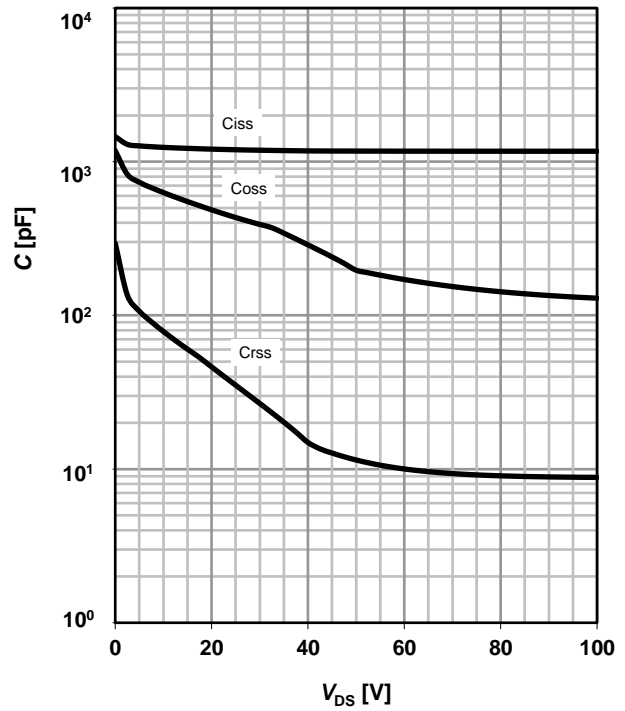
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

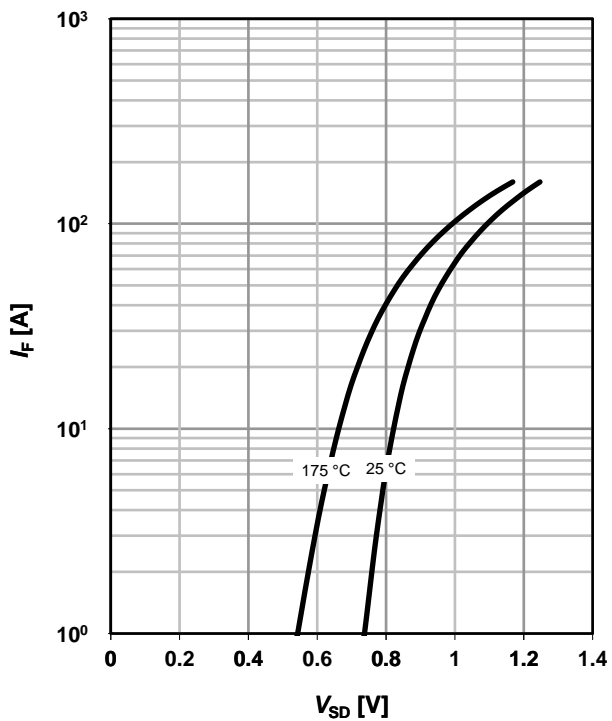
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

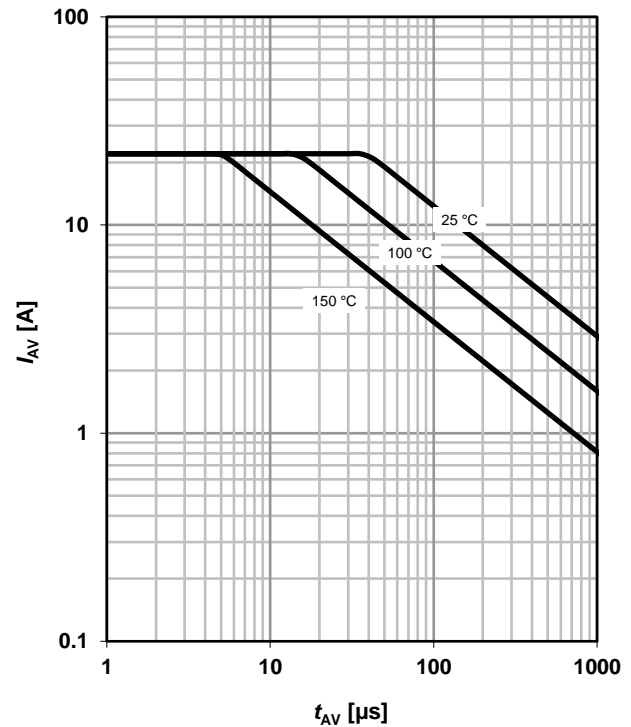
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

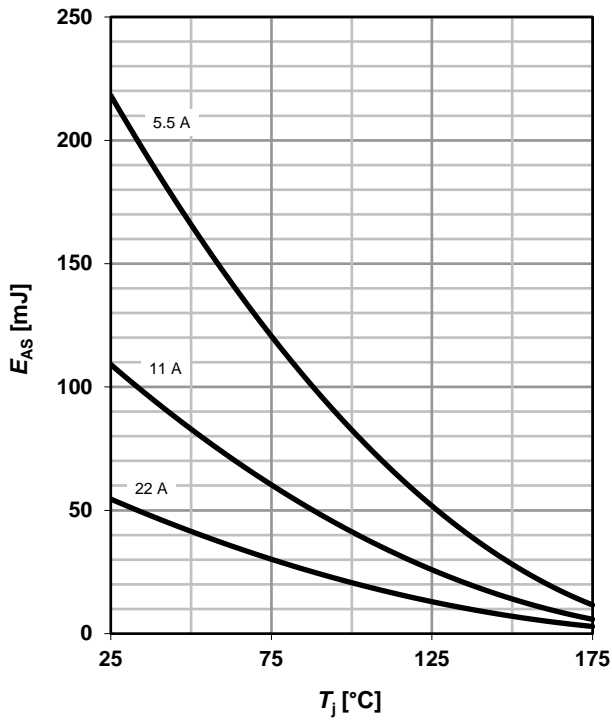
parameter: $T_{j(start)}$



13 Avalanche energy

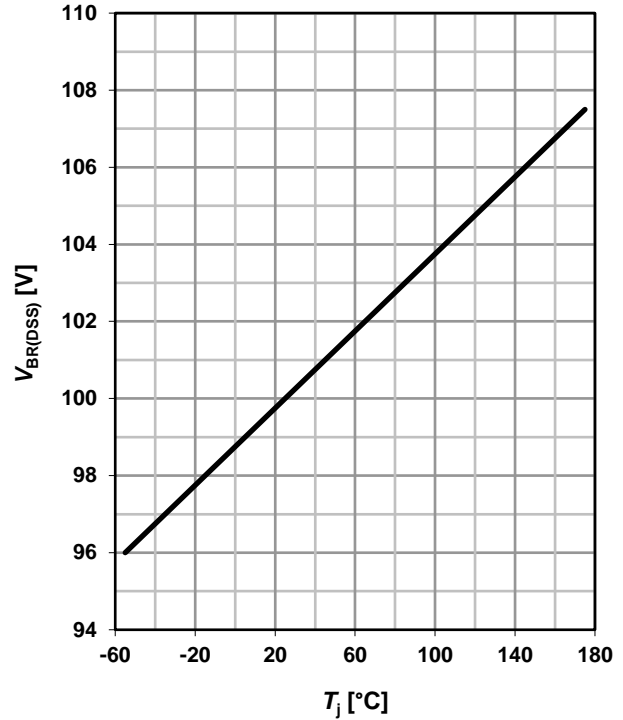
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

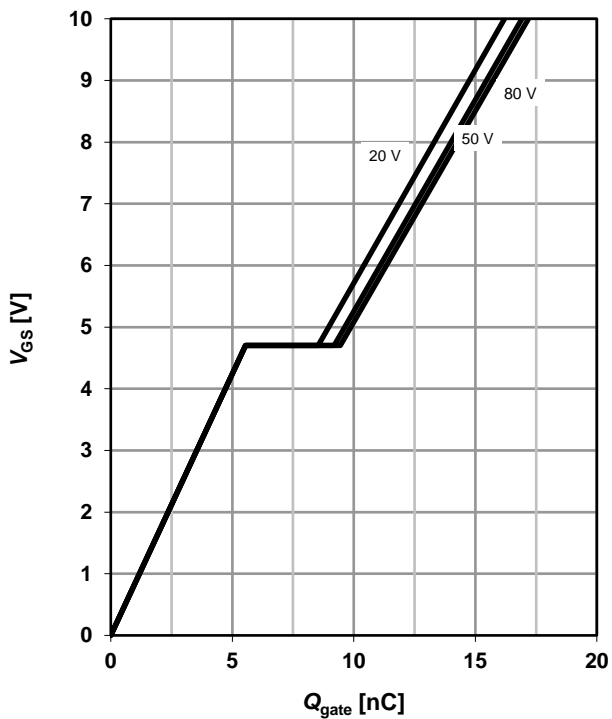
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



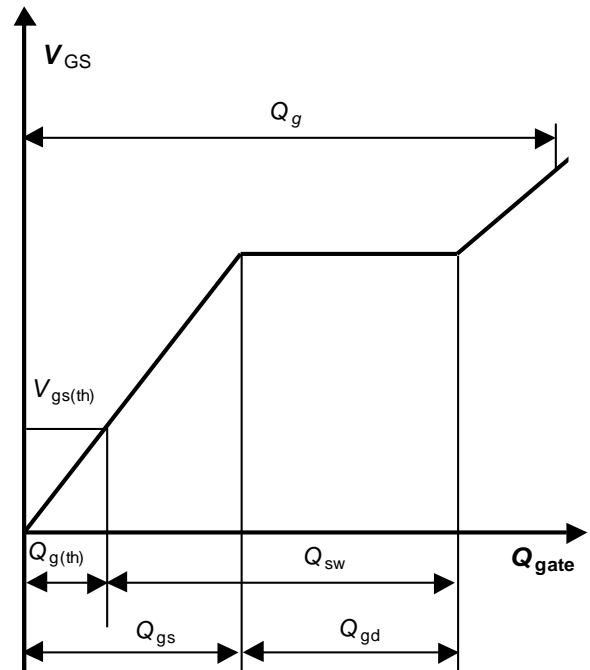
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

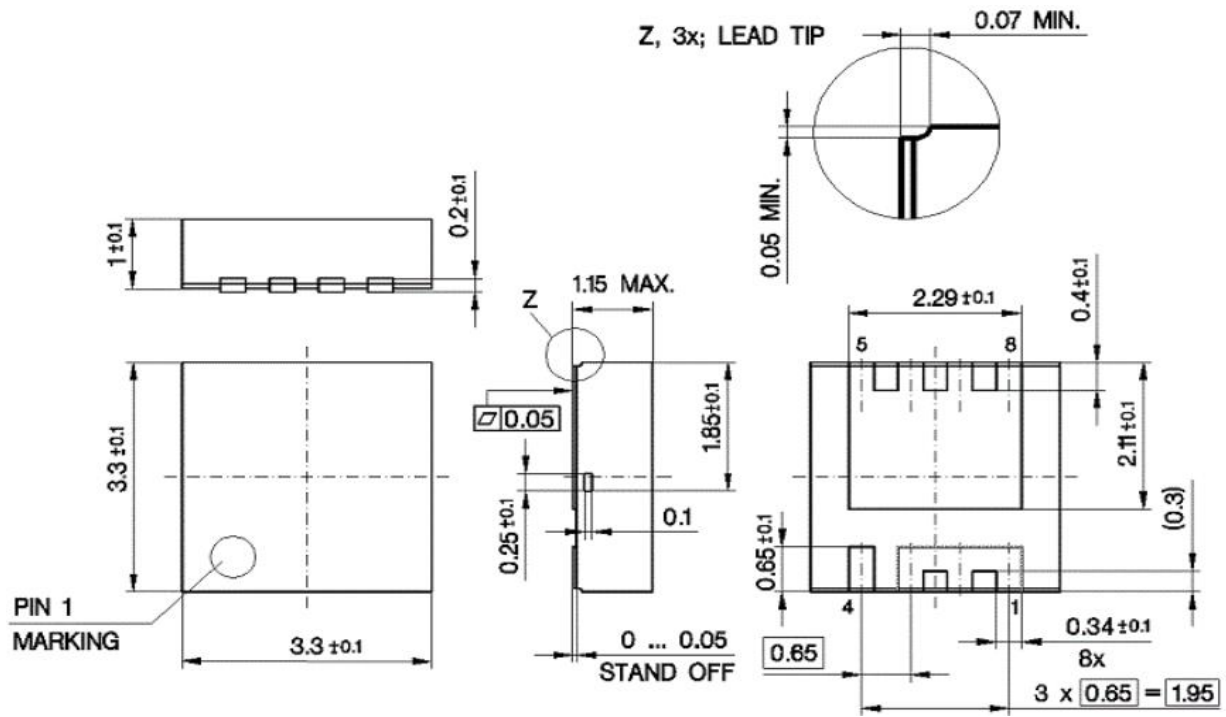
parameter: V_{DD}



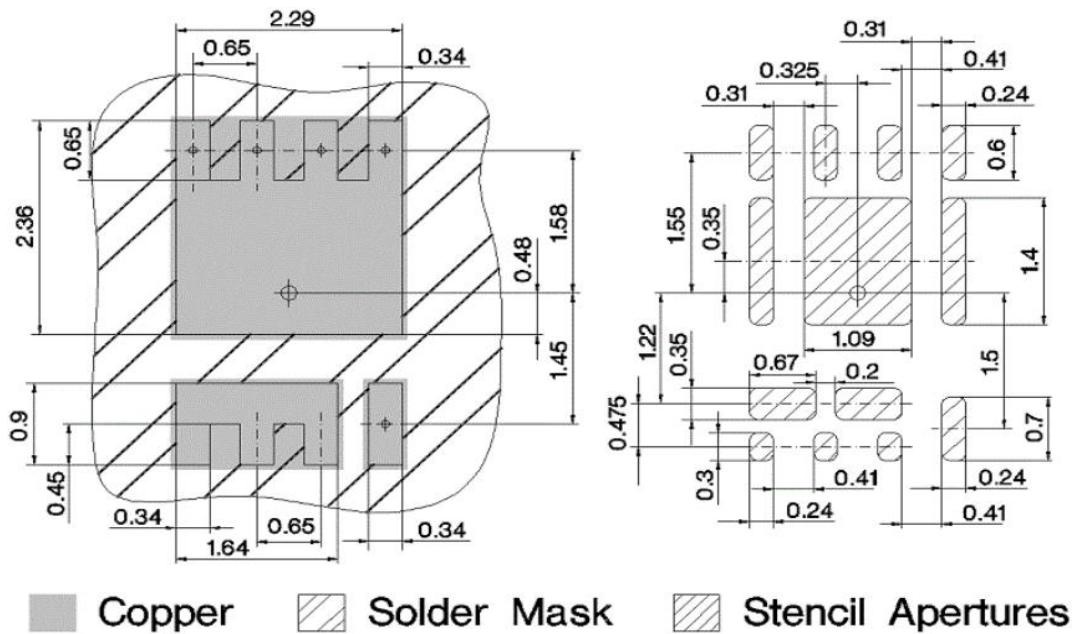
16 Gate charge waveforms



PG-TSDSON-8: Outline

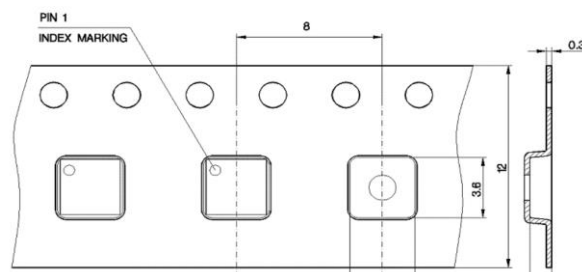


Footprint



Dimensions in mm

Packaging



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	23.07.2019	Final Data Sheet