5-V CAN TRANSCEIVER WITH I/O LEVEL ADAPTING AND LOW-POWER MODE SUPPLY OPTIMIZATION

Check for Samples: SN65HVDA540-Q1, SN65HVDA541-Q1, SN65HVDA542-Q1, SN65HVDA540-5-Q1, SN65HVDA541-5-Q1, SN65HVDA542-5-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Meets or Exceeds the Requirements of ISO 11898-2 and ISO 11898-5**
- **GIFT/ICT Compliant**
- **ESD Protection up to ±12 kV (Human-Body Model) on Bus Pins**
- **I/O Voltage Level Adapting**
  - **SN65HVDA54x: Adaptable I/O Voltage Range (V_{IO}) From 3 V to 5.33 V**
  - **SN65HVDA54x-5: 5 V V_{CC} Device Version**
- **Operating Modes:**
  - **Normal Mode: All Devices**
  - **Low Power Standby Mode (V_{CC} not required, only V_{IO} Supply Needed Saving System Power)**
    - **SN65HVDA540: No Wake Up**
    - **SN65HVDA541: RXD Wake Up Request**
  - **Silent (Receive Only) Mode: SN65HVDA542**
- **High Electromagnetic Compliance (EMC)**
- **Protection**
  - **Undervoltage Protection on V_{IO} and V_{CC}**
  - **Bus-Fault Protection of –27 V to 40 V**
  - **TXD Dominant State Time Out**
  - **RXD Wake Up Request Lock Out on CAN Bus Stuck Dominant Fault (SN65HVDA541)**
  - **Thermal Shutdown Protection**
  - **Power-Up/Down Glitch-Free Bus I/O**
  - **High Bus Input Impedance When Unpowered (No Bus Load)**

APPLICATIONS

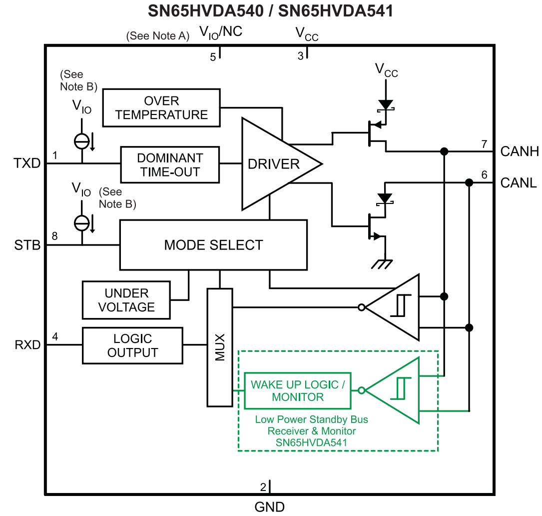
- **SAE J2284 High-Speed CAN for Automotive Applications**
- **SAE J1939 Standard Data Bus Interface**
- **GMW3122 Dual-Wire CAN Physical Layer**
- **ISO 11783 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**

DESCRIPTION

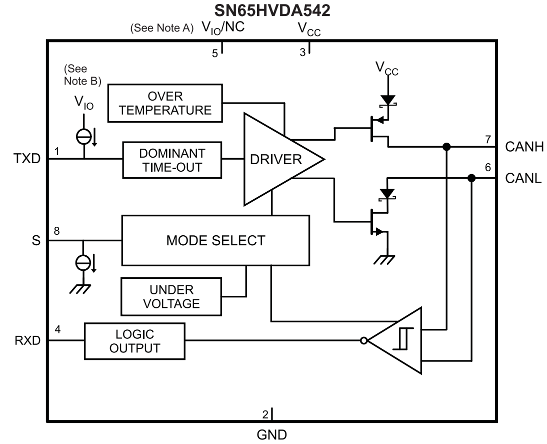
The device is designed and qualified for use in automotive applications and meets or exceeds the specifications of the ISO 11898 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver).

FUNCTIONAL BLOCK DIAGRAM

SN65HVDA540 / SN65HVDA541



SN65HVDA542



A. SN65HVDA54x devices pin 5 is V_{IO}. SN65HVDA54x-5 devices pin 5 is NC and V_{IO} is internally connected to V_{CC}.

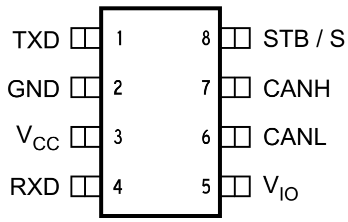
B. SN65HVDA54x-5 devices: V_{IO} is internally connected to V_{CC}

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

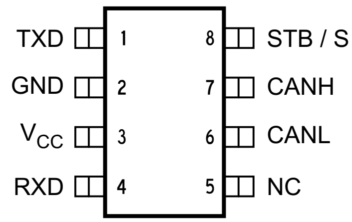
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SN65HVDA54x
D PACKAGE
(TOP VIEW)



SN65HVDA54x-5
D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	D Package (SOIC) NO.		
TXD	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
GND	2	GND	Ground connection
V_{CC}	3	Supply	Transceiver 5V supply voltage
RXD	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
V_{IO} / NC	5	Supply	HVDA54x: Transceiver logic level (IO) supply voltage HVDA54x-5: No connect
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
STB / S	8	I	Mode select: STB, Standby mode (SN65HVDA540/541) select pin (active high) S, Silent mode (SN65HVDA542) select pin (active high)

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	HVDA540QDRQ1	H540Q
			HVDA541QDRQ1	H541Q
			HVDA542QDRQ1	H542Q
			HVDA5405QDRQ1	H5405Q
			HVDA5415QDRQ1	H5415Q
			HVDA5425QDRQ1	H5425Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL DESCRIPTION

Generaral Description

The device meets or exceeds the specifications of the ISO 11898 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver). This device provides CAN transceiver functions: differential transmit capability to the bus and differential receive capability at data rates up to 1 megabit per second (Mbps). The device includes many protection features providing device and CAN network robustness.

Operating Modes

The device has two main operating modes: normal mode (all devices) and standby mode (SN65HVDA540 / 541) or silent mode (SN65HVDA542). Operating mode selection is made via the STB (SN65HVDA540 / 541) or the S (SN65HVDA542) input pin.

Table 1. Operating Modes

DEVICE	STB / S	MODE	DRIVER	RECEIVER	RXD Pin
All Devices	LOW	Normal Mode	Enabled (On)	Enabled (On)	Mirrors bus state(1)
SN65HVDA540	HIGH	Standby Mode (No Wake Up)	Disabled (Off)	Disabled (Off)	Recessive (HIGH)
SN65HVDA541	HIGH	Standby Mode (RXD Wake Up Request)	Disabled (Off)	Low power wake-up receiver and bus monitor enabled	Mirrors bus state via wake-up filter(2)
SN65HVDA542	HIGH	Silent Mode	Disabled (Off)	Enabled (On)	Mirrors bus state(1)

(1) Mirrors bus state: LOW if CAN bus is dominant, HIGH if CAN bus is recessive.
(2) See Figure 3 and Figure 4 for operation of the low power wake up receiver and bus monitor for RXD Wake Up Request behavior and Table 3 for the wake up receiver threshold levels.

Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic LOW) where the bus lines are driven differentially apart or recessive (logic HIGH) where the bus lines are biased to $V_{CC}/2$ via the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low power standby mode where the bus lines will be biased to GND via the high-ohmic internal input resistors R_{IN} of the receiver.

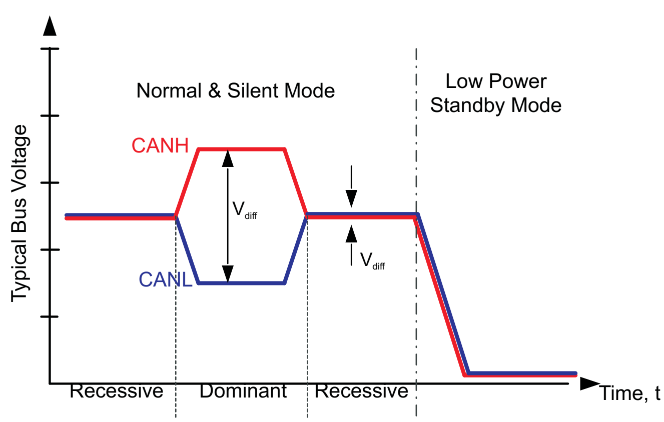


Figure 1. Bus States (Physical Bit Representation)

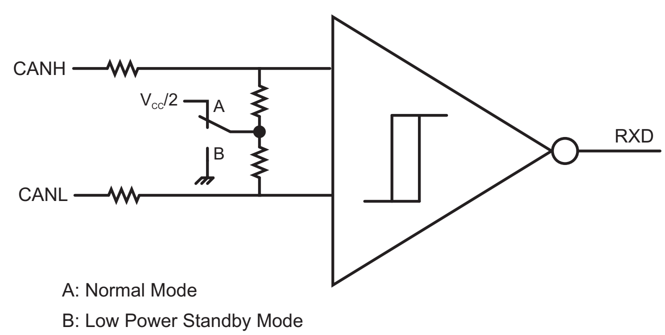


Figure 2. Simplified Common Mode Bias and Receiver Implementation

Normal Mode

This is the normal operating mode of the device. It is selected by setting STB or S low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the CAN bus pins (CANH and CANL) are biased to 0.5 × V_{CC}. In dominant state the bus pins are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

Standby Mode (SN65HVDA540)

This is the low power mode of the device. It is selected by setting STB high. The CAN driver and receiver are turned off and bi-directional CAN communication is not possible. There is no wake up capability in the SN65HVDA540, the RXD pin will remain recessive (high) while the device is in standby mode. This state is supplied via the V_{IO} supply, thus the V_{CC} (5V) supply may be turned off for additional power savings at the system level. The local protocol controller (MCU) should reactivate the device to normal mode to enable communication via the CAN bus. The 5 V (V_{CC}) supply needs to be reactivated by the local protocol controller to resume normal mode if it has been turned off for low-power standby operation. The CAN bus pins are weakly pulled to GND, see Figure 1 and Figure 2.

Standby Mode with RXD Wake Up-Request (SN65HVDA541)

This is the low power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bi-directional CAN communication is not possible. The low power receiver and bus monitor, both supplied via the V_{IO} supply, are enabled to allow for RXD wake up requests via the CAN bus. The V_{CC} (5V) supply may be turned off for additional power savings at the system level. A wake up request will be output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake up request. The 5 V (V_{CC}) supply needs to be reactivated by the local protocol controller to resume normal mode if it has been turned off for low-power standby operation. The CAN bus pins are weakly pulled to GND, see Figure 1 and Figure 2.

RXD Wake Up Request Lock Out for Bus Stuck Dominant Fault (SN65HVDA541)

If the bus has a fault condition where it is stuck dominant while the SN65HVDA541 is placed into standby mode via the STB pin, the device locks out the RXD wake up request until the fault has been removed to prevent false wake up signals in the system.

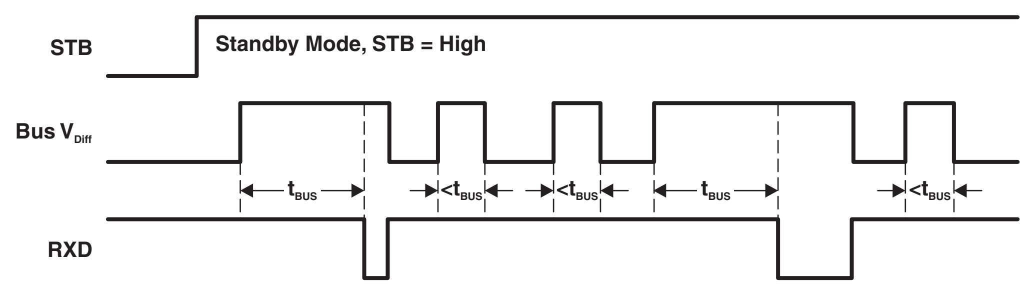


Figure 3. SN65HVDA541 RXD Wake Up Request With No Bus Fault Condition

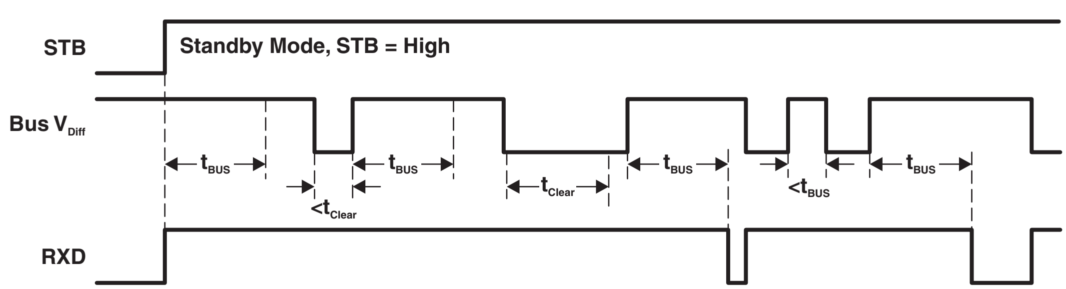


Figure 4. SN65HVDA541 RXD Wake Up Request Lock Out When Bus Dominant Fault Condition

Silent (Receive Only) Mode (SN65HVDA542)

This is the silent (receive only) mode of the device. It is selected by setting S high. The CAN driver is turned off while the receiver remains active and RXD will output the received bus state. There is no low power mode in the SN65HVDA542 except for V_{CC} and V_{IO} supply undervoltage conditions (see Undervoltage Lockout / Unpowered Device section of the datasheet).

Driver and Receiver Function Tables

Table 2. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	STB / S(1)	TXD(1)	CANH(1)	CANL(1)	
All Devices	L	L	H	L	Dominant
	L	H	Z	Z	Recessive
	L	Open	Z	Z	Recessive
SN65HVDA540/541(2)	H	X	Y	Y	Recessive
SN65HVDA542(3)	H	X	Z	Z	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = common mode bias to GND, Z = common mode bias to V_{CC}/2. See Figure 1 and Figure 2 for common mode bias information.
(2) SN65HVDA540/541 have internal pull up to V_{IO} on STB pin. If STB pin is open the pin will be pulled high and the device will be in standby mode.
(3) SN65HVDA542 has internal pull down to GND on S pin. If S pin is open the pin will be pulled low and the device will be in normal mode.

Table 3. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	BUS STATE	RXD PIN(1)
STANDBY (SN65HVDA540)(2)	X	X	H
STANDBY WITH RXD WAKE UP REQUEST (SN65HVDA541)(3)	$V_{ID} \geq 1.15$ V	DOMINANT	L
	0.4 V < V_{ID} < 1.15 V	?	?
	$V_{ID} \leq 0.4$ V	RECESSIVE	H
NORMAL OR SILENT	$V_{ID} \geq 0.9$ V	DOMINANT	L
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	RECESSIVE	H
ANY	Open	N/A	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate.
(2) While STB is high (standby mode) the RXD output of the SN65HVDA540 is always high (recessive) because it has no wake-up receiver.
(3) While STB is high (standby mode) the RXD output of the SN65HVDA541 functions according to the levels above and the wake-up conditions shown in Figure 3 and Figure 4.

Digital Inputs and Outputs

The SN65HVDA54x devices have an I/O supply voltage input pin (V_{IO}) to ratiometrically level shift the digital logic input and output levels with respect to V_{IO} for compatibility with protocol controllers having I/O supply voltages between 3 V and 5.33 V.

The SN65HVDA54x-5 devices have a single V_{CC} supply (5V). The digital logic input and output levels for these devices are with respect to V_{CC} for compatibility with protocol controllers having I/O supply voltages between 4.68 V and 5.33 V.

Protection Features

TXD Dominant State Time Out

During normal mode, the only mode where the CAN driver is active, the TXD dominant time out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period $t_{(DOM)}$. The dominant time out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit expires ($t_{(DOM)}$) the CAN bus driver is disabled freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the dominant state time out. The CAN bus pins will be biased to recessive level during a TXD dominant state time out.

APPLICATION NOTE: The maximum dominant TXD time allowed by the TXD Dominant state time out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = $11/t_{(DOM)}$

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device will turn off the CAN driver circuits. This condition is cleared once the temperature drops below the thermal shut down temperature of the device. The CAN bus pins will be biased to recessive level during a thermal shutdown.

Undervoltage Lockout / Unpowered Device

Both of the supply pins have undervoltage detection which place the device in forced standby mode to protect the bus during an undervoltage event on either the V_{CC} or V_{IO} supply pins. If V_{IO} is undervoltage the RXD pin is tri-stated and the device does not pass any wake-up signals from the bus to the RXD pin. Since the device is placed into forced standby mode the CAN bus pins have a common mode bias to ground protecting the CAN network, see Figure 1 and Figure 2.

The device is designed to be an "ideal passive" load to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is un-powered so they will not load down the bus but rather be "no load". This is critical, especially if some nodes of the network will be unpowered while the rest of the network remains in operation.

APPLICATION NOTE: Once an undervoltage condition is cleared and the V_{CC} and V_{IO} have returned to valid levels the device will typically need 300 µs to transition to normal operation.

Table 4. Undervoltage Protection

DEVICE	V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD
SN65HVDA540	Bad	Good	Forced Standby Mode	Common mode bias to GND(1)	HIGH (Recessive)
SN65HVDA541			Forced Standby Mode	Common mode bias to GND(1)	Mirrors bus state via wake-up filter(2)
SN65HVDA542			Forced Standby Mode	Common mode bias to GND(1)	HIGH (Recessive)
SN65HVDA54x	Good	Bad	Forced Standby Mode(3)	Common mode bias to GND(1)	tri-state
SN65HVDA54x-5	Bad	N/A	Forced Standby Mode	Common mode bias to GND(1)	HIGH (Recessive) or tri-state
All Devices	Unpowered		Unpowered	No Load	High Z

(1) See Figure 1 and Figure 2 for common mode bias information.
(2) See Figure 3 and Figure 4 for operation of the low power wake up receiver and bus monitor for RXD Wake Up Request behavior and Table 3 for the wake up receiver threshold levels.
(3) When V_{IO} is undervoltage, the device is forced into standby mode with respect to the CAN bus since there is not a valid digital reference to determine the digital I/O states or power the wake-up receiver.

Floating Pins

The device has integrated pull up and pull downs on critical pins to place the device into known states if the pins float. The TXD pin is pulled up to V_{IO} to force a recessive input level if the pin floats. The STB is pulled up to the IO supply pin, V_{IO}(SN65HVDA540 and SN65HVDA541), or V_{CC} (SN65HVDA540-5 and SN65HVDA541-5) to force the device in standby mode (low power) if the pin floats. The S pin is pulled down to GND to force the device into normal mode if the pin floats (SN65HVDA542 and SN65HVDA542-5).

CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive) and TXD dominant state time out to prevent continuously driving dominant. During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in termination resistance and common mode choke ratings the average short circuit current should be used. The device has TXD dominant state time out which prevents permanently having the higher short circuit current of dominant state. The CAN protocol also has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

APPLICATION NOTE: The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit * [(\%REC\_Bits * I_{OS(SS)\_REC}) + (\%DOM\_Bits * I_{OS(SS)\_DOM})] + [\%Receive * I_{OS(SS)\_REC}]$$

Where $I_{OS(AVG)}$ is the average short circuit current, %Transmit is the percentage the node is transmitting CAN messages, %Receive is the percentage the node is receiving CAN messages, %REC_Bits is the percentage of recessive bits in the transmitted CAN messages, %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages, $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current and $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current.

ABSOLUTE MAXIMUM RATINGS(1) (2)

1.1	V_{CC}	Supply voltage range	–0.3 V to 6 V	
1.2	V_{IO}	I/O supply voltage range	–0.3 V to 6 V	
1.3		Voltage range at bus terminals (CANH, CANL)	–27 V to 40 V	
1.4	I_O	Receiver output current (RXD)	20 mA	
1.5	V_I	Voltage input range (TXD, STB, S)	SN65HVDA54x	–0.3 V to 6 V and $V_I \leq V_{IO}$ + 0.3 V
			SN65HVDA54x-5	–0.3 V to 6 V
1.6	T_J	Operating virtual-junction temperature range	–40°C to 150°C	
1.7	T_{LEAD}	Lead temperature (soldering, 10 seconds)	260°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

ELECTROSTATIC DISCHARGE AND TRANSIENT PROTECTION(1)

PARAMETER		TEST CONDITIONS		VALUE
2.1	Electrostatic Discharge	Human-Body Model(2)	CANH and CANL(3)	±12 kV
2.2			All pins	±4 kV
2.3		Charged-Device Model(4)	All pins	±1 kV
2.4		Machine Model(5)		±200 V
2.5		IEC 61000-4-2 according to IBEE CAN EMC Test Specification(6)	CANH and CANL pins to GND	±7 kV
2.6	ISO 7637 Transients	ISO7637 transients according to IBEE CAN EMC Test Specification(7)	Pulse 1	-100 V
2.7			Pulse 2a	+75 V
2.8			Pulse 3a	-150 V
2.9			Pulse 3b	+100 V

(1) Stresses beyond those listed under "electrostatic discharge and transient protection" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) HBM Tested in accordance with AEC-Q100-002.
(3) HBM test method based on AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(4) CDM Tested in accordance with AEC-Q100-011.
(5) MM Tested in accordance with AEC-Q100-003.
(6) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations will lead to different results.
(7) ISO 7637 is a system level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations will lead to different results.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
3.1	V_{CC}	Supply voltage		4.68	5.33	V
3.2	V_{IO}	I/O supply voltage		3	5.33	V
3.3	V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
3.4	V_{IH}	High-level input voltage	TXD, STB, S(for SN65HVD54x-5: $V_{IO} = V_{CC}$)	0.7 × V_{IO}	V_{IO}	V
3.5	V_{IL}	Low-level input voltage	TXD, STB, S (for SN65HVD54x-5: $V_{IO} = V_{CC}$)	0	0.3 × V_{IO}	V
3.6	V_{ID}	Differential input voltage, bus	Between CANH and CANL	–6	6	V
3.7	I_{OH}	High-level output current	RXD	–2		mA
3.8	I_{OL}	Low-level output current	RXD		2	mA
3.9	T_A	Operating ambient free-air temperature	See *Thermal Characteristics* table	-40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), SN65HVDA54x-5 devices $V_{IO} = V_{CC}$

PARAMETER				TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
Supply Characteristics (SN65HVDA54x)								
4.1	I_{CC}	5-V supply current	Standby mode (SN65HVDA 540/541 Only)	STB at V_{IO}, V_{CC} = 5.33 V, V_{IO} = 3 V, TXD at V_{IO} [2]			5	µA
4.2			Normal mode (Dominant)	TXD at 0 V, 60-Ω load, STB / S at 0 V		50	70	mA
4.3			Normal mode (Recessive)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	mA
4.4			Silent Mode (SN65HVDA 542 only)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	mA
4.5	I_{IO}	I/O supply current	Standby mode (SN65HVDA 540/541 Only)	STB at V_{IO} , V_{CC} = 5.33 V or 0 V, RXD floating, TXD at V_{IO} T_A = –40°C, 25°C, 125°C[3]		7	15	µA
4.6			Normal mode (recessive or dominant) and Silent Mode (SN65HVDA 542 Only)	V_{CC} = 5.33 V, RXD floating, TXD at 0 V or V_{IO}. Normal Mode: STB or S at 0 V. Silent Mode (SN65HVDA542): S at V_{IO}.		75	300	µA
4.7	UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.2	3.6	4	V
4.8	$V_{HYS(UVVCC)}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode				200		mV
4.9	UV_{VIO}	Undervoltage detection on V_{IO} for forced standby mode			1.9	2.45	2.95	V
4.10	$V_{HYS(UVVIO)}$	Hysteresis voltage for undervoltage detection on UV_{VIO} for forced standby mode				130		mV
Supply Characteristics (SN65HVDA54x-5)								
4.1-5	I_{CC}	5-V supply current	Standby mode (SN65HVDA 540-5/541-5 Only)	STB at V_{CC}, V_{CC} = 5.33 V, TXD at V_{CC} [2]			20	µA
4.2-5			Normal mode (Dominant)	TXD at 0 V, 60-Ω load, STB / S at 0 V		50	70	mA
4.3-5			Normal mode (Recessive)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	mA
4.4-5			Silent Mode (SN65HVDA 542 only)	TXD at V_{IO}, No load, STB / S at 0 V or S at V_{IO}		5.5	10	mA
4.7-5	UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.2	3.6	4	V
4.8-5	$V_{HYS(UVVCC)}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode				240		mV

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 3.3 V.
(2) The V_{CC} supply is not needed during standby mode so in the application I_{CC} in standby mode may be zero. If the V_{CC} supply remains, then I_{CC} is per specification with V_{CC}.
(3) See *HVDA54x Errata*, Literature number SLLZ073.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), SN65HVDA54x-5 devices $V_{IO} = V_{CC}$

	PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
Device Switching Characteristics: Propagation Time (Loop Time TXD to RXD)								
5.1	$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant		Figure 12, STB at 0 V	70		230	ns
5.2	$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive		Figure 12, STB at 0 V	70		230	ns
Driver Electrical Characteristics								
6.1	$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB / S at 0 V, R_L = 60 Ω, See Figure 5 and Figure 1	2.9		4.5	V
6.2	$V_{O(D)}$	Bus output voltage (dominant)	CANL	V_I = 0 V, STB / S at 0 V, R_L = 60 Ω, See Figure 5 and Figure 1	0.8		1.75	V
6.3	$V_{O(R)}$	Bus output voltage (recessive)		$V_I = V_{IO}$, V_{IO} = 3 V, STB at 0 V or S at X[4], R_L = 60 Ω, See Figure 5 and Figure 1	2	2.5	3	V
6.4	$V_{O(STBY)}$	Bus output voltage, standby mode (SN65HVDA540, SN65HVDA541 only)		STB / S at V_{IO}, R_L = 60 Ω, See Figure 5 and Figure 1	–0.1		0.1	V
6.5	$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB / S at 0 V, See Figure 5, Figure 1, and Figure 6	1.5		3	V
6.6	$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 45 Ω, STB / S at 0 V, See Figure 5, Figure 1, and Figure 6	1.4		3	V
6.7	$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB / S at 0 V, R_L = 60 Ω, See Figure 5 and Figure 1	–0.012		0.012	V
6.8	$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB / S at 0 V, No load	–0.5		0.05	V
6.9	V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)		STB / S at 0 V, R_L = 60 Ω, See Figure 15	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
6.10	$V_{OC(SS)}$	Steady-state common-mode output voltage		STB / S at 0 V, R_L = 60 Ω, See Figure 11	2	2.5	3	V
6.11	$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		STB / S at 0 V, R_L = 60 Ω, See Figure 11		40		mV
6.12	$I_{OS(SS)\_DOM}$	Short-circuit steady-state output current, Dominant		V_{CANH} = 0 V, CANL open, TXD = low, See Figure 14	-100			mA
6.13	$I_{OS(SS)\_DOM}$	Short-circuit steady-state output current, Dominant		V_{CANL} = 32 V, CANH open, TXD = low, See Figure 14			100	mA
6.14	$I_{OS(SS)\_REC}$	Short-circuit steady-state output current, Recessive		–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 14	-10		10	mA
6.15	$I_{OS(SS)\_REC}$	Short-circuit steady-state output current, Recessive		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 14	-10		10	mA
6.16	C_O	Output capacitance		See receiver input capacitance				

(4) For the SN65HVDA542 device the bus output voltage (recessive) will be the same if the device is in normal mode with S pin at 0 V or if the device is in silent mode with the S pin at HIGH.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), SN65HVDA54x-5 devices V_{IO} = V_{CC}

	PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
Driver Switching Characteristics							
7.1	t_{PLH}	Propagation delay time, low-to-high level output	STB / S at 0 V, See Figure 7		65		ns
7.2	t_{PHL}	Propagation delay time, high-to-low level output	STB / S at 0 V, See Figure 7		50		ns
7.3	t_R	Differential output signal rise time	STB / S at 0 V, See Figure 7		25		ns
7.4	t_F	Differential output signal fall time	STB / S at 0 V, See Figure 7		55		ns
7.5	t_{EN}	Enable time from standby or silent mode to normal mode dominant	See Figure 10			20	µs
7.6	$t_{(DOM)}$ [5]	Dominant time out	See Figure 13	300	400	700	µs
Receiver Electrical Characteristics							
8.1	V_{IT+}	Positive-going input threshold voltage, normal mode	STB / S at 0 V, See Table 5		800	900	mV
8.2	V_{IT-}	Negative-going input threshold voltage, normal mode	STB / S at 0 V, See Table 5	500	650		mV
8.3	V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})		100	125		mV
8.4	$V_{IT(STBY)}$	Input threshold voltage, standby mode (SN65HVDA541 only)	STB at V_{IO}	400		1150	mV
8.5	$I_{I(OFF\_LKG)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} at 0 V, V_{IO} at 0 V, TXD at 0 V			3	µA
8.6	C_I	Input capacitance to ground (CANH or CANL)	SN65HVDA54x: TXD at V_{IO}, V_{IO} at 3.3 V. SN65HVDA54x-5: TXD at V_{CC} V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
8.7	C_{ID}	Differential input capacitance	SN65HVDA54x: TXD at V_{IO}, V_{IO} at 3.3 V. SN65HVDA54x-5: TXD at V_{CC} V_I = 0.4 sin(4E6πt)		5		pF
8.8	R_{ID}	Differential input resistance	SN65HVDA54x: TXD at V_{IO}, V_{IO} = 3.3 V, STB at 0 V SN65HVDA54x-5: TXD at V_{CC}, STB at 0 V	29		80	kΩ
8.9	R_{IN}	Input resistance (CANH or CANL)		14.5	25	40	kΩ
8.10	$R_{I(M)}$	Input resistance matching [1 – ®$_{IN(CANH)}$/$R_{IN(CANL)}$)] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$	–3	0	3	%
Receiver Switching Characteristics							
9.1	t_{PLH}	Propagation delay time, low-to-high-level output	STB / S at 0 V , See Figure 9		95		ns
9.2	t_{PHL}	Propagation delay time, high-to-low-level output	STB / S at 0 V , See Figure 9		60		ns
9.3	t_R	Output signal rise time	STB / S at 0 V , See Figure 9		13		ns
9.4	t_F	Output signal fall time	STB / S at 0 V , See Figure 9		10		ns
9.5	t_{BUS}	Dominant time required on bus for wake-up from standby (SN65HVDA541 only)	STB at V_{IO}, See Figure 3 and Figure 4	1.5		5	µs
9.6	t_{CLEAR}	Recessive time on the bus to clear the standby mode receiver output (RXD) if standby mode is entered while bus is dominant (SN65HVDA541 only)		1.5		5	µs

(5) The TXD dominant time out ($t_{(DOM)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(DOM)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{(DOM)}$ = 11 bits / 300 µs = 37 kbps

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), SN65HVDA54x-5 devices $V_{IO} = V_{CC}$

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
TXD Pin Characteristics							
10.1	V_{IH}	High-level input voltage	SN65HVD54x-5: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
10.2	V_{IL}	Low-level input voltage	SN65HVD54x-5: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
10.3	I_{IH}	High-level input current	SN65HVDA54x: TXD at V_{IO} SN65HVDA54x-5: TXD at V_{CC}	-2		2	µA
10.4	I_{IL}	Low-level input current	TXD at 0 V	–100		-7	µA
RXD Pin Characteristics							
11.1	V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 9 SN65HVD54x-5: $V_{IO} = V_{CC}$	0.8 × V_{IO}			V
11.2	V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 9 SN65HVD54x-5: $V_{IO} = V_{CC}$			0.2 × V_{IO}	V
STB Pin Characteristics (SN65HVDA540 and SN65HVDA541 Only)							
12.1	V_{IH}	High-level input voltage	SN65HVD54x-5: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
12.2	V_{IL}	Low-level input voltage	SN65HVD54x-5: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
12.3	I_{IH}	High-level input current	SN65HVDA54x: STB at V_{IO} SN65HVDA54x-5: STB at V_{CC}	–2		2	µA
12.4	I_{IL}	Low-level input current	STB at 0 V	–20			µA
S Pin Characteristics (SN65HVDA542 Only)							
13.1	V_{IH}	High-level input voltage	SN65HVD54x-5: $V_{IO} = V_{CC}$	0.7 × V_{IO}			V
13.2	V_{IL}	Low-level input voltage	SN65HVD54x-5: $V_{IO} = V_{CC}$			0.3 × V_{IO}	V
13.3	I_{IH}	High-level input current	SN65HVDA54x: S at V_{IO} SN65HVDA54x-5: S at V_{CC}			30	µA
13.4	I_{IL}	Low-level input current	S at 0 V	–2		2	µA

THERMAL CHARACTERISTICS

over recommended operating conditions, T_J = –40°C to 150°C (unless otherwise noted), SN65HVDA54x-5 devices $V_{IO} = V_{CC}$

THERMAL METRIC[1][2]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL METRIC - SOIC 'D' PACKAGE							
14.1-D	θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance [3]		140		°C/W
14.2-D	θ_{JA}	Junction-to-air thermal resistance	High-K thermal resistance [4]		112		°C/W
14.3-D	θ_{JB}	Junction-to-board thermal resistance[5]			50		°C/W
14.4-D	$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance[6]			56		°C/W
14.5-D	$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance[7]			N/A		°C/W
14.6-D	Ψ_{JT}	Junction-to-top characterization parameter[8]			13		°C/W
14.7-D	Ψ_{JB}	Junction-to-board characterization parameter[9]			55		°C/W
AVERAGE POWER DISSIPATION AND THERMAL SHUTDOWN							
14.8	P_D	Average power dissipation	V_{CC} = 5 V, $V_{IO} = V_{CC}$, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		140		mW
14.9	P_D	Average power dissipation	V_{CC} = 5.33 V, $V_{IO} = V_{CC}$, T_J = 130°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			215	mW
14.10		Thermal shutdown temperature			185		°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times \theta_{JA})$. $\theta_{JA}$is PCB dependent, both JEDEC-standard Low-K and High-K values are given as reference points to standardized reference boards.
(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, Low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(8) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

PARAMETER MEASUREMENT INFORMATION

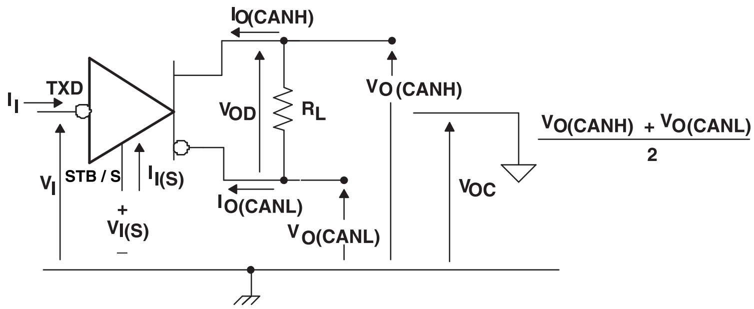


Figure 5. Driver Voltage, Current, and Test Definition

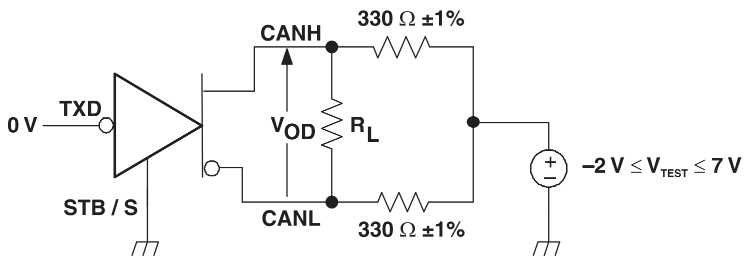
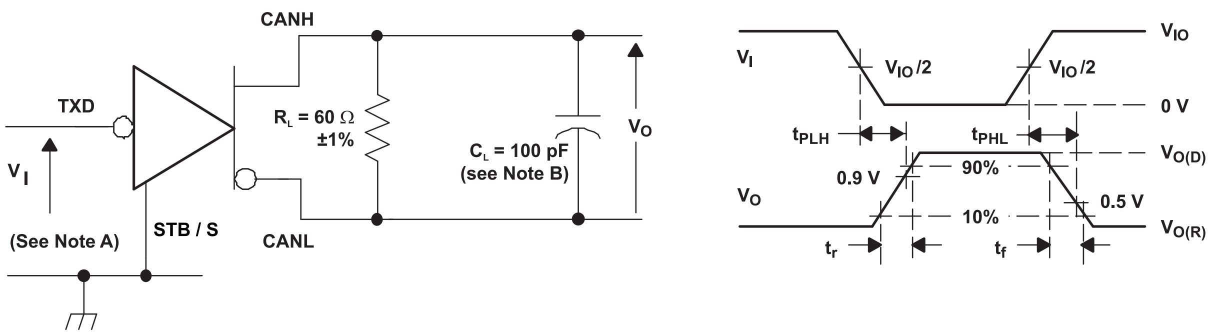


Figure 6. Driver V_{OD} Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

C. For SN65HVDA54x-5 device versions, $V_{IO} = V_{CC}$.

Figure 7. Driver Test Circuit and Voltage Waveforms

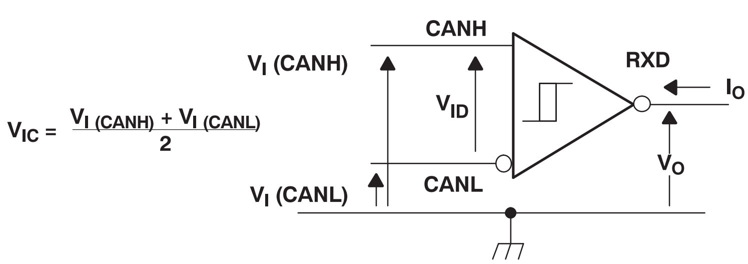
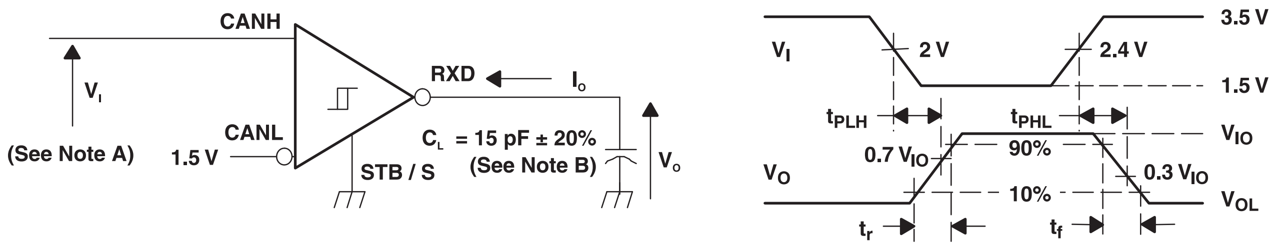


Figure 8. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

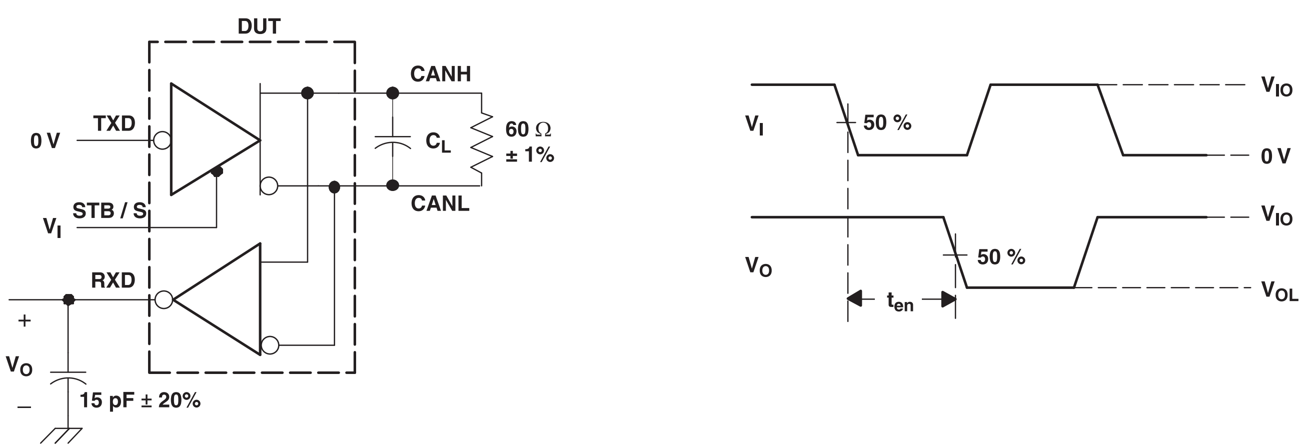
B. C_L includes instrumentation and fixture capacitance within ±20%.

C. C. For SN65HVDA54x-5 device versions $V_{IO} = V_{CC}$.

Figure 9. Receiver Test Circuit and Voltage Waveforms

Table 5. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

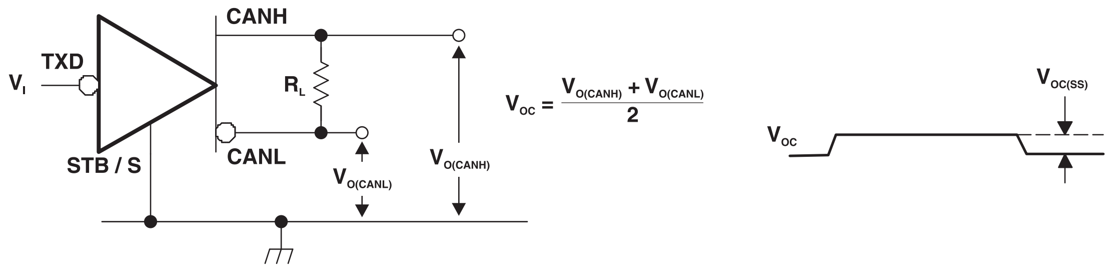


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle.

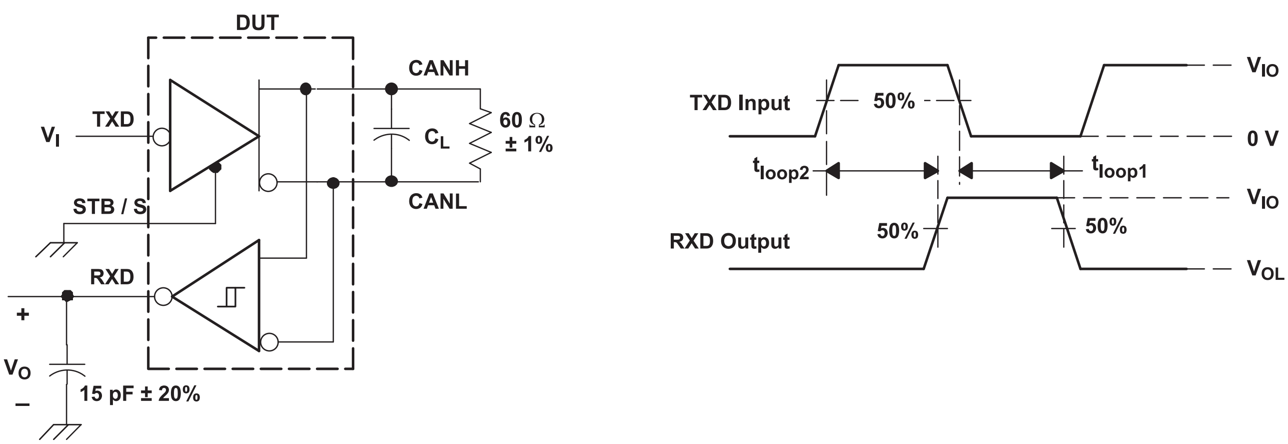
C. C. For SN65HVDA54x-5 device versions $V_{IO} = V_{CC}$.

Figure 10. t_{EN} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11. Common-Mode Output Voltage Test and Waveforms

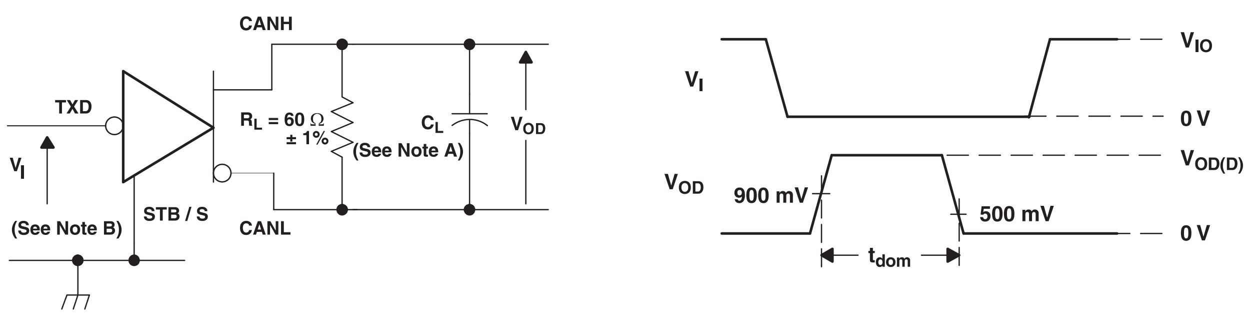


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

C. For SN65HVDA54x-5 device versions, $V_{IO} = V_{CC}$.

Figure 12. $t_{PROP(LOOP)}$ Test Circuit and Waveform

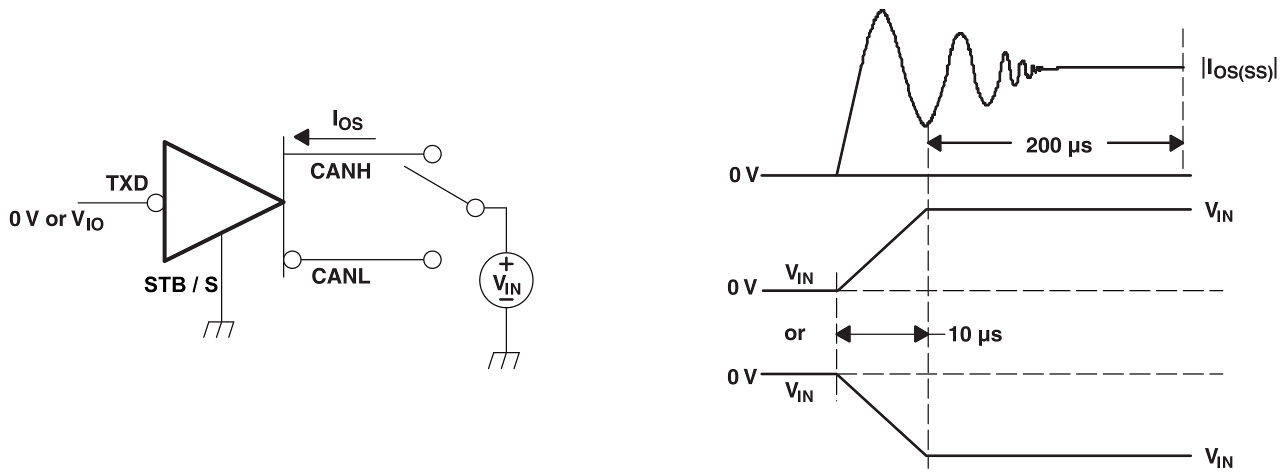


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

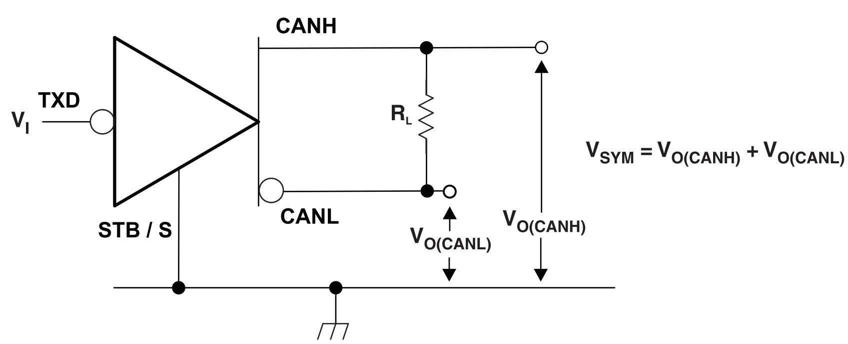
C. For SN65HVDA54x-5 device versions, $V_{IO} = V_{CC}$.

Figure 13. TXD Dominant Time Out Test Circuit and Waveforms



A. A. For SN65HVDA54x-5 device versions $V_{IO} = V_{CC}$.

Figure 14. Driver Short-Circuit Current Test and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6$ ns, Pulse Repetition Rate (PRR) = 250 kHz, 50% duty cycle.

Figure 15. Driver Output Symmetry Test Circuit

APPLICATION INFORMATION

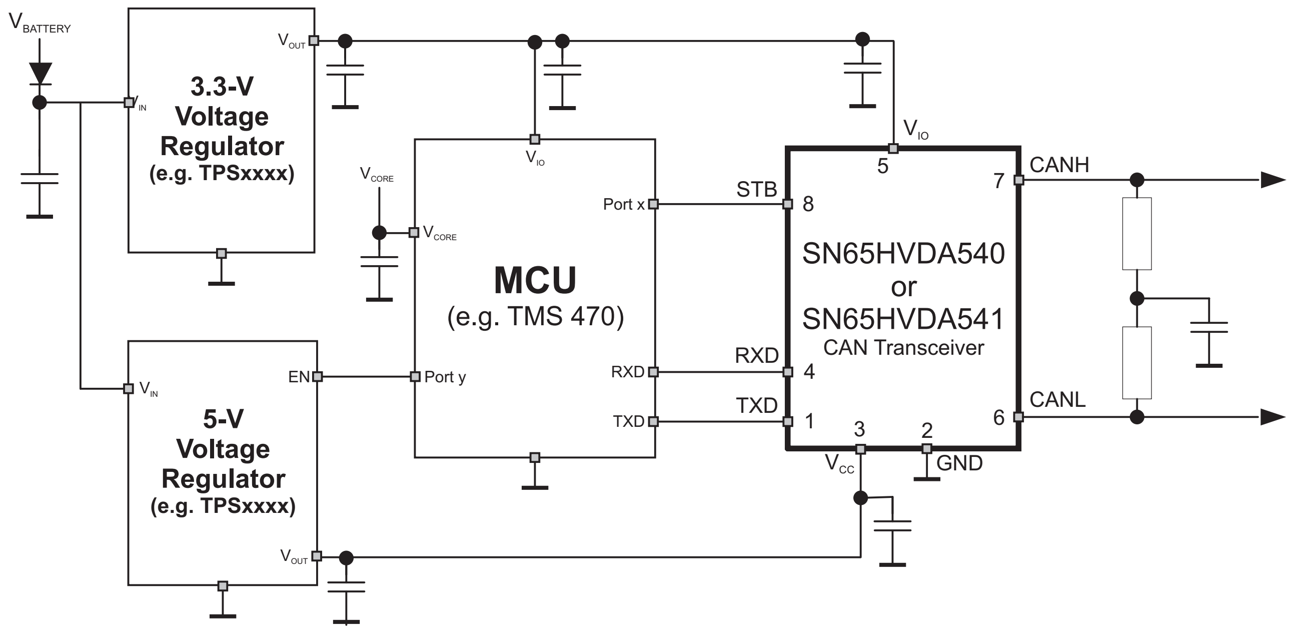


Figure 16. Typical Application Using 3.3-V I/O Voltage Level and Low-Power Mode (5-V V_{CC} Not Needed in Low-Power Mode)

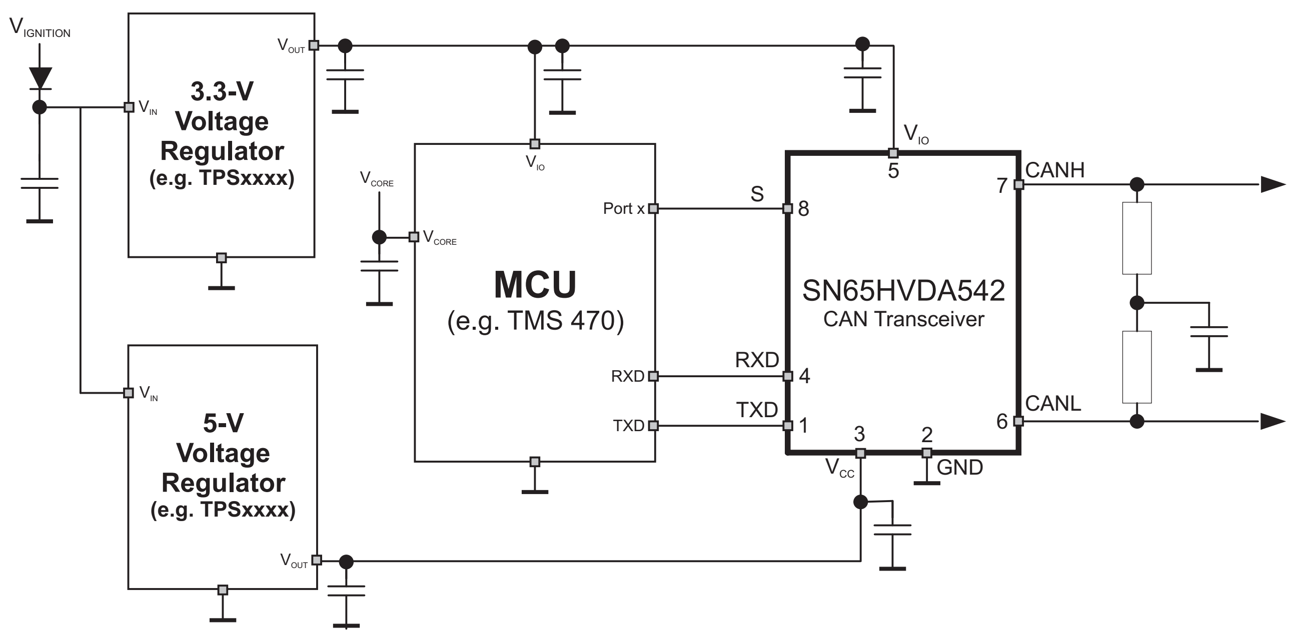


Figure 17. Typical Application Using 3.3-V I/O Voltage Level and No Low-Power Mode

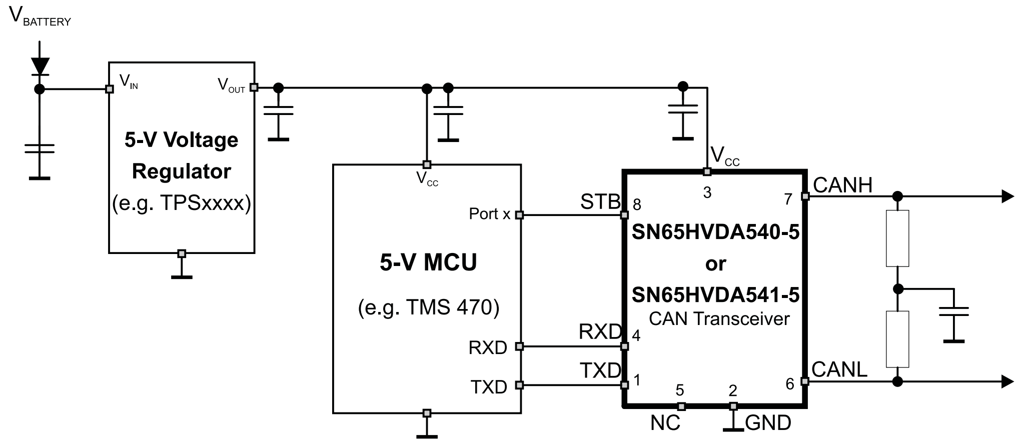


Figure 18. Typical Application Using 5-V MCU and Low-Power Mode

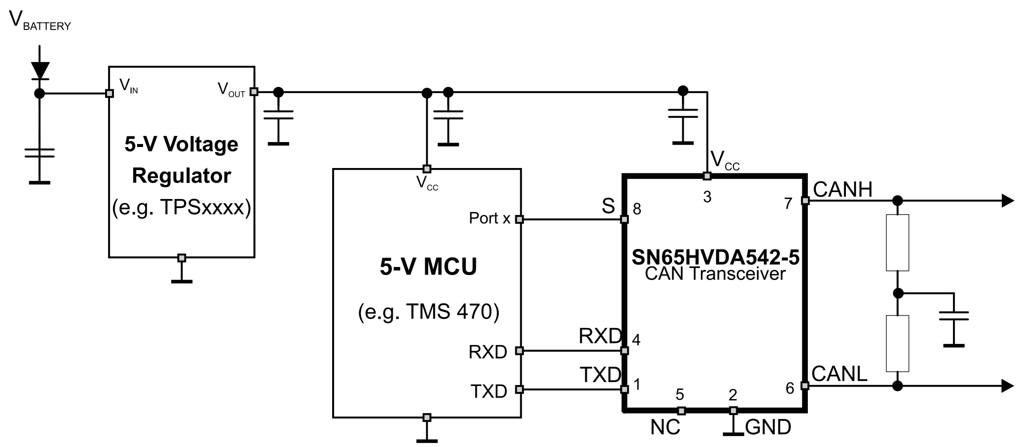


Figure 19. Typical Application Using 5-V MCU and No Low-Power Mode

REVISION HISTORY

Changes from Revision B (September 2010) to Revision C **Page**

- Deleted DSJ package info ... 1
- Deleted DSJ package info ... 2
- Deleted DSJ (VSON) package info ... 7
- Added note in line 4.5 Test Conditions, "T_A = –40°C, 25°C, 125°C" ... 9
- Deleted DSJ package info ... 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
HVDA5405QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H5405Q	Samples
HVDA540QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H540Q	Samples
HVDA5415QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H5415Q	Samples
HVDA541QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H541Q	Samples
HVDA5425QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H5425Q	Samples
HVDA542QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H542Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVDA540-Q1 :

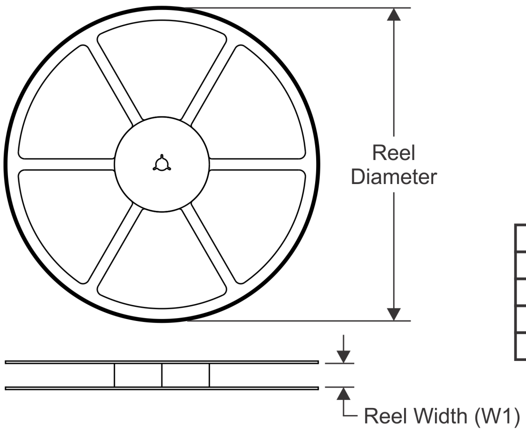
- Catalog: SN65HVDA540

NOTE: Qualified Version Definitions:

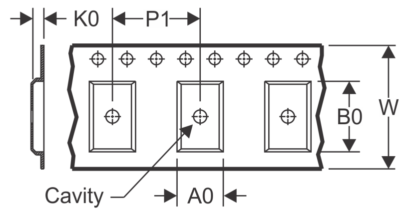
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

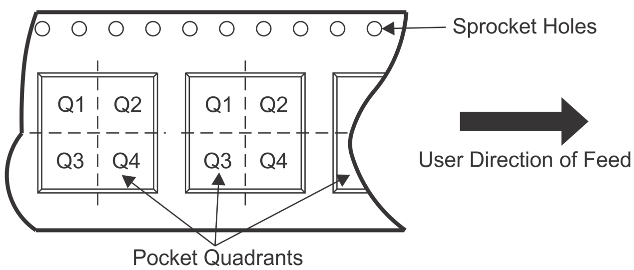


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

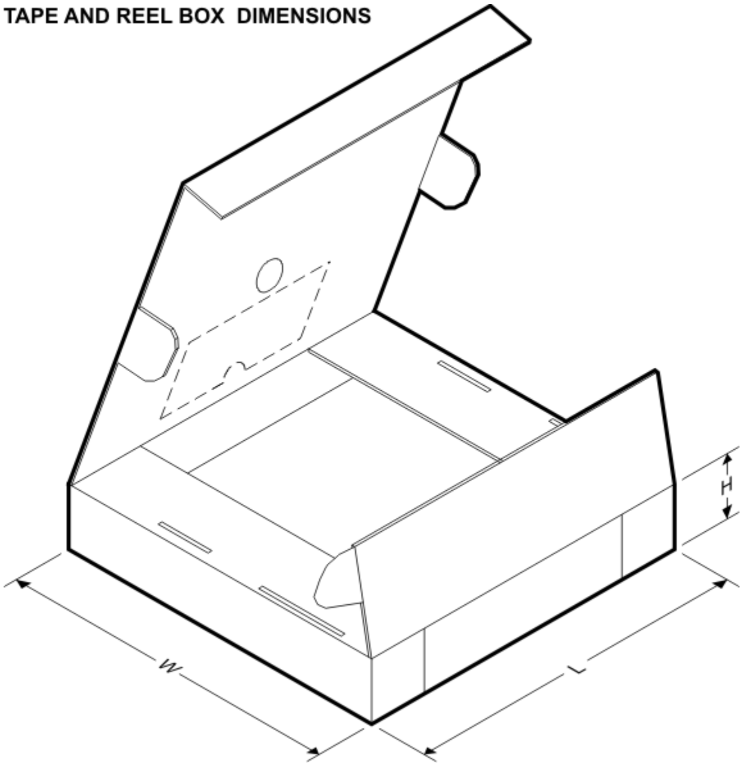
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HVDA5405QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5405QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA540QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5415QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5415QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA541QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA541QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5425QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA5425QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA542QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA542QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

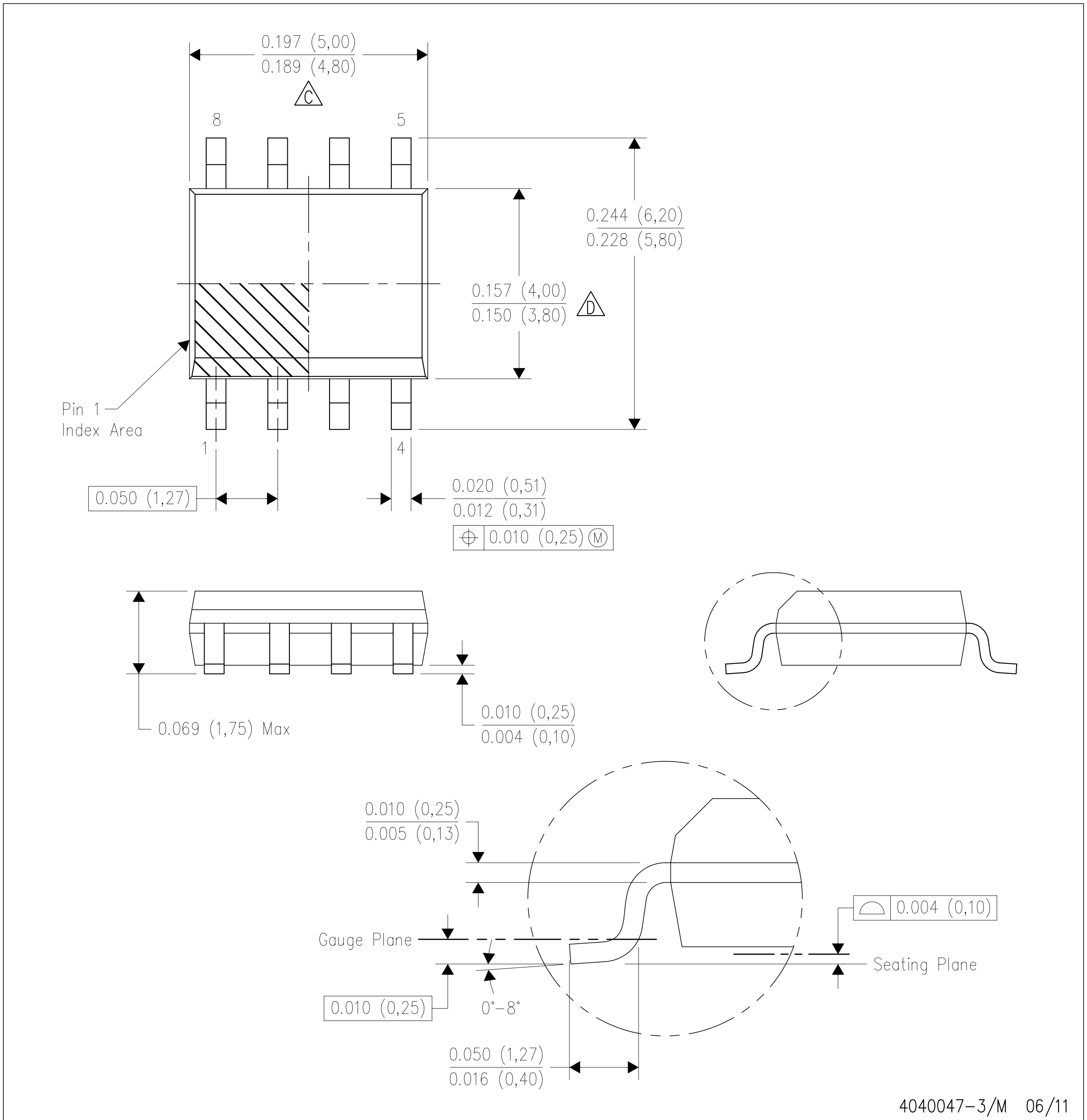
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

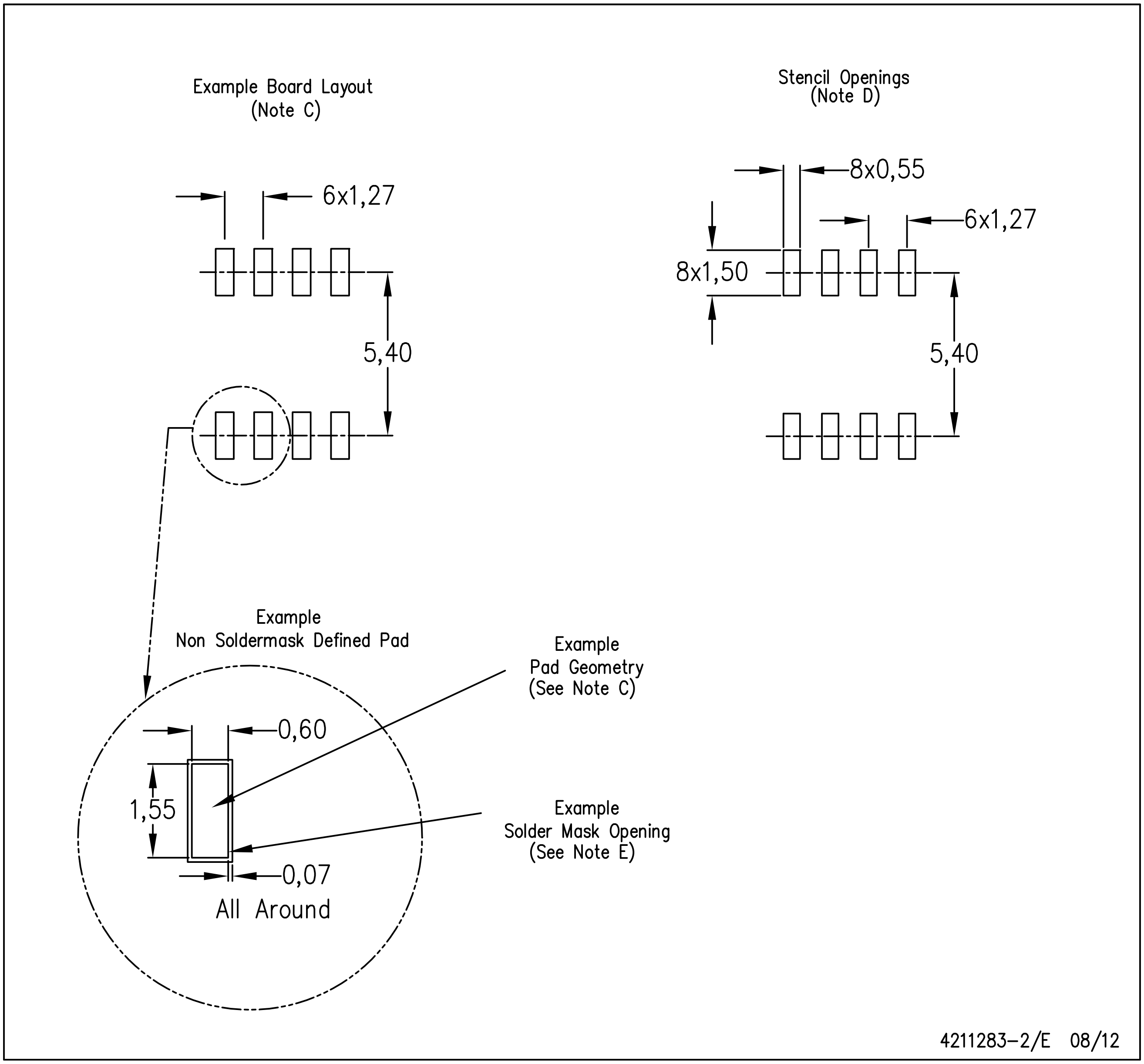
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HVDA5405QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA5405QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA540QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA5415QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA5415QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA541QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA541QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA5425QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA5425QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA542QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA542QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265