

High Voltage, Low Noise, Inductorless EL Lamp Driver

Features

- ▶ No external components required when using an external EL clock frequency
- ▶ EL frequency can be set by an external resistor
- ▶ Low Noise
- ▶ DC to AC converter
- ▶ Drives up to 5.3nF (approx. 1.5in² lamp) load
- ▶ Output voltage regulation
- ▶ Enable function

Applications

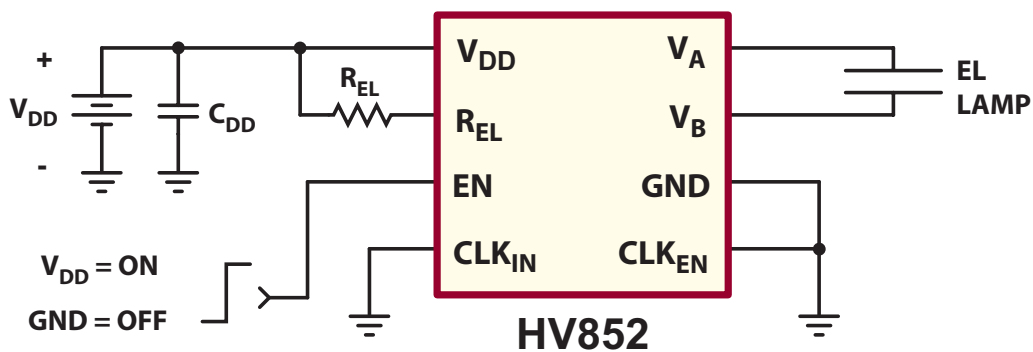
- ▶ Cellular phone keypad
- ▶ Watches
- ▶ Small handheld wireless devices
- ▶ MP3 Players

General Description

The Supertex HV852 is a high voltage, low noise, inductorless EL (electroluminescent) lamp driver. It is designed to drive EL lamps of up to 1.5in², with capacitive values up to 5.3nF over an input voltage range of 2.4V to 5.0V. The HV852 converts a low voltage DC input to a high voltage AC output across an EL lamp. It uses a charge pump scheme to boost the input voltage eliminating the need for an external inductor, diode, and high voltage capacitor commonly found in conventional topologies.

The charge pump circuit discharges its energy into an EL lamp through a high voltage H-bridge. Once the voltage reaches its regulated limit, it is turned off to conserve power. The EL lamp is then discharged to ground and the H-bridge changes state to allow the charge pump to charge the EL lamp in the opposite direction.

Typical Application Circuit



EL Lamp frequency set by R_{EL}

Ordering Information

Device	Package Options	
	8-Lead MSOP 3x3mm body, 1.10mm height (max), 0.65mm pitch	10-Lead DFN 3x3mm body, 0.80mm height (max), 0.50mm pitch
HV852	HV852MG-G	HV852K7-G

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

Parameter	Value
V _{DD} , Supply Voltage	-0.5V to 6.5V
Operating Temperature	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation 8-Lead MSOP	300mW
Power Dissipation 10-Lead DFN	1.6W

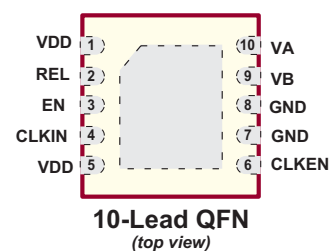
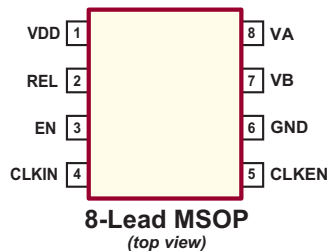
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified: T_A = 25°C, V_{DD} = 3.5V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I _{DDQ}	Quiescent current	-	-	200	nA	EN = 0V
V _A or V _B	Peak output voltage	72	82	92	V	No load
V _A -V _B	Peak to Peak output voltage	144	164	184	V	
I _{DD}	Operating current	-	15.2	30	mA	See Figure 1, V _{DD} = 3.5V, R _{EL} = 1.5MΩ, Load = 3.3nF+1KΩ
V _A or V _B	Peak output voltage	72	82	92	V	
V _A -V _B	Peak to Peak output voltage	144	164	184	V	
f _{EL}	EL lamp frequency	210	250	300	Hz	1.0in ² lamp, 0V to 90% of final value
t _{rou}	Output voltage rise time	-	640	-	μs	

Pin Configurations

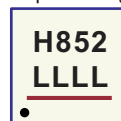


Note:

Pads are at the bottom of the package. Center heat slug is at ground potential.

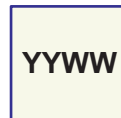
Product Marking

Top Marking

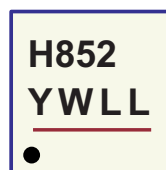


L = Lot Number
YY = Year Sealed
WW = Week Sealed
— = "Green" Packaging

Bottom Marking



8-Lead MSOP



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
— = "Green" Packaging

10-Lead DFN

Logic Inputs

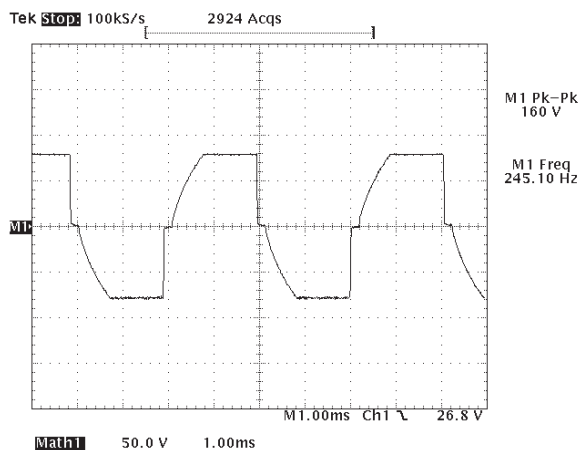
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input logic low voltage	0	-	0.5	V	---
V_{IH}	Input logic high voltage	1.75	-	V_{DD}	V	$V_{DD} = 2.4$ to $4.3V$. Temp = -25° to $85^{\circ}C$
		2.0	-	V_{DD}	V	$V_{DD} = 4.3$ to $5.0V$. Temp = -25° to $85^{\circ}C$
I_{IL}	Input logic low current	-	-	1.0	μA	---
I_{IH}	Input logic high current	-	-	1.0	μA	---
EN_{rise}	Enable input rise time (for delay turn off)	0.01	-	10	ms	Using external R-C circuit, see Figure 2
EN_{fall}	Enable input fall time (for delay turn off)	10	-	5	μs	
C_{in}	Logic input capacitance	-	-	10	pF	---

Recommended Operating Conditions

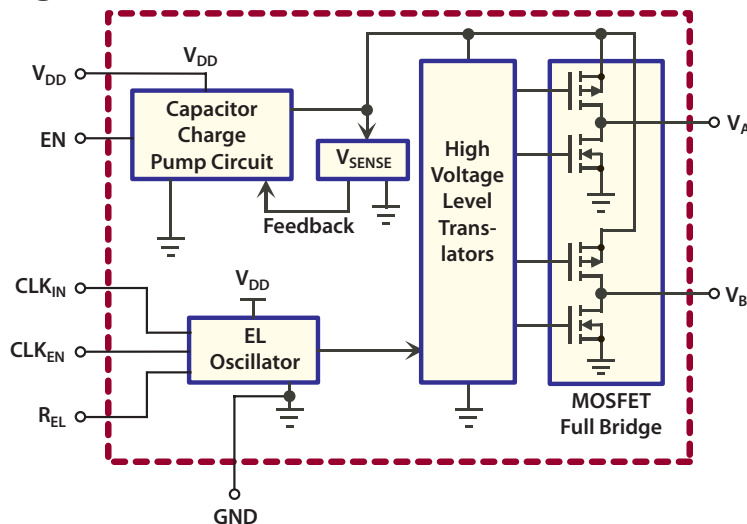
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Input voltage	2.4	-	5.0	V	---
f_{EL}	EL lamp frequency	50	-	500	Hz	---
C_{load}	EL lamp capacitance	0	-	5.3	nF	---
T_A	Operating Temperature	-25	-	+85	$^{\circ}C$	---

Typical Output Waveform

Test Conditions:
 HV852 driving a 1.0in² EL lamp
 $V_{DD} = 3.6V$ and $R_{EL} = 1.5M\Omega$,
 $V_A - V_B$ waveform



Functional Block Diagram



Pin Description

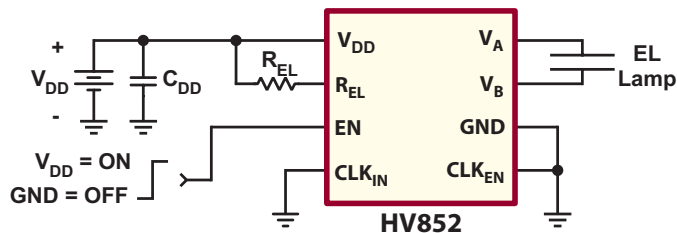
Name	Description
V _{DD}	Input supply voltage pin.
R _{EL}	An external resistor to V _{DD} will set the EL lamp frequency. The EL frequency is inversely proportional to the R _{EL} resistor value. A 1.5MΩ resistor would provide a nominal lamp frequency of 250Hz. $f_{EL} = \frac{(1.5M\Omega)(250Hz)}{R_{EL}}$ When using an external clock to set the EL lamp frequency, the R _{EL} pin should be connected to ground.
EN	Enable input pin. Logic high will turn the device on. An external R-C circuit can be added for a delayed turn off.
CLK _{IN}	Logic input pin. An external logic clock applied to this pad can be used to set the EL lamp frequency (see Figure 3). The EL lamp frequency is the external clock frequency divided by 128. This is useful for applications requiring the EL lamp to be synchronized to a system clock. Connect to ground when not in use.
CLK _{EN}	Logic input pin. Logic high will cause the EL lamp frequency to be set by the CLK _{IN} input. Logic low will cause the EL lamp frequency to be set by the external R _{EL} resistor.
Gnd	IC ground pin.
V _B	EL lamp driver output pin. The EL lamp is connected across V _A and V _B terminals.
V _A	EL lamp driver output pin. The EL lamp is connected across V _A and V _B terminals.

Typical Performance

(The following was the observed performance when driving a 1.0in² green lamp)

Load	R _{EL}	V _{DD}	I _{DD}	V _A -V _B	f _{EL}
3.3nF+1KΩ	1.5MΩ	2.4V	17.56mA	77V	245Hz
		3.0V	17.53mA	79V	
		3.6V	17.44mA	79V	
		4.2V	17.65mA	79V	
		5.0V	18.35mA	79V	

Figure 1: Typical Application



Note: $C_{DD} = 2.2\mu F$, 6.3V ceramic capacitor

Figure 2: Push Button Turn on with Delay Turn off

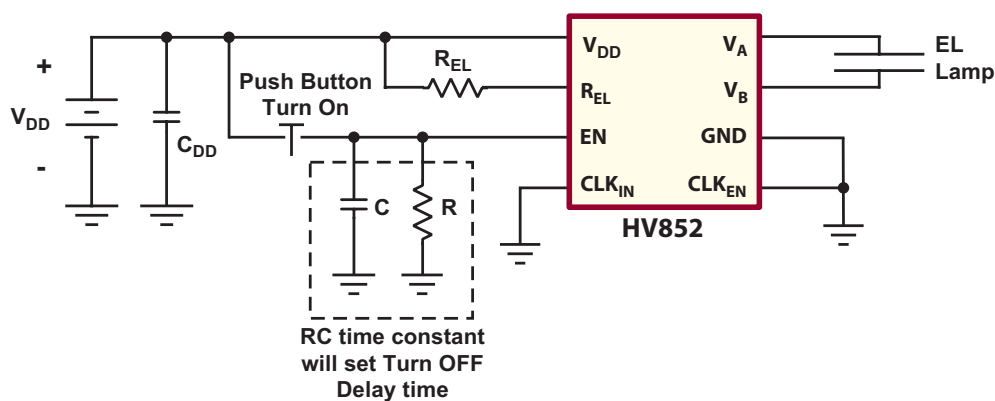
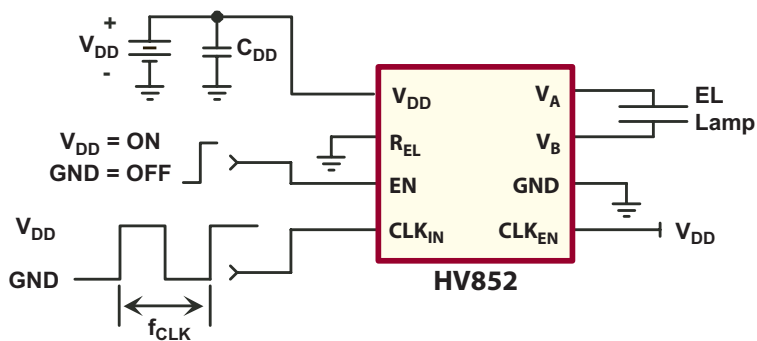


Figure 3: Independent Programmable Output Frequency (f_{EL})

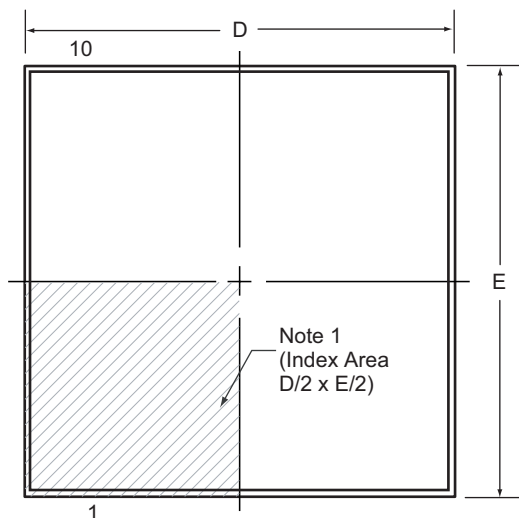


EL Lamp frequency set by an external clock

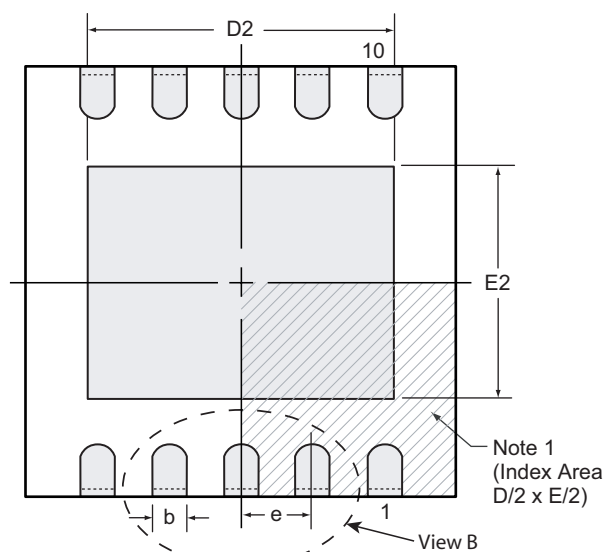
Note: $f_{EL} = f_{CLK}/128$

10-Lead DFN Package Outline (K7)

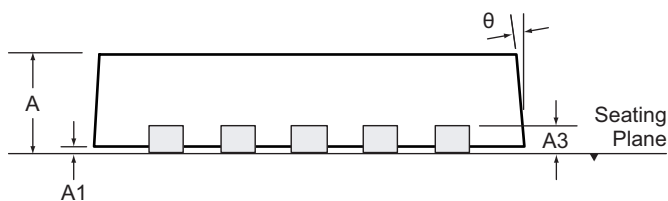
3x3mm body, 0.80mm height (max), 0.50mm pitch



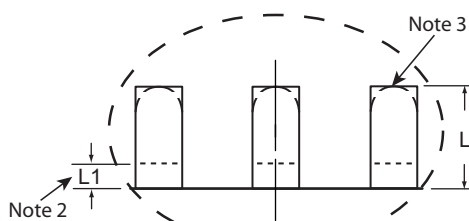
Top View



Bottom View



Side View



View B

Notes:

1. Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

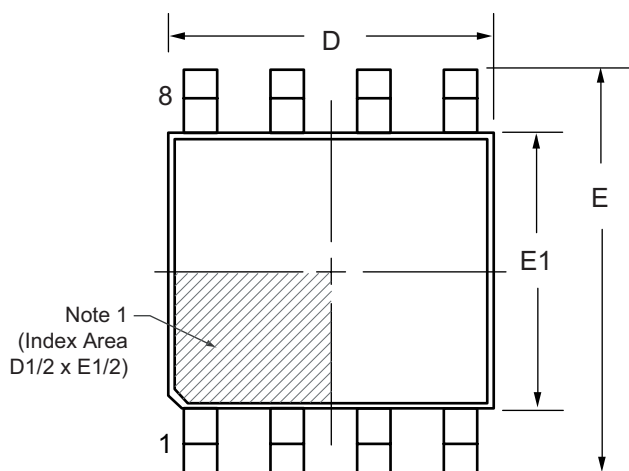
Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85	2.20	2.85	1.40	0.50 BSC	0.30	-	0°
	NOM	0.75	0.02		0.25	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.30	3.15	2.70	3.15	1.75		0.50	0.15	14°

JEDEC Registration MO-229, Variation WEED-5, Issue C, Aug. 2003.

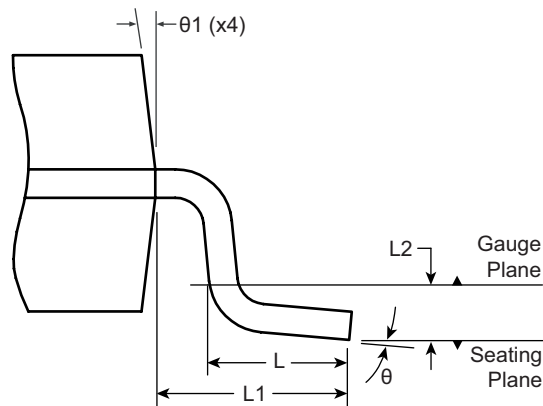
Drawings not to scale.

8-Lead MSOP Package Outline (MG)

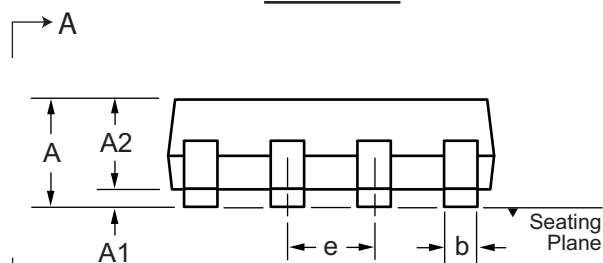
3x3mm body, 1.10mm height (max), 0.65mm pitch



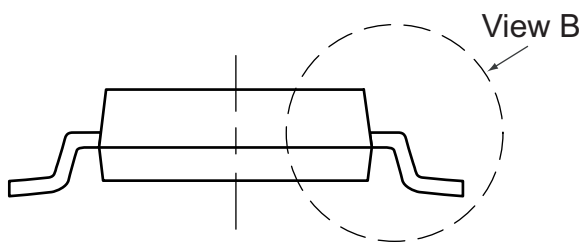
Top View



View B



Side View



View A-A

Note 1:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol	A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	0.75	0.00	0.75	0.22	2.80	4.65	2.80	0.65 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60			-	-
	MAX	1.10	0.15	0.95	0.38	3.20	5.15	3.20		0.80			8°	15°

JEDEC Registration MO-187, Variation AA, Issue E, Dec. 2004.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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