

# Data Sheet

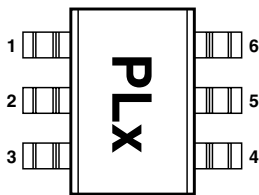


## Description

Avago's HSMS-286x family of DC biased detector diodes have been designed and optimized for use from 915 MHz to 5.8 GHz. They are ideal for RF/ID and RF Tag applications as well as large signal detection, modulation, RF to DC conversion or voltage doubling.

Available in various package configurations, this family of detector diodes provides low cost solutions to a wide variety of design problems. Avago's manufacturing techniques assure that when two or more diodes are mounted into a single surface mount package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

## Pin Connections and Package Marking



Notes:

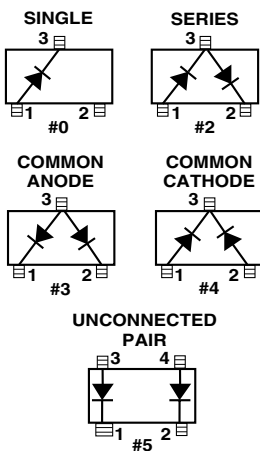
1. Package marking provides orientation and identification.
2. The first two characters are the package marking code.  
The third character is the date code.

## Features

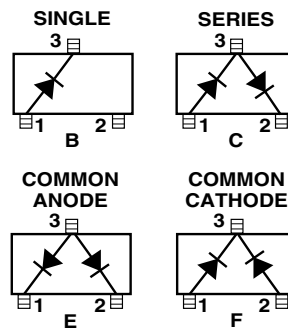
- Surface Mount SOT-23/SOT-143 Packages
- Miniature SOT-323 and SOT-363 Packages
- High Detection Sensitivity:
  - up to 50 mV/μW at 915 MHz
  - up to 35 mV/μW at 2.45 GHz
  - up to 25 mV/μW at 5.80 GHz
- Low FIT (Failure in Time) Rate\*
- Tape and Reel Options Available
- Unique Configurations in Surface Mount SOT-363 Package
  - increase flexibility
  - save board space
  - reduce cost
- HSMS-286K Grounded Center Leads Provide up to 10 dB Higher Isolation
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free

\* For more information see the Surface Mount Schottky Reliability Data Sheet.

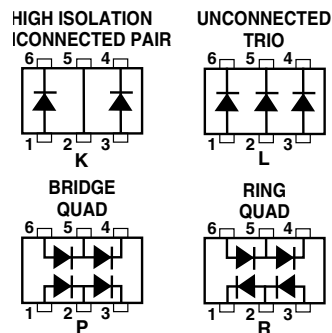
## SOT-23 / SOT-143 Package Lead Code Identification (top view)



## SOT-323 Package Lead Code Identification (top view)



## SOT-363 Package Lead Code Identification (top view)



### SOT-23/SOT-143 DC Electrical Specifications, $T_c = +25^\circ\text{C}$ , Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Forward Voltage $V_F$ (mV)		Typical Capacitance $C_T$ (pF)
2860	T0	0	Single	250 Min.	350 Max.	0.30
2862	T2	2	Series Pair <sup>[1,2]</sup>			
2863	T3	3	Common Anode <sup>[1,2]</sup>			
2864	T4	4	Common Cathode <sup>[1,2]</sup>			
2865	T5	5	Unconnected Pair <sup>[1,2]</sup>			
Test Conditions				$I_F = 1.0 \text{ mA}$		$V_R = 0 \text{ V}, f = 1 \text{ MHz}$

Notes:

1.  $\Delta V_F$  for diodes in pairs is 15.0 mV maximum at 1.0 mA.

2.  $\Delta C_T$  for diodes in pairs is 0.05 pF maximum at  $-0.5\text{V}$ .

### SOT-323/SOT-363 DC Electrical Specifications, $T_c = +25^\circ\text{C}$ , Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Forward Voltage $V_F$ (mV)		Typical Capacitance $C_T$ (pF)
286B	T0	B	Single	250 Min.	350 Max.	0.25
286C	T2	C	Series Pair <sup>[1,2]</sup>			
286E	T3	E	Common Anode <sup>[1,2]</sup>			
286F	T4	F	Common Cathode <sup>[1,2]</sup>			
286K	TK	K	High Isolation Unconnected Pair			
286L	TL	L	Unconnected Trio			
286P	TP	P	Bridge Quad			
286R	ZZ	R	Ring Quad			
Test Conditions				$I_F = 1.0 \text{ mA}$		$V_R = 0 \text{ V}, f = 1 \text{ MHz}$

Notes:

1.  $\Delta V_F$  for diodes in pairs is 15.0 mV maximum at 1.0 mA.

2.  $\Delta C_T$  for diodes in pairs is 0.05 pF maximum at  $-0.5\text{V}$ .

## RF Electrical Specifications, $T_C = +25^\circ\text{C}$ , Single Diode

Part Number	Typical Tangential Sensitivity TSS (dBm) @ f =			Typical Voltage Sensitivity g (mV/ $\mu\text{W}$ ) @ f =			Typical Video Resistance RV (K $\Omega$ )
	915 MHz	2.45 GHz	5.8 GHz	915 MHz	2.45 GHz	5.8 GHz	
2860	-57	-56	-55	50	35	25	5.0
2862							
2863							
2864							
2865							
286B							
286C							
286E							
286F							
286K							
286L							
286P							
286R							
Test Conditions	Video Bandwidth = 2 MHz $I_b = 5 \mu\text{A}$			Power in = -40 dBm $R_L = 100 \text{K}\Omega$ , $I_b = 5 \mu\text{A}$			$I_b = 5 \mu\text{A}$

## Absolute Maximum Ratings, $T_C = +25^\circ\text{C}$ , Single Diode

Symbol	Parameter	Unit	Absolute Maximum <sup>[1]</sup>	
			SOT-23/143	SOT-323/363
$P_{IV}$	Peak Inverse Voltage	V	4.0	4.0
$T_J$	Junction Temperature	$^\circ\text{C}$	150	150
$T_{STG}$	Storage Temperature	$^\circ\text{C}$	-65 to 150	-65 to 150
$T_{OP}$	Operating Temperature	$^\circ\text{C}$	-65 to 150	-65 to 150
$\theta_{jc}$	Thermal Resistance <sup>[2]</sup>	$^\circ\text{C}/\text{W}$	500	150

Notes:

- Operation in excess of any one of these conditions may result in permanent damage to the device.
- $T_C = +25^\circ\text{C}$ , where  $T_C$  is defined to be the temperature at the package pins where contact is made to the circuit board.



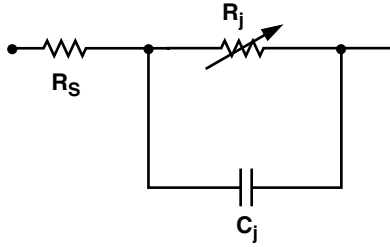
**Attention:**  
Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)

ESD Human Body Model (Class 0)

Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

### Equivalent Linear Circuit Model, Diode chip



$R_S$  = series resistance (see Table of SPICE parameters)

$C_j$  = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5} \text{ nT}}{I_b + I_s}$$

where

$I_b$  = externally applied bias current in amps

$I_s$  = saturation current (see table of SPICE parameters)

$T$  = temperature, °K

$n$  = ideality factor (see table of SPICE parameters)

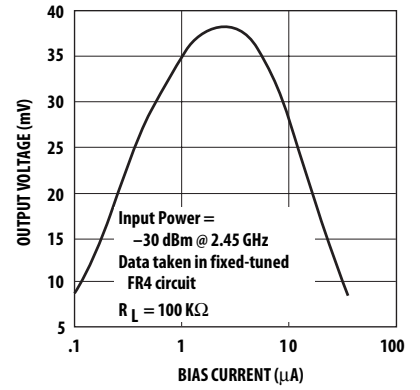
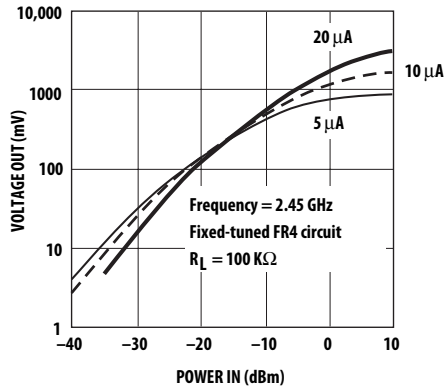
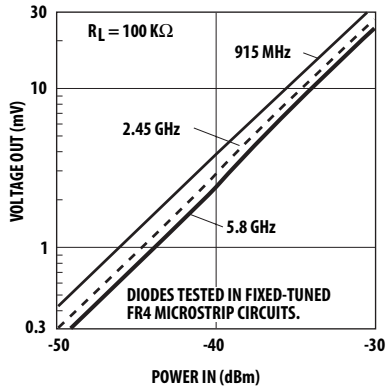
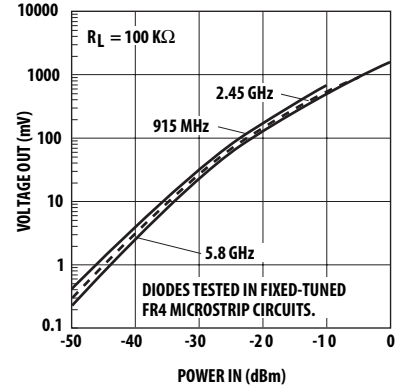
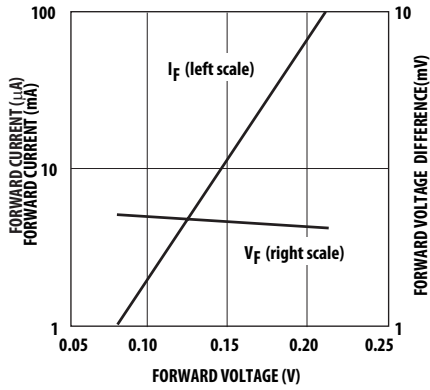
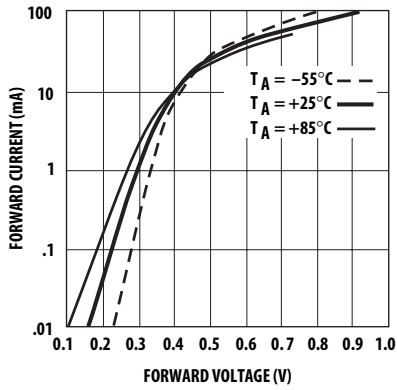
Note:

To effectively model the packaged HSMS-286x product, please refer to Application Note AN1124.

### SPICE Parameters

Parameter	Units	Value
$B_V$	V	7.0
$C_{J0}$	pF	0.18
$E_G$	eV	0.69
$I_{BV}$	A	1 E - 5
$I_S$	A	5 E - 8
$N$		1.08
$R_S$	$\Omega$	6.0
$P_B$ (VJ)	V	0.65
$P_T$ (XTI)		2
$M$		0.5

# Typical Parameters, Single Diode



## Applications Information

### Introduction

Avago's HSMS-286x family of Schottky detector diodes has been developed specifically for low cost, high volume designs in two kinds of applications. In small signal detector applications ( $P_{in} < -20$  dBm), this diode is used with DC bias at frequencies above 1.5 GHz. At lower frequencies, the zero bias HSMS-285x family should be considered.

In large signal power or gain control applications ( $P_{in} > -20$  dBm), this family is used without bias at frequencies above 4 GHz. At lower frequencies, the HSMS-282x family is preferred.

### Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 7, along with its equivalent circuit.



Figure 7. Schottky Diode Chip.

$R_s$  is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into  $R_s$  is lost as heat — it does not contribute to the rectified output of the diode.  $C_j$  is parasitic junction capacitance of the diode, controlled by the thickness of the epitaxial layer and the diameter of the Schottky contact.  $R_j$  is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5} n T}{I_s + I_b} = R_V - R_s$$

$$= \frac{0.026}{I_s + I_b} \text{ at } 25^\circ\text{C}$$

where

- $n$  = ideality factor (see table of SPICE parameters)
- $T$  = temperature in  $^\circ\text{K}$
- $I_s$  = saturation current (see table of SPICE parameters)
- $I_b$  = externally applied bias current in amps

$I_s$  is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5  $\mu\text{A}$  for very low barrier diodes.

### The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

$$I = I_s \left( \exp \left( \frac{V - IR_s}{0.026} \right) - 1 \right)$$

On a semi-log plot (as shown in the Avago catalog) the current graph will be a straight line with inverse slope  $2.3 \times 0.026 = 0.060$  volts per cycle (until the effect of  $R_s$  is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current,  $I_s$ , and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time  $C_j$  and  $R_s$  will be changed. In general, very low barrier height diodes (with high values of  $I_s$ , suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of  $R_s$  than do the n-type. Thus, p-type diodes are generally reserved for small signal detector applications (where very high values of  $R_V$  swamp out high  $R_s$ ) and n-type diodes are used for mixer applications (where high L.O. drive levels keep  $R_V$  low) and DC biased detectors.

### Measuring Diode Linear Parameters

The measurement of the many elements which make up the equivalent circuit for a packaged Schottky diode is a complex task. Various techniques are used for each element. The task begins with the elements of the diode chip itself. (See Figure 8).

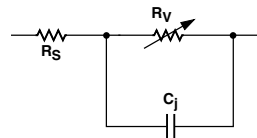


Figure 8. Equivalent Circuit of a Schottky Diode Chip.

$R_s$  is perhaps the easiest to measure accurately. The V-I curve is measured for the diode under forward bias, and the slope of the curve is taken at some relatively high value of current (such as 5 mA). This slope is converted into a resistance  $R_d$ .

$$R_s = R_d - \frac{0.026}{I_f}$$

For n-type diodes with relatively low values of saturation current,  $C_j$  is obtained by measuring the total capacitance (see AN1124).  $R_j$ , the junction resistance, is calculated using the equation given above.

The characterization of the surface mount package is too complex to describe here — linear equivalent circuits can be found in AN1124.

### Detector Circuits (small signal)

When DC bias is available, Schottky diode detector circuits can be used to create low cost RF and microwave receivers with a sensitivity of -55 dBm to -57 dBm.<sup>[1]</sup> Moreover, since external DC bias sets the video impedance of such circuits, they display classic square law response over a wide range of input power levels<sup>[2,3]</sup>. These circuits can take a variety of forms, but in the most simple case they appear as shown in Figure 9. This is the basic detector circuit used with the HSMS-286x family of diodes.

Output voltage can be virtually doubled and input impedance (normally very high) can be halved through the use of the voltage doubler circuit<sup>[4]</sup>.

In the design of such detector circuits, the starting point is the equivalent circuit of the diode. Of interest in the design of the video portion of the circuit is the diode's video impedance—the other elements of the equivalent circuit disappear at all reasonable video frequencies. In general, the lower the diode's video impedance, the better the design.

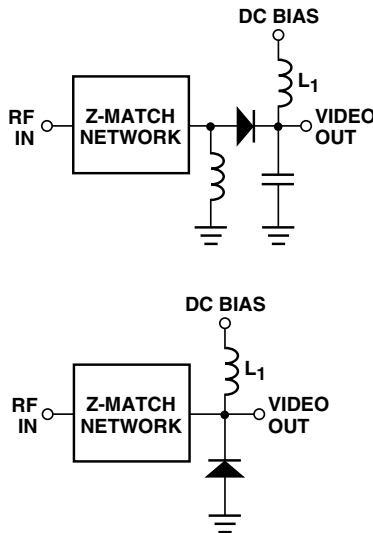


Figure 9. Basic Detector Circuits.

The situation is somewhat more complicated in the design of the RF impedance matching network, which includes the package inductance and capacitance (which can be tuned out), the series resistance, the junction capacitance and the video resistance. Of the elements of the diode's equivalent circuit, the parasitics are constants and the video resistance is a function of the current flowing through the diode.

$$R_V = R_j + R_S$$

The sum of saturation current and bias current sets the detection sensitivity, video resistance and input RF impedance of the Schottky detector diode. Where bias current is used, some tradeoff in sensitivity and square law dynamic range is seen, as shown in Figure 5 and described in reference <sup>[3]</sup>.

The most difficult part of the design of a detector circuit is the input impedance matching network. For very broadband detectors, a shunt 60 Ω resistor will give good input match, but at the expense of detection sensitivity.

When maximum sensitivity is required over a narrow band of frequencies, a reactive matching network is optimum. Such networks can be realized in either lumped or distributed elements, depending upon frequency, size constraints and cost limitations, but certain general design principals exist for all types.<sup>[5]</sup> Design work begins with the RF impedance of the HSMS-286x series when bias current is set to 3 μA. See Figure 10.



Figure 10. RF Impedance of the Diode.

<sup>[1]</sup> Avago Application Note 923, Schottky Barrier Diode Video Detectors.

<sup>[2]</sup> Avago Application Note 986, Square Law and Linear Detection.

<sup>[3]</sup> Avago Application Note 956-5, Dynamic Range Extension of Schottky Detectors.

<sup>[4]</sup> Avago Application Note 956-4, Schottky Diode Voltage Doubler.

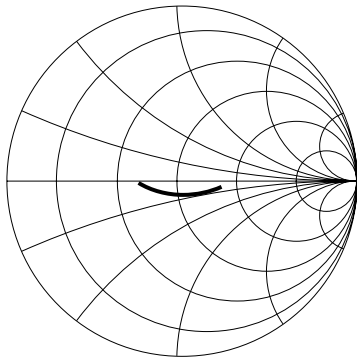
<sup>[5]</sup> Avago Application Note 963, Impedance Matching Techniques for Mixers and Detectors.

## 915 MHz Detector Circuit

Figure 11 illustrates a simple impedance matching network for a 915 MHz detector.



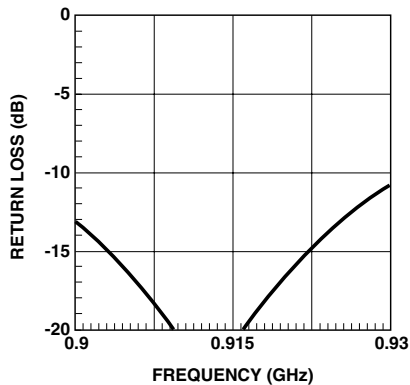
**Figure 11. 915 MHz Matching Network for the HSMS-286x Series at 3  $\mu$ A Bias.**  
A 65 nH inductor rotates the impedance of the diode to a point on the Smith Chart where a shunt inductor can pull it up to the center. The short length of 0.065" wide microstrip line is used to mount the lead of the diode's SOT-323 package. A shorted shunt stub of length  $<\lambda/4$  provides the necessary shunt inductance and simultaneously provides the return circuit for the current generated in the diode. The impedance of this circuit is given in Figure 12.



FREQUENCY (GHz): 0.9-0.93

**Figure 12. Input Impedance.**

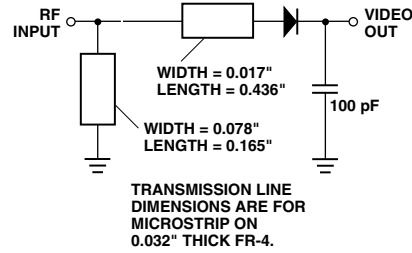
The input match, expressed in terms of return loss, is given in Figure 13.



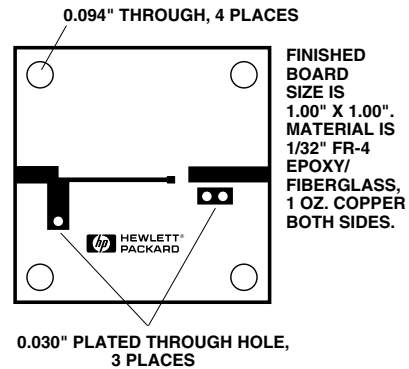
**Figure 13. Input Return Loss.**

As can be seen, the band over which a good match is achieved is more than adequate for 915 MHz RFID applications.

The HSMS-282x family is a better choice for 915 MHz applications—the foregoing discussion of a design using the HSMS-286B is offered only to illustrate a design approach for technique.



**Figure 14. 2.45 GHz Matching Network.**

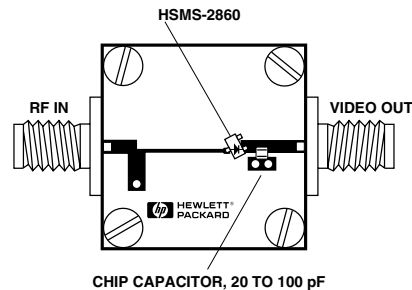


**Figure 15. Physical Realization.**

## 2.45 GHz Detector Circuit

At 2.45 GHz, the RF impedance is closer to the line of constant susceptance which passes through the center of the chart, resulting in a design which is realized entirely in distributed elements — see Figure 14.

In order to save cost (at the expense of having a larger circuit), an open circuit shunt stub could be substituted for the chip capacitor. On the other hand, if space is at a premium, the long series transmission line at the input to the diode can be replaced with a lumped inductor. A possible physical realization of such a network is shown in Figure 15, a demo board is available from Avago.

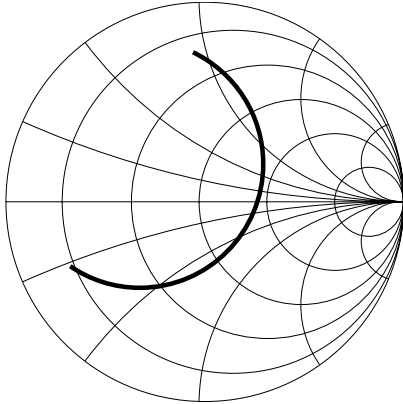


**Figure 16. Test Detector.**



Two SMA connectors (E.F. Johnson 142-0701-631 or equivalent), a high-Q capacitor (ATC 100A101MCA50 or equivalent), miscellaneous hardware and an HSMS-286B are added to create the test circuit shown in Figure 16.

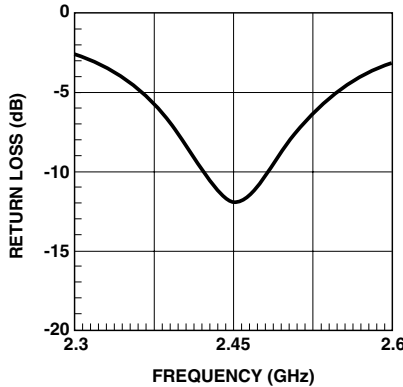
The calculated input impedance for this network is shown in Figure 17.



**FREQUENCY (GHz): 2.3-2.6**

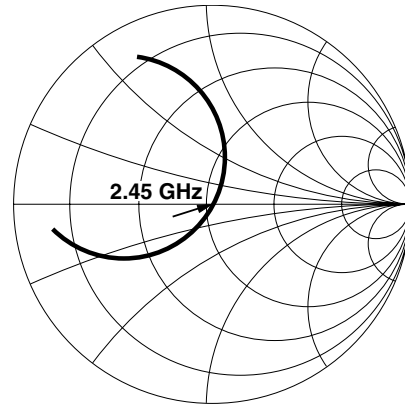
**Figure 17. Input Impedance, 3 μA Bias.**

The corresponding input match is shown in Figure 18. As was the case with the lower frequency design, bandwidth is more than adequate for the intended RFID application.



**Figure 18. Input Return Loss, 3 μA Bias.**

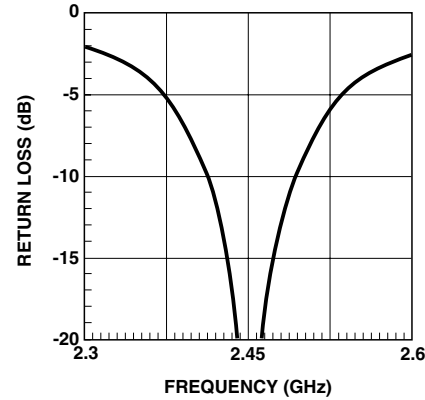
A word of caution to the designer is in order. A glance at Figure 17 will reveal the fact that the circuit does not provide the optimum impedance to the diode at 2.45 GHz. The temptation will be to adjust the circuit elements to achieve an ideal single frequency match, as illustrated in Figure 19.



**FREQUENCY (GHz): 2.3-2.6**

**Figure 19. Input Impedance. Modified 2.45 GHz Circuit.**

This does indeed result in a very good match at midband, as shown in Figure 20.

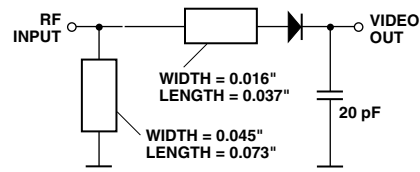


**Figure 20. Input Return Loss. Modified 2.45 GHz Circuit.**

However, bandwidth is narrower and the designer runs the risk of a shift in the midband frequency of his circuit if there is any small deviation in circuit board or diode characteristics due to lot-to-lot variation or change in temperature. The matching technique illustrated in Figure 17 is much less sensitive to changes in diode and circuit board processing.

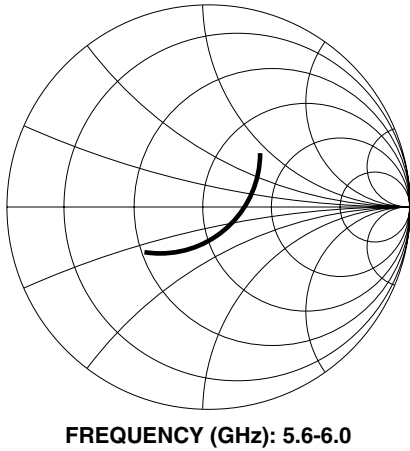
### 5.8 GHz Detector Circuit

A possible design for a 5.8 GHz detector is given in Figure 21.



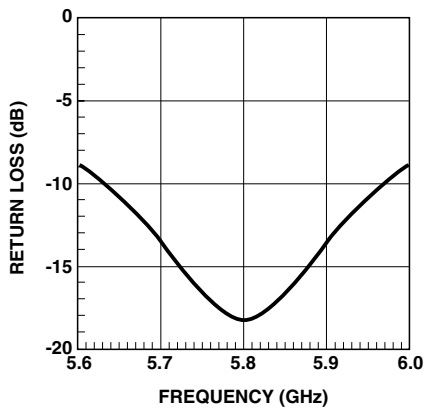
**Figure 21. 5.8 GHz Matching Network for the HSMS-286x Series at 3 μA Bias.**

As was the case at 2.45 GHz, the circuit is entirely distributed element, both low cost and compact. Input impedance for this network is given in Figure 22.



**Figure 22. Input Impedance.**

Input return loss, shown in Figure 23, exhibits wideband match.



**Figure 23. Input Return Loss.**

### Voltage Doublers

To this point, we have restricted our discussion to single diode detectors. A glance at Figure 9, however, will lead to the suggestion that the two types of single diode detectors be combined into a two diode voltage doubler<sup>[4]</sup> (known also as a full wave rectifier). Such a detector is shown in Figure 24.



**Figure 24. Voltage Doubler Circuit.**

Such a circuit offers several advantages. First the voltage outputs of two diodes are added in series, increasing the overall value of voltage sensitivity for the network (compared to a single diode detector). Second, the RF impedances of the two diodes are added in parallel, making the job of reactive matching a bit easier. Such a circuit can easily be realized using the two series diodes in the HSMS-286C.

### The “Virtual Battery”

The voltage doubler can be used as a virtual battery, to provide power for the operation of an I.C. or a transistor oscillator in a tag. Illuminated by the CW signal from a reader or interrogator, the Schottky circuit will produce power sufficient to operate an I.C. or to charge up a capacitor for a burst transmission from an oscillator. Where such virtual batteries are employed, the bulk, cost, and limited lifetime of a battery are eliminated.

### Temperature Compensation

The compression of the detector’s transfer curve is beyond the scope of this data sheet, but some general comments can be made. As was given earlier, the diode’s video resistance is given by

$$R_V = \frac{8.33 \times 10^{-5} \text{ nT}}{I_s + I_b}$$

where T is the diode’s temperature in °K.

As can be seen, temperature has a strong effect upon  $R_V$ , and this will in turn affect video bandwidth and input RF impedance. A glance at Figure 6 suggests that the proper choice of bias current in the HSMS-286x series can minimize variation over temperature.

The detector circuits described earlier were tested over temperature. The 915 MHz voltage doubler using the HSMS-286C series produced the output voltages as shown in Figure 25. The use of 3  $\mu\text{A}$  of bias resulted in the highest voltage sensitivity, but at the cost of a wide variation over temperature. Dropping the bias to 1  $\mu\text{A}$  produced a detector with much less temperature variation.

A similar experiment was conducted with the HSMS-286B series in the 5.8 GHz detector. Once again, reducing the bias to some level under 3  $\mu\text{A}$  stabilized the output of the detector over a wide temperature range.

It should be noted that curves such as those given in Figures 25 and 26 are highly dependent upon the exact design of the input impedance matching network. The designer will have to experiment with bias current using his specific design.



Figure 25. Output Voltage vs. Temperature and Bias Current in the 915 MHz Voltage Doubler using the HSMS-286C.

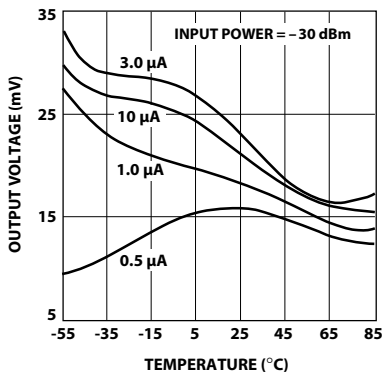


Figure 26. Output Voltage vs. Temperature and Bias Current in the 5.80 GHz Voltage Detector using the HSMS-286B Schottky.

### Six Lead Circuits

The differential detector is often used to provide temperature compensation for a Schottky detector, as shown in Figures 27 and 28.

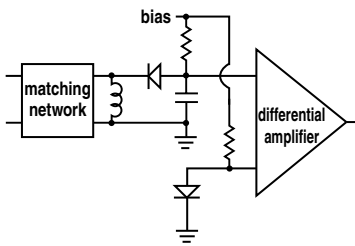


Figure 27. Differential Detector.

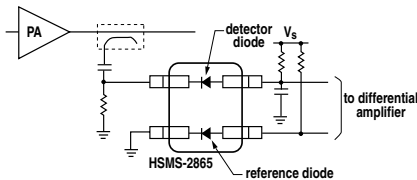


Figure 28. Conventional Differential Detector.

These circuits depend upon the use of two diodes having matched  $V_f$  characteristics over all operating temperatures. This is best achieved by using two diodes

in a single package, such as the SOT-143 HSMS-2865 as shown in Figure 29.

In high power differential detectors, RF coupling from the detector diode to the reference diode produces a rectified voltage in the latter, resulting in errors.

Isolation between the two diodes can be obtained by using the HSMS-286K diode with leads 2 and 5 grounded. The difference between this product and the conventional HSMS-2865 can be seen in Figure 29.

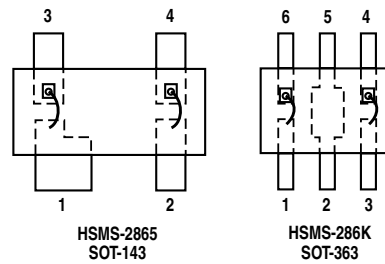


Figure 29. Comparing Two Diodes.

The HSMS-286K, with leads 2 and 5 grounded, offers some isolation from RF coupling between the diodes. This product is used in a differential detector as shown in Figure 30.

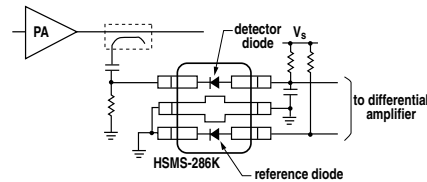


Figure 30. High Isolation Differential Detector.

In order to achieve the maximum isolation, the designer must take care to minimize the distance from leads 2 and 5 and their respective ground via holes.

Tests were run on the HSMS-282K and the conventional HSMS-2825 pair, which compare with each other in the same way as the HSMS-2865 and HSMS-286K, with the results shown in Figure 31.

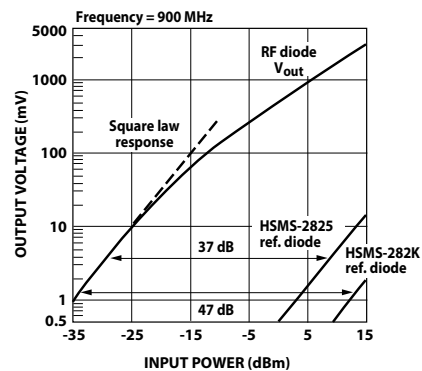


Figure 31. Comparing HSMS-282K with HSMS-2825.

The line marked “RF diode,  $V_{out}$ ” is the transfer curve for the detector diode—both the HSMS-2825 and the HSMS-282K exhibited the same output voltage. The data were taken over the 50 dB dynamic range shown. To the right is the output voltage (transfer) curve for the reference diode of the HSMS-2825, showing 37 dB of isolation. To the right of that is the output voltage due to RF leakage for the reference diode of the HSMS-282K, demonstrating 10 dB higher isolation than the conventional part.

Such differential detector circuits generally use single diode detectors, either series or shunt mounted diodes. The voltage doubler offers the advantage of twice the output voltage for a given input power. The two concepts can be combined into the differential voltage doubler, as shown in Figure 32.



**Figure 32. Differential Voltage Doubler, HSMS-286P.**

Here, all four diodes of the HSMS-286P are matched in their  $V_f$  characteristics, because they came from adjacent sites on the wafer. A similar circuit can be realized using the HSMS-286R ring quad.

Other configurations of six lead Schottky products can be used to solve circuit design problems while saving space and cost.

### Thermal Considerations

The obvious advantage of the SOT-363 over the SOT-143 is combination of smaller size and two extra leads. However, the copper leadframe in the SOT-323 and SOT-363 has a thermal conductivity four times higher than the Alloy 42 leadframe of the SOT-23 and SOT-143, which enables it to dissipate more power.

The maximum junction temperature for these three families of Schottky diodes is 150°C under all operating conditions. The following equation, equation 1, applies to the thermal analysis of diodes:

$$T_j = (V_f I_f + P_{RF}) \theta_{jc} + T_a \quad \text{Equation (1)}$$

where

- $T_j$  = junction temperature
- $T_a$  = diode case temperature
- $\theta_{jc}$  = thermal resistance
- $V_f I_f$  = DC power dissipated

$$P_{RF} = \text{RF power dissipated}$$

Note that  $\theta_{jc}$ , the thermal resistance from diode junction to the foot of the leads, is the sum of two component resistances,

$$\theta_{jc} = \theta_{pkg} + \theta_{chip} \quad \text{Equation (2)}$$

Package thermal resistance for the SOT-323 and SOT-363 package is approximately 100°C/W, and the chip thermal resistance for these three families of diodes is approximately 40°C/W. The designer will have to add in the thermal resistance from diode case to ambient—a poor choice of circuit board material or heat sink design can make this number very high.

Equation (1) would be straightforward to solve but for the fact that diode forward voltage is a function of temperature as well as forward current. The equation, equation 3, for  $V_f$  is:

$$I_f = I_s \left[ e^{\frac{11600 (V_f - I_f R_s)}{nT}} - 1 \right] \quad \text{Equation (3)}$$

where

- $n$  = ideality factor
- $T$  = temperature in °K
- $R_s$  = diode series resistance

and  $I_s$  (diode saturation current) is given by

$$I_s = I_0 \left( \frac{T}{298} \right)^{\frac{2}{n}} e^{-4060 \left( \frac{1}{T} - \frac{1}{298} \right)} \quad \text{Equation (4)}$$

Equations (1) and (3) are solved simultaneously to obtain the value of junction temperature for given values of diode case temperature, DC power dissipation and RF power dissipation.

## Diode Burnout

Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.<sup>[6]</sup> Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Avago offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) or HSMP-482B (SOT-323) can act as a very fast (nano-second) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

## Assembly Instructions

### SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 33 (dimensions are in inches).



**Figure 33. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.**

A recommended PCB pad layout for the miniature SOT-363 (SC-70 6 lead) package is shown in Figure 34 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.



**Figure 34. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.**

<sup>[6]</sup> Avago Application Note 1050, Low Cost, Surface Mount Power Limiters.

## SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT packages, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 35. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat

zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone ( $T_{MAX}$ ) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

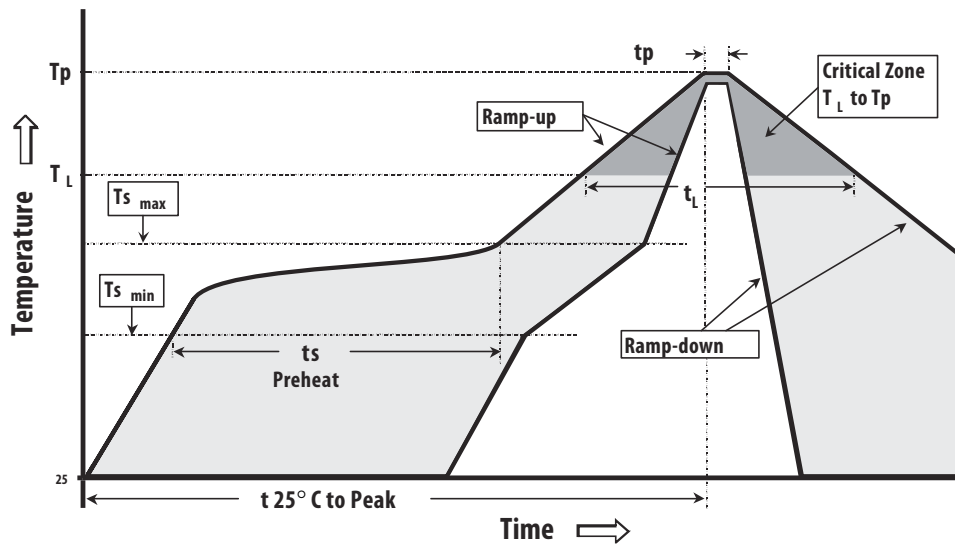


Figure 35. Surface Mount Assembly Profile.

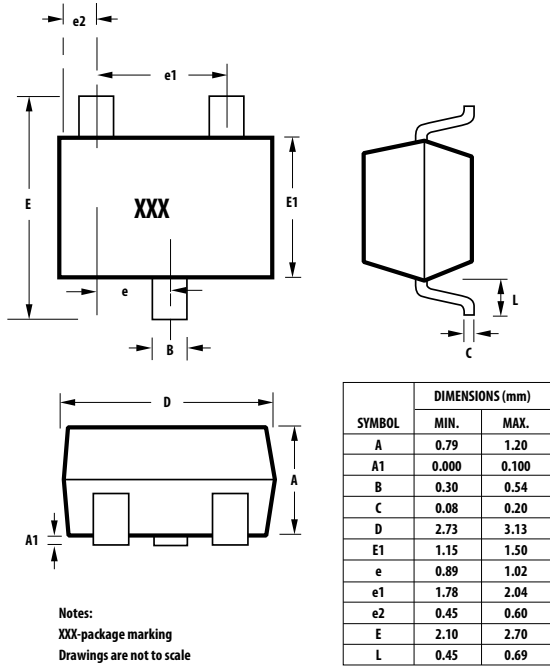
### Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter	Lead-Free Assembly	
Average ramp-up rate (Liquidus Temperature ( $T_{S(max)}$ ) to Peak)	3°C/ second max	
Preheat	Temperature Min ( $T_{S(min)}$ )	150°C
	Temperature Max ( $T_{S(max)}$ )	200°C
	Time (min to max) ( $t_s$ )	60-180 seconds
$T_{S(max)}$ to $T_L$ Ramp-up Rate	3°C/second max	
Time maintained above:	Temperature ( $T_L$ )	217°C
	Time ( $t_L$ )	60-150 seconds
Peak Temperature ( $T_p$ )	260 +0/-5°C	
Time within 5 °C of actual Peak temperature ( $t_p$ )	20-40 seconds	
Ramp-down Rate	6°C/second max	
Time 25 °C to Peak Temperature	8 minutes max	

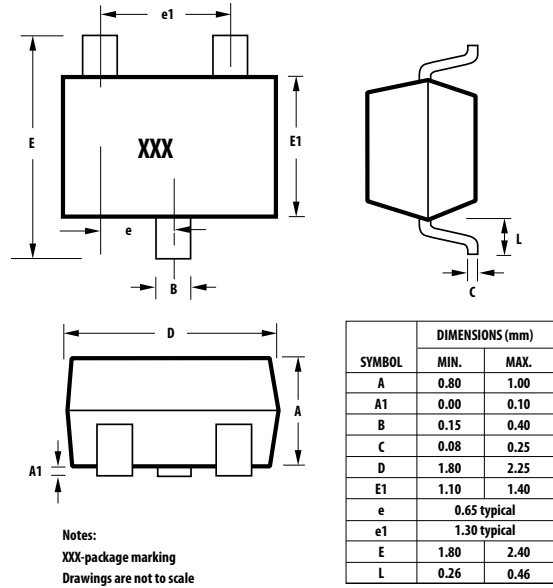
Note 1: All temperatures refer to topside of the package, measured on the package body surface

# Package Dimensions

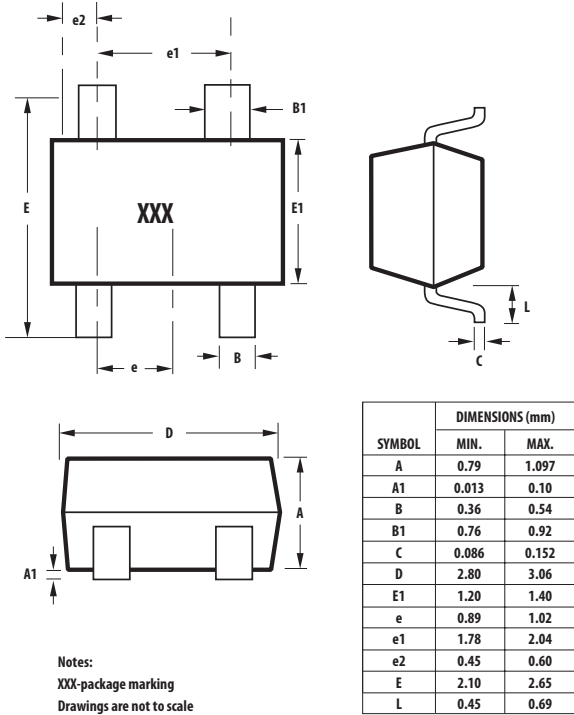
## Outline 23 (SOT-23)



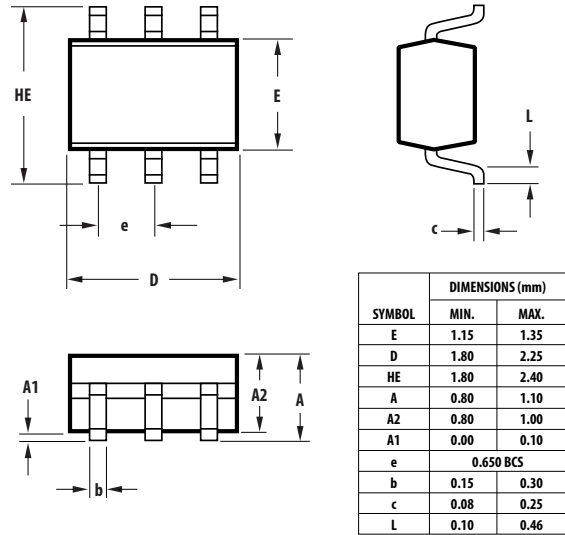
## Outline SOT-323 (SC-70 3 Lead)



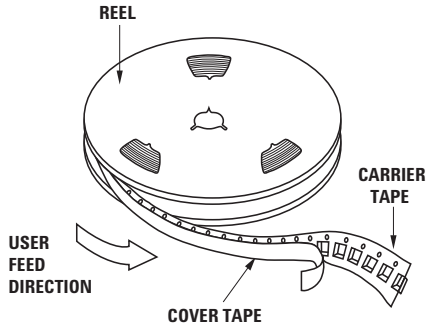
## Outline 143 (SOT-143)



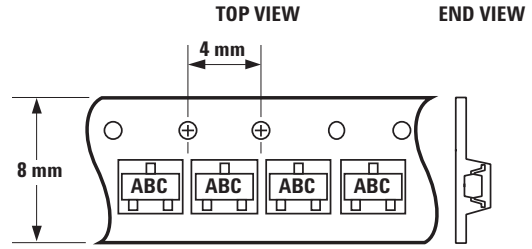
## Outline SOT-363 (SC-70 6 Lead)



**Device Orientation**

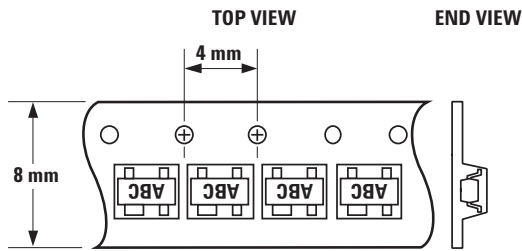


**For Outlines SOT-23, -323**



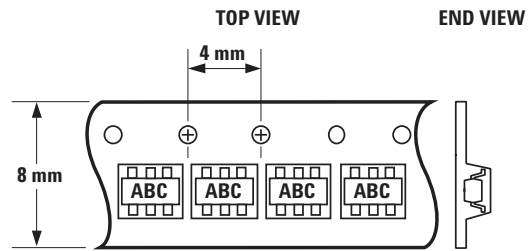
Note: "AB" represents package marking code.  
"C" represents date code.

**For Outline SOT-143**



Note: "AB" represents package marking code.  
"C" represents date code.

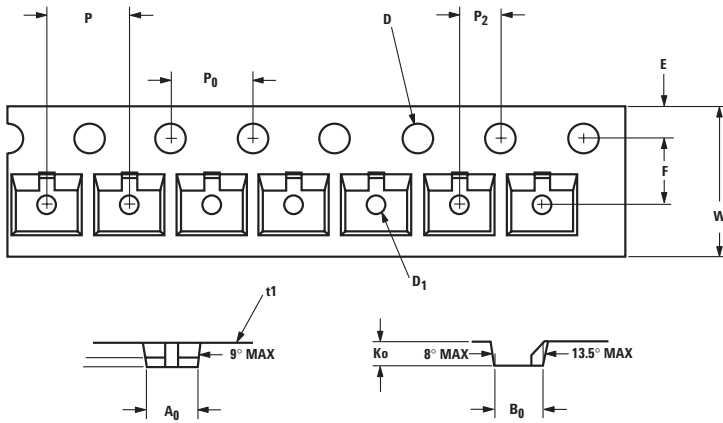
**For Outline SOT-363**



Note: "AB" represents package marking code.  
"C" represents date code.

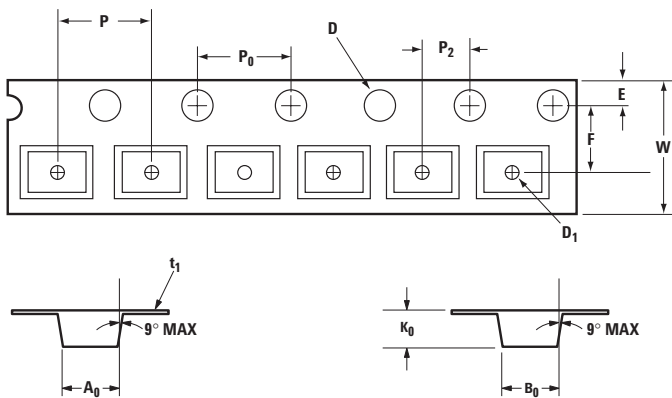


## Tape Dimensions and Product Orientation For Outline SOT-23



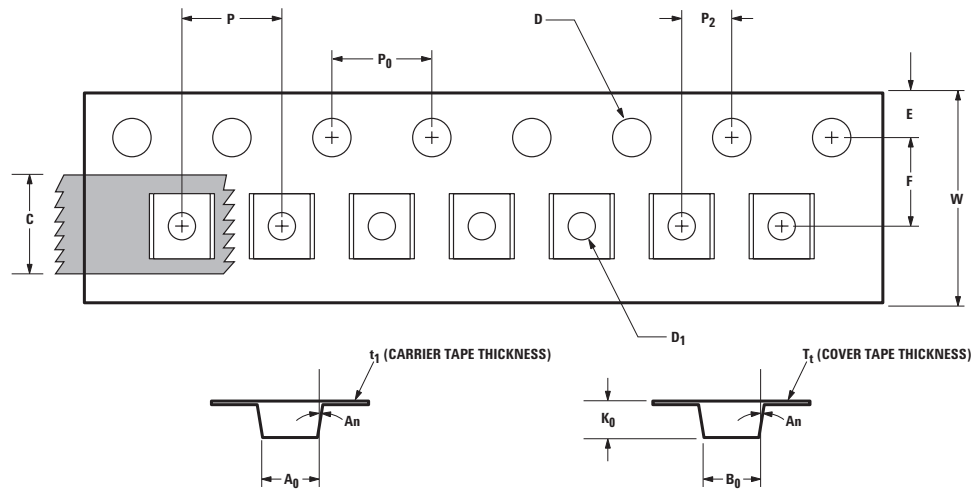
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A <sub>0</sub>	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B <sub>0</sub>	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K <sub>0</sub>	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D <sub>1</sub>	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P <sub>0</sub>	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t <sub>1</sub>	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P <sub>2</sub>	2.00 ± 0.05	0.079 ± 0.002

## For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A <sub>0</sub>	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B <sub>0</sub>	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K <sub>0</sub>	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D <sub>1</sub>	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P <sub>0</sub>	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t <sub>1</sub>	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P <sub>2</sub>	2.00 ± 0.05	0.079 ± 0.002

## Tape Dimensions and Product Orientation For Outlines SOT-323, -363



	DESCRIPTION	SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	$A_0$	$2.40 \pm 0.10$	$0.094 \pm 0.004$
	WIDTH	$B_0$	$2.40 \pm 0.10$	$0.094 \pm 0.004$
	DEPTH	$K_0$	$1.20 \pm 0.10$	$0.047 \pm 0.004$
	PITCH	$P$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	BOTTOM HOLE DIAMETER	$D_1$	$1.00 + 0.25$	$0.039 + 0.010$
PERFORATION	DIAMETER	$D$	$1.55 \pm 0.05$	$0.061 \pm 0.002$
	PITCH	$P_0$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	POSITION	$E$	$1.75 \pm 0.10$	$0.069 \pm 0.004$
CARRIER TAPE	WIDTH	$W$	$8.00 \pm 0.30$	$0.315 \pm 0.012$
	THICKNESS	$t_1$	$0.254 \pm 0.02$	$0.0100 \pm 0.0008$
COVER TAPE	WIDTH	$C$	$5.4 \pm 0.10$	$0.205 \pm 0.004$
	TAPE THICKNESS	$T_t$	$0.062 \pm 0.001$	$0.0025 \pm 0.00004$
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	$F$	$3.50 \pm 0.05$	$0.138 \pm 0.002$
	CAVITY TO PERFORATION (LENGTH DIRECTION)	$P_2$	$2.00 \pm 0.05$	$0.079 \pm 0.002$
ANGLE	FOR SOT-323 (SC70-3 LEAD) FOR SOT-363 (SC70-6 LEAD)	$A_n$	8°C MAX 10°C MAX	

### Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-286x-TR2G	10000	13" Reel
HSMS-286x-TR1G	3000	7" Reel
HSMS-286x-BLKG	100	antistatic bag

where x = 0, 2, 3, 4, 5, B, C, E, F, K, L, P or R for HSMS-286x.

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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