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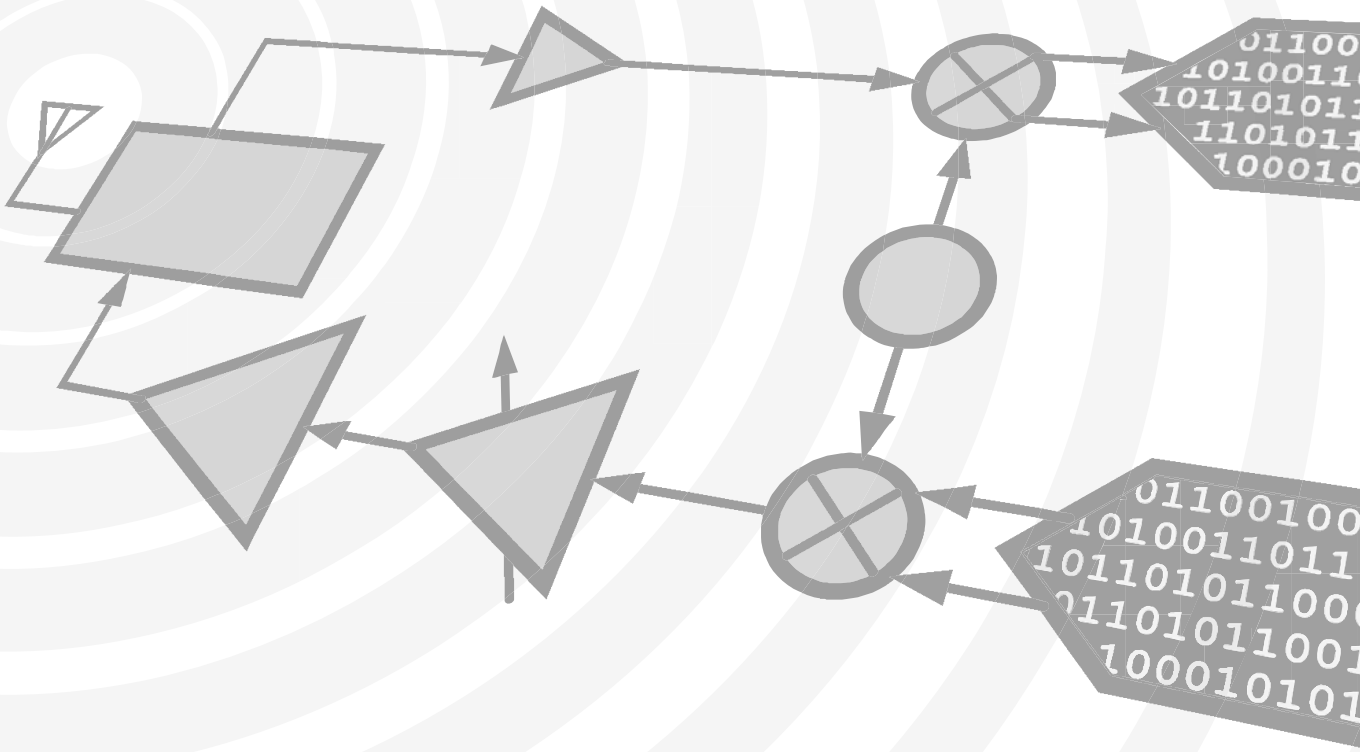
**NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED**



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# HMC1120LP4E

## RMS POWER DETECTOR & ENVELOPE TRACKER, DC - 3.9 GHz



### Typical Applications

The HMC1120LP4E is ideal for:

- Log –> Root-Mean-Square (RMS) Conversion
- Tx/Rx Signal Strength Indication (TSSI/RSSI)
- RF Power Amplifier Efficiency Control
- Receiver Automatic Gain Control
- Transmitter Power Control
- Envelope Tracking
- PA Linearization

### Features

Broadband Single-Ended RF Input

RMS Detector with ±1 dB Detection Accuracy up to 3.9 GHz

Input Dynamic Range: -60 dBm to +8 dBm

±1 dB Envelope Detection Accuracy over 30 dB Input Range

Envelope Detection Bandwidth > 150MHz

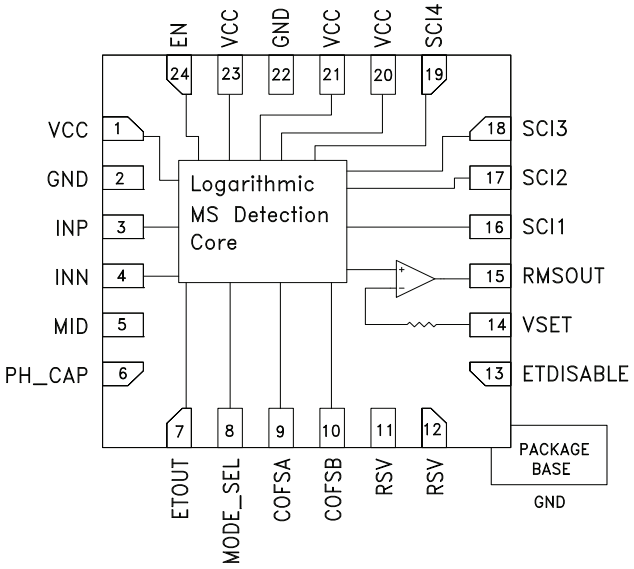
Digitally Programmable Integration Bandwidth

Power-Down Mode

24 Lead 4x4mm SMT Package: 16mm²

Envelope Tracking Power-Down Mode

### Functional Diagram




### General Description

The HMC1120LP4E is an RMS power detector with an integrated high bandwidth envelope detector. The RMS output is a temperature compensated, monotonic, linear-in-dB representation of real RF signal power, measured over an input sensing range of 70 dB. The envelope detector provides an accurate voltage output which is linearly proportional to the amplitude envelope of the RF input signal for modulation bandwidths up to 150 MHz. The high bandwidth envelope detection of the HMC1120LP4E makes it ideal for detecting broadband and high crest factor RF signals commonly used in GSM, WCDMA, and LTE systems. Additionally, the instantaneous envelope output can be used to create fast, excessive RF power protection, PA linearization, and efficiency enhancing envelope-tracking PA implementations.

The HMC1120LP4E's RMS detector integration bandwidth is digitally programmable via input pins SCI1-4 over a range of more than 4 decades. This allows the user to dynamically set the operation bandwidth and also permits the detection of different types of modulations on the same platform.

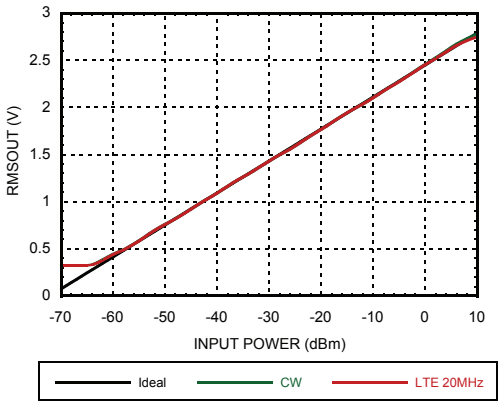
The HMC1120LP4E features an internal op-amp at the RMS output stage, which accommodates slope and intercept adjustments and supports a wide range of applications.

### Table 1. Electrical Specifications, $T_A$ = +25 °C, Vcc = 3.3V, SCI4 = SCI3 = SCI2 = SCI1 = 3.3V, Unless Otherwise Noted

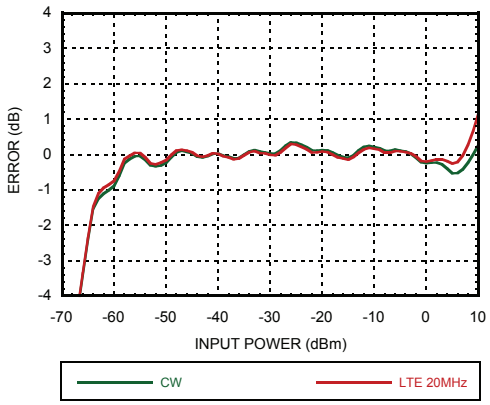
| Parameter | Typ. | Typ. | Typ. | Typ. | Typ. | Typ. | Typ. | Units |
|---|---|---|---|---|---|---|---|---|
| **Input Frequency** | **100** | **900** | **1900** | **2200** | **2700** | **3500** | **3900** | **MHz** |
| **Dynamic Range** (±1dB Error) [1] | | | | | | | | |
| RMSOUT Output | 72 | 72 | 72 | 72 | 72 | 67 | 62 | dB |
| ETOUT Output | 27 | 27 | 27 | 27 | 28 | 27 | 27 | dB |
| **Deviation vs Temperature:** (Over full temperature range -40 °C to 85 °C). Deviation is measured from reference, which is the same LTE input at 25 °C. | | | | | | | | dB |
| **Modulation Deviation** (Output deviation from reference, which is measured with CW input at equivalent input signal power) | | | | | | | | |
| LTE 20MHz at +25 °C | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.15 | dB |
| LTE 20MHz at +85°C | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.15 | dB |
| LTE 20MHz at -40 °C | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.2 | dB |
| **RMSOUT Logarithmic Slope and Intercept** [1] | | | | | | | | |
| Logarithmic Slope | 34.4 | 34.4 | 33.9 | 33.9 | 34 | 35.2 | 37 | mV/dB |
| Logarithmic Intercept | -71 | -71.5 | -72.2 | -72.2 | -71.5 | -69 | -66 | dBm |
| Max. Input Power at ±1dB Error | 10 | 10 | 10 | 10 | 10 | 7 | 5 | dBm |
| Min. Input Power at ±1dB Error | -62 | -62 | -62 | -62 | -62 | -60 | -57 | dBm |
| **ETOUT Linear Slope and Intercept** | | | | | | | | |
| Linear Slope | 1.3 | 1.32 | 1.45 | 1.52 | 1.55 | 1.7 | 1.72 | V/Vp |
| Linear Intercept | -725 | -710 | -635 | -615 | -605 | -550 | -550 | mV |
| Max. Input Power at ±1dB Error | 6 | 5 | 5 | 4 | 4 | 3 | 2 | dBm |
| Min. Input Power at ±1dB Error | -21 | -22 | -22 | -23 | -24 | -24 | -25 | dBm |

[1] With LTE 20MHz

### RMSOUT vs. Pin with Different Modulations @ 1900 MHz [1]




### RMSOUT Error vs. Pin with Different Modulations @ 1900 MHz [1]

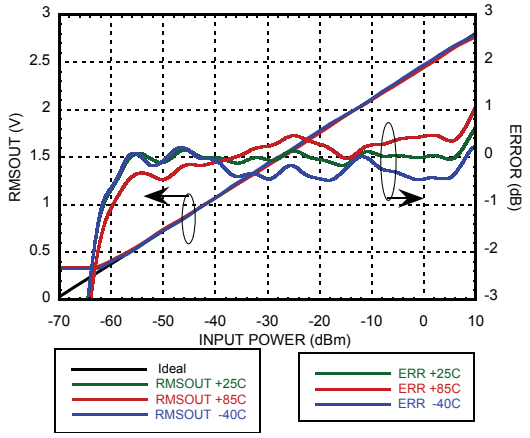



[1] Data was taken at SCI4=SCI3=SCI2=SCI1=3.3V.

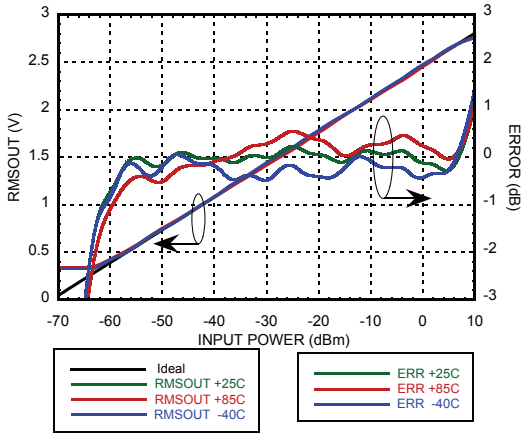
### Table 2. Electrical Specifications II, $T_A$ = +25 °C, Vcc = 3.3V, SCI4 = SCI3 = SCI2 = SCI1 = 3.3V, Unless Otherwise Noted

| Parameter | Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| **Single-Ended Input Configuration** | | | | | |
| Input Network Return Loss | up to 3.9 GHz | | > 12 | | dB |
| Input Resistance between INP and INN | Between pins 3 and 4 | | 100 | | Ω |
| Input Voltage Range | AC Coupled Peak Voltage at INP_ | | | 1 | V |
| **RMSOUT Output** | | | | | |
| Output Voltage Range | | | 0.32 to 2.7 | | V |
| Source/Sink Current Compliance | RMSOUT held at VCC/2 | | +8 / -8 | | mA |
| Output Slew Rate (rise / fall) | Sci4=Sci3=Sci2=Sci1=0V, Cofs=1nF | | 10.4 / 3.1 | | $10^6$ V/s |
| **ETOUT Output** | | | | | |
| Modulation Bandwidth | | | 150 | | MHz |
| Output Voltage Range | | | 0.95 to 1.65 | | V |
| Source/Sink Current Compliance | | | 8 / -3.9 | | mA |
| Output Slew Rate (rise / fall) | | | 210 / 242 | | $10^6$ V/s |
| Peak Hold Time | %1 voltage drop from last peak, no external capacitor is connected | | 154 | | µs |
| **VSET Input (Negative Feedback Terminal)** | | | | | |
| Input Voltage Range | For control applications with nominal slope/intercept settings | | 0.13 to 2.7 | | V |
| Input Resistance | | | 5 | | MΩ |
| **SCI1-4 Inputs, EN Logic Input (Power Down Control)** | | | | | |
| Input High Voltage | | 0.7xVCC | | | V |
| Input Low Voltage | | | | 0.3xVCC | V |
| Input High Current | | | | 1 | µA |
| Input Low Current | | | | 1 | µA |
| Input Capacitance | | | 0.5 | | pf |
| **Power Supply** | | | | | |
| Supply Voltage | | 3.15 | 3.3 | 3.45 | V |
| Supply Current with no input power | EN = VCC, ETDISABLE = GND | 77 | 82 | 90 | mA |
| | EN = VCC, ETDISABLE = VCC | | 62 | | mA |
| Supply Current with 0 dBm | | 84 | 87 | 100 | mA |
| Standby Mode Supply Current | EN = GND, ETDISABLE = VCC | 7 | 9 | 12 | mA |

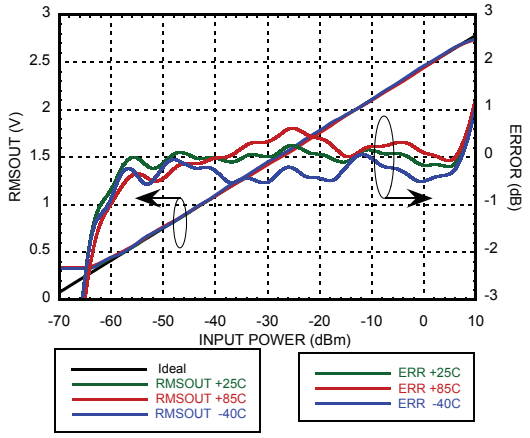
### RMSOUT & Error vs. Pin @ 100 MHz [1] [2]



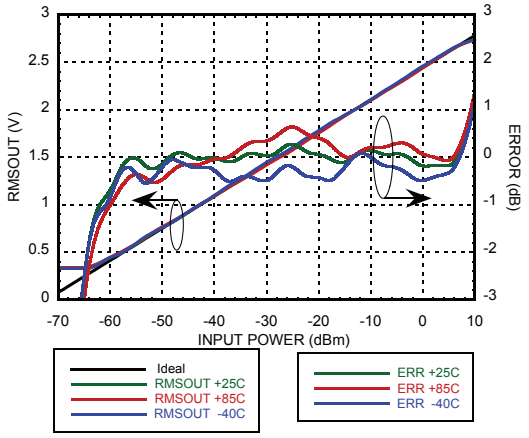

### RMSOUT & Error vs. Pin @ 900 MHz [1] [2]



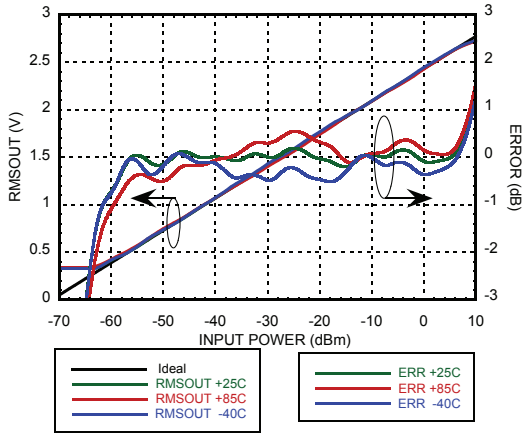

### RMSOUT & Error vs. Pin @ 1900 MHz [1] [2]



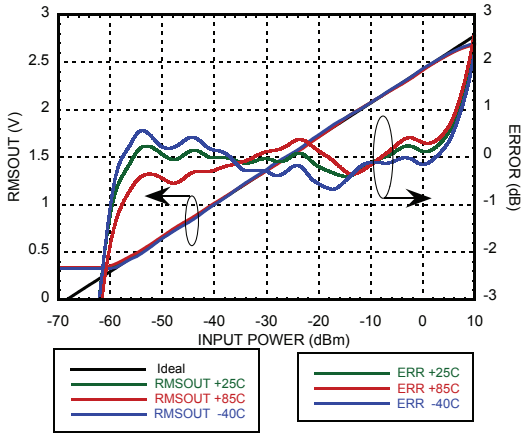

### RMSOUT & Error vs. Pin @ 2200 MHz [1] [2]




### RMSOUT & Error vs. Pin @ 2700 MHz [1] [2]



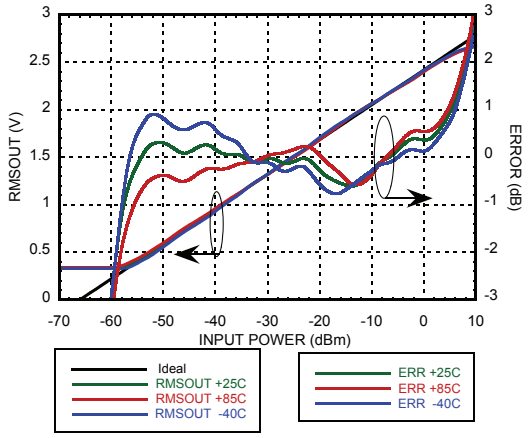

### RMSOUT & Error vs. Pin @ 3500 MHz [1] [2]



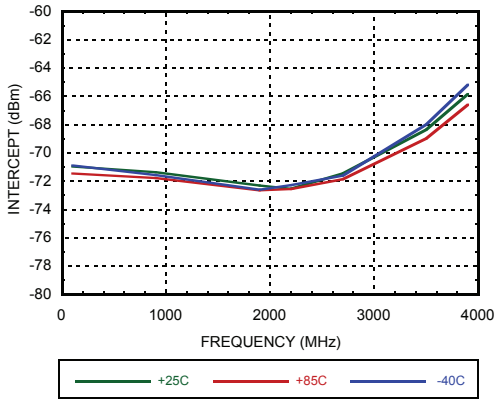

[1] Data was taken at SCI4=SCI3=SCI2=SCI1=3.3V.

[2] LTE 20MHz input waveform.

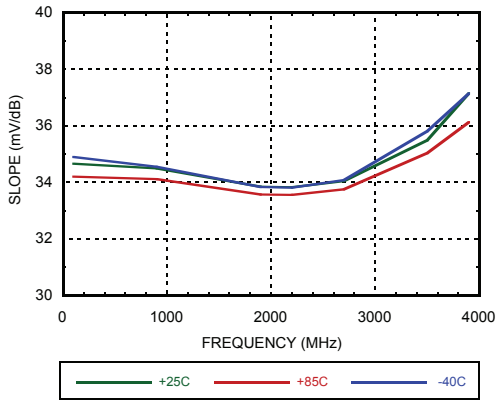
### RMSOUT & Error vs. Pin @ 3900 MHz [1] [2]



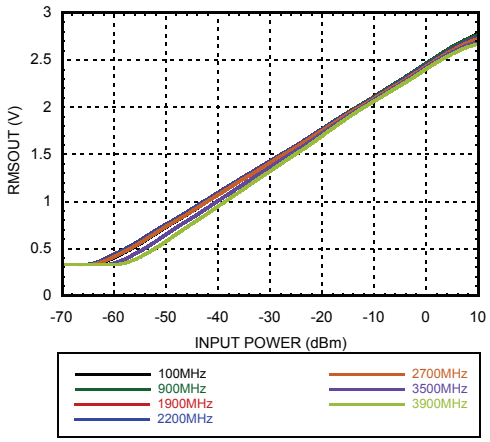

### RMSOUT Intercept vs. Frequency [1] [2]



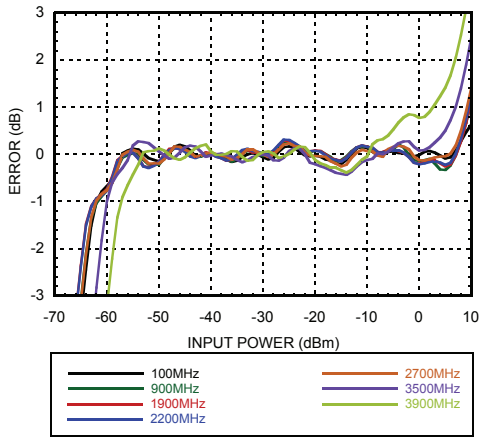

### RMSOUT Slope vs. Frequency [1] [2]



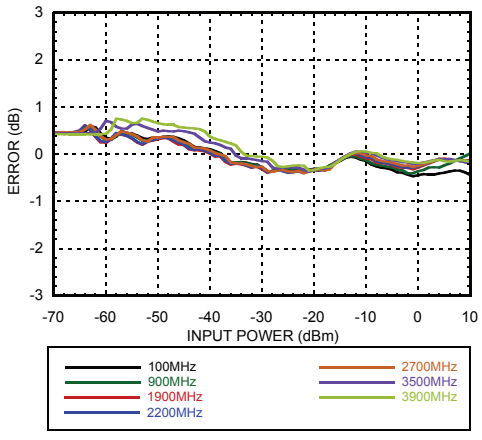

### RMSOUT vs. Pin with LTE 20MHz @ +25 °C [1]




### RMSOUT Error vs. Pin with LTE 20MHz @ +25 °C [1]



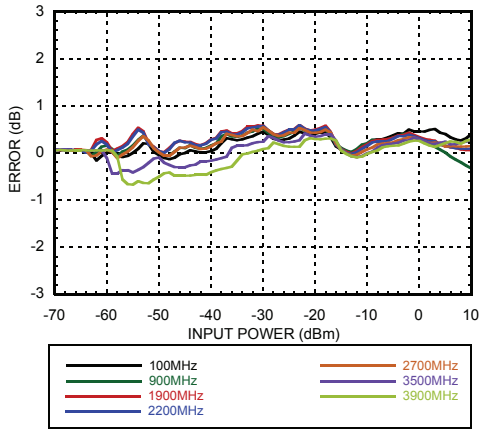

### RMSOUT Error vs. Pin with LTE 20MHz @ +85 °C wrt +25 °C Ideal [1]



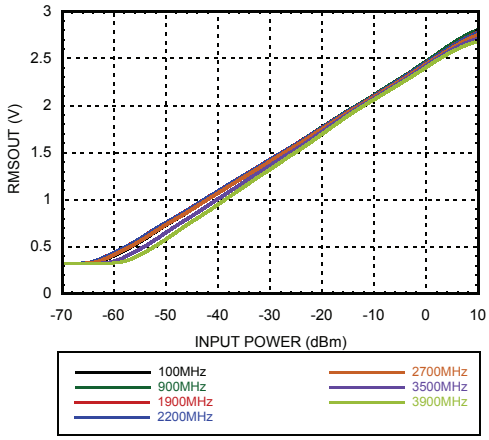

[1] Data was taken at SCI4=SCI3=SCI2=SCI1=3.3V

[2] LTE 20MHz input waveform

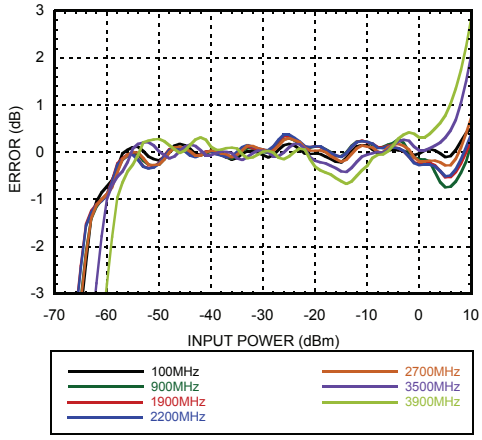
### RMSOUT Error vs. Pin with LTE 20MHz @ -40 °C wrt +25 °C Ideal [1]



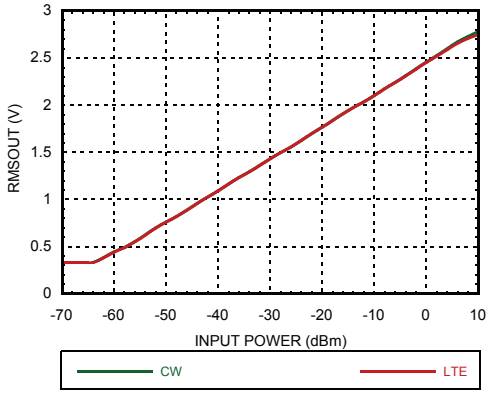

### RMSOUT vs. Pin with CW @ +25 °C [1]



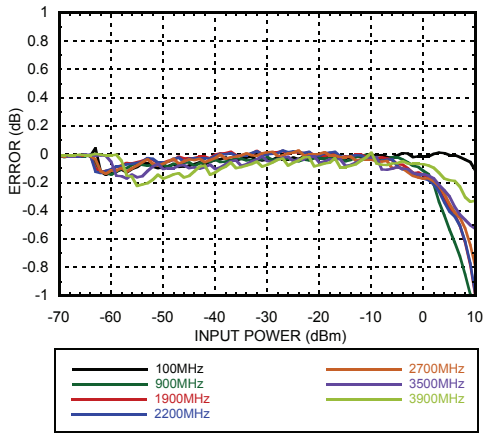

### RMSOUT Error vs. Pin with CW @ +25 °C [1]



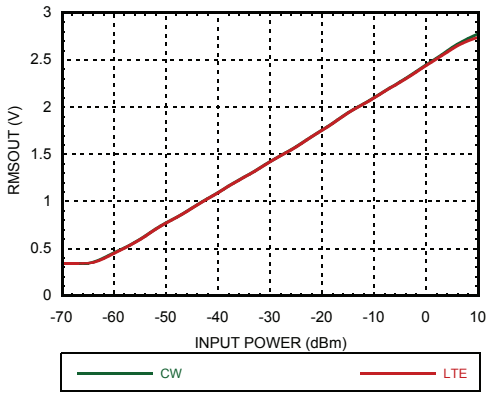

### RMSOUT vs. Pin w/ CW & LTE 20MHz @ 1900 MHz & +25 °C [1]




### Reading Error for LTE 20MHz wrt CW Response @ +25 °C [1]

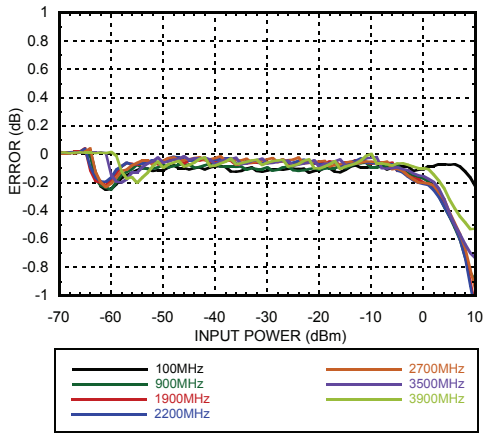



### RMSOUT vs. Pin w/ CW & LTE 20MHz @ 1900 MHz & +85 °C [1]

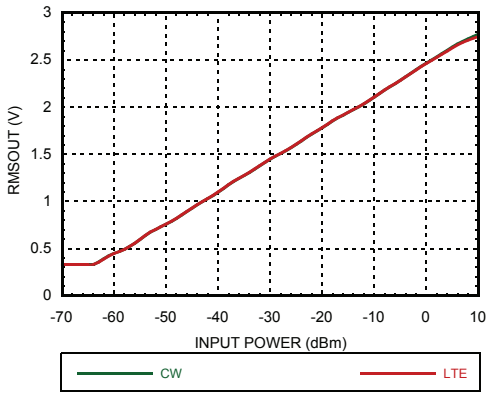



[1] Data was taken at SCI4=SCI3=SCI2=SCI1=3.3V

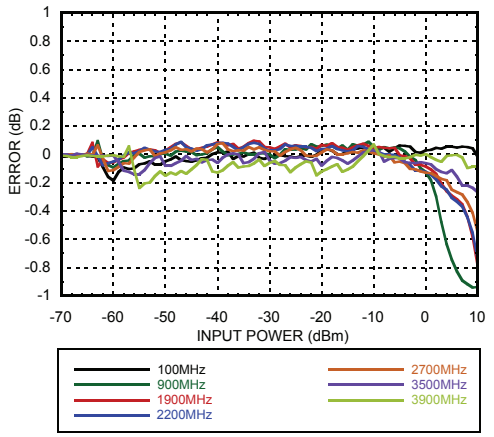
### Reading Error for LTE 20MHz wrt CW Response @ +85 °C [1]



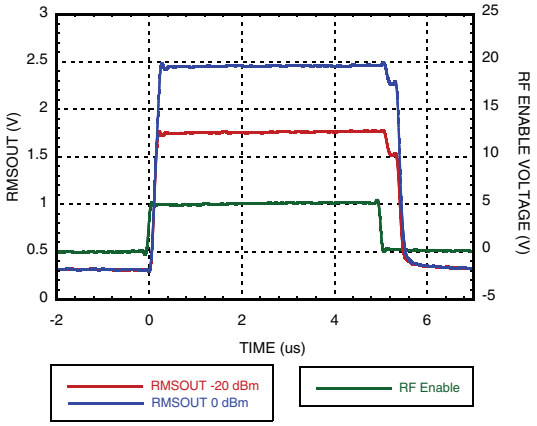

### RMSOUT vs. Pin w/ CW & LTE 20MHz @ 1900 MHz & -40 °C [1]



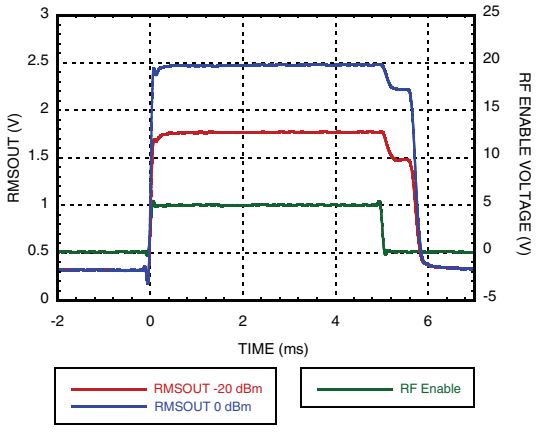

### Reading Error for LTE 20MHz wrt CW Response @ -40 °C [1]



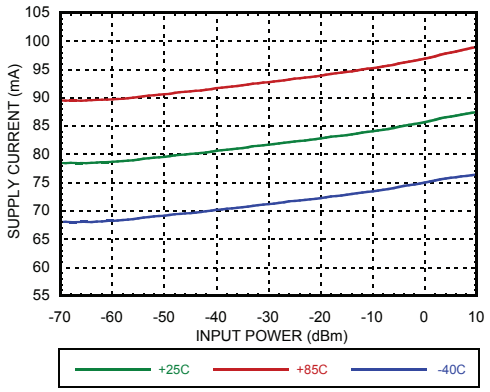

### RMSOUT Output Response with SCI = 0000 @ 1900 MHz [2]




### RMSOUT Output Response with SCI = 1100 @ 1900 MHz [2]



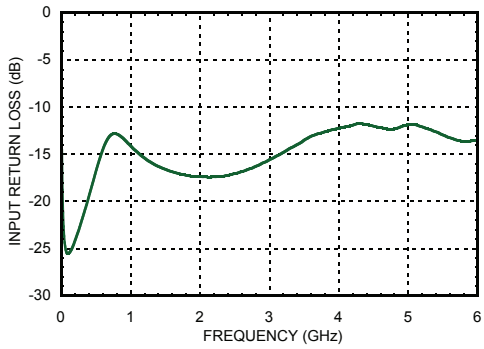

### Typical Supply Current vs. Pin, Vcc = 3.3V



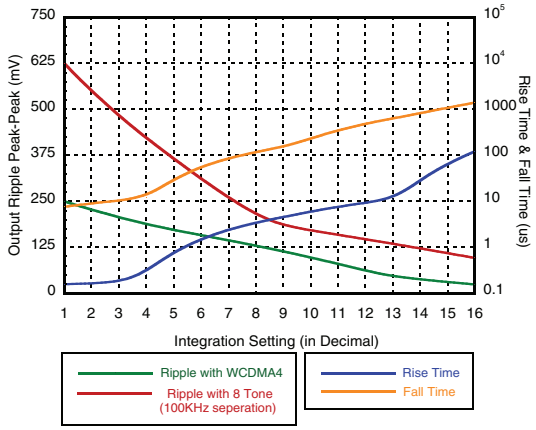

[1] Data was taken at SCI4=SCI3=SCI2=SCI1=3.3V

[2] CW input waveform

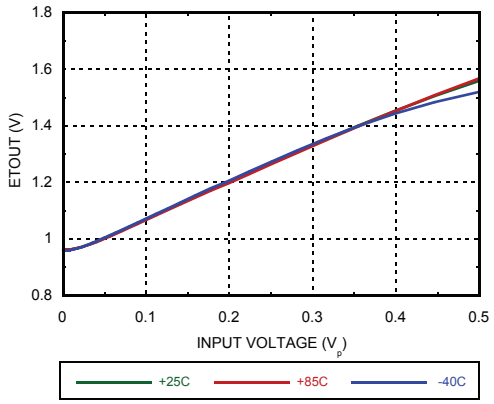
### Input Return Loss vs. Frequency



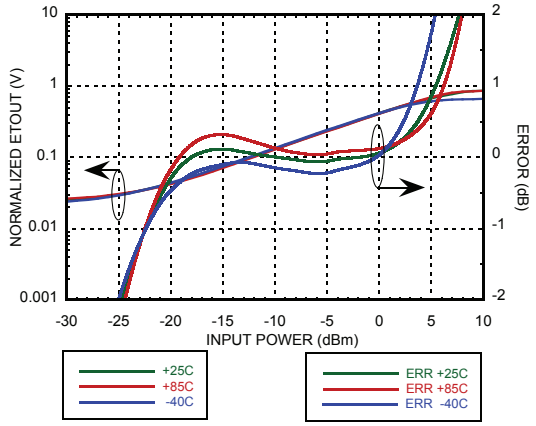

### Output Ripple & Rise/Fall Time vs. Integration Setting [Sci4, Sci3, Sci2, Sci1] in Decimal




### ETOUT vs. Vin with CW @ 900 MHz




### ETOUT & ETOUT Error vs. Pin with CW @ 900 MHz

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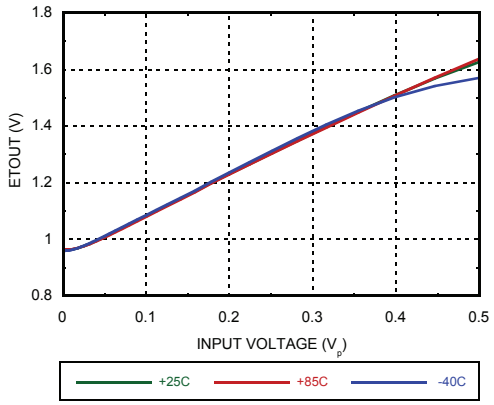
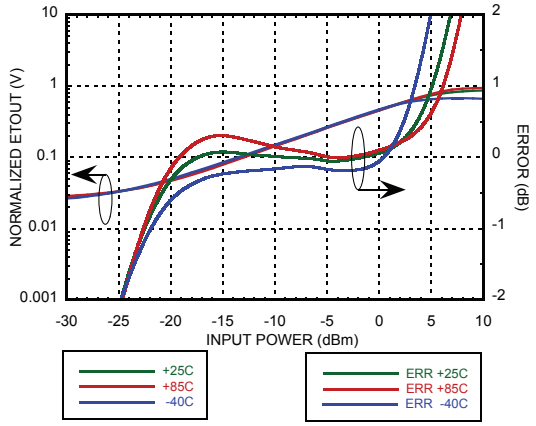
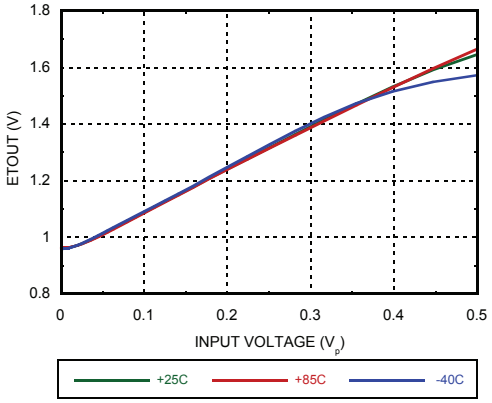


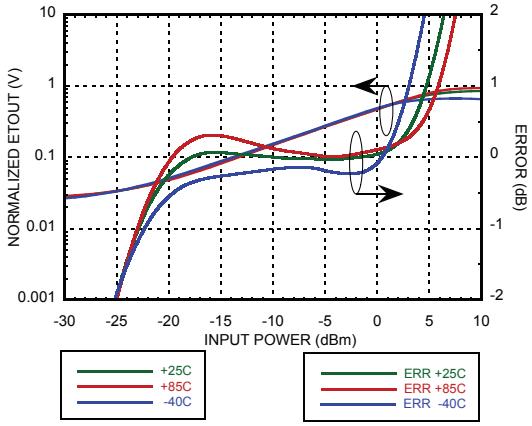

### ETOUT & ETOUT Error vs. Pin with CW @ 1900 MHz



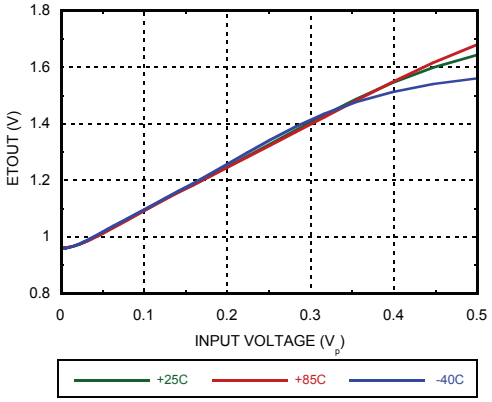
### ETOUT vs. Pin with CW @ 2200 MHz



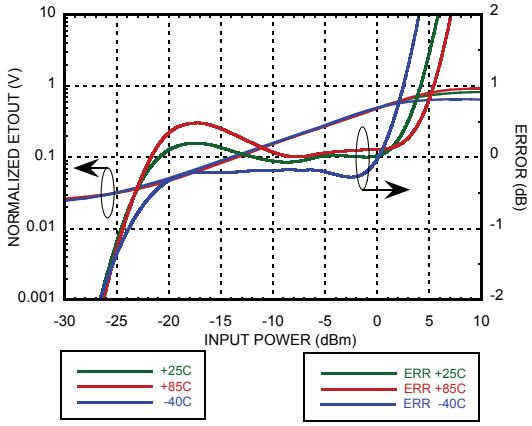

### ETOUT & ETOUT Error vs. Pin with CW @ 2200 MHz



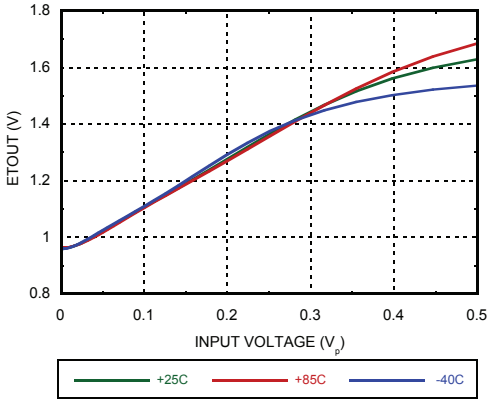

### ETOUT vs. Pin with CW @ 2700 MHz



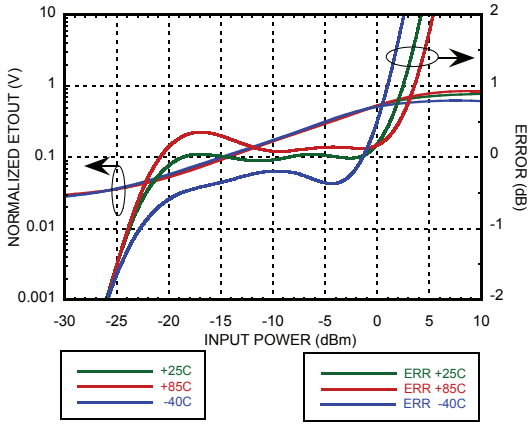

### ETOUT & ETOUT Error vs. Pin with CW @ 2700 MHz



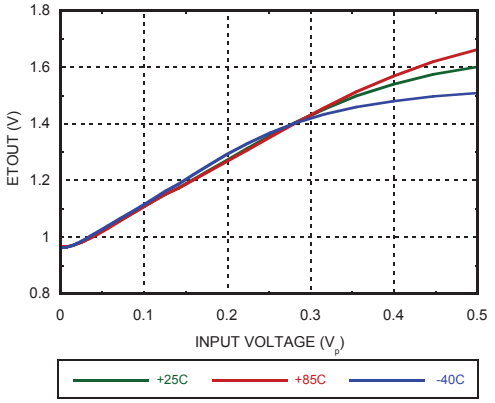

### ETOUT vs. Pin with CW @ 3500 MHz



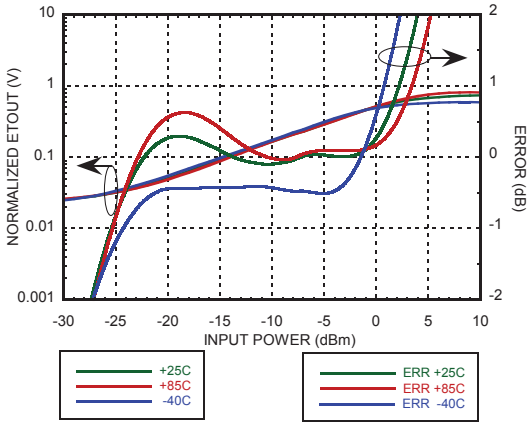

### ETOUT & ETOUT Error vs. Pin with CW @ 3500 MHz



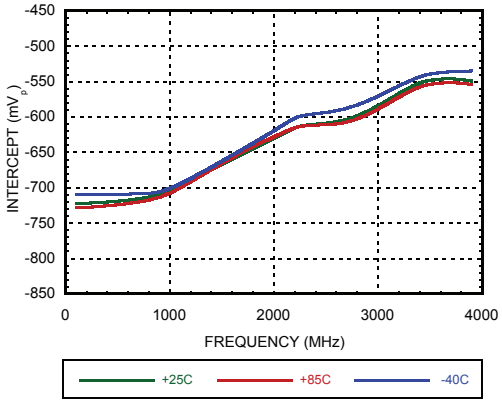
### ETOUT vs. Pin with CW @ 3900 MHz



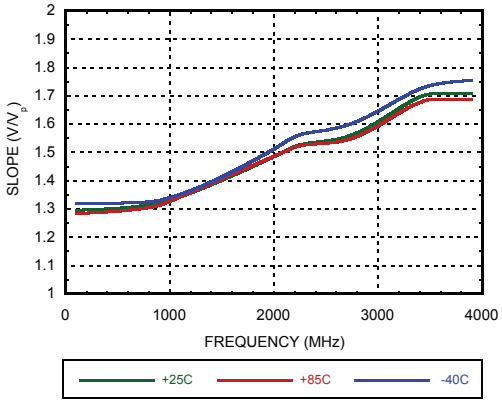

### ETOUT & ETOUT Error vs. Pin with CW @ 3900 MHz




### ETOUT Intercept vs. Frequency with CW




### ETOUT Slope vs. Frequency with CW



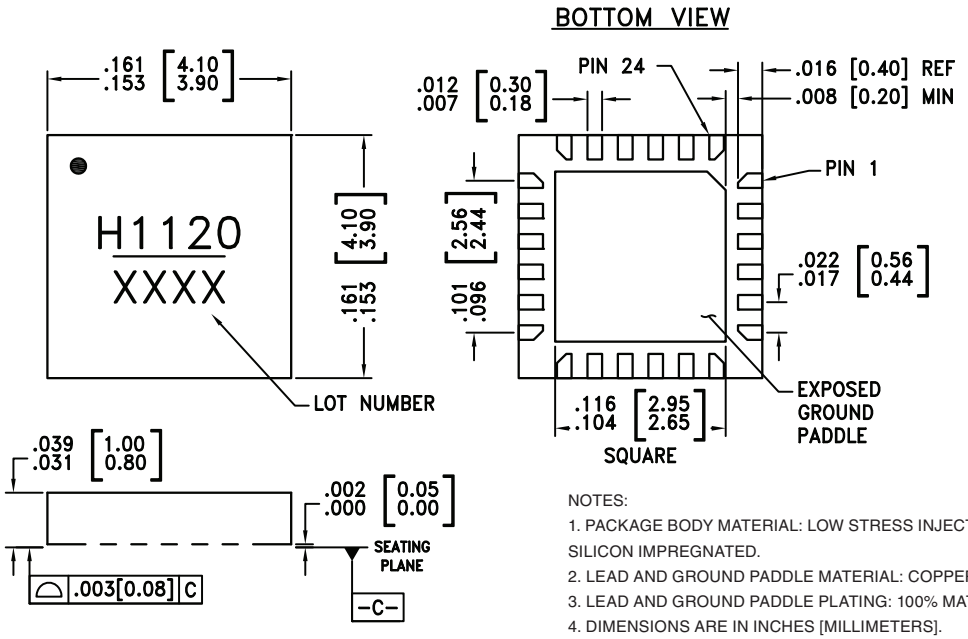
# RMS POWER DETECTOR & ENVELOPE TRACKER, DC - 3.9 GHz

## Absolute Maximum Ratings

| | |
|---|---|
| Power Supply Voltage ($V_{CC}$) | 3.8V |
| RF Input Power | 13 dBm |
| Input Voltage | VCC + 0.6V |
| Junction Temperature | 125 °C |
| Thermal Resistance ($R_{th}$) (junction to ground paddle) | 23.82 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1B |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing




NOTES:

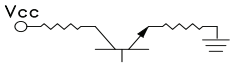
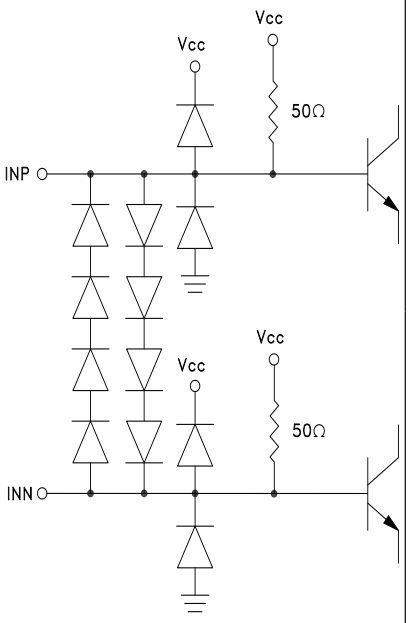
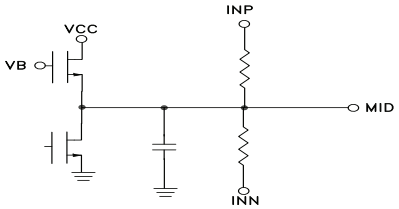
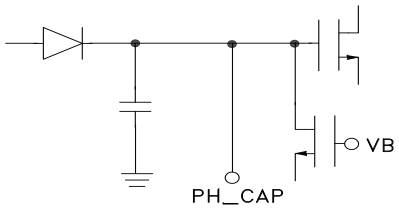
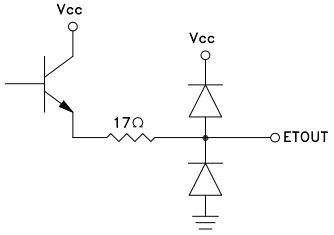
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

## Package Information

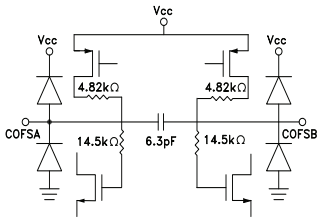
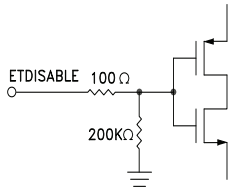
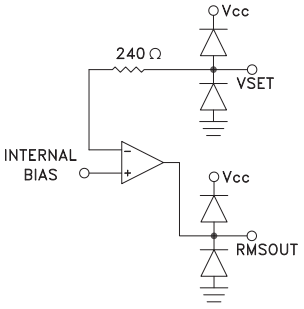
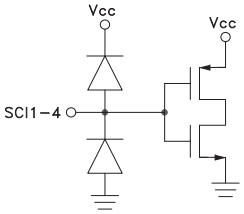
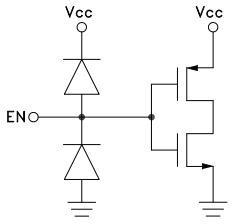
| Part Number | Package Body Material | Lead Finish | MSL Rating [2] | Package Marking [1] |
|---|---|---|---|---|
| HMC1120LP4E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 | H1120<br>XXXX |

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

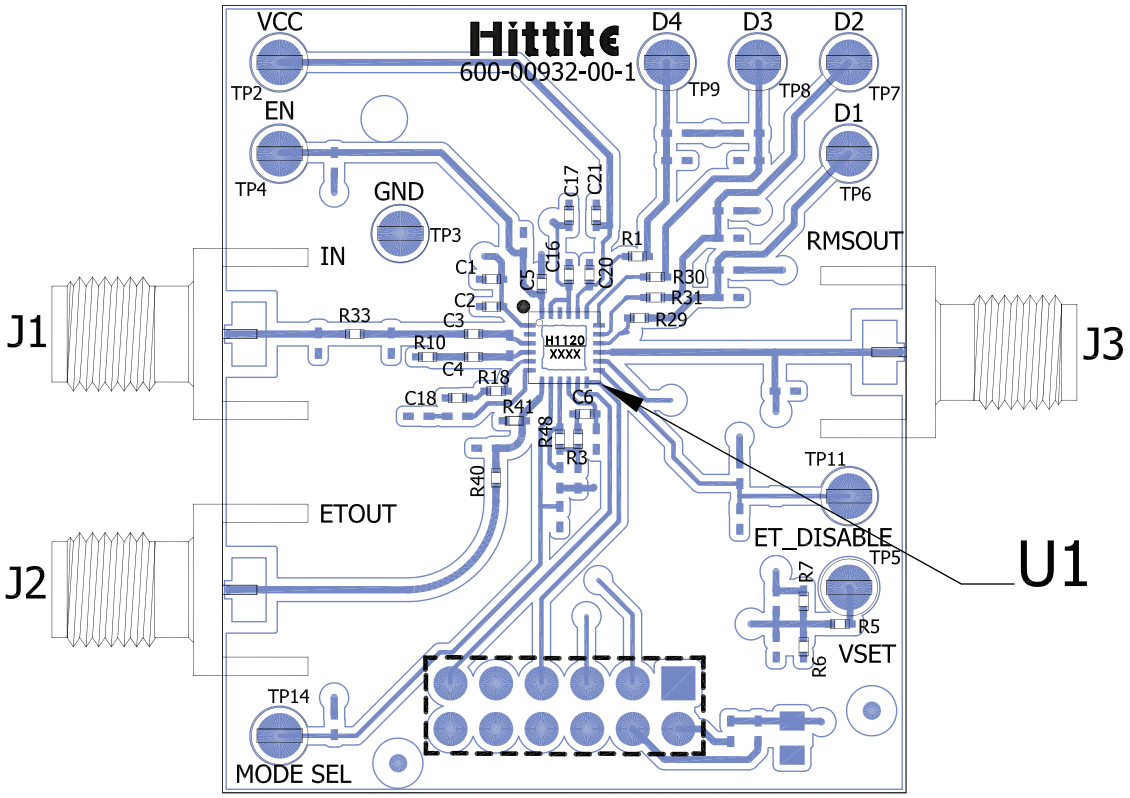
## Pin Descriptions

| Pin Number | Function | Description | Pin Schematic |
|---|---|---|---|
| 1, 20-21, 23 | VCC | Bias Supply. Connect supply voltage to these pins with appropriate filtering. |  |
| 2, 22 | GND | Package bottom has an exposed metal paddle that must be connected to RF/DC ground. | |
| 3 | INP | RF input pins |  |
| 4 | INN | | |
| 5 | MID | DC Bias pin of input circuitry. Connect a larger capacitor to operate in lower frequencies. |  |
| 6 | PH_CAP | Peak/Hold capacitor pin. Connect a larger capacitor from PH_CAP to GND for longer droop rate. |  |
| 7 | ETOUT | Linear output that provides an indication of envelope of the input signal. Can be operated in two operation modes (controlled by MODE_SEL pin). Instantaneous Envelope track and PEAK_HOLD. |  |

## Pin Descriptions

| Pin Number | Function | Description | Pin Schematic |
|---|---|---|---|
| 8 | MODE_SEL | Operation mode selection pin for ETOUT. GND sets ET MODE, VCC sets PEAK/HOLD MODE. Toggle this pin to reset the PEAK/HOLD capacitor. | |
| 9 | COFSA | Input high pass filter capacitor. Connect a capacitor between COFSA and COFSB to determine 3 dB point of input signal high-pass filter. |   |
| 10 | COFSB | | |
| 11-12 | RSV | Reserved for internal use. Should be left floating. | |
| 13 | ETDISABLE | Envelope Tracking disable pin. Apply voltage V > 0.8xVcc to disable ETOUT. |   |
| 14 | VSET | Set input point for controller mode. |   |
| 15 | RMSOUT | Logarithmic output that provides an indication of mean square input power. | |
| 16 | SCI1 | Digital input pins that control the internal integration time constant for mean square calculation. SCI4 is the most significant bit. Set V < 0.2xVcc to disable. Shortest integration time is for SCI=0000. Each step changes the integration time by 1 octave. |   |
| 17 | SCI2 | | |
| 18 | SCI3 | | |
| 19 | SCI4 | | |
| 24 | EN | Enable pin. Connect to VCC for normal operation. Apply voltage V < 0.2xVcc to disable whole chip. |   |

## Evaluation PCB




## Evaluation Order Information

| Item | Contents | Part Number |
|---|---|---|
| Evaluation PCB Only | HMC1120LP4E Evaluation PCB | EV1HMC1120LP4 [1] |

[1] Reference this number when ordering Evaluation PCB Only

## List of Materials for Evaluation PCB

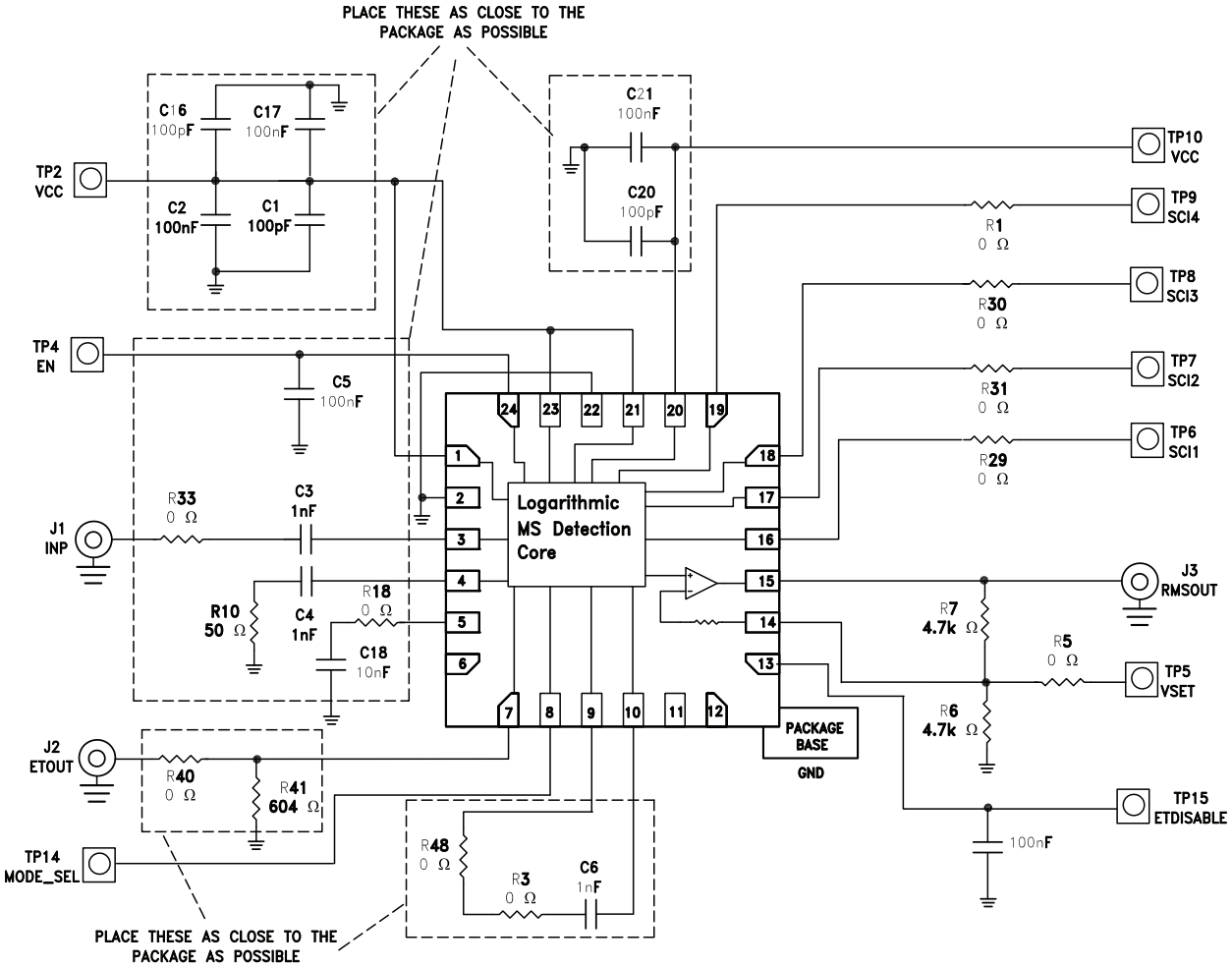
| Item | Description |
|---|---|
| J1-J3 | SMA Connector |
| TP2-TP9, TP11, TP14 | DC Pin |
| C1, C16, C20 | 100 pF Capacitor, 0402 Pkg. |
| C2, C5, C17, C21 | 100 nF Capacitor, 0402 Pkg. |
| C3-C4, C6 | 1 nF Capacitor, 0402 Pkg. |
| C18 | 10 nF Capacitor, 0402 Pkg. |
| R1, R3, R5, R18,R23-R24, R29-R31, R33, R40, R48 | 0 Ohm Resistor, 0402 Pkg. |
| R6-R7 | 4.7k Ohm Resistor, 0402 Pkg. |
| R10 | 49.9 Ohm Resistor, 0402 Pkg. |
| R41 | 604 Ohm Resistor, 0402 Pkg. |
| U1 | HMC1120LP4E<br>RMS Power Detector & Envelope Detector |
| PCB [2] | 600-00932-00 Evaluation PCB |

[1] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

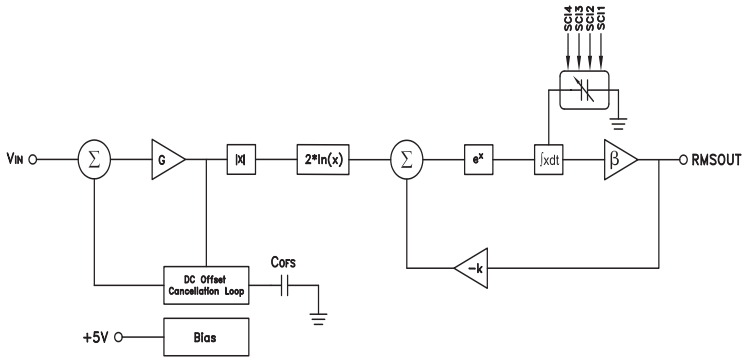
Board is configured with wideband single-ended input interface suitable for input signal frequencies above 100 MHz. Refer to wideband single-ended input interface section in application information for operating with signals below 100 MHz.

## Application Circuit



## 1.0 Application Information

### 1.1 Principle of Operation




The HMC1120LP4E combines an RMS detector core with an Envelope Detector in a single package which is capable of extracting envelope information of the modulated RF signal with modulation bandwidths in excess of 150 MHz. The extracted envelope information is independent of the average power and the crest factor of the RF signal. The RMS detector core provides a linear-in-dB output of the average RF power, whereas the envelope detector core provides a linear representation of the instantaneous envelope waveform. The instantaneous envelope output ETOUT may be used in ultra-fast excessive RF power protection systems, PA linearization techniques and in efficiency enhancing Envelope-Tracking PA implementations.

The HMC1120LP4E's RMS detector core is designed to measure the actual RMS power of the input signal, independent of the modulated signal waveform complexity or modulation scheme. The RMS detector core architecture of HMC1120LP4E is composed of a full-wave rectifier, log/antilog circuit, and an integrator as shown above. The RMSOUT signal is directly proportional to the logarithm of the time-average of $V_{IN}^2$. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signal levels can be measured accurately.

The HMC1120LP4E achieves exceptional RF power measurement accuracy independent of the modulation of the carrier with the system architecture shown in the block diagram figure. The relation between the HMC1120LP4E's RMSOUT output and the RF input power is given below:

$$RMSOUT = \frac{1}{k}\ln\left(\beta k G^2 \int {V_{IN}}^2 dt\right)$$

$P_{IN}$ = RMSOUT / [log-slope] + [log-intercept], dBm

## 1.2 Configuration For The Typical Application

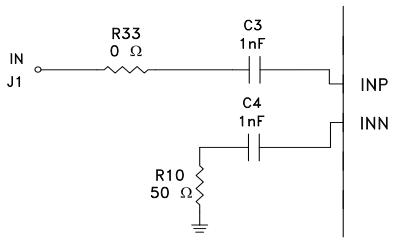
The HMC1120LP4E is a logarithmic RMS detector that can be directly driven with a single-ended 50-Ohm RF source. The integrated broadband single-ended input interface of HMC1120LP4E eliminates the requirement for an external balun transformer or matching network. The HMC1120LP4E can be operated from DC to 3.9 GHz by using only standard DC blocking capacitors. This simple input interface provides cost and PCB area reductions and increases measurement repeatability.

The RMS output signal is typically connected to VSET through a resistive network providing a Pin -> RMSOUT transfer characteristic slope of 35 mV/dBm ( at 900 MHz). However the RMS output can be re-scaled to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output. Refer to the section under the “Log-Slope and Intercept” section for details.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements; refer to the “System Calibration” section for more details.

## 1.3 Broadband Single-Ended Input Interface

The HMC1120LP4E operates with a single-ended input inter-face and requires only two external DC blocking capacitors and an external 50Ohm resistor. The HMC1120LP4E input interface shown below provides a compact, broadband solution.




Note that the provided single-ended input interface covers the whole operating spectrum of the HMC1120LP4Eand does not require matching/tuning for different frequencies. The performance of the HMC1120LP4E at different frequencies is shown below:

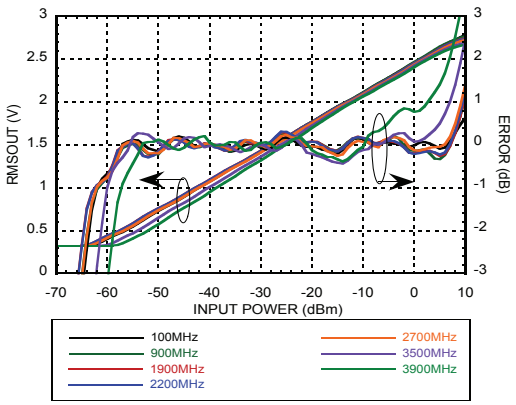



*Figure 1.RMSOUT & Error vs. Pin*

## 1.4 Envelope Detector Output

The HMC1120LP4E's ETOUT output provides a linearly scaled replica of the instantaneous envelope of the modulated RF signal for modulation bandwidths up to 150 MHz. For optimum performance, the ETOUT pin of the HMC1120LP4E should be terminated with a 604 Ω load resistor to GND. Note that any capacitive loading on the ETOUT pin would reduce the modulation bandwidth of the envelope detection. The envelope output has a conversion gain of 1.35V/V with an output voltage ranging from 1.2V to 2.2V.

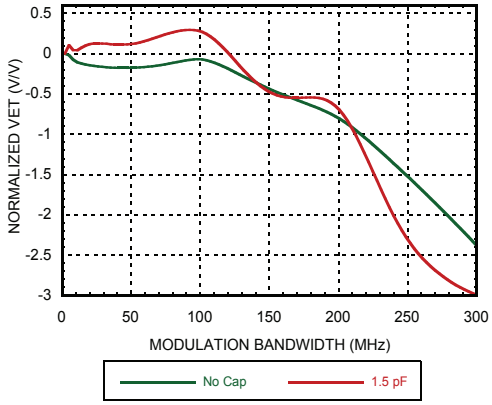



*Figure 2.ETOUT Bandwidth*

The waveform below shows the HMC1120LP4E's envelope detector response to an RF input signal with a 120 MHz modulation bandwidth.

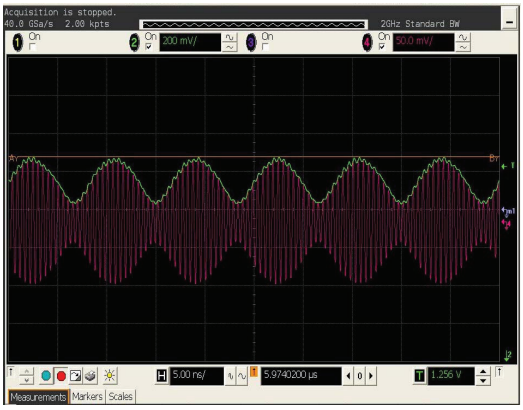


*Figure 3. ETOUT Response to an RF Input Signal with a 120 MHz Modulation Bandwidth*

## 1.5 RMS Output Interface and Transient Response

The HMC1120LP4E features digital input pins (SCI1-SCI4) that control the internal integration time constant. Output transient response is determined by the digital integration controls, and output load conditions.

The shortest integration time is for SCI=0000 and the longest integration time is for SCI=1111.

Using larger values of SCI will narrow the operating bandwidth of the integrator, resulting in a longer averaging time interval and a more filtered output signal. It will also slow the power detector's transient response. A larger SCI value favors output accuracy over speed. For the fastest possible transient settling times set SCI to 0000. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. For most applications an SCI setting may be selected to maintain a balance between speed and accuracy. Furthermore, error performance over modulation bandwidth is dependent on the SCI setting. For example modulations with relatively low frequency components and high crest factors may require higher SCI (integration) settings.

**Table 3. Transient Response vs. SCI Setting [1]**

| | RMSOUT Rise-Time 10% -> 90% (µs) [3] | | RMSOUT Rise Settling Time (µs) [2] | | RMSOUT Fall-time 90% -> 10% (µs) [4] | |
|---|---|---|---|---|---|---|
| SCI4,3,2,1 | Pin = 0 dBm | Pin = -20 dBm | Pin = 0 dBm | Pin = -20 dBm | Pin = 0 dBm | Pin = -20 dBm |
| 0000 | 0.162 | 0.112 | 1.09984 | 1.410667 | 1.53 | 0.374 |
| 0010 | 0.162 | 0.119 | 1.147096 | 1.479386 | 2.17 | 0.999 |
| 0100 | 0.164 | 0.323 | 2.624 | 5.491 | 3.92 | 0.953 |
| 0110 | 0.848 | 1.38 | 32.224 | 25.71818 | 11.33 | 3.32 |
| 1000 | 2.65 | 1.207 | 67.12306 | 22.933 | 42.57 | 12.71 |
| 1010 | 16.4 | 17.82 | 628 | 256.0615 | 161.01 | 48.60 |
| 1100 | 9.74 | 65.22 | 2951.22 | 1773.44 | 616.15 | 187.15 |

[1] Input signal is 1900 MHz CW -tone switched on and off
[2] Measured from 10% to 90%
[3] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.
[4] Measured from 90% to 10%

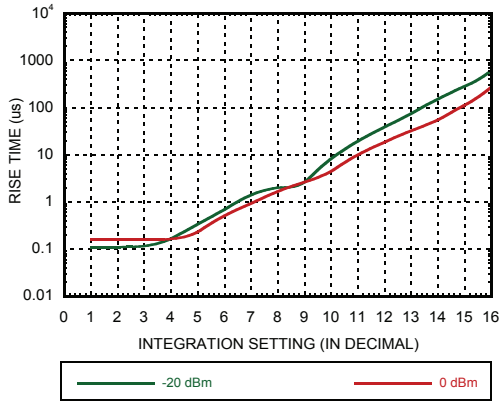



*Figure 4.Rise Time[2] vs. SCI Setting over Input Power*

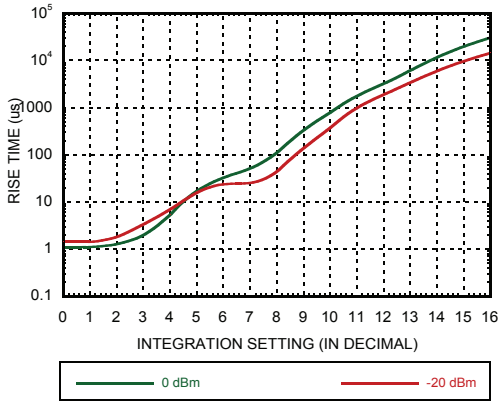



*Figure 5.Rise Settling Time [3] vs. SCI Setting over Input Power*

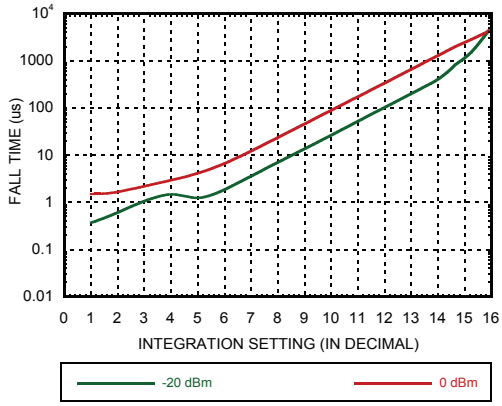



*Figure 6.Fall Time [4] vs. SCI Setting over Input Power*

For increased load drive capability, consider a buffer amplifier on the RMS output. Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC1120LP4E with a lower SCI value.

Following figures show how the peak-to-peak ripple decreases with higher SCI settings along with the RF pulse response over different modulations.

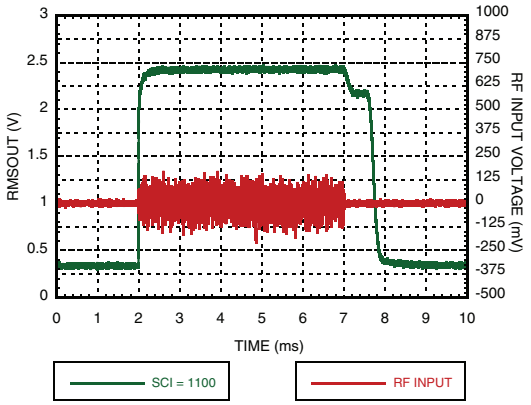



*Figure 7.Residual Ripple for 1900 MHz WCDMA4C @ SCI=1100*

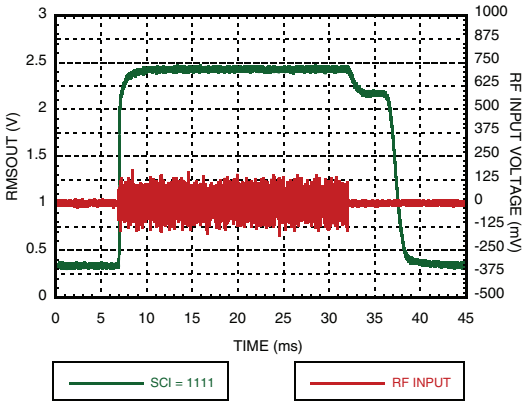



*Figure 8.Residual Ripple for 1900 MHz WCDMA4C @ SCI=1111*

[1] Input signal is 1900 MHz CW -tone switched on and off
[2] Measured from 10% to 90%
[3] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.
[4] Measured from 90% to 10%

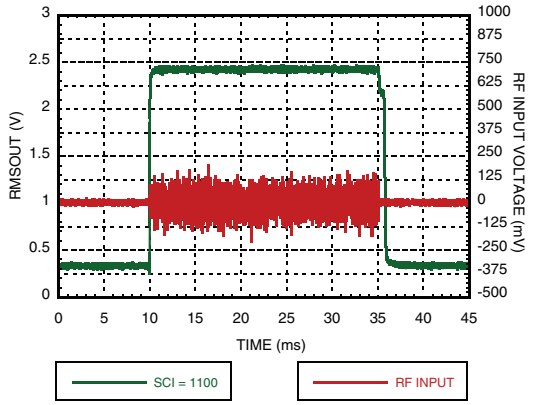



*Figure 9.Residual Ripple for 1900 MHz LTE @ SCI=1100*

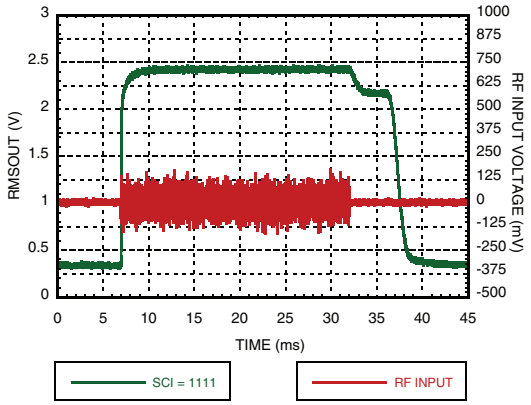



*Figure 10.Residual Ripple for 1900 MHz LTE @ SCI=1111*

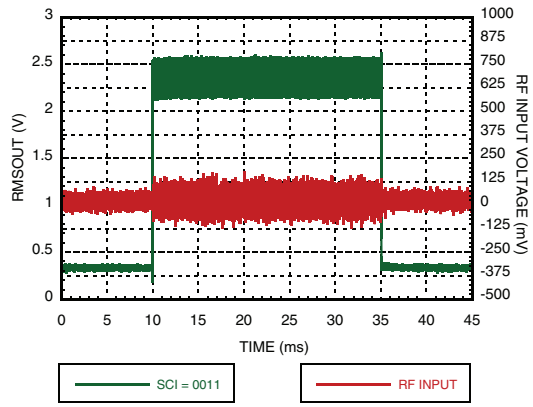



*Figure 11.Residual Ripple for 1900 MHz GSM6C @ SCI=0011*

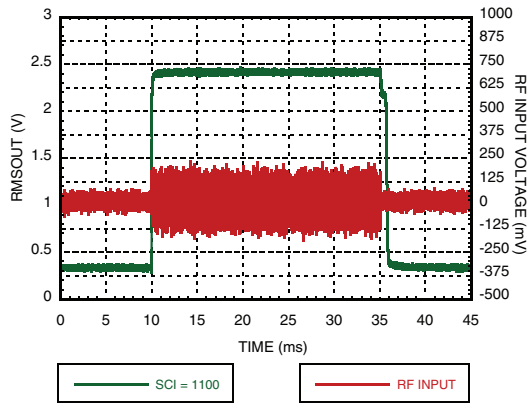



*Figure 12.Residual Ripple for 1900 MHz GSM6C @ SCI=1100*

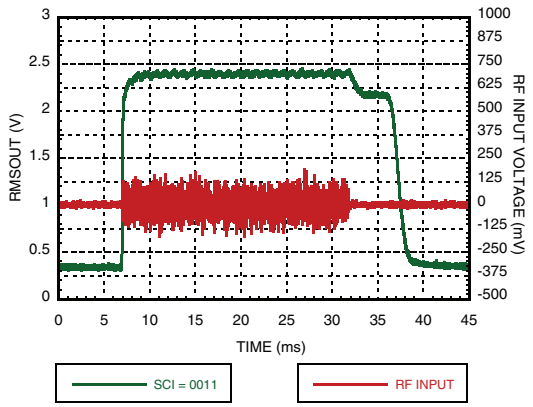


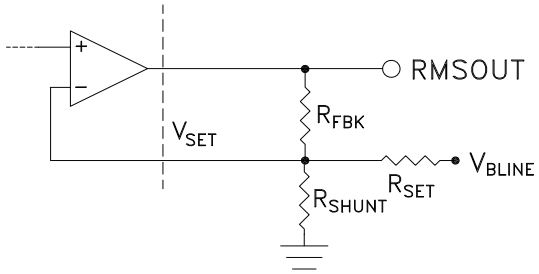

*Figure 13.Residual Ripple for 1900 MHz LTE @ SCI=1111*

## 1.6 LOG-Slope and Intercept

The HMC1120LP4E provides for an adjustment of output scale with the use of an integrated operational amplifier. Log-slope and intercept can be adjusted to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output.

A log-slope of 33.4 mV/dB (@1900 MHz) is set by connecting RMS Output to VSET through a resistor network for ß=1 (see application schematic).

The log-slope is adjusted by applying the appropriate resistors on the RMS and VSET pins. Log-intercept is adjusted by applying a DC voltage to the VSET pin.




Optimized slope = ß * log-slope

Optimized intercept = log_intercept – ($R_{FBK}$ /$R_{SET}$ ) * $V_{BLINE}$

$$ß = \frac{1}{2} \cdot \frac{R_{FBK}}{R_{FBK} // R_{SHUNT} // R_{SET}}$$

When $R_{FBK}$=0 to set RMSOUT=$V_{SET}$, then ß=1/2

If $R_{SET}$ is not populated, then ß = ½ * ($R_{FBK}$/ ($R_{FBK}$ // $R_{SHUNT}$)) and intercept is at nominal value.

Example: The logarithmic slope can be simply increased by choosing appropriate $R_{FBK}$ and $R_{SHUNT}$ values while not populating the RSET resistor on the evaluation board to keep the intercept at nominal value.

Setting $R_{FBK}$ =4.7KΩ and $R_{SHUNT}$ = 12KΩ results in an optimized slope of:

Optimized Slope = ß * log_slope = 1.39* 33.4mV / dB

Optimized Slope = 46.6 mV / dB

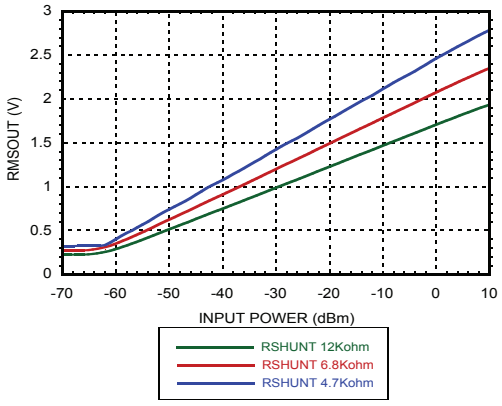



Figure 14.Slope Adjustment

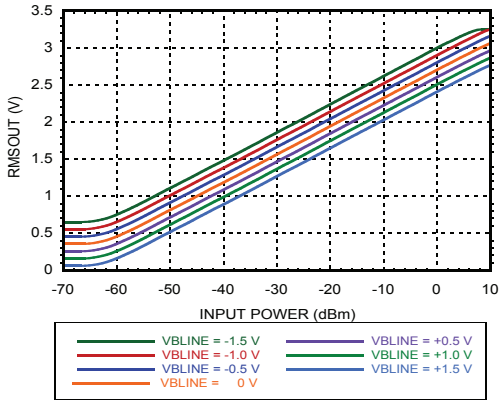



Figure 15.Intercept Adjustment

## 1.7 DC Offset Compensation Loop

Internal DC offsets, which are input signal dependent, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance (COFS) connected between COFSA & COFSB pins.

COFS capacitor sets the loop bandwidth of the DC offset compensations. Higher COFS values are required for measuring lower RF frequencies. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

**Table 4. Loop Bandwidth for DC Cancellation**

| CAP Value (nF) | Bandwidth | Unit |
|---|---|---|
| 0.1 | 1000 | KHz |
| 1 | 220 | KHz |
| 10 | 35 | KHz |
| 100 | 20 | KHz |

## 1.8 Standby Mode

The EN pin can be used to force the power detector into a low-power standby mode. As EN is activated, power is restored to all of the circuits. There is no memory of previous conditions. Coming out of stand by mode, internal integration and COFS capacitors will require recharging, so if large SCI values have been chosen, the wake-up time will be lengthened.

## 1.9 Envelope Disable Mode

The ETDISABLE pin can be used to force the Envelope Tracking module into a low power standby mode. As ETDISABLE is deactivated power is restored to the Envelope Tracking module. There is no memory of previous conditions. Coming out of stand by mode, PEAK/HOLD capacitors will require recharging. The state of the ETDISABLE pin doesn't affect RMS performance.

## 1.10 Modulation Performance – Crest factor performance

The HMC1120LP4E is able to detect the average power of RF signals with complex modulation schemes with exceptional accuracy. The proprietary RMS detection core is optimized to accurately detect the RMS power of the modulated RF signals with very high crest factors. This crest factor immune detection architecture of HMC1120LP4E results in detection accuracy of better than 0.2 dB over the entire operating frequency and temperature range, compared with the CW response under actual WCDMA4TM test signals shown below:

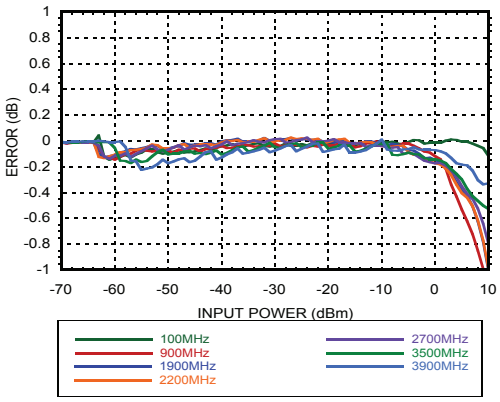



*Figure 16.Reading Error for LTE wrt CW Response @ +25 °C*

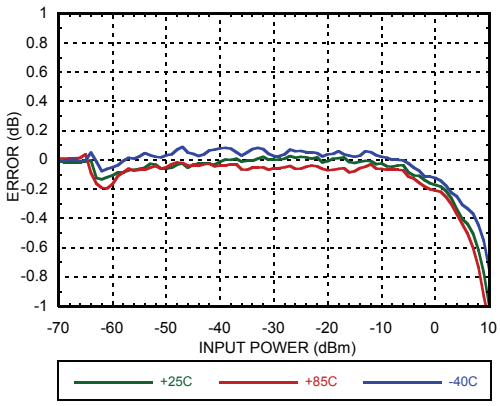



*Figure 17.Reading Error for LTE wrt CW Response @ 2200 MHz*

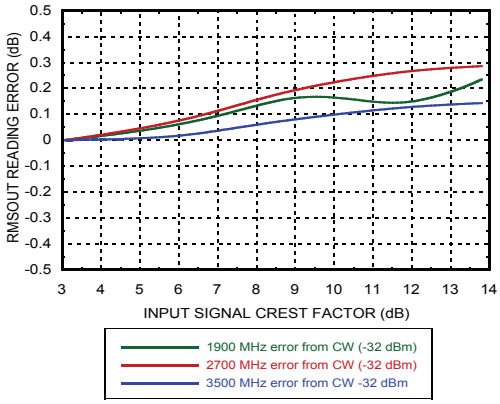



*Figure 18.RMSOUT Error vs. Crest Factor over Frequency*

## 1.11 System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, two test points near the top end and bottom-end of the desired detection dynamic range should be chosen. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. The log-slope and log-intercept parameters should be derived and then stored in nonvolatile memory. These parameters relate the RMSOUT output voltage reading of HMC1120LP4E to the actual RMS power level as shown below:

$P_{IN}$ = RMSOUT / [log-slope] + [log-intercept], dBm

The derivation procedure of the log-slope and log-intercept parameters is elaborated below:

For example if the following two calibration points were measured at 2.2 GHz:

With RMSOUT = 2.0816V at Pin = -10 dBm,

and RMSOUT = 0.5673V at Pin = -50 dBm

slope calibration constant = SCC

SCC = (-50+10)/(0.5673-2.0816) = 26.41 dB/V

intercept calibration constant = ICC

ICC = Pin – SCC *RMSOUT = -10 – 26.41 * 2.0816 = -64.98 dBm

Now performing a power measurement at -30 dBm:

RMSOUT measures 1.3283V

[Measured Pin] = [Measured RMSOUT]*SCC + ICC

[Measured Pin] = 1.3283*26.41 – 64.98 = -29.89 dBm

An error of only 0.11 dB

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector is intended to operate over a wide range of frequencies, then a central frequency should be chosen for calibration.

## 1.12 Peak Hold Time

Peak hold time is defined as 1 percent voltage drop from the last peak. The capacitor value at the PH_CAP pin can be used to adjust the droop rate of the Peak Hold output. Increasing the capacitor value increases the droop rate, at the cost of modulation bandwidth. Below table represents droop rate performance with different capacitor values.

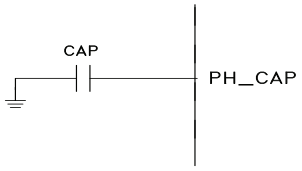



**Table 5. Peak Hold Time vs. CAP values**

| CAP Value | Droop Rate | Unit |
|---|---|---|
| No Cap | 154 | uS |
| 3.3 pF | 253 | uS |
| 10 pF | 424 | uS |
| Input power is -2 dBm @ 1900 MHz | | |

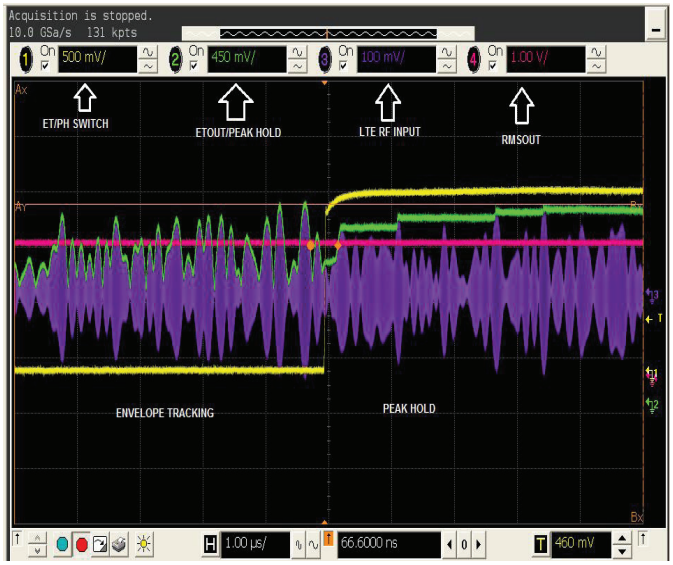



*Figure 19.RMSOUT, Envelope Tracking, Peak Hold Performance with LTE signal @ 1900 MHz*

## 1.13 Layout Considerations

• Mount RF input coupling capacitors close to the INP and INP pins.

• Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.

• Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

## 1.14 Definitions

• Log-slope: slope of PIN –> RMSOUT transfer characteristic. In units of mV/dB

• Log-intercept: x-axis intercept of PIN –> RMSOUT transfer characteristic. In units of dBm.

• RMS Output Error: The difference between the measured PIN and actual PIN using a line of best fit.

[measured_PIN] = [measured_ RMSOUT] / [best-fit-slope] + [best-fit-intercept], dBm

• Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with “RMS Output Error” falling within a specific error tolerance.

• Crest Factor: Peak power to average power ratio for time-varying signals.