HMC1033LP6GE

v01.0712

HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 550 MHz

Typical Applications

- 10G/40G/100G Optical Modules, Transponders, Line Cards
- OTN and SONET/SDH Applications
- Data Converters, Sample Clock Generation
- Cellular/4G Infrastructure
- High Frequency Processor/FPGA Clocks
- Any Frequency Clock Rate Generation
- Low Jitter SAW Oscillator Replacement
- DDS Replacement
- Frequency Translation
- Frequency Margining

Features

3.3 V Only, Single Supply Rail Operation

Output Frequency Range: 25 MHz - 550 MHz

Integer or Fractional-N mode Frequency Translation

Configurable LVDS-compatible or LVPECL type Differential Outputs

“Power Priority” and“Performance Priority” modes

99 fs RMS Jitter Generation (12 kHz - 20 MHz, 550 MHz, Typ)

-163 dBc/Hz Phase Noise Floor to Improve ADC/DAC SNR (maximum output swing levels).

Adjustable PLL Loop BW via External Filter

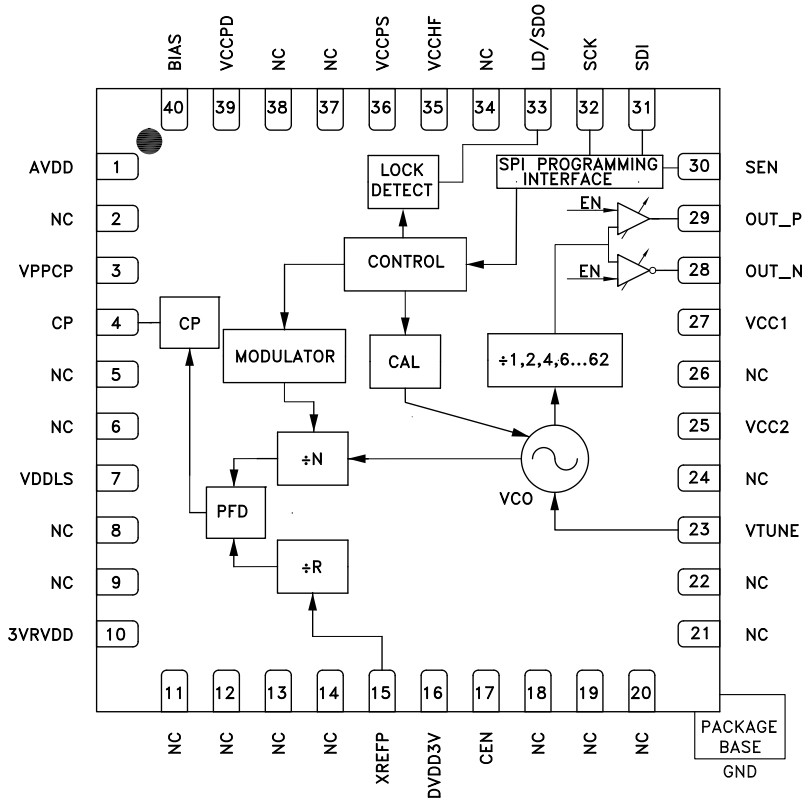
Output Disable/Mute Control

Lock Detect Signal

Exact Frequency Mode to achieve reference frequency tuning, and 0 Hz frequency error

40 Lead 6x6 mm SMT Package: 36 mm^2

Functional Diagram



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HIGH PERFORMANCE, +3.3 V CLOCK GENERATOR 25 - 550 MHz

General Description

The HMC1033LP6GE is a low-noise, wide-band 3.3 V clock generator IC with a fractional-N Phase Locked Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO). The device provides differential clock outputs between 25 MHz and 550 MHz range. The HMC1033LP6GE features a low noise Phase Detector (PD) and Delta-Sigma modulator, capable of operating at up to 100 MHz which permits wider loop-bandwidths and excellent spurious performance.

The HMC1033LP6GE features industry leading phase noise and jitter performance, across the operating range, that enable it to improve link level jitter performance, Bit-Error-Rates (BER) and eye diagram metrics. The superior noise floor (<-162 dBc/Hz) makes the HMC1033LP6GE an ideal source for a variety of applications –such as clock references for high speed data converters, physical layer devices (PHY), serializer/deserializer (SERDES) circuits, FPGAs and processors. The HMC1033LP6GE can also be used as an LO for 10G/40G/100G optical modules and transponders, as well as primary reference clock for 10G/40G/100G line cards, and for jitter attenuation and frequency translation.

The differential output of the HMC1033LP6GE can be set to either External Termination, which could be used for LVPECL operation, or Internal Termination for operation in an LVDS compatible mode or LVPECL, see Figure 18. Additionally, an ouput swing adjustment makes the device flexible and compatible with a wide variety of signal level requirements. The output can be internally terminated to reduce component count and cost or could be terminated externally using standard LVPECL termination methods such as Figure 21. An Output Mute function allows the user to shut off the outputs, such as may be required for board testing or debugging. The LVPECL/LVDS, amplitude select and Output Mute function are all programmed SPI serial programming

The HMC1033LP6GE is designed to select between a Power Priority or a Performance Priority mode. The Power Priority setting reduces the current consumption of the part, whereas the Performance Priority setting improves the Jitter and Phase Noise performance.

The 24 bit Delta-Sigma Modulator further enhances Hittite's Exact Frequency Mode, which enables users to generate output frequencies with 0 Hz frequency error in many applications.

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Electrical Specifications, VPPCP, VDDLS, 3VRVDD, VCC1, VCC2, VCCHF, VCCPS, VCCPD, = 3.3V Min & Max Specified across Temperature -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
OUT_N, OUT_P Output Characteristics					
Output Frequency		25		550	MHz
Differential Output Amplitude	Gain Setting = 0000		690		mVpp
	Gain Setting = 0001		780		mVpp
	Gain Setting = 0010		900		mVpp
	Gain Setting = 0011		980		mVpp
	Gain Setting = 0100		1100		mVpp
	Gain Setting = 0101		1260		mVpp
	Gain Setting = 0110		1400		mVpp
	Gain Setting = 0111		1590		mVpp
	Gain Setting = 1000		1810		mVpp
	Gain Setting = 1001		1980		mVpp
	Gain Setting = 1010		2250		mVpp
	Gain Setting = 1011		2560		mVpp
Output Common Mode Voltage					
LVDS Mode			1.2		mV
LVPECL Mode			2.0		V
Output Rise and Fall Time	LVDS mode, Gain = 0001		120		ps
Output Rise and Fall Time	LVPECL mode, Gain = 0110		130		ps
Duty Cycle	AC coupled, measured at the 0 V crossing, 622.080 MHz and 2.5 GHz Outputs	49	50	51	%
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional Nominal Divide Ratio Varies (-4 / +4) Dynamically Max	20		524,283	
CLKIN Input Characteristics					
Max Input Frequency[2]				350	MHz
Input Amplitude	AC Coupled [1]	0.2		3.3	Vp-p
Input Capacitance				5	pF
Input Slew Rate		157			mV/ns
14 Bit R-Divider Range				16,383	
Phase Detector (PD) [2]					
PD Frequency Fractional Mode		0.006		100	MHz
PD Frequency Integer Mode		0.006		100	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-152		dBc/Hz
Logic Inputs					
Vsw	Switching threshold for logic levels	40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Voltages					
+ 3.3V Supplies	AVDD, VPPCP, VDDLS,3VRVDD, DVDD3V, VCC1, VCC2, VCCHF, VCCPS, VCCPD	3.15	3.3	3.5	V
Power Supply Currents					
+3.3V	LVPECL, Performance Priority Mode, 350 MHz output, Excluding Load		208		mA
	LVPECL Performance Priority Mode, 350 MHz output, Includes Termination		240		mA
	LVPECL Performance Priority Mode, 155.52 MHz Output, Includes Termination		242		mA
	LVDS, Power Priority Mode, 350 MHz Output, Includes Termination		195		mA
	LVDS, Power Priority Mode, 155.52 MHz Output, Includes Termination		197		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		5		mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Minimum DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-227		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-226		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
Phase Jitter RMS, Integer Mode	155.52 MHz Output , 12 kHz to 20 MHz		107		fs
	350 MHz Output 12 kHz -20MHz		99		fs
Phase Jitter RMS, Fractional Mode	155.52 MHz Output , 12 kHz to 20 MHz		122		fs
	350 MHz Output 12 kHz -20MHz		124		fs

[1] Measurements made are AC coupled into a 100 differential load (Except Phase Noise).
[2] The maximum phase detector frequency can only be achieved if the minumum N value is respected, eg in the case of fractional feedback mode, the maximum PFD rate = fvco/20 or 100 MHz whichever is less. Operation > 70MHz may require offsett currents to be disabled and reenabled.

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Figure 1. Typical Phase Noise, Integer Mode, Power Priority[1]

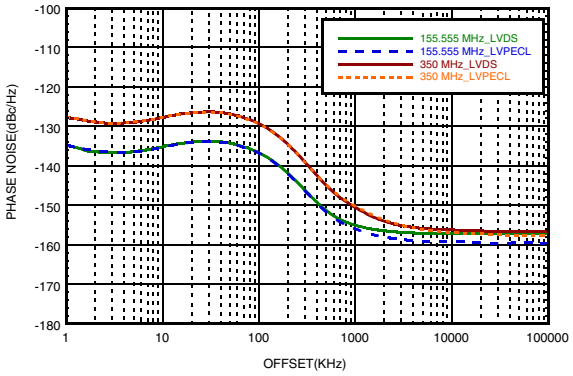


Figure 2. Typical Phase Noise, Integer Mode, Performance Priority[1]

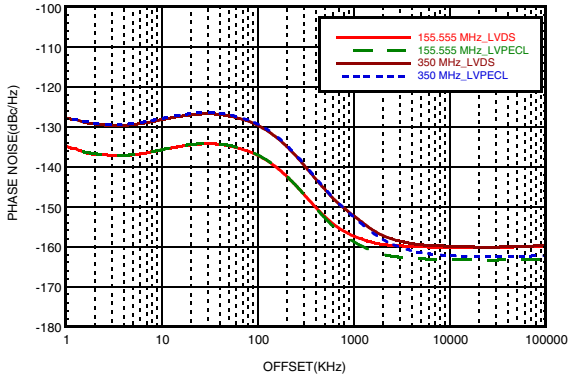


Figure 3. Typical Phase Noise, Fractional Mode, Power Priority[1]

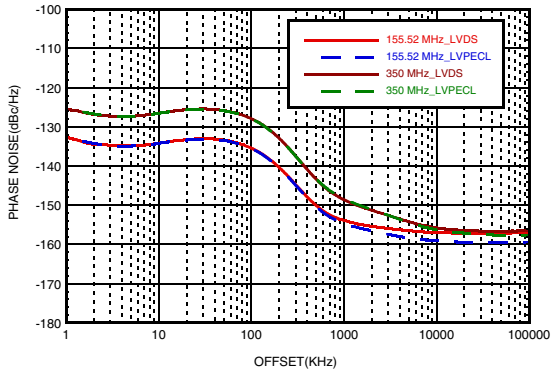


Figure 4. Typical Phase Noise, Fractional Mode, Performance Priority[1]

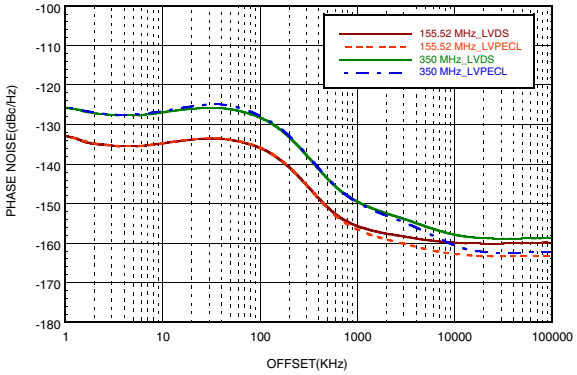


Figure 5. Integer Phase Noise vs Reference Source[2]

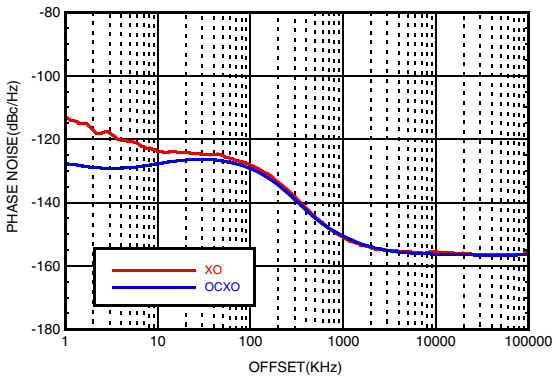
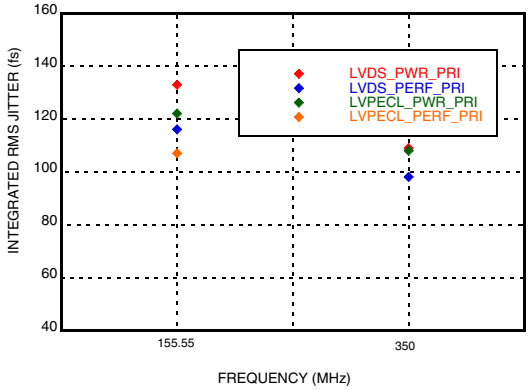


Figure 6. Jitter from Integrated Phase Noise vs Output Frequency, Integer Mode[2]



[1] The PN plot is measured with a 100MHz OCXO followed with a divide by 2, using the Loop Filter in the Loop Filter Configuration Table
[2] The PN plot is measured with 50 MHz Crystal Oscillator (red) versus a 50MHz OCXO (blue).
[3] Jitter is Integrated over a 12kHz to 20MHz Band

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Figure 7. Jitter from Integrated Phase Noise vs. Frequency, Fractional Mode[3]

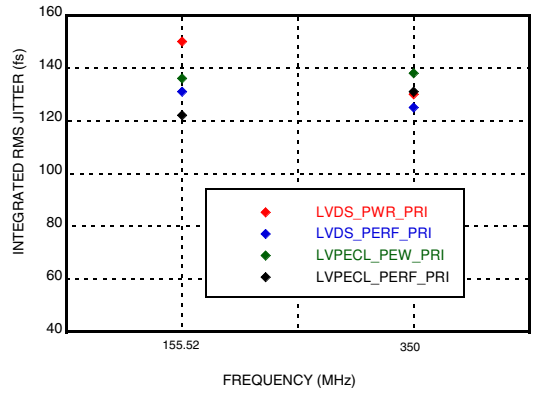


Figure 8. Lock Time vs. Phase Error[4]

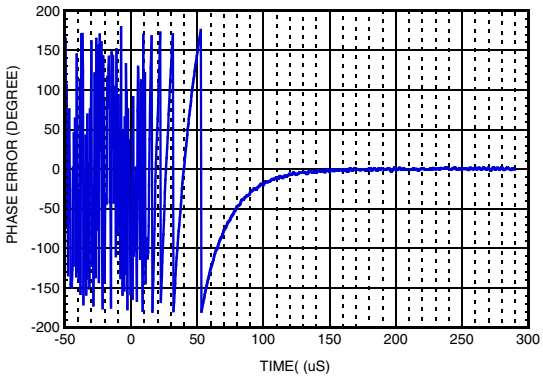


Figure 9. Lock Time vs Frequency Error[4]

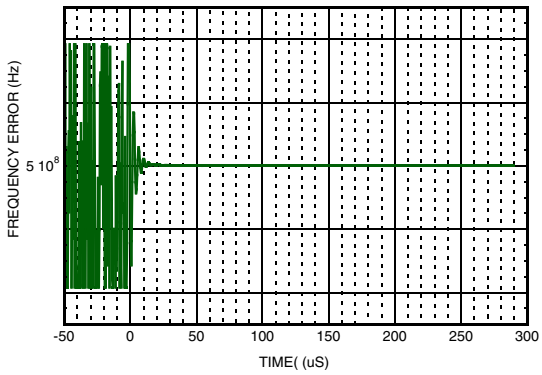


Figure 10. Output Amplitude vs Output Frequency[5]

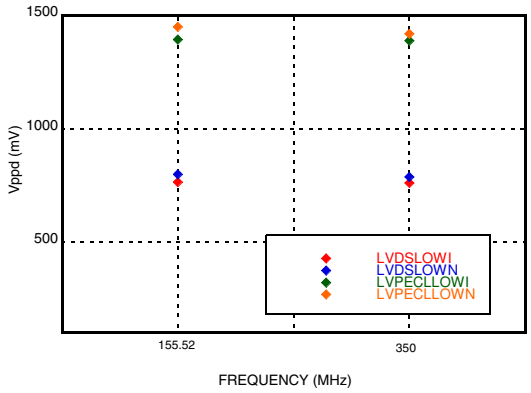


Figure 11. Output Rise Time vs. Output Frequency[6]

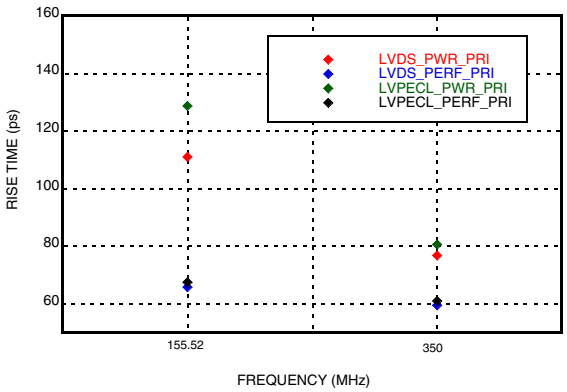
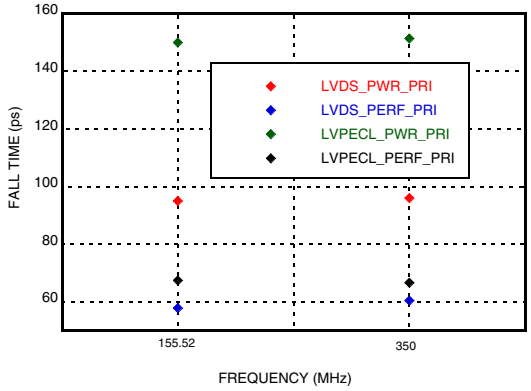


Figure 12. Output Fall Time vs. Output Frequency



[4] The HMC1033LP6GE has a preloaded register file for a 2GHz Output and time is measured from VCO disable to VCO enable, using the Loop Filter in the Loop Filter Configuration Table.
[5] The output signal amplitude is measured with HMC1035 AC coupled to a 100 ohm differntial loadinstrument
[6] Measured at 20% to 80% levels.

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Figure 13. Output Duty Cycle vs. Output Frequency[7]

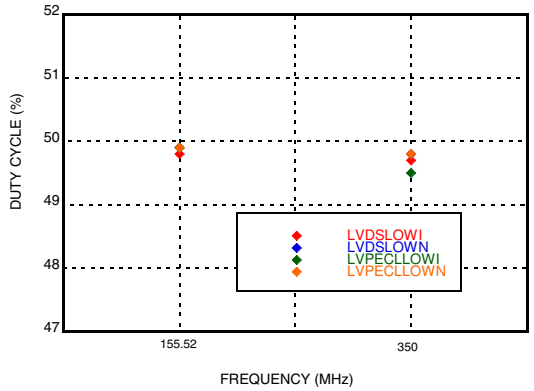


Figure 14. Supply Current vs. Output Frequency[8]

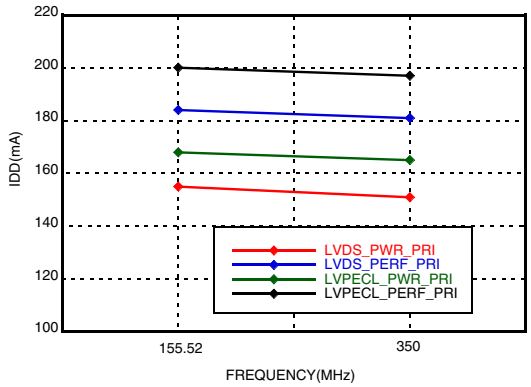


Figure 15. Output Amplitude vs. Gain Setting over Temperature

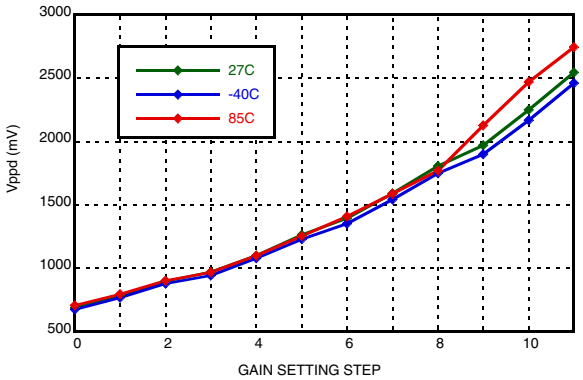
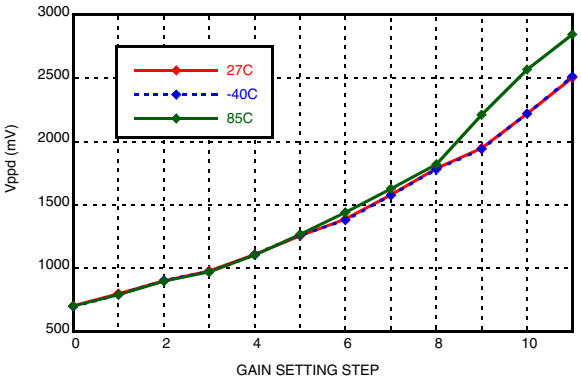
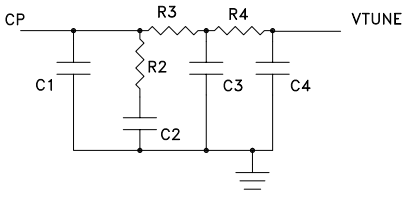


Figure 16. Out Waveform, Performance Priority and Power Priority in LVDS and LVPECL Mode



[7] Duty Cycle is measured with the Output AC coupled at the 0 crossing level.
[8] The current is measured at Nominal VCO VDD Supply under Fractional Locked Condition by varying different the output divider ratio.

Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Loop Filter Design
127	390	10	82	82	750	300	300	
75	270	27	200	390	430	390	390	

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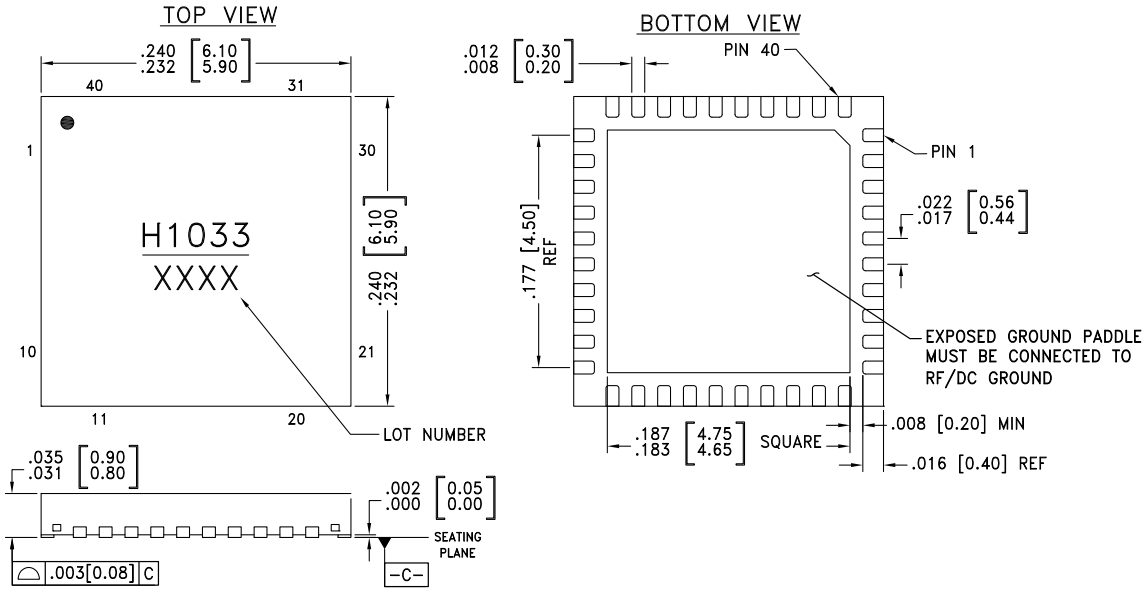
Absolute Maximum Ratings

AVDD, VPPCP, VDDLS, 3VRVDD, DVDD3V, VCC1, VCC2, VCCHF, VCCPS, VCCPD	-0.3V to +3.6V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature	125 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	10 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1033LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1035 XXXX

[1] 4-Digit lot number XXXX

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Pin Descriptions

Pin Number	Function	Description
1	AVDD	3.3 VDC Power Supply for Analog Circuitry
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	NC	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	3.3V Power Supply for Charge Pump Analog Section
4	CP	Charge Pump Output
7	VDDLS	3.3V Power Supply for the Charge Pump Digital Section
10	3VRVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	3.3V DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	3.3V VCO Analog Supply 2
27	VCC1	3.3V VCO Analog Supply 1
28	OUT_N	Negative Output Signal (Differential)
29	OUT_P	Positive Output Signal (Differential)
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD/SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	3.3 V DC Power Supply for Analog Circuitry
36	VCCPS	3.3 V DC Power Supply for Analog Prescaler
39	VCCPD	3.3 V DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

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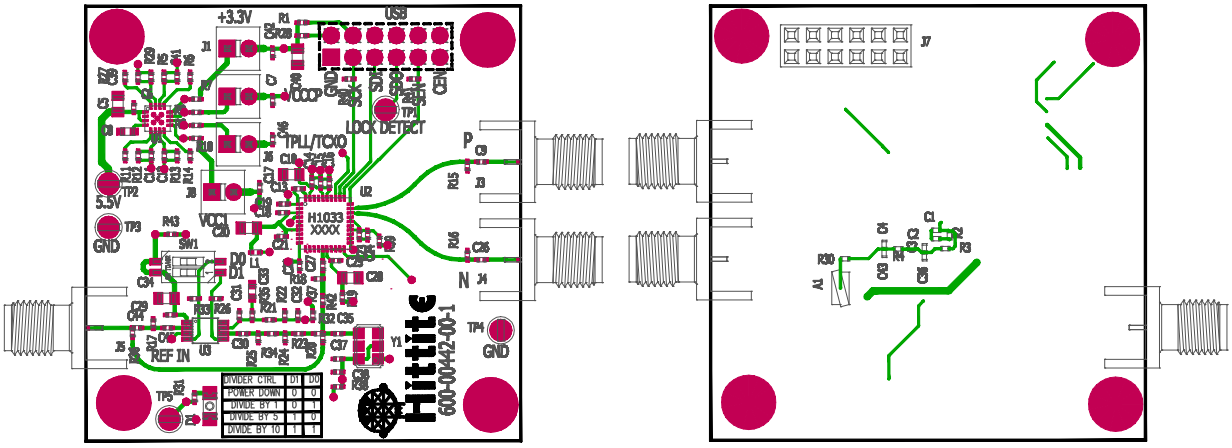
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

The HMC1033 evaluation board and associated software offers the user an easy way to quickly evaluate the performance and flexibility of the HMC1033. The evaluation board operates off a +5V supply and includes an HMC1060 LDO, which generates a low noise 3.3V source, and a precision PLL which generates a 50MHz clock, which is locked to an externally supplied 10 MHz reference.

The PLL design is an HMC1031 phase/frequency detector, passive loop filter and a low noise 50 MHz VCXO. The PLL is normally, or default upon shipping, set to lock on to a 10 MHz reference feed into “REF IN”. A 5MHz input reference can be used if D1, D0 is reconfigured to “1,1”, or 50 MHz if D1, D0 is reconfigured to “0,1”. The “REF IN” would normally have a +/-50 ppm tolerance which falls within the VCXO pull range. Although not recommended, the HMC1033 EB can be operated without supplying an external reference, and the PLL will pull the VCXO to about 49.992 MHz, or 180 ppm low. Alternatively, an external 50 MHz reference can be feed into the HMC1033 evaluation board which requires removing C44,C35, R32 and J6, the TPLL/TCXO, and placing a 0 Ohm resistor in the R20 and R36 locations.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC1033LP6GE from the “Search by Part Number” pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1033LP6G Evaluation PCB	EVA01-HMC1033LP6G
Evaluation Kit	HMC1033LP6G Evaluation PCB USB Interface Board 6’ USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1033LP6G

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HMC1033LP6GE Input Stage

A representative schematic for the HMC1033LP6GE output stage is given in Figure 17 below. The buffer is internally DC biased with 100 ohm internal termination. For 50 ohm match, an external 100 ohm resistor to ground should be added, followed by an AC coupling capacitor (impedance < 1 ohm) then to the XREFP pin of the part.

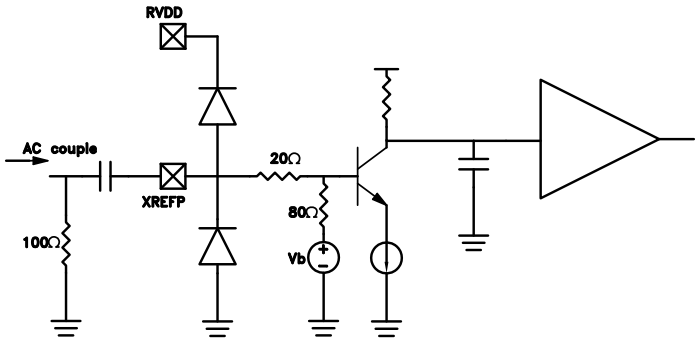

Figure 17. Input Stage

HMC1033LP6GE Output Stage

A representative schematic for the HMC1033LP6GE output stage is given in Figure 18 below. The output is derived from an emitter which can be internally biased to a current source (the default setting), or the Internal Termination switch can be opened, VCO_Reg03[4], and external termination used. The internal bias would be used when LVDS levels are required and the load would normally be a 100 differential load as shown in Figure 19. With the internal bias set, the HMC1033LP6GE output can also be used to drive 50 ohm single ended loads, see Figures 19 and 20. This would simplify LVPECL designs and reduce component cost.

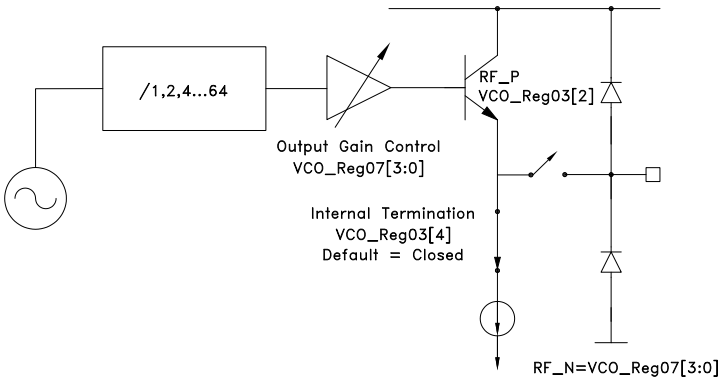

Figure 18. Output Stage

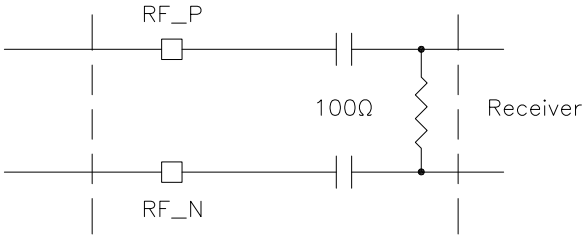

Figure 19. AC Coupling into 100 Ohm Differential Load

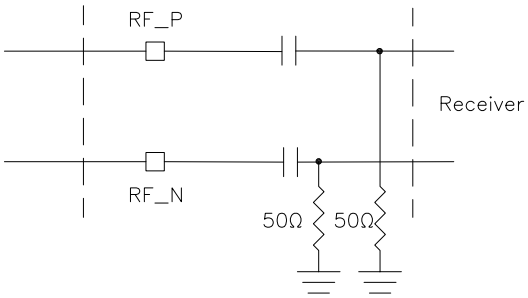

Figure 20. AC Coupling into a 50 Ohm Load

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Alternatively, the user can disable the internal bias, VCO_Reg 03h[4]=0, and use a standard LVPECL termination scheme. One of the most common methods is shown in Figure 21, with the resistors being located near the receiver. AC coupling can be used after the DC biasing resistor network

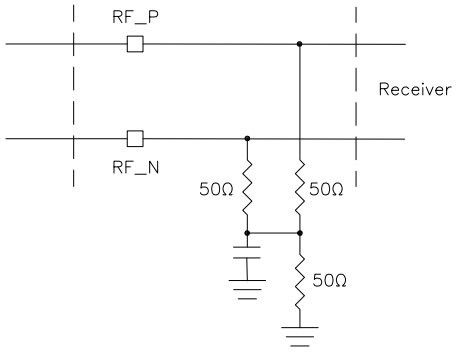

Figure 21. LVPECL Termination

The outputs can either be DC or AC coupled and the loads may be internal to the receiver or ADC etc - consult the manufacture for internal biasing and loading requirements. Selecting the AC coupling capacitors is a balance between impedance loading and rise and fall time versus signal loss and DC level drooping during the logic high and logic low levels - a low value such as 10 pF can be used for high frequency signals in the GHz range to ensure optimized rise and fall times, while a 100 nF capacitor can be used to insure low loss and minimal DC drooping when the output is a low value such as 25 MHz.

Waveform Diagrams

See Figure 22 which shows the definition for rise and fall time as well as VCM and VAMP. Figure 23 shows the Duty Cycle, which is defined as (On Time/Period) were On Time is positive going/logic high level . Measurements are made using the Internal Bias Setting.

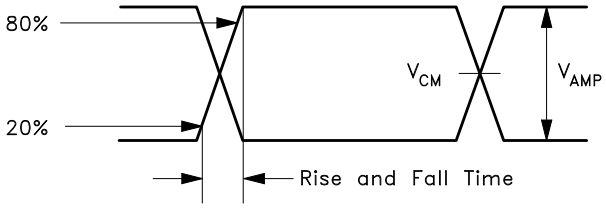

Figure 22. Rise and Fall Time, V_{CM} V_{AMP}

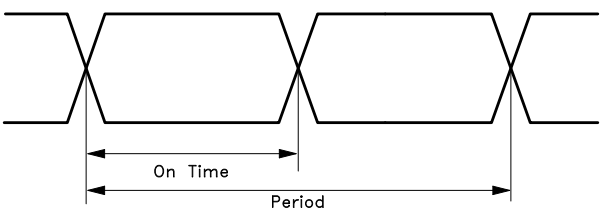

Figure 23. Duty Cycle

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1.1 SERIAL PORT

1.1.1 Serial Port Modes of Operation

The HMC1033LP6GE serial port interface can operate in two different modes of operation.

a. HMCSPI HMC Mode (HMC Legacy Mode) - Single slave per HMCSPI Bus

b. HMCSPI Open Mode - Up to 8 slaves per HMCSPI Bus.

Both Modes support 5-bits of register address space. HMC Mode can support up to 6 bits of register address.

Register 0 has a dedicated function in each mode. Open Mode allows wider compatibility with other manufacturers SPI protocols.

Register 0 Comparison - Single vs Multi-User Modes

	Single User HMC Mode	Multi-User Open Mode
READ	Chip ID 24-bits	Chip ID 24-bits
WRITE	Soft Reset, General Strobes	Read Address [4:0] Soft reset [5] General Strobes [23:6]

1.1.2 HMCSPI Protocol Decision after Power-On Reset

On power up both types of modes are active and listening.

A decision to select the desired SPI protocol is made on the first occurrence of SEN or SCLK following a hard reset, after which the protocol is fixed and only changeable by cycling the power OFF and ON.

a. If a rising edge on SEN is detected first HMC Mode is selected.
b. If a rising edge on SCLK is detected first Open mode is selected.

1.1.3 Serial Port HMC Mode - Single PLL

HMC Mode (Legacy Mode) serial port operation can only address and talk to a single PLL, and is compatible with most Hittite PLLs and PLLs with Integrated VCOs.

The HMC Mode protocol, shown in Figure 24 and, Figure 25 is designed for a 4 wire interface with a fixed protocol featuring

a. 1 Read/Write bit
b. 6 Address bits
c. 24 data bits
d. 3 wire for Write only, 4 wire for Read/Write capability

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1.1.3.1 HMC Mode - Serial Port WRITE Operation

AVDD = DVDD = 3.3V ±5%, AGND = DGND = 0V

SPI HMC Mode - Write Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			ns
t_2	SDI to SCLK setup time	3			ns
t_3	SCLK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCK to SEN fall	10			ns
	Max Serial port Clock Speed		50		MHz

A typical HMC Mode WRITE cycle is shown in Figre 24.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low indicates a Write cycle (/WR).
c. Host places the six address bits on the next six falling edges of SCK, MSB first.
d. Slave shifts the address bits in the next six rising edges of SCK (2-7).
e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first.
f. Slave shifts the data bits on the next 24 rising edges of SCK (8-31).
g. The data is registered into the chip on the 32nd rising edge of SCK.
h. SEN is cleared after a minimum delay of t_5. This completes the write cycle.

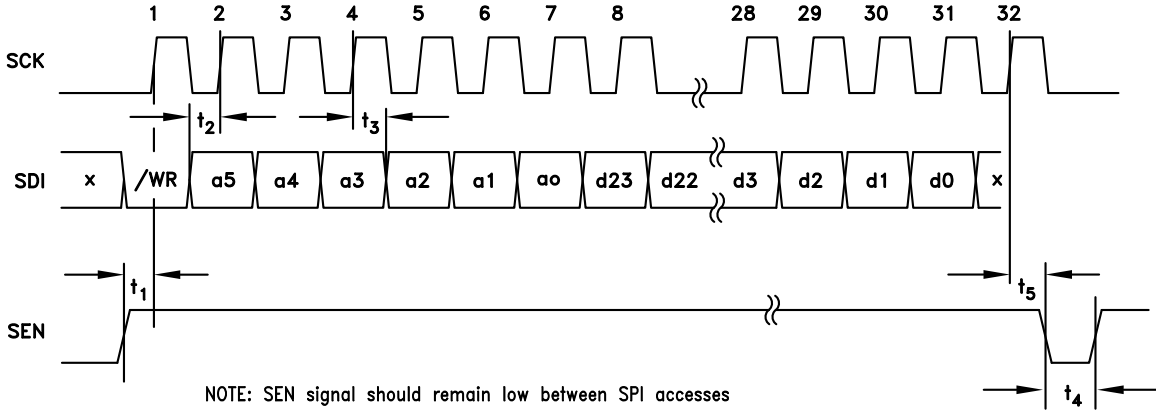

Figure 24. HMC Mode - Serial Port Timing Diagram Write

1.1.3.2 HMC Mode - Serial Port READ Operation

A typical HMC Mode READ cycle is shown in Figure 25.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCLK. Note: The Lock Detect (LD) function is usually multiplexed onto the LD_SDO pin. It is suggested that LD only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in Figure 25.

b. The slave (HMC1033LP6GE) reads SDI on the 1st rising edge of SCLK after SEN. SDI high initiates the READ cycle (RD)

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c. Host places the six address bits on the next six falling edges of SCLK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCLK (2-7).

e. Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. Slave restores Lock Detect on the 32nd rising edge of SCK.

h. De-assertion of SEN completes the cycle

SPI HMC Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			ns
t_2	SDI to SCLK setup time	3			ns
t_3	SCLK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCLK to SDO delay			8.2ns+0.2 ns/pF	ns
t_6	Recovery Time	10			ns

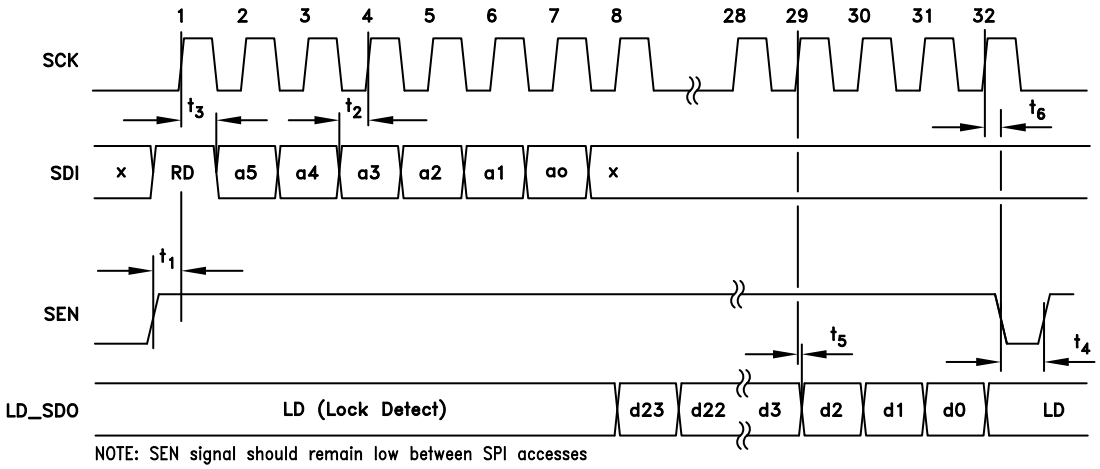

Figure 25. HMC Mode - Serial Port Timing Diagram - READ

1.1.4 Serial Port Open Mode

The Serial Port Open Mode, shown in Figure 26 and Figure 27, features:

a. Compatibility with general serial port protocols that use shift and strobe approach to communication

b. Compatible with Hittite PLL with Integrated VCO solutions, useful to address multiple chips of various types from a single serial port bus.

The Open Mode protocol has the following general features:

a. 3-bit chip address , can address up to 8 devices connected to the serial bus

b. Wide compatibility with multiple protocols from multiple vendors

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c. Simultaneous Write/Read during the SPI cycle

d. 5-bit address space

e. 3 wire for Write Only capability, 4 wire for Read/Write capability

Hittite PLLs with integrated VCOs support Open Mode. Some legacy PLL and microwave PLLs with integrated VCOs only support HMC Mode. Consult the relevant data sheets for details.

Typical serial port operation can be run with SCLK at speeds up to 50 MHz.

1.1.4.1 Open Mode - Serial Port WRITE Operation

AVDD = DVDD = 3.V ±5%, AGND = DGND = 0V

SPI Open Mode - WRITE Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK 32 Rising Edge to SEN Rising Edge	10			ns
t_6	Recovery Time	20			ns
	Max Serial port Clock Speed		50		MHz

A typical WRITE cycle is shown in Figure 26.

a. The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.

b. the slave (HMC1033LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK

c. Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK (25-29)

d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).

e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32). Hittite reserves chip address a2:a0 = 000 for all RF PLL with Integrated VCOs.

f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).

g. Master asserts SEN after the 32nd rising edge of SCLK.

h. Slave registers the SDI data on the rising edge of SEN.

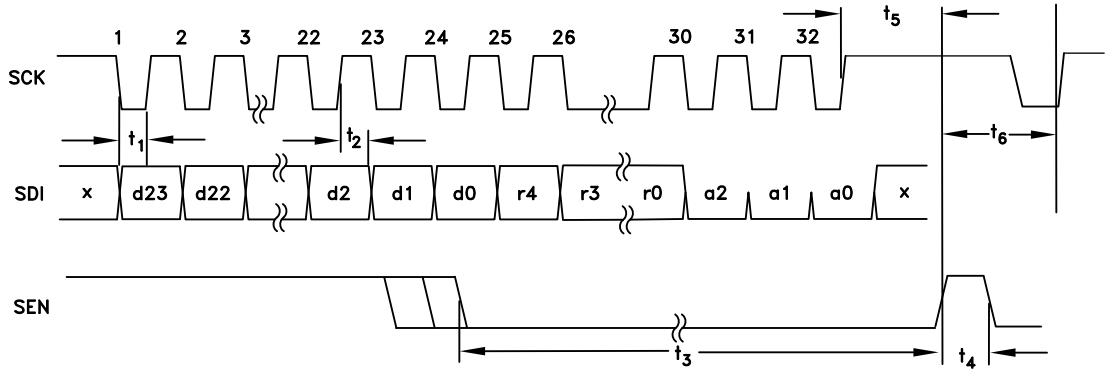

Figure 26. Open Mode - Serial Port Timing Diagram - WRITE

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1.1.4.2 Open Mode - Serial Port READ Operation

A typical READ cycle is shown in Figure 27.

In general, in Open Mode the LD_SDO line is always active during the WRITE cycle. During any Open Mode SPI cycle LD_SDO will contain the data from the current address written in Reg 00h[7:3]. If Reg 00h[7:3] is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg 00h[7:3], then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the Open Mode two cycle procedure to read from any random address is as follows:

a. The Master (host), on the first 24 falling edges of SCLK places 24-bit data, d23:d0, MSB first, on SDI as shown in Figure 27. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on the next cycle.

b. the slave (HMC1033LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK

c. Master places 5-bit register address , r4:r0, (the READ ADDRESS register), MSB first, on the next 5 falling edges of SCLK (25-29). r4:r0=00000.

d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).

e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32)..Chip address is always 000 for RF PLL with Integrated VCOs.

f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).

g. Master asserts SEN after the 32nd rising edge of SCLK.

h. Slave registers the SDI data on the rising edge of SEN.

i. Master clears SEN to complete the address transfer of the two part READ cycle.

j. If one does not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.

k. Master places the same SDI data as the previous cycle on the next 32 falling edges of SCLK.

l. Slave (HMC1033LP6GE) shifts the SDI data on the next 32 rising edges of SCLK.

m. Slave places the desired read data (ie. data from the address specified in Reg 00h[7:3] of the first cycle) on LD_SDO which automatically switches to SDO mode from LD mode, disabling the LD output.

m. Master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to Lock Detect on LD_SDO.

SPI Open Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK Rising Edge to SDO time		8.2ns+0.2ns/pF		ns
t_6	Recovery TIme	10			ns
t_7	SCK 32 Rising Edge to SEN Rising Edge	10			ns

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1.1.4.3 HMCSPI Open Mode READ Operation - 2 Cycles

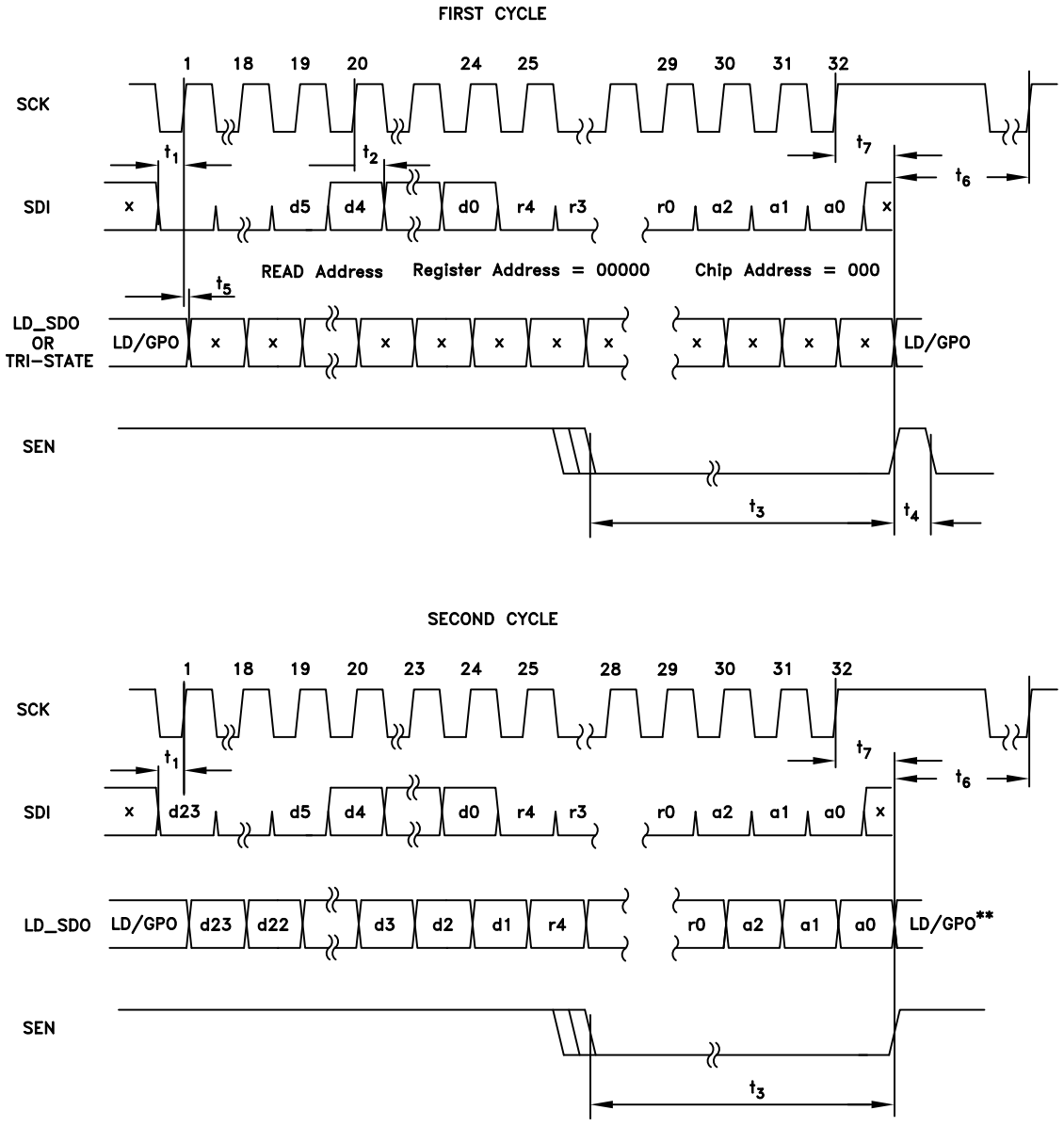

Figure 27. Serial Port Timing Diagram - READ

For more information on using the GPO pin while in SPI Open Mode please see section 1.15.

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1.2 Configuration at Start-Up

To configure the PLL after power up, follow the instructions below:

1. Configure the reference divider (write to Reg 02h), if required.
2. Configure the delta-sigma modulator (write to Reg 06h).
   - Configuration involves selecting the mode of the delta-sigma modulator (Mode A or Mode B), selection of the delta-sigma modulator seed value, and configuration of the delta-sigma modulator clock scheme. It is recommended to use the values found in the Hittite PLL evaluation board control software register files.
3. Configure the charge pump current and charge pump offset current (write to Reg 09h)
4. Configure the VCO Subsystem (write to Reg 05h, for more information see section 1.3.1, and "VCO Subsystem Register Map. Detailed writes to the VCO subsystem via PLL Reg 05h at start-up are available in the Register Setting Files found in the Hittite PLL Evaluation Software received with a product evaluation kit or downloaded from www.hittite.com.
5. Program the frequency of operation
   - Program the integer part (write to Reg 03h)
   - Program the fractional part (write to Reg 04h)
6. Configure the VCO output divider, if needed in the VCO subsystem via PLL Reg 05h.

Once the HMC1033LP6GE is configured after startup, in most cases the user only needs to change frequencies by writing to Reg 03h integer register, Reg 04h fractional register, and Reg 05h to change the VCO output divider or doubler setting if needed, and possibly adjust the charge pump settings by writing to Reg 09h

For detailed and most up-to-date start-up configuration please refer to the appropriate Register Setting Files found in the Hittite PLL Evaluation Software received with a product evaluation kit or downloaded from www.hittite.com.

1.3 VCO Serial Port Interface (SPI)

The HMC1033LP6GE communicates with the internal VCO subsystem via an internal 16 bit VCO Serial Port, (e.g. see Figure 25). The internal serial port is used to control the step tuned VCO and other VCO subsystem functions, such as RF output divider / doubler control and RF buffer enable.

Note that the internal VCO subsystem SPI (VSPI) runs at the rate of the AutoCal FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by Reg 0Ah*[14:13]* with a default setting = 1, or XREFP divided by 4.

Writes to the VCO's control registers are handled indirectly, via writes to Reg 05h of the PLL. A write to PLL Reg 05h causes the PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where it is interpreted.

The VCO serial port has the capability to communicate with multiple subsystems inside the IC. For this reason each subsystem has a subsystem ID, Reg 05h[2:0].

Each subsystem has multiple registers to control the functions internal to the subsystem, which may be different from one subsystem to the next. Hence each subsystem has internal register addresses bits ("Reg 05h"6:3])

Finally the data required to configure each register within the VCO subsystem is contained in Reg 05h[15:7].

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1.3.1 VSPI Use of Reg05h

The packet data written into, Reg 05h is sub-parsed by logic at the VCO subsystem into the following 3 fields:

1. [2:0] - 3 bits - VCO_ID, target subsystem address = 000b.
2. [6:3] - 4 bits - VCO_REGADDR, the internal register address inside the VCO subsystem.
3. [15:7] - 9- bits- VCO_DATA, data field to write into the VCO register.

For example, to write 0_1111_1110 into register 2 of the VCO subsystem (VCO_ID = '000'b), and set the VCO output divider to divide by 62, the following needs to be written to Reg 05h ='0_1111_1110, 0010, 000' b.

During AutoCal, the AutoCal controller only updates the data field of Reg 05h. The VCO subsystem register address (Reg 05h[6:3]) must be set to 0000 for the AutoCal data to be sent to the correct address.

VCO subsystem ID and register address are not modified by the AutoCal state machine. Hence, if a manual access is done to a VCO Subsystem register the user must reset the register address to zero before a change of frequency which will re-run AutoCal.

Since every write to Reg 05h will result in a transfer of data to the VCO subsystem, if the VCO subsystem needs to be reset manually, it is important to make sure that the VCO switch settings are not changed. Hence the switch settings in Reg 10h[7:0] need to be read first, and then rewritten to Reg 05h[15:8].

In summary, first read "Reg 10h", then write to "Reg 05h" as follows:

Reg 10h[7:0]	= vv x yyyyy
Reg 05h	= vv x yyyyy 0 0000 iii
Reg 05h[2:0]	= iii, subsystem ID, 3 bits (000)
Reg 05h[6:3]	= 0000, subsystem register address
Reg 05h[7]	= 0 , calibration tune voltage off
Reg 05h[12:8]	= yyyyy, VCO caps
Reg 05h[13]	= x, don't care
Reg 05h[15:14]	= vv, VCO Select

1.0 PLL Register Map

1.1 Reg 00h ID Register (Read Only)

Bit	Type	Name	Width	Default	Description
[23:0]	RO	chip_ID	24	A7975	HMC1033LP6GE chip ID

1.2 Reg 00h Open Mode Read Address/RST Strobe Register (Write Only)

Bit	Type	Name	Width	Default	Description
[4:0]	WO	Read Address	5	-	(WRITE ONLY) Read Address for next cycle - Open Mode Only
[5]	WO	Soft Reset	1	-	Soft Reset - both SPI modes reset (set to 0 for proper operation)
[23:6]	WO	Not Defined	18	-	Not Defined (set to 0 for proper operation)

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1.3 Reg 01h RST Register

(Default 000002h)

Bit	Type	Name	Width	Default	Description
[0]	R/W	Reserved	1	0	Reserved
[1]	R/W	Reserved	1	1	Reserved
[2]	R/W	Reserved	1	0	Reserved
[3]	R/W	Reserved	1	0	Reserved
[4]	R/W	Reserved	1	0	Reserved
[5]	R/W	Reserved	1	0	Reserved
[6]	R/W	Reserved	1	0	Reserved
[7]	R/W	Reserved	1	0	Reserved
[8]	R/W	Reserved	1	0	Reserved
[9]	R/W	Reserved	1	0	Reserved

1.4 Reg 02h REFDIV Register

(Default 000001h)

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	rdiv	14	1	Reference Divider 'R' Value " Divider use also requires refBufEn Reg08[3]=1and Divider min 1d max 16383d

1.5 Reg 03h Frequency Register - Integer Part

(Default 000019h)

Bit	Type	Name	Width	Default	Description
[18:0]	R/W	intg	19	25d	VCO Divider Integer part, used in all modes) Fractional Mode min 20d max 2^{19} -4 = 7FFFCh = 524,284d Integer Mode min 16d max 2^{19}-1 = 7FFFFh = 524,287d

1.6 Reg 04h Frequency Register - Fractional Part

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[23:0]	R/W	frac	24	0	VCO Divider Fractional part (24-bit unsigned) see Fractional Frequency Tuning Used in Fractional Mode only (N_{frac}=Reg 04h/2^{24} min 0d max 2^{24}-1

1.7 Reg 05h VCO SPI Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	VCO Subsystem_ID,	3	0	Internal VCO Subsystem ID
[6:3]	R/W	VCO Subsystem register address	4	0	For interfacing with the VCO please see section 1.3.1.
[15:7]	R/W	VCO Subsystem data	9	0	Data

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Note:Reg 05h is a special register used for indirect addressing of the VCO subsystem. Writes to Reg 05h are automatically forwarded to the VCO subsystem by the VCO SPI state machine controller.

Reg05h is a Read-Write register. However, Reg05h only holds the contents of the last transfer to the VCO subsystem. Hence it is not possible to read the full contents of the VCO subsystem. Only the content of the last transfer to the VCO subsystem can be read. Please take note special considerations for AutoCal related to Reg 05h

1.8 Reg 06h SD CFG Register

(Default 200B4Ah)

Bit	Type	Name	Width	Default	Description
[1:0]	R/W	seed	2	2	Selects the Seed in Fractional Mode 00: 0 seed 01: lsb seed 02: B29D08h seed 03: 50F1CDh seed Note; Writes to this register are stored in the HMC1033LP6GE and are only loaded into the modulator when a frequency change is executed and if AutoSeed *Reg06h[8] =1*
[3:2]	R/W	Reserved	2	2	Reserved
[6:4]	R/W	Reserved	3	4	Reserved
[7]	R/W	frac_bypass	1	0	0: Use Modulator, Required for Fractional Mode, 1: Bypass Modulator, Required for Integer Mode Note: In bypass fractional modulator output is ignored, but fractional modulator continues to be clocked if *frac_rstb =1,* Can be used to test the isolation of the digital fractional modulator from the VCO output in integer mode
[8]	R/W	Reserved	1	1	Reserved
[9]	R/W	Reserved	1	1	Reserved
[10]	R/W	Reserved	1	0	Reserved
[11]	R/W	SD Enable	1	1	0: disable frac core, use for Integer Mode or Integer Mode with CSP 1: Enable Frac Core, required for Fractional Mode, or Integer isolation testing This register controls whether AutoCal starts on an Integer or a Fractional write
[12]	R/W	Reserved	1	0	Reserved
[13]	R/W	Reserved	1	0	Reserved
[15:14]	R/W	Reserved	2	0	Reserved
[17:16]	R/W	Reserved	2	0	Reserved
[18]	R/W	Reserved	1	0	Reserved
[20:19]	R/W	Reserved	2	0	Reserved
[21]	R/W	Reserved	1	1	Reserved
[22]	R/W	Reserved	1	0	Reserved

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1.9 Lock Detect:

HMC1033LP6GE features a robust digital lock detect function that provides faster and more accurate lock detect information compared to conventional analog lock detect schemes, and offers serial port monitoring of lock detect for visibility into device status from the host controller.

Lock Detect Enable Reg 07h[3]=1 is a global enable for all lock detect functions. The Lock Detect circuit effectively measures the difference between the arrival of the reference and the divided VCO signals at the Phase Detector. The arrival time difference must consistently be less than the Lock Detect window length, to declare lock. Either signal may arrive first, only the difference in arrival times is considered.

wincnt_max in Reg 07h[2:0] defines the number of consecutive counts of the divided VCO that must land inside the lock detect window to declare lock.

1.9.1 Analog or Digital Lock Detect

Analog Lock Detect

The lock detect window may be generated by either an analog one shot circuit or a digital one shot based upon an internal timer. Clearing Reg 07h[6]=0 will result in a fixed, analog, nominal 10 ns window, as shown in Figure 28 below. The analog window cannot be used if the PD rate is above 50 MHz, or if the charge pump offset is too large. If charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.

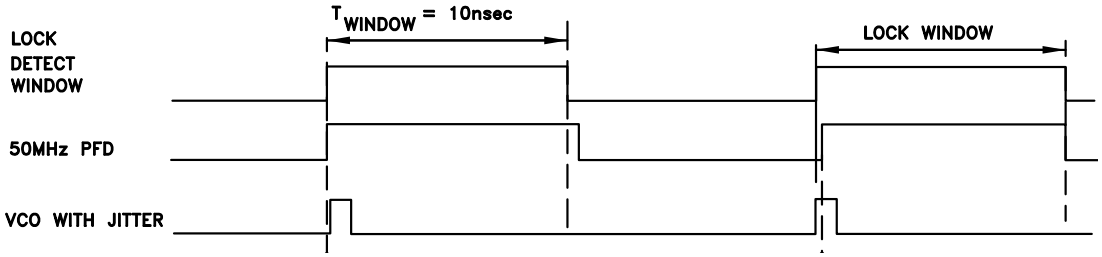

Figure 28. Lock Detect

1.9.2 Digital Lock Detect:

Setting Reg 07h[6]=1 will result in a variable length lock detect window based upon an internal digital timer. The timer period is set by the number of cycles of the internal LD clock as programmed by Reg 07h[9:7]. The LD clock frequency is adjustable by Reg 07h[11:10]. The LD clock signal can be viewed via the GPO test pins.

1.9.3 Declaration of Lock:

The Lock Detect Flag status is always readable in Reg 12h[1], if locked = 1. Lock Detect status is also output to the LD_SDO pin according to Reg 0Fh[4:0]=1. Again, if locked, LD_SDO will be high. Clearing Reg 0Fh[6]=0 will display the Lock Detect Flag on LD_SDO except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the Lock Detect Flag after the read is completed.

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1.9.4 Reg 07h Lock Detect Register

(Default 00014Dh)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	lkd_wincnt_max	3	5d	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65535
[3]	R/W	Enable Internal Lock Detect	1	1	1: Enabled
[5:4]	R/W	Reserved	2	0	Reserved
[6]	R/W	Lock Detect Window type	1	1	Lock Detection Window Timer Selection 1: Digital programmable timer 0: Analog one shot, nominal 10 ns window
[9:7]	R/W	LD Digital Window duration	3	2	0 Lock Detection - Digital Window Duration 0: 1/2 cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles 4: 8 cycles 5: 16 cycles 6: 32 cycles 7: 64 cycles
[11:10]	R/W	Reserved	2	0	Reserved
[12]	R/W	Reserved	1	0	Reserved
[13]	R/W	Reserved	1	0	Reserved

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1.10 Reg 08h Analog EN Register

(Default C1BEFFh)

Bit	Type	Name	Width	Default	Description
[0]	R/W	Reserved	1	1	Reserved
[1]	R/W	Reserved	1	1	Reserved
[2]	R/W	Reserved	1	1	Reserved
[3]	R/W	Reserved	1	1	Reserved
[4]	R/W	Reserved	1	1	Reserved
[5]	R/W	gpo_pad_en	1	1	0 - Pin LD_SDO disabled 1 - and RegFh[7]=1 , Pin LD_SDO is always on required for use of GPO port 1 - and RegFh[7]=0 SPI LDO_SPI is off if unmatched chip address is seen on the SPI, allowing a shared SPI with other compatible parts
[6]	R/W	Reserved	1	1	Reserved
[7]	R/W	Reserved	1	1	Reserved
[8]	R/W	Reserved	1	0	Reserved
[9]	R/W	Prescaler Clock enable	1	1	Reserved
[10]	R/W	VCO Buffer and Prescaler Bias Enable	1	1	VCO Buffer and Prescaler Bias Enable
[11]	R/W	Reserved	1	1	Reserved
[14:12]	R/W	Reserved	3	011	Reserved
[17:15]	R/W	Reserved	3	011	Reserved
[18]	R/W	Reserved	1	0	Reserved
[19]	R/W	Reserved	1	0	Reserved
[20]	R/W	Reserved	1	0	Reserved
[21]	R/W	High Frequency Reference	1	0	Program to 1 for XTAL > 200 MHz
[22]	R/W	Reserved	1	1	Reserved
[23]	R/W	Reserved	1	1	Reserved

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1.11 Charge Pump Current Selection

HMC1033LP6GE features provides a charge pump current with programmable gain. This enables the user to refine and maintain optimal PLL loop bandwidth over a wide range of output frequencies and feedback divide ratios.

A straight forward method for determining the charge pump gain setting for a fixed loop filter (e.g., 127 kHz) and reference frequency (e.g., 50MHz) is to follow the following equation:

Icp_up = Icp_dn = 1.1mA + (2.3mA – 1.1mA) * (Fvco – 1.5 GHz) / (3 GHz – 1.5 GHz)

Here, charge pump current (Icp) is linearly modified to compensate for the feedback divide ratio (N) as it scales with VCO output frequency (Fvco).

The charge pump current is set by register configuration (Reg_09h [6:0] and Reg_09h [13:7]).

Charge Pump Phase Offset – Fractional Mode

The HMC1033LP6GE provides a programmable charge pump phase offset feature to aid in minimizing integer boundary spurs and maintain low in-band phase noise, while the PLL is in Fractional Mode of operation.

Phase offset is achieved by introducing a constant “leakage” current into the loop filter. The amount of leakage current that is recommended is related to the charge pump gain (Icp) and the PFD comparison frequency (Fcomp) by the following equation(s):

Tcomp = 1 / Fcomp
I_leak = (2.5x10-9 + 4*Tvco) * Icp / Tcomp

Where:
Tvco: is the RF period at the input of the feedback divider
Icp: is the selected charge pump current

Leakage (I_leak) can be applied with either positive or negative current driven into the loop filter, (“up” or “down” respectively). Up leakage is recommended for the HMC1033LP6GE.

Leakage magnitude and direction are set through registers Reg_09h [20:14] and Reg_09h [22], respectively.

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1.12 Reg 09h Charge Pump Register

(Default 403264h)

Bit	Type	Name	Width	Default	Description
[6:0]	R/W	CP DN Gain	7	100d 64h	Charge Pump DN Gain Control 20 µA√step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA
[13:7]	R/W	CP UP Gain	7	100d 64h	Charge Pump UP Gain Control 20 µA per step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA
[20:14]	R/W	Offset Magnitude	7	0	Charge Pump Offset Control 5 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 5 µA 2d = 10 µA ... 127d = 635 µA
[21]	R/W	Offset UP enable	1	0	recommended setting = 0
[22]	R/W	Offset DN enable	1	1	recommended setting = 1 in Fractional Mode, 0 otherwise
[23]	R/W	Reserved	1	0	Reserved

1.13 Reg 0Ah VCO AutoCal Configuration Register

(Default 002205h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	Vtune Resolution	3	5	R Divider Cycles 0 - 1 1 - 2 2 - 4 3 - 8 4 - 32 5 - 64 6 - 128 7 - 256
[5:3]	R/W	Reserved	3	0	Reserved
[7:6]	R/W	Reserved	2	0	Reserved
[9:8]	R/W	Reserved	2	0	Reserved
[10]	R/W	Force Curve	1	0	Force curve sent during Tuning Tune from Reg5
[11]	R/W	Bypass VCO Tuning	1	0	Bypass VCO Tuning
[12]	R/W	No VSPI Trigger	1	0	Don't trigger a transfer on writes to Reg 05h
[14:13]	R/W	FSM/VSPI Clock Select	2	1	Set the AutoCal FSM and VSPI Clock (50 MHz maximum) 0: Input Crystal Reference 1: Input Crystal Reference/4 2: Input Crystal Reference/16 3: Input Crystal Reference/32
[15]	R/W	Reserved	1	0	Reserved
[16]	R/W	Reserved	1	0	Reserved

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1.14 Reg 0Bh PD Register

(Default 0F8061h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	PD_del_sel	3	1	Sets PD reset path delay (Recommended setting 001)
[3]	R/W	Reserved	1	0	Reserved
[4]	R/W	Reserved	1	0	Reserved
[5]	R/W	PD_up_en	1	1	Enables the PD UP output
[6]	R/W	PD_dn_en	1	1	Enables the PD DN output
[8:7]	R/W	CSP Mode	2	0	Cycle Slip Prevention Mode Extra current is driven into the loop filter when the phase error is larger than: 0: Disabled 1: 5.4ns 2: 14.4ns 3: 24.1ns This delay varies by +- 10% with temperature, and +- 12% with process.
[9]	R/W	Force CP UP	1	0	Forces CP UP output on - Use for Test only
[10]	R/W	Force CP DN	1	0	Forces CP DN output on - Use for Test only
[11]	R/W	Reservedl	1	0	Reserved
[14:12]	R/W	Reserved	3	0	Reserved
[16:15]	R/W	Reserved	2	3	Reserved
[18:17]	R/W	Reserved	2	3	Reserved
[19]	R/W	reserved	1	1	Reserved
[21:20]	R/W	reserved	2	0	Reserved
[23:22]	R/W	reserved	2	0	Reserved

1.15 Exact Frequency Mode

Hittite's family of clock generation products have a unique feature called exact frequency mode which allows nearly arbitrary frequency conversion, or "gear" ratios.

There are 5 registers which control the 3 frequency dividers in the part, and thus the overall frequency translation ratio:

1) Reference Divider (R) – PLL Register 2 - Takes in up to 350MHz reference, and optionally divides down to < 100MHz for the PFD comparison rate.

2) VCO N-Divider (NDIV) – Integer (PLL Reg 3) + Fractional section (PLL Reg 4). Accepts values from 16 to 525287 in integer mode, or 20.0 to 242284.0 in fractional mode

3) VCO Output Divider (NOUT) – VCO Register 2.

The output frequency is given by:

Gear Ratio = (1/R) * (NDIV) * (1/NOUT)

Since the PLL supports a fractional division ratio, N can be further broken down into a fraction N = (M/N).

To achieve a certain multiplication ratio, we recommend the following procedure – along with a worked example.

Example: Assume we want a multiplication ratio of M/N = 944/255, with an input frequency of 168.04MHz- Thus fout ~ 622MHz.

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1) Calculate NOUT: Determine the fundamental frequency of the VCO, relative to your desired output frequency. The VCO cores run internally from 1.5 to 3GHz.

a. Since the VCO output divider is only capable of even division ratios, there is a factor of '2' in the calculation.
b. NOUT = 2*floor(fmax/(2*fout))
eg. NOUT = 2 * floor (3G / 2*622M)
NOUT=2 * floor (2.41…)
NOUT = 2 * 2
NOUT = 4

So the VCO will run at ~ 4 * 622 MHz.

2) Calculate RDIV: Determine if the Rdivider needs to be used to keep the PFD rate under its limit, and if so, its value.

a. The PFD comparison rate can be as high as 100MHz. To avoid a 2 stage locking process, we recommend running the PFD below 70MHz.
b. R = ceiling (fpfd_max / freference)
eg. R = ceiling (168.04MHz / 70 MHz)
R = ceiling (2.4)
R = 3

So the PFD comparison rate will be 168.04MHz / 3, or ~ 56MHz

3) Calculate NDIV: We have now determined an R and NOUT value which keep the PLL in a valid operating condition, and we are left to choose the fractional division ratio NDIV which provides the desired gear ratio.

a. Calculate the desired NDIV value (which could be a fraction) , such that your overall gear ratio is maintained:
i. (M / N)_desired = (1/R) * NDIV * (1/NOUT)
ii. NDIV = (M / N)_desired * R * NOUT
eg. NDIV = (944 / 255) * 3 * 4
NDIV = 7728 / 255
b. Reduce the fraction into a integer + fractional portion:
eg. NDIV = 7728 / 255
NDIV = 30 + 78/255
NDIV = 30 + 26/85 = NINT + (NUM / DEN)
NDIV = ~ 30 + 0.306…
c. Confirm that the minimum divide ratio limit is respected. In fractional mode, the minimum divide ratio is 20.0, in integer mode it is 16. If NDIV is too low, increase the reference divide ratio (step 2b), and recalculate. For example, doubling the reference divide ratio R, will double the corresponding NDIV setting.
eg. In this example, NDIV of ~ 30.3 is > 20.0, so it is accetptable and R of 3 is okay.

4) Calculate the Integer, and approximate Fractional Setpoint to implement NDIV calculated in step 3.

Example
Nint = floor (NDIV)
Nint = 30
Nfrac = ceil(2^24 * (NDIV-Nint))
Nfrac = ceiling(16,777216 * 26/85) = ceiling(5,131854.306) = 5,131,854 dec

5) Note that the 24-bit quantized NDIV ratio = 30 + (5,131,854 / 16,777,216) has a slight frequency offset of ~2.3Hz relative to the desired ratio of 30 + 26/85. To eliminate this offset, and generate the exact multiplication ratio the user desires, set the exact frequency counter (REG0Ch) to the reduced denominator as calculated in step 3b. Exact Frequency Counter = DEN (from step 3b) eg. Set Register 0Ch = 85 dec.

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1.15.1 Reg 0Ch Exact Frequency Mode Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	Number of Channels per Fpd	14	0	Comparison Frequency divided by the Correction Rate, Must be an integer. Frequencies at exactly the correction rate will have zero frequency error. 0: Disabled 1: Disabled 2:16383d (3FFFh)

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1.16 GPO_LD/SPO Register

HMC1033LP6GE features a GPO (General Purpose Output) that enables users to control and read various states of the device including PLL and VCO properties.

The HMC1033LP6GE shares the LD_SDO (Lock-Detect/Serial Data Out) pin to perform various functions. It is driven by a tri-state CMOS driver with ~200 Ω Rout. In its default configuration, after power-on-reset, the output driver is disabled, and only drives during appropriately addressed SPI reads. This allows it to share the output with other devices on the same bus. To monitor any of the GPO signals, including Lock Detect, set Reg 0Fh[7] = 1 to keep the SDO driver always on. This stops the LDO driver from tristating and means that the SDO line cannot be shared with other devices. The signals available on the GPO are selected by changing “GPO Select”, Reg 0Fh[4:0].

1.16.1 Reg 0Fh GPO_LD/SPO Register

(Default 000001h)

Bit	Type	Name	Width	Default	Description
[4:0]	R/W	gpo_select	5	1d	Signal selected here is output to SDO pin when enabled 0: Data from Reg0F[5] 1: Lock Detect Output 2. Lock Detect Trigger 3: Lock Detect Window Output 4: Ring Osc Test 5. Pullup Hard from CSP 6. PullDN hard from CSP 7. Reserved 8: Reference Buffer Output 9: Ref Divider Output 10: VCO divider Output 11. Modulator Clock from VCO divider 12. Auxiliary Clock 13. Aux SPI Clock 14. Aux SPI Enable 15. Aux SPI Data Out 16. PD DN 17. PD UP 18. SD3 Clock Delay 19. SD3 Core Clock 20. AutoStrobe Integer Write 21. Autostrobe Frac Write 22. Autostrobe Aux SPI 23. SPI Latch Enable 24. VCO Divider Sync Reset 25. Seed Load Strobe 26.-29 Not Used 30. SPI Output Buffer En 31. Soft RSTB
[5]	R/W	GPO Test Data	1	0	1 - GPO Test Data
[6]	R/W	Prevent Automux SDO	1	0	1- Outputs GPO data only 0 - Automuxes between SDO and GPO data
[7]	R/W	LDO Driver Always On	1	0	1- LD_SDO Pin Driver always on 0 - LD_SDO Pin driver only on during SPI read cycle
[8]	R/W	Disable PFET	1	0	program to 0
[9]	R/W	Disable NFET	1	0	program to 0

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1.17 Reg 10h VCO Tune Register

(Default 000020h)

Bit	Type	Name	Width	Default	Description
[7:0]	RO	VCO Switch Setting	8	32	Read Only Register. Indicates the VCO switch setting selected by the AutoCal state machine to yield the nearest free running VCO frequency to the desired operating frequency. Not valid when Reg10h[8] = 1, AutoCal Busy. Note if a manual change is done to the VCO switch settings this register will not indicate the current VCO switch position. 0 = highest frequency 1 = 2nd highest ... 256 = lowest frequency Note: VCO subsystems may not use all the MSBs, in which case the unused bits are don't care
[8]	RO	AutoCal Busy	1	0	Busy when AutoCal state machine is searching for the nearest switch setting to the requested frequency.

1.18 Reg 11h SAR Register

(Default 007FFFh)

Bit	Type	Name	Width	Default	Description
[18:0]	RO	SAR Error Mag Counts	19	2^{19}-1	SAR Error Magnitude Counts
[19]	RO	SAR Error Sign	1	0	SAR Error Sign 0=+ve 1=-ve

1.19 Reg 12h GPO2 Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[0]	RO	GPO	1	0	GPO State
[1]	RO	Lock Detect	1	0	Lock Detect Status 1 = Locked 0 = Unlocked

1.20 Reg 13h BIST Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[15:0]	RO	Reserved	19	4697d	Reserved
[16]	RO	Reserved	1	0	Reserved

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2.0 VCO Subsystem Register Map

Please note that the VCO subsystem uses indirect addressing via Reg 05h. For more detailed information on how to write to the VCO subsystem please see section VCO Subsystem Register Map.

2.1 VCO_Reg 00h Tuning

Bit	Type	Name	Width	Default	Description
[0]	WO	Cal	1	0	VCO tune voltage is redirected to a temperature compensated calibration voltage
[8:1]	WO	CAPS	8	16	VCO sub-band selection. 0 - max frequency 1111 1111 - min frequency. Not all sub-bands are used on the various products.

2.2 VCO_Reg 01h Enables

Bit	Type	Name	Width	Default	Description
[0]	WO	Master Enable VCO Subsystem	1	1	0 - All VCO subsystem blocks Off
[1]	WO	VCO Enable	1	1	Enables VCOs
[2]	WO	PLL Buffer Enable	1	1	Enables PLL Buffer to N Divider
[3]	WO	IO Master Enable	1	1	Enables output stage and the Output Divider. It does not enable/disable the VCO.
[4]	WO	Spare	1	1	don't care
[5]	WO	Output Stage Enable	1	1	Output Stage Enable
[7:6]	WO	Reserved	2	2	Reserved
[8]	WO	don't care	1	1	don't care

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For example, to disable the output stage of the VCO subsystem of the HMC1033LP6GE, bit 5 in VCO_Reg 01h needs to be cleared. If the other bits are left unchanged, then '1 1101 1111' needs to be written into VCO_Reg 01h. The VCO subsystem register is accessed via a write to PLL subsystemReg 05h = '1 1101 1111 0001 000' = EF88h

Reg 05h[2:0] = 000; VCO subsystem ID 0
Reg 05h[6:3] = 0001; VCO subsystem register address
Reg 05h[7] = 1; Master enable
Reg 05h[8] = 1; VCO enable
Reg 05h[9] = 1; PLL Buffer enable
Reg 05h[10] = 1; IO Master enable
Reg 05h[11] = 1; Reserved
Reg 05h[12] = 0; Disable the output stage
Reg 05h[14:13] = '01'b
Reg 05h[15] = 1; don't care

2.3 VCO_Reg 02h Biases

Bit	Type	Name	Width	Default	Description
[5:0]	WO	RF Divide ratio	6	1	0 - Mute 1 - Fo 2 - Fo/2 3 - invalid, defaults to 2 4 - Fo/4 5 - invalid, defaults to 4 6 - Fo/6 ... 60 - Fo/60 61 - invalid, defaults to 60 62 - Fo/62 > 62 - invalid, defaults to 62
[7:6]	WO	Reserved	2	0	Reserved
[8]	WO	Don't Care	1	0	Don't Care

For example, to write 0_1111_1110 into VCO_Reg 03h VCO subsystem (VCO_ID = '000'b), and set the VCO output divider to divide by 62, the following needs to be written to Reg 05h ='0_1111_1110, 0010, 000' b.

Reg 05h[2:0] = 00; subsystem ID 0
Reg 05h[6:3] = 0010; VCO register address 2d
Reg 05h16:7] = 0_1111_1110; Divide by 62, max output RF gain

HMC1033LP6GE Power versus Performance Priority Modes:

The HMC1033LP6GE is designed with 2 major configuration options: Power Priority and Performance Priority. The Power Priority setting reduces the current consumption of the part, whereas the Performance Priority setting improves the Jitter and Phase Noise performance. The settings are selected via the appropriate SPI registers, VCO_Reg 03h [1:0].

The "Power Priority Mode" is used in order to reduce the current consumption from 237 mA to 173 mA, such as may be required in power sensitive applications, where the lowest phase noise performance may not be critical. The Power Priority mode does not cause a reduction on the output signal power, but it degrades the phase noise, and thus jitter, performance.

In order to realize the best phase noise and jitter performance, the HMC1033LP6GE should be operated in the "Performance Priority Mode". By invoking this mode, the phase noise will improve or decrease by 10 dB resulting in a -163 dBc/Hz floor. The "Performance Priority Mode" is optimal in driving the sample clock inputs of ADC/DAC's and high speed SERDES reference clock inputs where jitter performance is of utmost importance.

The Power versus Performance Priority mode is set by the VCO_Reg03h bits [1:0] and the default condition is Power Priority Mode, bit set to a logic 1.

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2.4 VCO_Reg 03h Config

Bit	Type	Name	Width	Default	Description
[1:0]	WO	Power- Performance Priroirty	2	2	Selects output noise floor performance level at a cost of increased current consumption 01: Power Priority Lowest Current Consumption 11: Performance Priority Best Phase Noise Other states (00 and 10) not fully characterized.
[2]	WO	RF_P output enable	1	0	Logic 1 enables the output on RF_P pin. Required for differential operation, or single-ended output on RF_P pin.
[3]	WO	RF_N output enable	1	0	Logic 1 enables the output on RF_N pin. Required for differential operation, or single-ended output on RF_N pin.
[4]	WO	Internal Termination Enable	1	1	Logic 1 enables the internal bias termination, is used for LVDS level outputs. Set to logic 0 for external termination
[5]	WO	Increase Internal Output Resistance	1	0	Logic 1 increase internal output termination by ~ 15 Ω on each pin (RF_N and RF_P)
[6]	WO	Reserved	1	0	Reserved
[8:7]	WO	Mute Mode	2	1	Defines when the Mute Function is enabled (the output is muted): • 00: Mute enabled when divide ratio (VCO_Reg 02h[5:0] = 0 • 01: During VCO Calibration (• 10: During VCO Calibration or when Lock Detect/ GPO output is off (For more information see section • 11: Mute always On.

2.5 VCO_Reg 04h Cal/Bias

Specified performance is only guaranteed with the required settings in this table. Other settings are not supported.

Bit	Type	Name	Width	Default	Description
[0]	WO	Reserved	1	1	Reserved
[1]	WO	Reserved	1	0	Reserved
[2]	WO	Reserved	1	0	Reserved
[4:3]	WO	Reserved	2	1	Reserved
[6:5]	WO	Reserved	2	2	Reserved
[8:7]	WO	Reserved	2	1	Reserved

2.6 VCO_Reg05h CF_Cal

Bit	Type	Name	Width	Default	Description
[1:0]	WO	Reserved	2	2	Reserved
[3:2]	WO	Reserved	2	2	Reserved
[5:4]	WO	Reserved	2	2	Reserved
[7:6]	WO	Reserved	2	2	Reserved
[8]	WO	Reserved	1	0	Reserved

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2.7 VCO_Reg06h MSB Cal

Bit	Type	Name	Width	Default	Description
[1:0]	WO	Reserved	2	3	Reserved
[3:2]	WO	Reserved	2	3	Reserved
[5:4]	WO	Reserved	2	3	Reserved
[7:6]	WO	Reserved	2	3	Reserved
[8]	WO	Reserved	1	0	Reserved

2.8 VCO_Reg 07h MSB Cal

Bit	Type	Name	Width	Default	Description
[3:0]	WO	Output Stage Gain Control	4	0001	0000 -> Output = 690 mV 0001 -> Output = 780 mV 0010 -> Output = 900 mV 0011 -> Output = 980 mV 0100 -> Output = 1100 mV 0101 -> Output = 1260 mV 0110 -> Output = 1400 mV 0111 -> Output = 1590 mV 1000 -> Output = 1810 mV 1001 -> Output = 1980 mV 1010 -> Output = 2250 mV 1011 -> Output = 2560 mV 1100 -> Invalid 1110 -> Invalid 1111 -> Invalid
[4]	WO	Reserved	1	1	Reserved
[6:5]	WO	Reserved	2	3	Reserved
[7]	WO	Reserved	1	1	Reserved
[8]	WO	Reserved	1	0	Reserved

Note: All Reserved bits should be programmed to default conditions

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HMC1033LP6GE Application Information

The HMC1033LP6GE features a flexible Output Frequency Range (25 MHz to 2500 MHz), industry leading phase noise and phase jitter performance, excellent noise floor (<-162 dBc/Hz), and a high level of integration. HMC1033LP6GE is ideal as a high frequency, low jitter processor clock, a clock source for high-frequency data converters or as a reference oscillator for Physical Layer Devices (PHY).

The HMC1033LP6GE can also be used as an LO for 10G/40G/100G optical modules and transponders, as a reference clock for 10G/40G/100G line cards, and for jitter attenuation and frequency translation. Synchronous Ethernet, SONET/SDH, and OTN applications often require jitter attenuation and frequency translation on the recovered line clock.

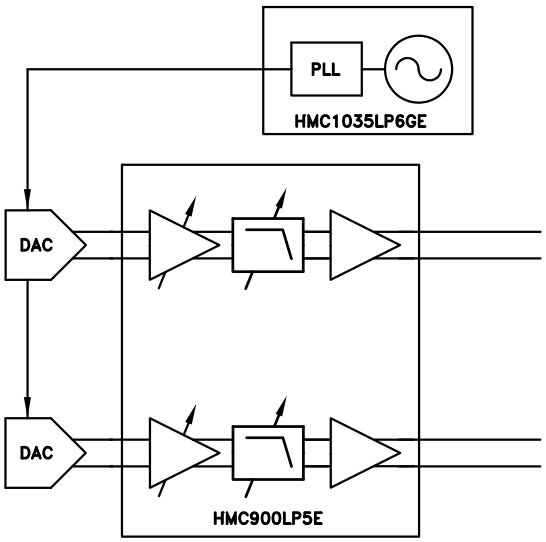

Figure 29. HMC1033LP6GE in a typical transmit chain

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HMC1033LP6GE Application Information

The HMC1033LP6GE can also be used as an LO for 10G optical modules and transponders (Figure 30), as a reference clock for 1G/10G line cards (Figure 31), and for jitter attenuation and frequency translation (Figure 32).

Synchronous Ethernet, SONET/SDH, and OTN applications often require jitter attenuation and frequency translation on the recovered line clock.

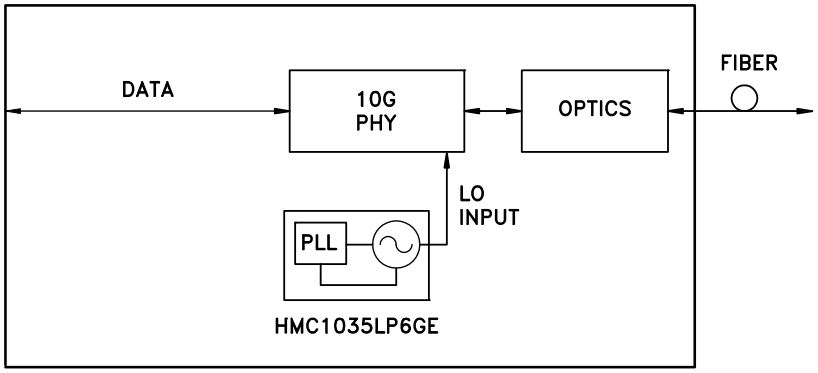

Figure 30. HMC1033LP6GE used as a local oscillator (LO) for 10G modules/transponders

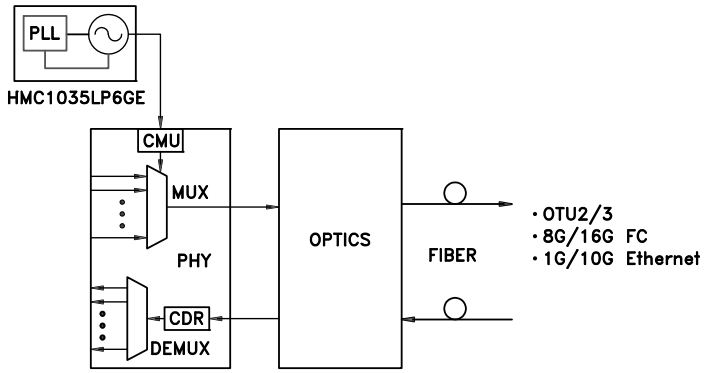

Figure 31. HMC1033LP6GE used as a reference clock for 1G/10G line cards

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HMC1033LP6GE Application Information

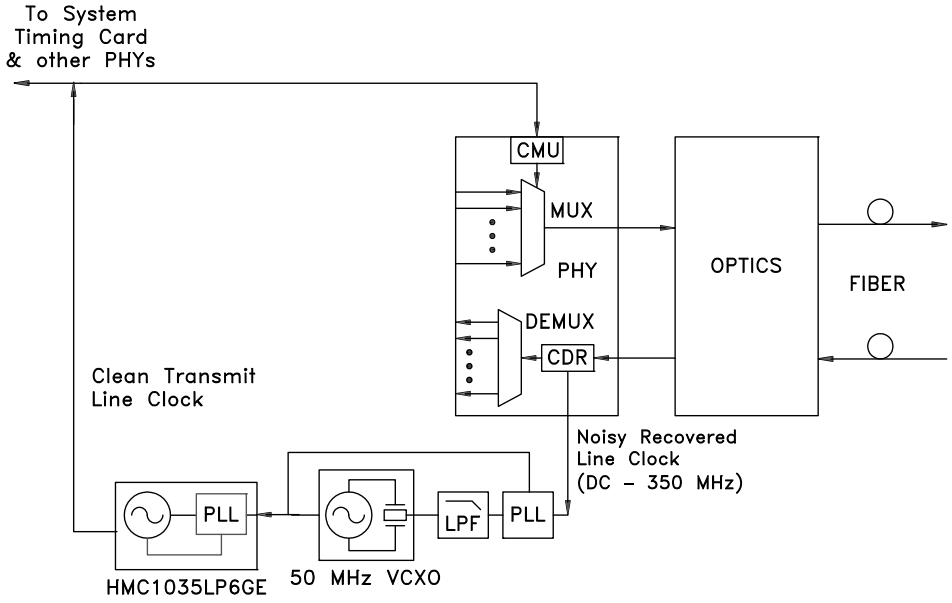

Figure 32. HMC1033LP6GE used in a jitter attenuation application for Synchronous Ethernet & Line Timing

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Line and Reference Clock Rate

OTN	Line Rates (Gbps)	Typical Reference Clock Rates (MHz)	
OTU2	10.709	669.31	167.33
OTU2e	11.095	693.44	173.36
OTU1e	11.049	690.56	172.64
OTU2f	11.317	707.31	176.83
OTU1f	11.27	704.38	176.09
OTU3	43.018	2688.63	672.16
OTU4	111.809		1747.02
OTU4v	127.156		1986.82

SONET/SDH			
STS-192/STM-64	9.95328	622.08	155.52
STS-768/STM-256	39.81312	2488.32	622.08

Ethernet			
10GE LAN	10.3125		156.25
10GE WAN	9.95328	622.08	155.52
XAUI (4 x 3.125G)	3.125		156.25
40GE (4 x 10G)	10.3125		156.25
100GE (4 x 25G)	25.78125	805.66	156.25

Fibre Channel (FC)			
10GFC	10.52		164.38
16GFC	14.025		212.5
32GFC	28.5		425

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