4-Channel High-Performance Differential Switch

Check for Samples: HD3SS3415

FEATURES

- **Compatible with Multiple Interface Standards Operating up to 12Gbps Including PCI Express Gen III and USB 3.0**
- **Wide –3dB Differential BW of over 8GHz**
- **Excellent Dynamic Characteristics (at 4GHz)**
  - **Crosstalk = –35dB**
  - **Off Isolation = –19dB**
  - **Insertion Loss = –1.5dB**
  - **Return Loss = –11dB**
- **VDD Operating Range 3.3 V ±10%**
- **Small 3.5 mm x 9.0 mm, 42-Pin TQFN Package**
- **Common Industry Standard Pinout**

APPLICATIONS

- **Desktop and Notebook PCs**
- **Server/Storage Area Networks**
- **PCI Express Backplanes**
- **Shared I/O Ports**

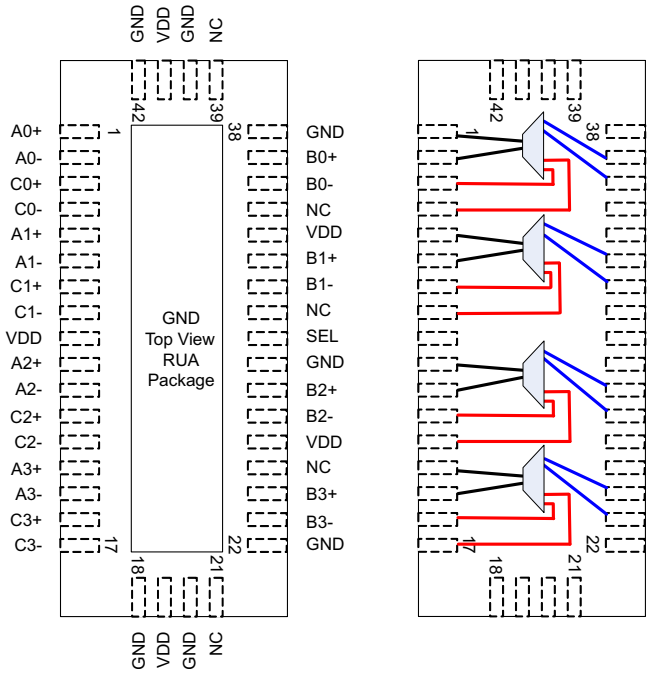


Figure 1. HD3SS3415 Pinout & Switch Flow Through Routing

DESCRIPTION

The HD3SS3415 is a high-speed passive switch capable of switching four differential channels, including applications such as two full PCI Express x1 lanes from one source to one of two target locations in a PC/server application. With its bidirectional capability the HD3SS3415 will also support applications that allow connections between one target and two source devices, such as a shared peripheral between two platforms. The HD3SS3415 has a single control line (SEL Pin) which can be used to control the signal path between Port A and either Port B or Port C.

The HD3SS3415 is offered in an industry standard 42-pin QFN package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3V over the full industrial temperature range of –40°C to 85ºC

The HD3SS3415 is a generic 4-CH high speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. Although it was designed specifically to address PCI Express Gen III applications, the HD3SS3415 will also support several other high-speed data protocols with a differential amplitude of <1800mVpp and a common mode voltage of <2.0V, as with USB 3.0 and DisplayPort 1.2. The device's one select input (SEL) pin can easily be controlled by an available GPIO pin within a system or from a micro-controller.

ORDERING INFORMATION(1)

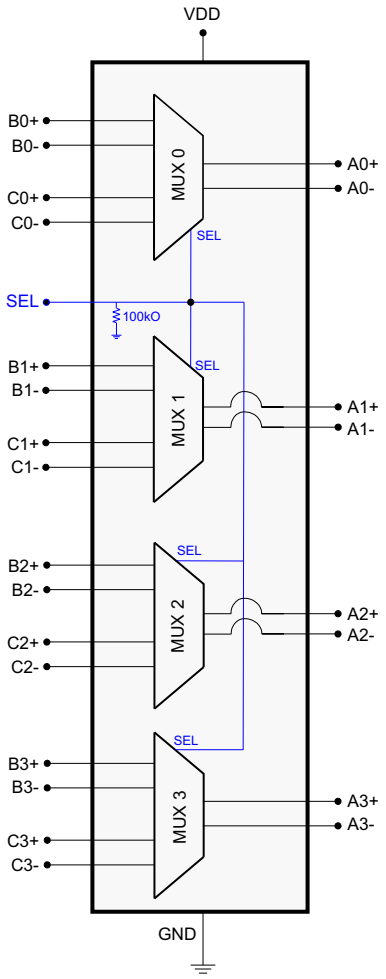
PART NUMBER	PART MARKING	PACKAGE
HD3SS3415RUAR	HD3SS3415	42-pin RUA Reel (Large)
HD3SS3415RUAT	HD3SS3415	42-pin RUA Reel (Small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com

Table 1. HD3SS3415 Control Logic

CONTROL PIN (SEL)	PORT A TO PORT B CONNECTION STATUS	PORT A TO PORT C CONNECTION STATUS
L (Default State)	Connected	Disconnected
H	Disconnected	Connected

FUNCTIONAL DIAGRAM



PIN FUNCTIONS

PIN	PIN NAME	I/O	DESCRIPTION
SWITCH PORT A			
1 2	A0+ A0–	I/O	Port A, Channel 0, High Speed Positive Signal Port A, Channel 0, High Speed Negative Signal
5 6	A1+ A1–	I/O	Port A, Channel 1, High Speed Positive Signal Port A, Channel 1, High Speed Negative Signal

PIN FUNCTIONS (continued)

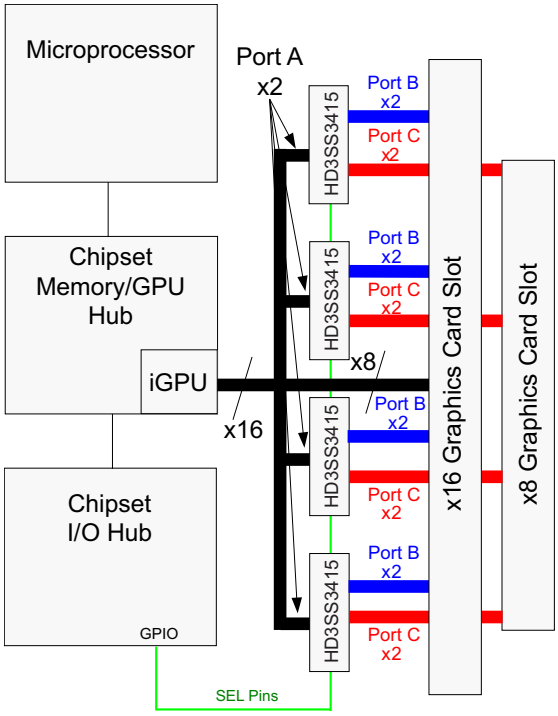
PIN	PIN NAME	I/O	DESCRIPTION
10 11	A2+ A2–	I/O	Port A, Channel 2, High Speed Positive Signal Port A, Channel 2, High Speed Negative Signal
14 15	A3+ A3–	I/O	Port A, Channel 3, High Speed Positive Signal Port A, Channel 3, High Speed Negative Signal
SWITCH PORT B			
37 36	B0+ B0–	I/O	Port B, Channel 0, High Speed Positive Signal lPort B, Channel 0, High Speed Negative Signal
33 32	B1+ B1–	I/O	Port B, Channel 1, High Speed Positive Signal Port B, Channel 1, High Speed Negative Signal
28 27	B2+ B2–	I/O	Port B, Channel 2, High Speed Positive Signal Port B, Channel 2, High Speed Negative Signal
24 23	B3+ B3–	I/O	Port B, Channel 3, High Speed Positive Signal Port B, Channel 3, High Speed Negative Signal
SWITCH PORT C			
3 4	C0+ C0–	I/O	Port C, Channel 0, High Speed Positive Signal Port C, Channel 0, High Speed Negative Signal
7 8	C1+ C1–	I/O	Port C, Channel 1, High Speed Positive Signal Port C, Channel 1, High Speed Negative Signal
12 13	C2+ C2–	I/O	Port C, Channel 2, High Speed Positive Signal Port C, Channel 2, High Speed Negative Signal
16 17	C3+ C3–	I/O	Port C, Channel 3, High Speed Positive Signal Port C, Channel 3, High Speed Negative Signal
CONTROL, SUPPLY, AND NO CONNECT			
30	SEL	I	Select between port B or port C. Internally tied to GND via 100kΩ resistor
9, 19, 26, 34, 41	VDD	Supply	Positive power supply voltage
18, 20, 22, 29, 38, 40, 42, Center Pad	GND	Supply	Negative power supply voltage
21, 25, 31, 35, 39	NC		Electrically not connected

Table 2. MUX Pin Connections(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0+	B0+	C0+
A0–	B0–	C0–
A1+	B1+	C1+
A1–	B1–	C1–
A2+	B2+	C2+
A2–	B2–	C2–
A3+	B3+	C3+
A3–	B3–	C3–

(1) The HD3SS3415 can tolerate polarity inversions for all differential signals on Ports A, B and C. Care should be taken to ensure the same polarity is maintained on Port A vs. Port B/C.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range (V_{DD})	Absolute minimum/maximum supply voltage range	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control pin (SEL)	–0.5	VDD+0.5	
Electrostatic discharge	Human body model(3)		±4,000	V
	Charged-device model(4)		±1,500	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC/ESDA JS-001-2011
(4) Tested in accordance with JEDEC JESD22 C101-E

THERMAL INFORMATION

THERMAL METRIC(1)		HD3SS3415	UNITS
		42-PIN TQFN (RUA)	
θ_{JA}	Junction-to-ambient thermal resistance	53.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	38.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	21.9	
θ_{JB}	Junction-to-board thermal resistance	27.4	
ψ_{JT}	Junction-to-top characterization parameter	5.6	
ψ_{JB}	Junction-to-board characterization parameter	27.3	
Device Power Dissipation (P_D)		15.5 (Typ) 21.6 (Max)	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

Typical values for all parameters are at V_{DD} = 3.3V and T_A = 25°C. (Temperature limits are specified by design)

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage (SEL Pin)		2.0		VDD	V
V_{IL}	Input low voltage (SEL Pin)		–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (differential pins)	Switch I/O diff voltage	0		1.8	VPP
V_{I/O_CM}	Common voltage (differential pins)	Switch I/O common mode voltage	0		2.0	V
T_A	Operating free-air temperature	Ambient temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{IH}	Input High Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = VDD			95	µA
I_{IL}	Input Low Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = GND			1	µA
I_{LK}	Leakage Current (Differential I/O pins)	V_{DD} = 3.6 V; V_{IN} = 0 V; V_{OUT} = 2 V (I_{LK} On OPEN outputs) [Ports B and C]			130	µA
		V_{DD} = 3.6 V, V_{IN} = 2 V; V_{OUT} = 0 V (I_{LK} On OPEN outputs) [Port A]			4	
I_{DD}	Supply Current	V_{DD} = 3.6 V; SEL = V_{DD}/GND; Outputs Floating		4.7	6	mA
C_{ON}	Outputs ON Capacitance	V_{IN} = 0 V; Outputs Open; Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	V_{IN} = 0 V; Outputs Open, Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V; V_{CM} = 0.5 V to 1.5 V ; I_O = –8 mA		5	8	Ω
ΔR_{ON}	On resistance match between channels	V_{DD} = 3.3 V ; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			2	Ω
	On resistance match between pairs of the same channel	V_{DD} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON(MAX)}$ – $R_{ON(MAIN)}$)	V_{DD} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V			1.15	Ω
DEVICE PARAMETERS (Continued) R_{SC} and R_{LOAD} = 50Ω and C_L = 50 pF unless otherwise noted						
t_{PD}	Switch propagation delay	Rsc and R_{LOAD} = 50Ω			85	ps
	SEL-to-switch Ton	Rsc and R_{LOAD} = 50Ω		70	250	ns
	SEL-to-switch Toff			70	250	
T_{SKEW_Inter}	Inter-pair output skew (CH-CH)	Rsc and R_{LOAD} = 50Ω			20	ps
T_{SKEW_Intra}	Intra-pair output skew (bit-bit)				8	ps
R_L	Differential return loss (VCM = 0V) Also see typical plots section	f = 0.3 MHz		–28		dB
		f = 2500 MHz		–12		
		f = 4000 MHz		–11		
X_{TALK}	Differential Crosstalk(VCM = 0V) Also see typical plots section	f = 0.3 MHz		–90		dB
		f = 2500 MHz		–39		
		f = 4000 MHz		–35		
O_{IRR}	Differential Off-Isolation(VCM = 0V) Also see typical plots section	f = 0.3 MHz		–75		dB
		f = 2500 MHz		–22		
		f = 4000 MHz		–19		
I_L	Differential Insertion Loss (VCM = 0V) Also see typical plots section	f = 0.3 MHz		–0.5		dB
		f = 2500 MHz		–1.1		
		f = 4000 MHz		–1.5		
BW	Band Width	At –3 dB		8		GHz

TEST TIMING DIAGRAMS

Select to Switch Output On (T_{ON}) and Off (T_{OFF})

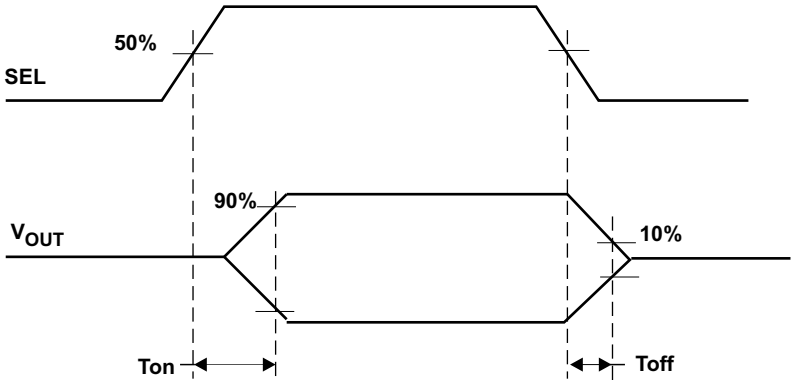
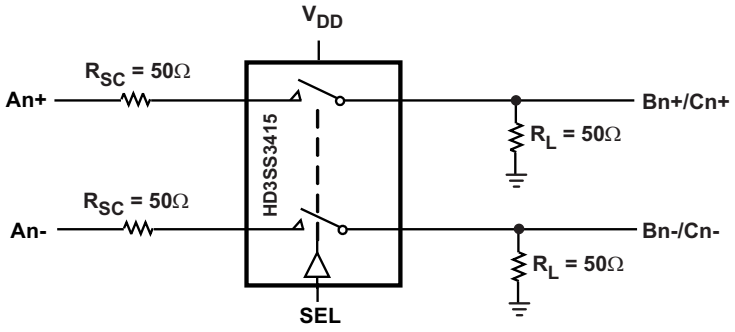
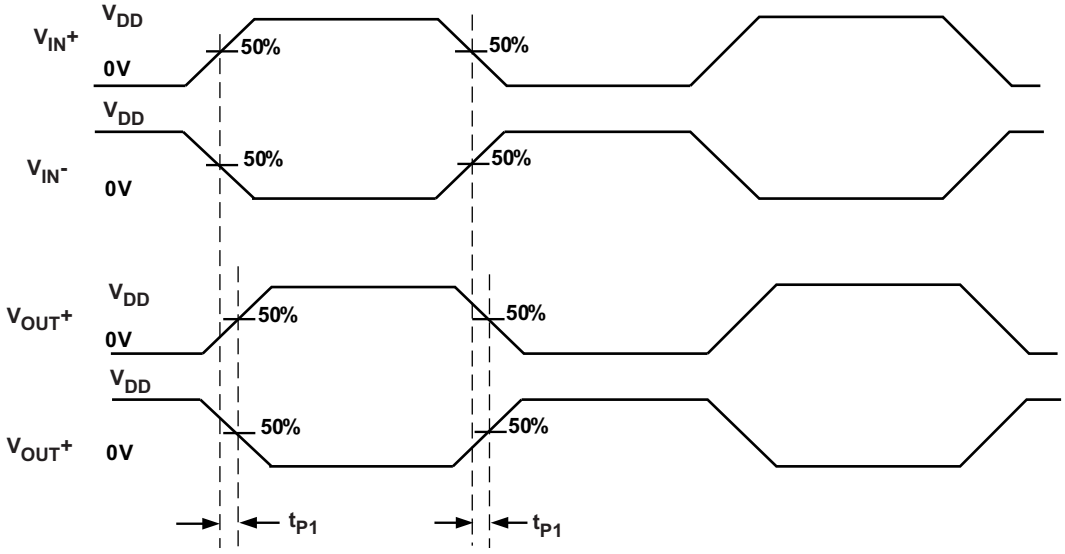


Figure 2. Switch On/Off Timing Diagram

Propagation Delay and Skew





$T_{SKEWInter}$ = Difference between t_{PD} for any two pairs of outputs

$T_{SKEWIntra}$ = Difference between t_{P1} and t_{P2} of same pair

Figure 3. Propagation Delay Timing Diagram and Test Setup

TYPICAL PERFORMANCE PLOTS

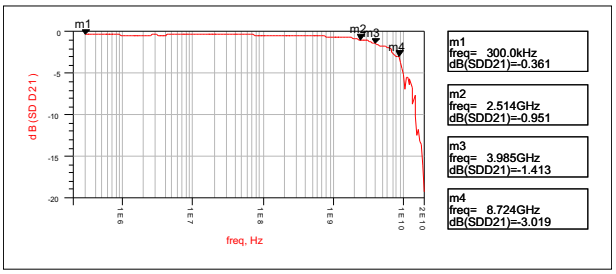


Figure 4. Differential Insertion Loss

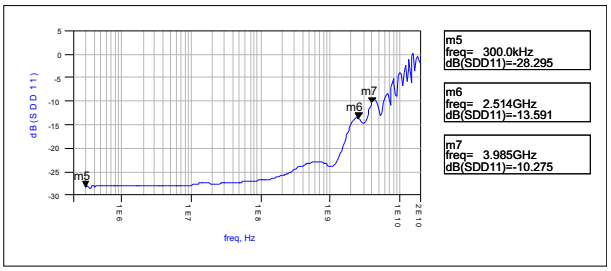


Figure 5. Differential Return Loss

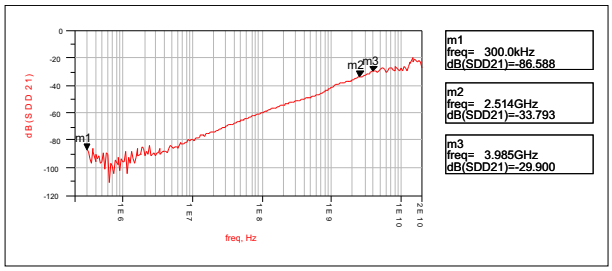


Figure 6. Differential Crosstalk

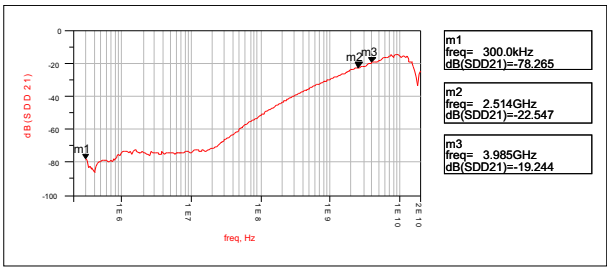


Figure 7. Differential Off Isolation

SOURCE EYE DIAGRAM

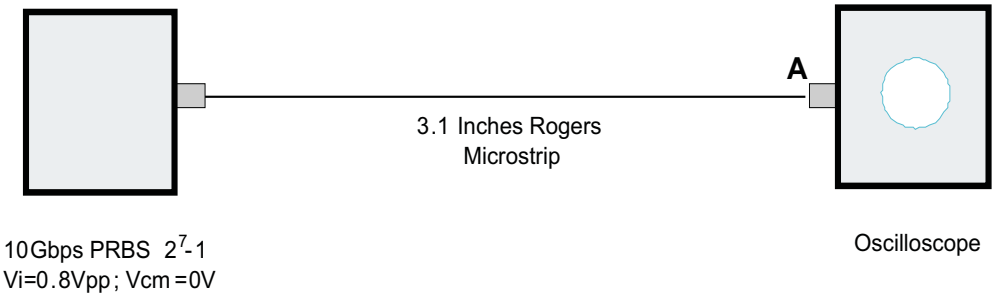


Figure 8. Source Eye Diagram Test Setup

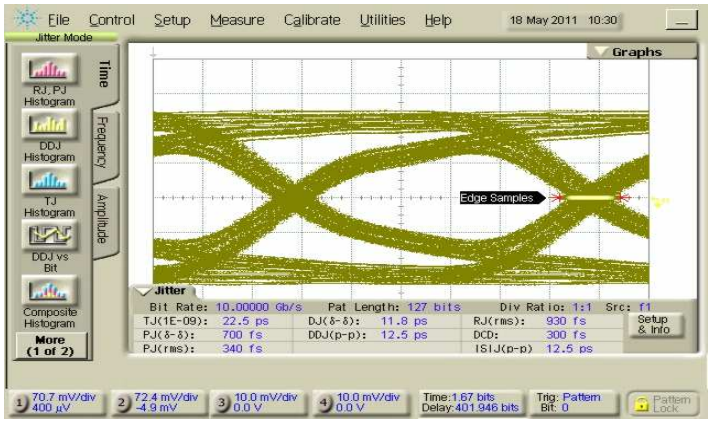


Figure 9. 10Gbps Source Eye Diagram at A: V_{ID} = 800mVpp; 2^7-1 PRBS; V_{CM}=0V

TYPICAL PERFORMANCE PLOTS (continued)

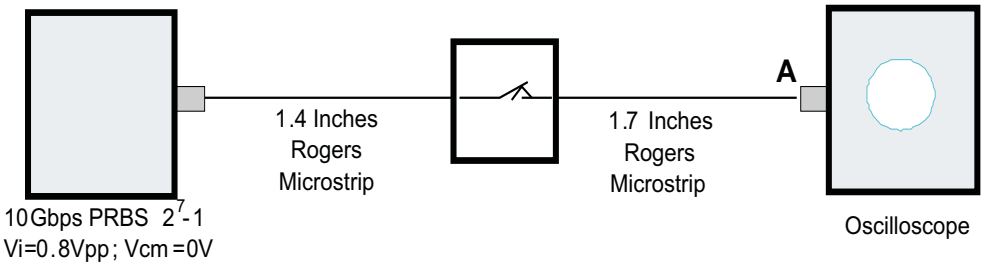


Figure 10. Output Eye Diagram Test Setup

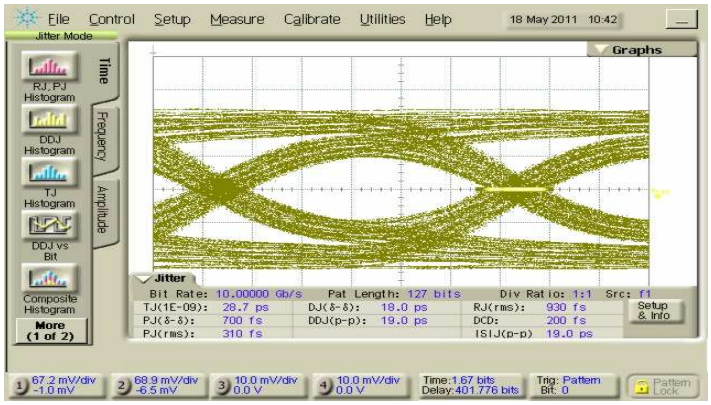
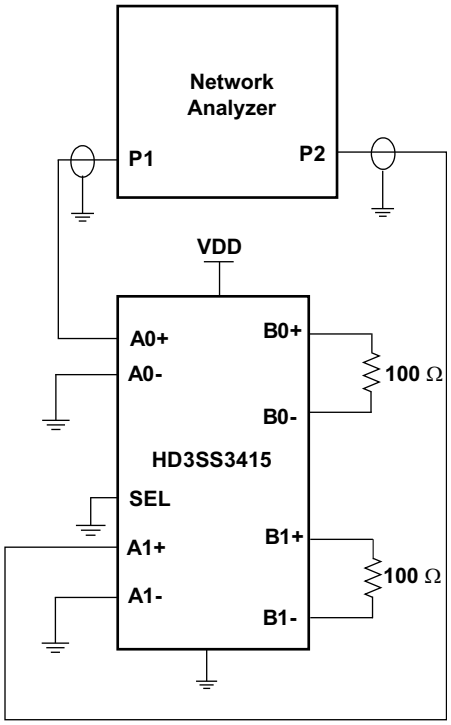


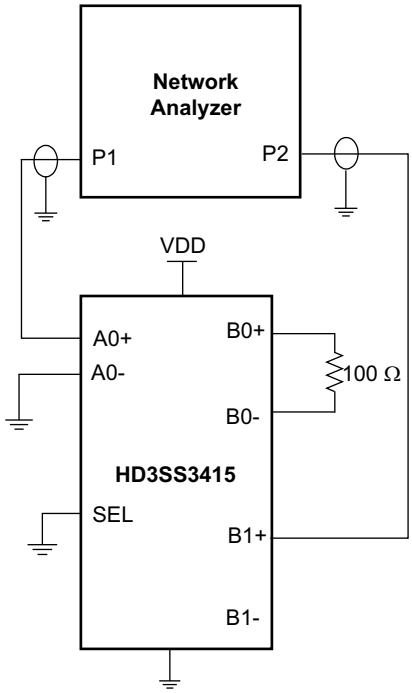
Figure 11. 10Gbps Output Eye Diagram at A: V_{ID} = 800mVpp; 2^7-1 PRBS; V_{CM}= 0V; V_{DD}= 3.3v; SEL= 0V

CROSS TALK MEASUREMENT SETUP



TYPICAL PERFORMANCE PLOTS (continued)

OFF ISOLATION MEASUREMENT SETUP



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HD3SS3415RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
HD3SS3415RUAT	ACTIVE	WQFN	RUA	42	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	

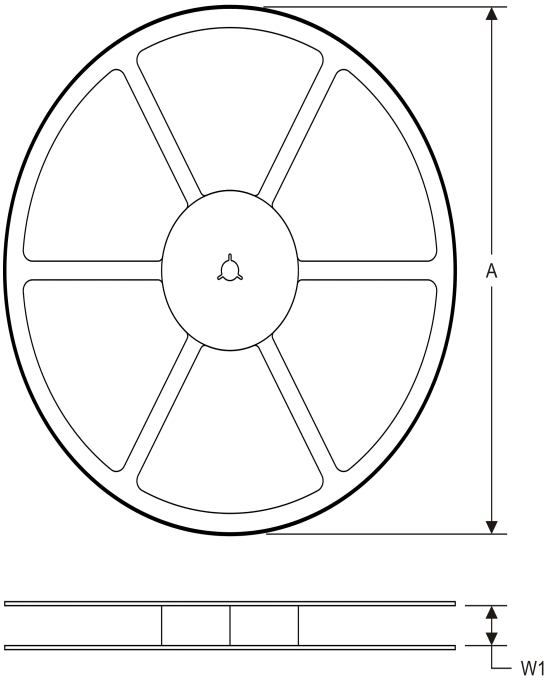
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

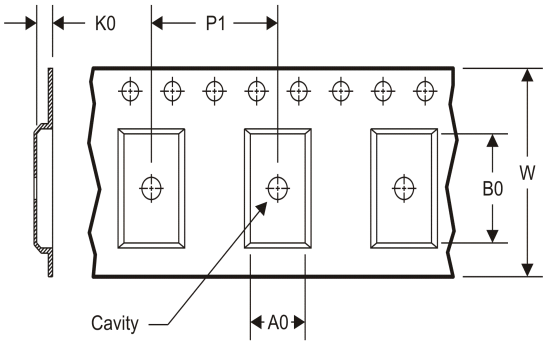
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



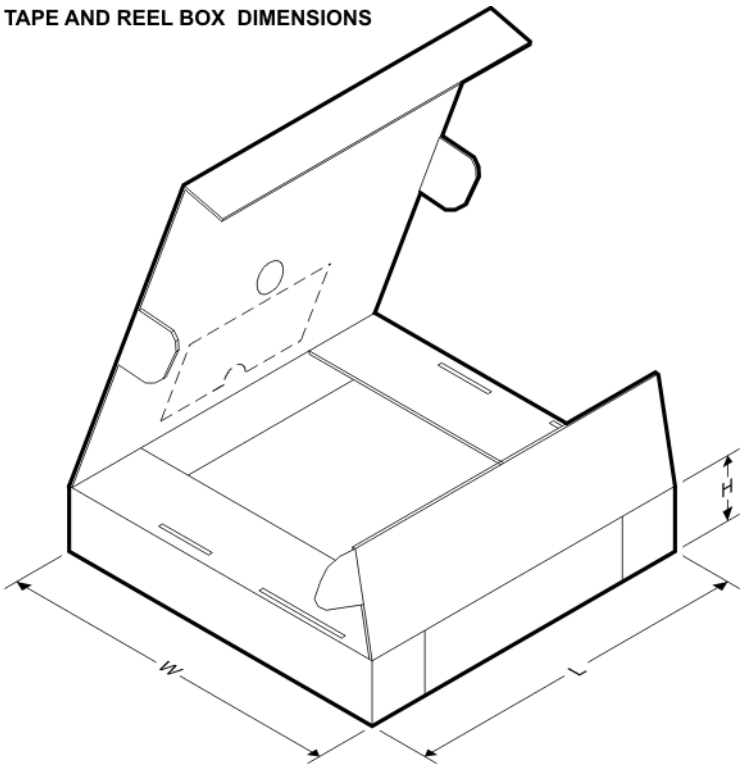
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3415RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
HD3SS3415RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

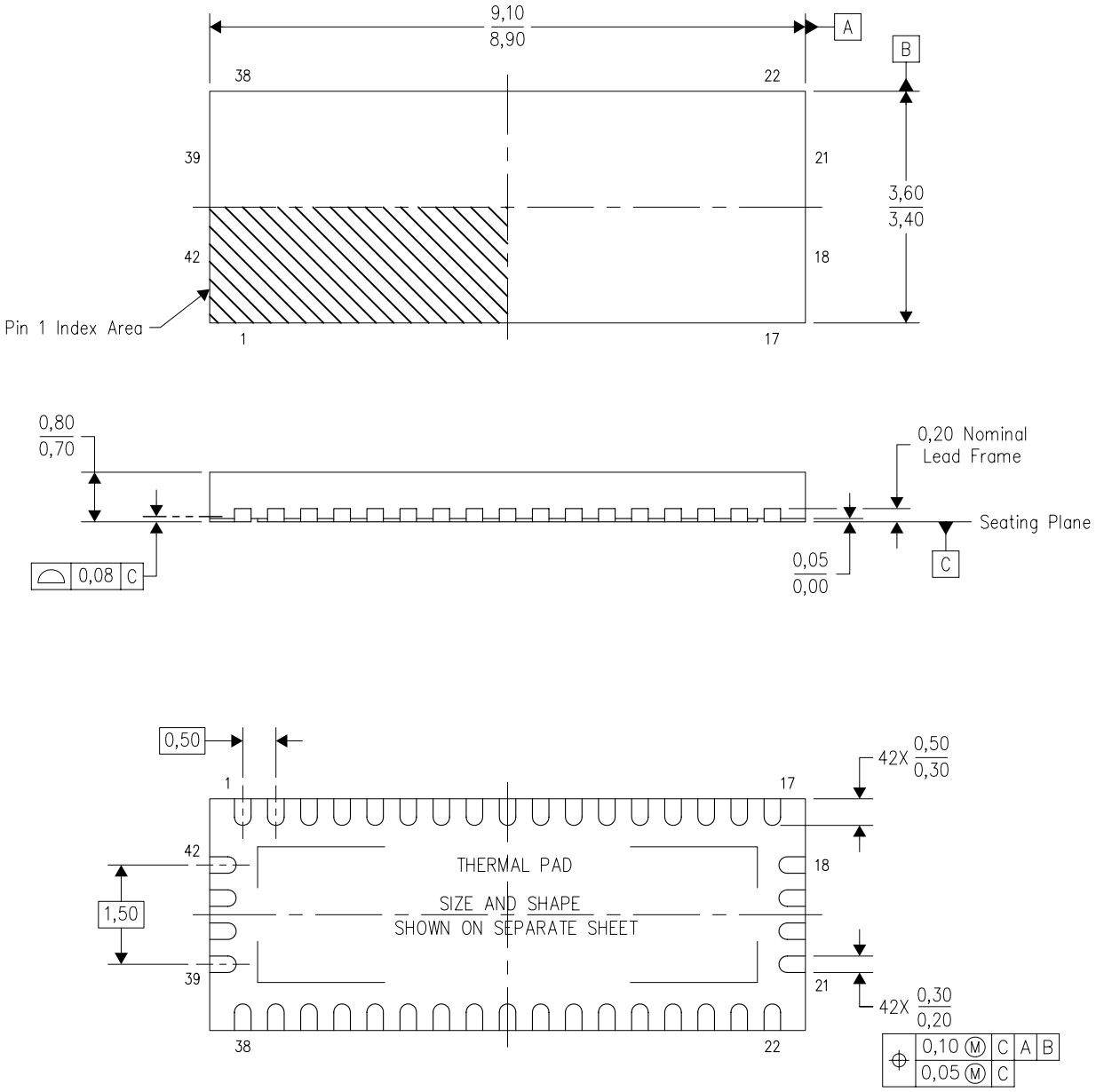
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3415RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0
HD3SS3415RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

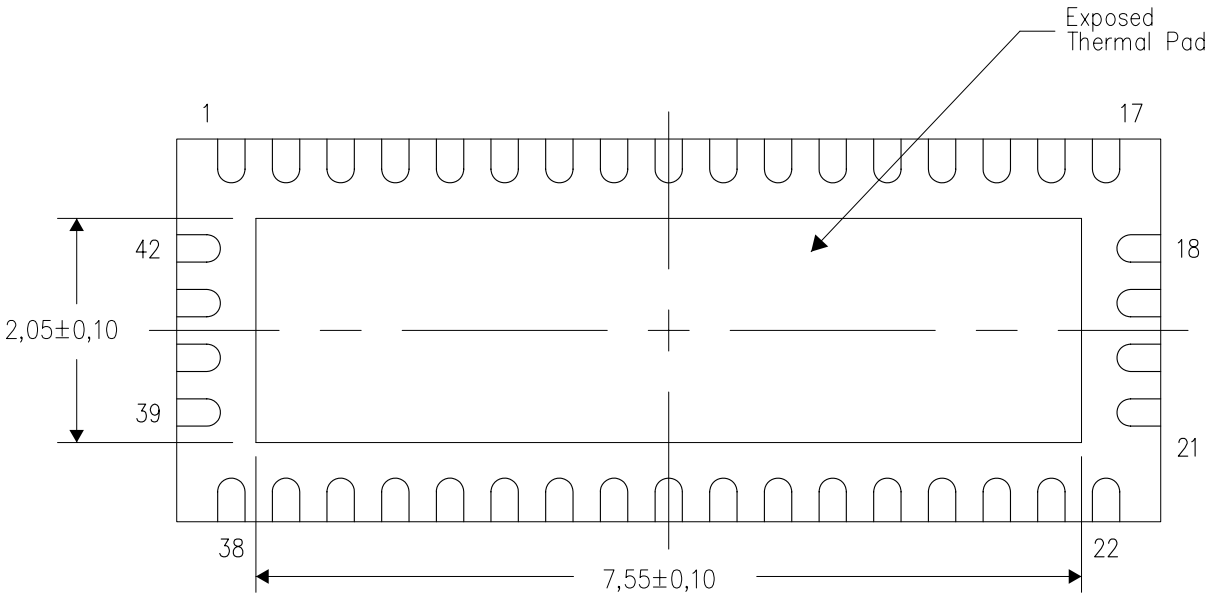
RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



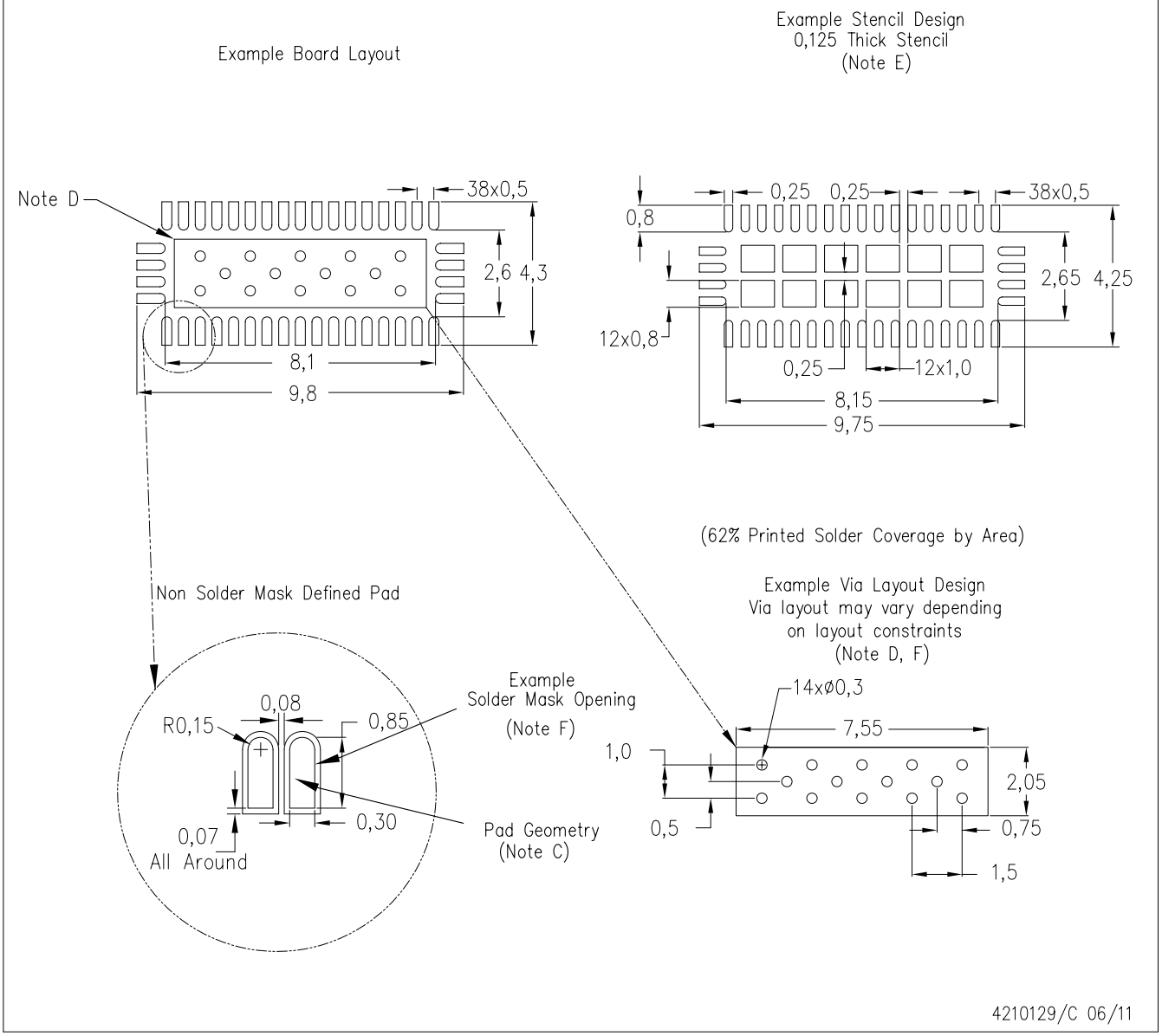
Bottom View

Exposed Thermal Pad Dimensions

4208352/D 06/11

NOTE: All linear dimensions are in millimeters

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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