HCPL-4100
Optically Coupled 20 mA Current Loop Transmitter

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-4100 optocoupler is designed to operate as a transmitter in equipment using the 20 mA current loop. 20 mA current loop systems conventionally signal a logic high state by transmitting 20 mA of loop current (MARK), and signal a logic low state by allowing no more than a few milliamperes of loop current (SPACE). Optical coupling of the signal from the logic input to the 20 mA current loop breaks ground loops and provides very high immunity to common mode interference.

The HCPL-4100 data input is compatible with LSTTL, TTL, or CMOS logic gates. The input integrated circuit drives a GaAsP LED. The light emitted by the LED is sensed by a second integrated circuit that allows 20 mA to pass with a voltage drop of less than 2.7 volts when no light is emitted and allows less than 2 mA to pass when light is emitted. The transmitter output is capable of withstanding 27 volts. The input integrated circuit provides a controlled amount of LED drive current and takes into account any LED light output degradation. The internal shield allows a guaranteed 1000 V/µs common mode transient immunity.

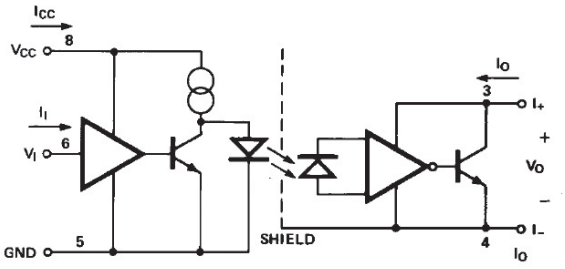
Features

- Guaranteed 20 mA loop parameters
- Data input compatible with LSTTL, TTL and CMOS Logic
- Internal shield for High Common Mode rejection
- 20 kBaud data rate at 400 metres line length
- Guaranteed On and Off output current levels
- Safety approval
  UL Recognized -3750 V rms for 1 minute
  CSA Approved
- Optically coupled 20 mA current loop receiver, HCPL-4200, also available

Applications

- Isolated 20 mA current loop transmitter in:
  Computer peripherals
  Industrial control equipment
  Data communications equipment

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)*

V_I	V_{CC}	I_O
H	ON	H
L	ON	L
H	OFF	H
L	OFF	H

*CURRENT LOOP CONVENTION —
H = MARK: $I_O \geq 12$ mA,
L = SPACE: $I_O \leq 2$ mA.

A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

HCPL-4100 is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part number	Option: RoHS Compliant	Option: Non-RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	Quantity
HCPL-4100	-000E	No option	300 mil DIP-8				50 per tube
	-300E	#300		X	X		50 per tube
	-500E	#500		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-4100-500E to order product of Gull Wing Surface Mount package in Tape and Reel packaging in RoHS compliant.

Example 2:

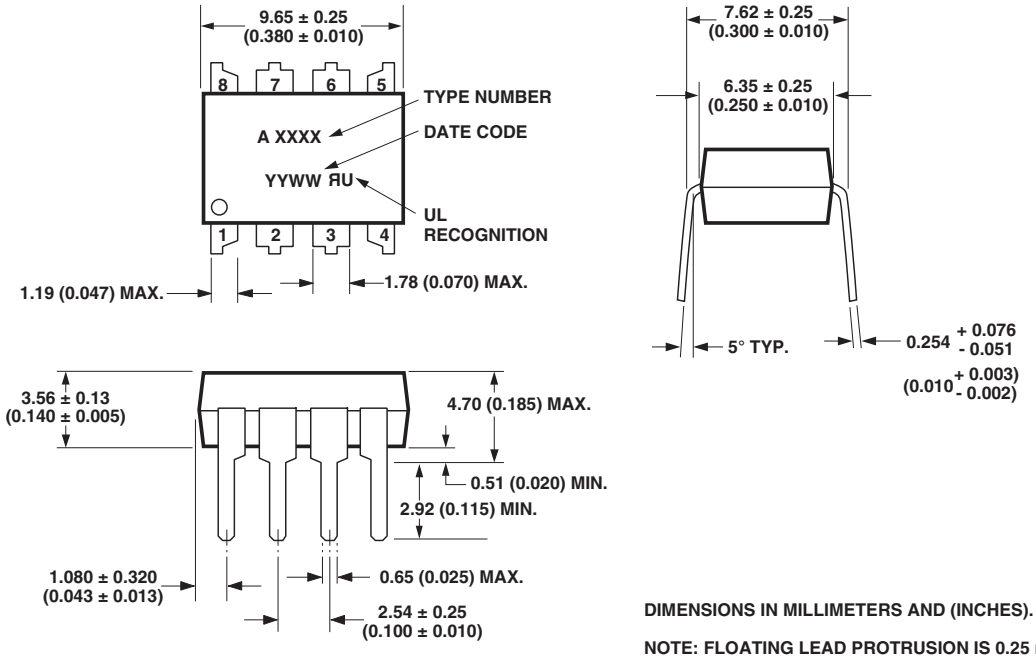
HCPL-4100 to order product of 300 mil DIP package in tube packaging and non-RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

Package Outline Drawings

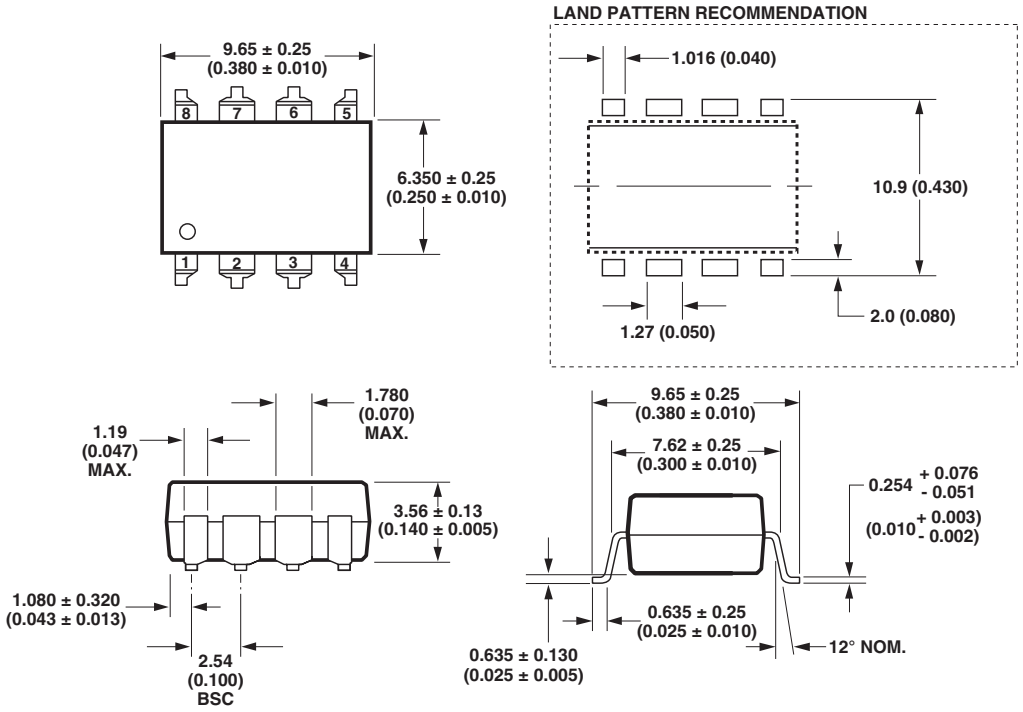
8-Pin DIP Package (HCPL-4100)



DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

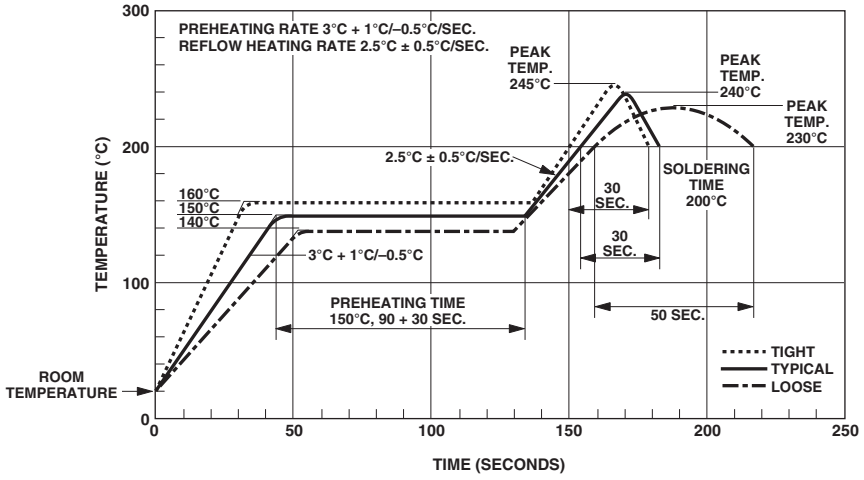
8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4100)



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

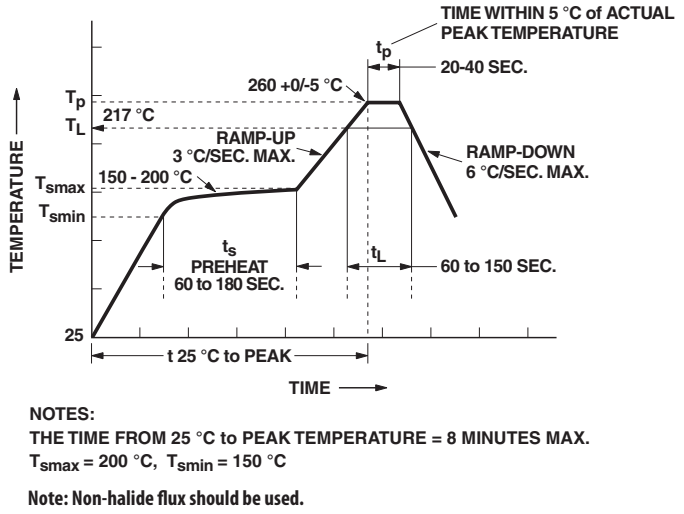
Solder Reflow Thermal Profile



Note: Non-halide flux should be used.

Figure 1. Solder Reflow Thermal Profile.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Figure 2. Pb-Free IR Profile.

Regulatory Information

The HCPL-4100 has been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	Volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

(No Derating Required up to 55°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s (1.6 mm below seating plane)
Supply Voltage – V_{CC} ..... 0 V to 20 V
Average Output Current - I_O ..... -30 mA to 30 mA
Peak Output Current - I_O ..... Internally Limited
Output Voltage – V_O ..... -0.4 V to 27 V
Input Voltage – V_I ..... -0.5 V to 20 V
Input Power Dissipation – P_I ..... 265 mW[1]
Output Power Dissipation – P_O ..... 125 mW[2]
Total Power Dissipation – P ..... 360 mW[3]
Infrared and Vapor Phase Reflow Temperature
(Option #300) ..... see Fig. 1, Thermal Profile

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Voltage Low	V_{IL}	0	0.8	Volts
Input Voltage High	V_{IH}	2.0	20	Volts
Operating Temperature	T_A	0	70	°C
Output Voltage	V_O	0	27	Volts
Output Current	I_O	0	24	mA

DC Electrical Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 12.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Mark State Output Voltage	V_{MO}		1.8	2.25	Volts	I_O = 2 mA, V_I = 2.0 V	2, 3	
			2.2		Volts	I_O = 12 mA, V_I = 2.0 V		
			2.35	2.7	Volts	I_O = 20 mA, V_I = 2.0 V		
Mark State Short Circuit Output Current	I_{SC}	30	85		mA	V_I = 2 V, V_O = 5 V to 27 V	4	
Space State Input Current	I_{SO}	0.5	1.1	2.0	mA	V_I = 0.8 V, V_O = 27 V	4	
Low Level Input Current	I_{IL}		-0.12	-0.32	mA	V_{CC} = 20 V, V_I = 0.4 V		
Low Level Input Voltage	V_{IL}			0.8	Volts			
High Level Input Voltage	V_{IH}	2.0			Volts			
High Level Input Current	I_{IH}			20	µA	V_I = 2.7 V		
				100	µA	V_I = 5.5 V		
			0.005	250	µA	V_I = 20 V		
Supply Current	I_{CC}		7.0	11.5	mA	V_{CC} = 5.5 V, 0 V ≤ V_I ≤ 20 V		
			7.8	13	mA	V_{CC} = 20 V , 0 V ≤ V_I ≤ 20 V		

Switching Specifications

For 0°C ≤ T_A ≤ 70°C, 4.5 V ≤ V_{CC} ≤ 20 V, all typicals at T_A = 25°C and V_{CC} = 5 V unless otherwise noted. See note 12.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic High Output Level	t_{PLH}		0.3	1.6	µs	C_O = 1000 pF, C_L = 15 pF, I_O = 20 mA	5, 6, 7	6
Propagation Delay Time to Logic Low Output Level	t_{PHL}		0.2	1.0	µs	C_O = 1000 pF, C_L = 15 pF, I_O = 20 mA	5, 6, 7	7
Propagation Delay Time Skew	$t_{PLH} - t_{PHL}$		0.1		µs	I_O = 20 mA		
Output Rise Time (10-90%)	t_r		16		ns	I_O = 20 mA, C_O = 1000 pF, C_L = 15 pF	6, 8	8
Output Fall Time (90-10%)	t_f		23		ns	I_O = 20 mA, C_O = 1000 pF, C_L = 15 pF	6, 8	9
Common Mode Transient Immunity at Logic High Output Level	$\|CM_H\|$	1,000	10,000		V/µs	V_I = 2 V, T_A = 25°C V_{CM} = 50 V (peak), V_{CC} = 5 V I_O (min.) = 12 mA	9, 10	10
Common Mode Transient Immunity at Logic Low Output Level	$\|CM_L\|$	1,000	10,000		V/µs	V_I = 0.8 V, T_A = 25°C V_{CM} = 50 V (peak), V_{CC} = 5 V I_O (max.) = 3 mA	9, 10	11

Package Characteristics

For 0°C ≤ T_A ≤ 70°C, unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		5, 13
Resistance, Input-Output	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 V dc		5
Capacitance, Input-Output	C_{I-O}		1		pF	f = 1 MHz, V_{I-O} = 0 V dc		5

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification, or Avago Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 55°C free air temperature at a rate of 3.8 mW/°C. Proper application of the derating factors will prevent IC junction temperatures from exceeding 125°C for ambient temperatures up to 85°C.
2. Derate linearly above a free-air temperature of 70°C at a rate of 2.3 mW/°C. A significant amount of power may be dissipated in the HCPL-4100 output circuit during the transition from the SPACE state to the MARK state when driving a data line or capacitive load (C_{OUT}). The average power dissipation during the transition can be estimated from the following equation which assumes a linear discharge of a capacitive load: $P = I_{SC} (V_{SO} + V_{MO})/2$, where V_{SO} is the output voltage in the SPACE state. The duration of this transition can be estimated as $t = C_{OUT} (V_{SO} - V_{MO})/I_{SC}$. For typical applications driving twisted pair data lines with NRZ data as shown in Figure 12, the transition time will be less than 10% of one bit time.
3. Derate linearly above 55°C free-air temperature at a rate of 5.1 mW/°C.
4. The maximum current that will flow into the output in the mark state (I_{SC}) is internally limited to protect the device. The duration of the output short circuit shall not exceed 10 ms.
5. The device is considered a two terminal device, pins 1, 2, 3, and 4 are connected together, and pins 5, 6, 7, and 8 are connected together.
6. The t_{PLH} propagation delay is measured from the 1.3 volt level on the leading edge of the input pulse to the 10 mA level on the leading edge of the output pulse.
7. The t_{PHL} propagation delay is measured from the 1.3 volt level on the trailing edge of the input pulse to the 10 mA level on the trailing edge of the output pulse.
8. The rise time, t_r, is measured from the 10% to the 90% level on the rising edge of the output current pulse.
9. The fall time, t_f, is measured from the 90% to the 10% level on the falling edge of the output current pulse.
10. Common mode transient immunity in the logic high level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Mark ("H") state (i.e., $I_O > 12$ mA).
11. Common mode transient immunity in the logic low level is the maximum (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, that can be sustained with the output in a Space ("L") state (i.e., $I_O < 3$ mA).
12. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is momentary withstand proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ µA).

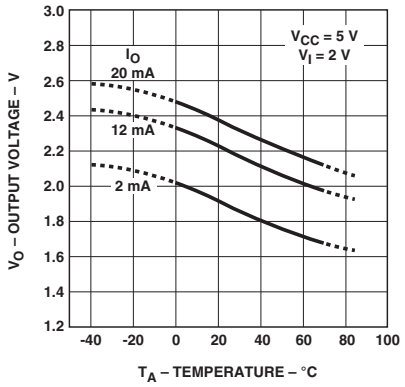


Figure 3. Typical Mark State Output Voltage vs. Temperature.

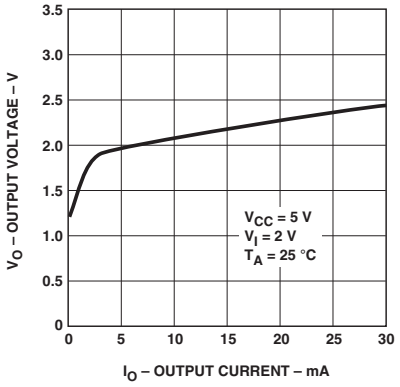


Figure 4. Typical Output Voltage vs. Loop Current.

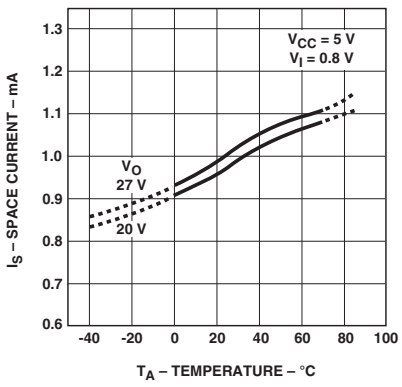


Figure 5. Typical Space State Output Current vs. Temperature.

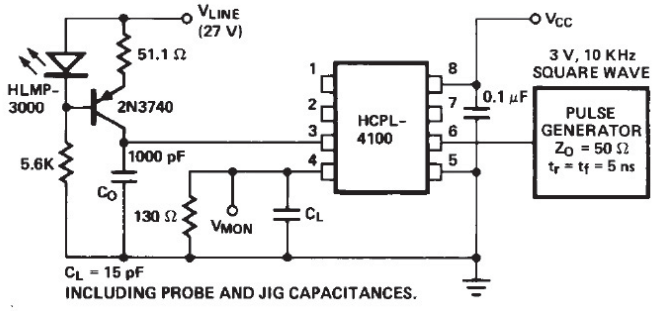


Figure 6. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

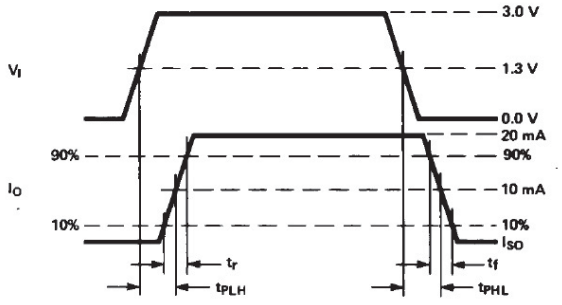


Figure 7. Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f.

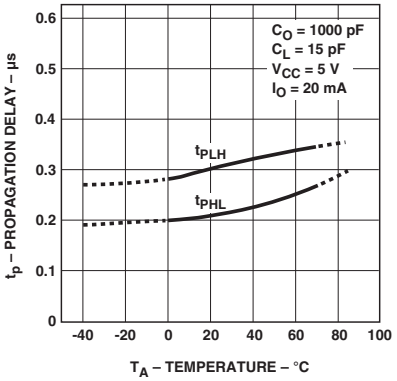


Figure 8. Typical Propagation Delay vs. Temperature.

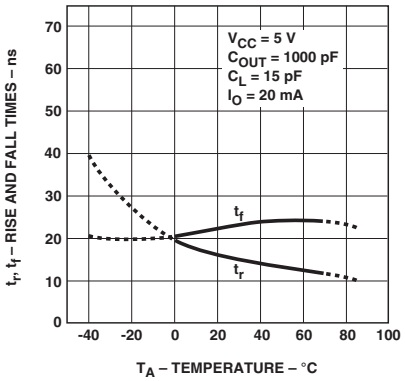


Figure 9. Typical Rise, Fall Times vs. Temperature.

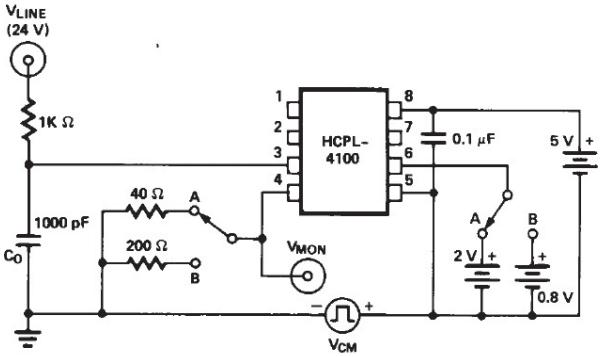


Figure 10. Test Circuit for Common Mode Transient Immunity.

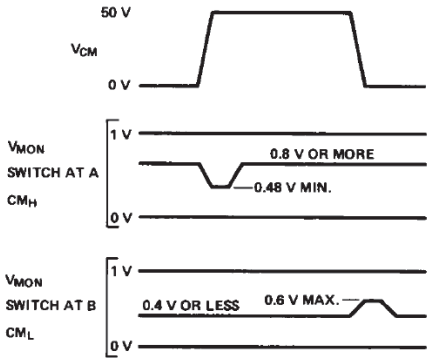


Figure 11. Typical Waveforms for Common Mode Transient Immunity.

Applications

Data transfer between equipment which employs current loop circuits can be accomplished via one of three configurations: simplex, half duplex or full duplex communication. With these configurations, point-to-point and multidrop arrangements are possible. The appropriate configuration to use depends upon data rate, number of stations, number and length of lines, direction of data flow, protocol, current source location and voltage compliance value, etc.

Simplex

The simplex configuration, whether point to point or multidrop, gives unidirectional data flow from transmitter to transmitter(s). This is the simplest configuration for use in long line length (two wire), moderate data rate, and low current source compliance level applications. A block diagram of simplex point to point arrangement is given in Figure 12 for the HCPL-4100 transmitter optocoupler.

Major factors which limit maximum data rate performance for a simplex loop are the location and compliance voltage of the loop current source as well as the total line capacitance. Application of the HCPL-4100 transmitter in a simplex loop necessitates thtat a non-isolated active receiver (containing current source) be used at the opposite end of the current loop. With long line length, large line capacitance will need to be charged to the compliance voltage level of the current source before the receiver loop current decreases to zero. This effect limits upper data rate performance. Slower data rates will occur with larger compliance voltage levels. The maximum compliance level is determined by the transmitter breakdown characteristic. In addition, adequate compliance of the current source must be available for voltage drops across station(s) during the MARK state in multidrop applications for long line lengths.

In a simplex multidrop application with multiple HCPL-4100 transmitters and one non-isolated active receiver, priority of transmitters must be established.

A recommended non-isolated active receiver circuit which can be used with the HCPL-4100 in point-to-point or in multidrop 20 mA current loop applications is given in Figure 13. This non-isolated active receiver current threshold must be chosen properly in order to provide adequate noise immunity as well as not to detect SPACE state current (bias current) of the HCPL-4100 transmitter. The receiver input threshold current is Vth/Rth ≈ 10 mA. A simple transistor current source provides a nominal 20 mA loop current over a V_{CC} compliance range of 6 V dc to 27 V dc. A resistor can be used in place of the constant current source for simple applications where the wire loop distance and number of stations on the loop are fixed. A minimum transmitter output load capacitance of 1000 pF is required between pins 3 and 4 to ensure absolute stability.

Length of current loop (one direction) versus minimum required DC supply voltage, V_{CC}, of the circuit in Figure 13 is graphically illustrated in Figure 14. Multidrop configurations will require larger V_{CC} than Figure 14 predicts in order to account for additional station terminal voltage drops.

Typical data rate performance versus distance is illustrated in Figure 15 for the combination of a non-isolated active receiver and HCPL-4100 optically coupled current loop transmitter shown in Figure 13. Curves are shown for

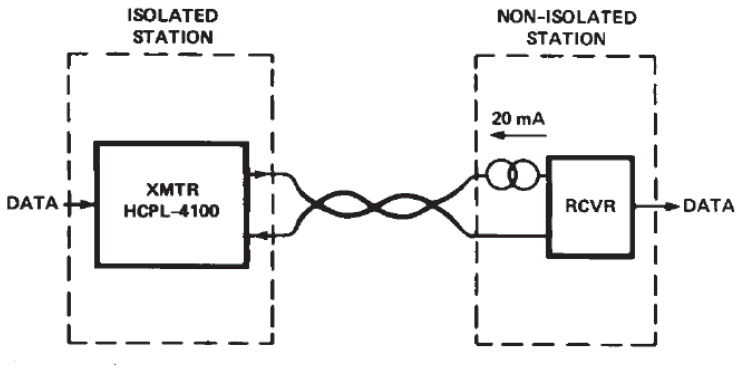


Figure 12. Simplex Point to Point Current Loop System Configuration.

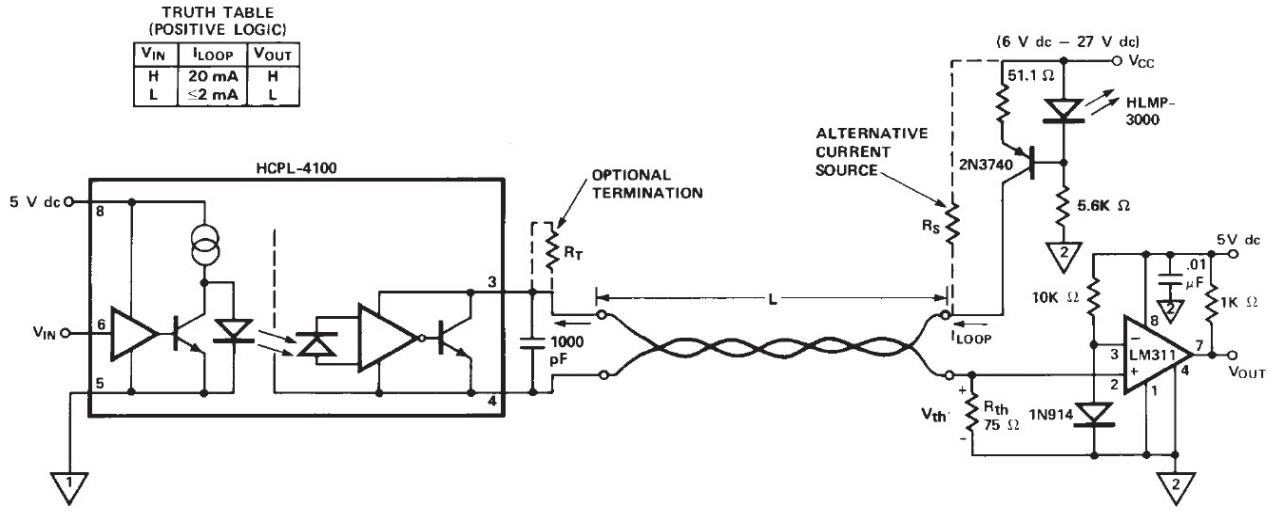


Figure 13. Recommended Non-Isolated Active Receiver with HCPL-4100 Isolated Transmitter for Simplex Point to Point 20 mA Current Loop.

25% distortion data rate at different V_{CC} values. 25% distortion data rate is defined as that rate at which 25% distortion occurs to output bit interval with respect to the input bit interval. Maximum data rate (dotted line) is restricted by device characteristics. An input Non-Return-to-Zero (NRZ) test waveform of 16 bits (0000001011111101) was used for data rate distortion measurements. Enhanced speed performance of the loop system can be obtained with lower V_{CC} supply levels, as illustrated in Figure 15. In addition, when loop current is supplied through a resistor instead of by a current source, an additional series termination resistance equal to the characteristic line impedance can be used at the HCPL-4100 transmitter end to enhance speed of response by approximately 20%.

The cable used contained five pairs of unshielded, twisted, 22 AWG wire (Dearborn #862205). Loop current is 20 mA nominal. Input and output logic supply voltages are 5 V dc.

Full Duplex

The full duplex point-to-point communication of Figure 16 uses a four wire system to provide simultaneous, bidirectional data communication between local and remote equipment. The basic application uses two simplex point-to-point loops which have two separate, active, non-isolated units at one common end of the loops. The other end of each loop is isolated.

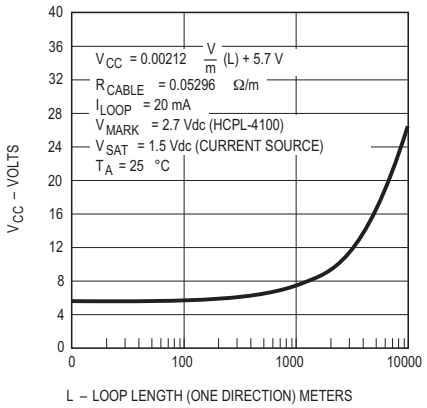


Figure 14. Minimum Required Supply Voltage, V_{CC}, vs. Loop Length for Current Loop Circuit of Figure 13.

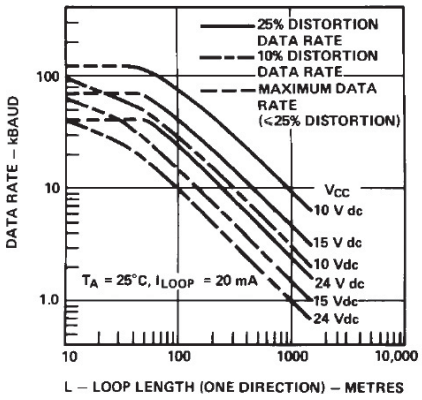


Figure 15. Typical Data Rate vs. Distance and Supply Voltage.

As Figure 16 illustrates, the combination of Avago current loop optocouplers, HCPL-4100 transmitter and HCPL-4200 receiver, can be used at the isolated end of current loops. Cross talk and common mode coupling are greatly reduced when optical isolation is implemented at the same end of both loops, as shown. Full duplex data rate is limited by the non-isolated active transmitter current loop. Comments mentioned under simplex configuration apply to the full duplex case. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

Half Duplex

The half duplex configuration, whether point to point or multidrop, gives non-simultaneous bidirectional data flow from transmitters to transmitters shown in Figures 17a and 17b. This configuration allows the use of two wires to carry data back and forth between local and remote units. However, protocol must be used to determine which specific transmitter can operate at any given time. Maximum data rate for a half duplex system is limited by the loop current charging time. These considerations were explained in the Simplex configuration section.

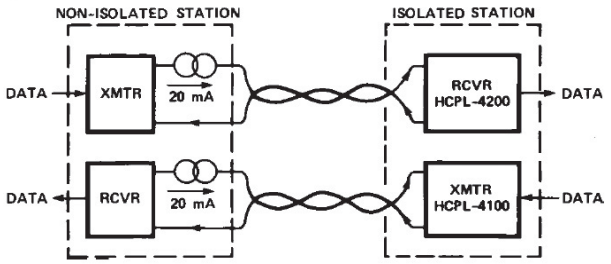


Figure 16. Full Duplex Point to Point Current Loop System Configuration.

Figures 17a and 17b illustrate half duplex application for the combination of HCPL-4100/-4200 optocouplers. The unique and complementary designs of the HCPL-4100 transmitter and HCPL-4200 receiver optocouplers provide many designed-in benefits. For example, total optical isolation at one end of the current loop is easily accomplished, which results in substantial removal of common mode influences, elimination of ground potential differences and reduction of power supply requirements. With this combination of HCPL-4100/-4200 optocouplers, specific current loop noise immunity is provided, i.e., minimum SPACE state current noise immunity is 1 mA, MARK state noise immunity is 8 mA.

Voltage compliance of the current source must be of an adequate level for operating all units in the loop while not exceeding 27 V dc, the maximum breakdown voltage for the HCPL-4100. Note that the HCPL-4100 transmitter will allow output loop current to conduct when input V_{CC} power is off. Consult the HCPL-4200 receiver optocoupler data sheet for specified device performance.

For more information about the HCPL-4100/-4200 optocouplers, consult Application Note 1018.

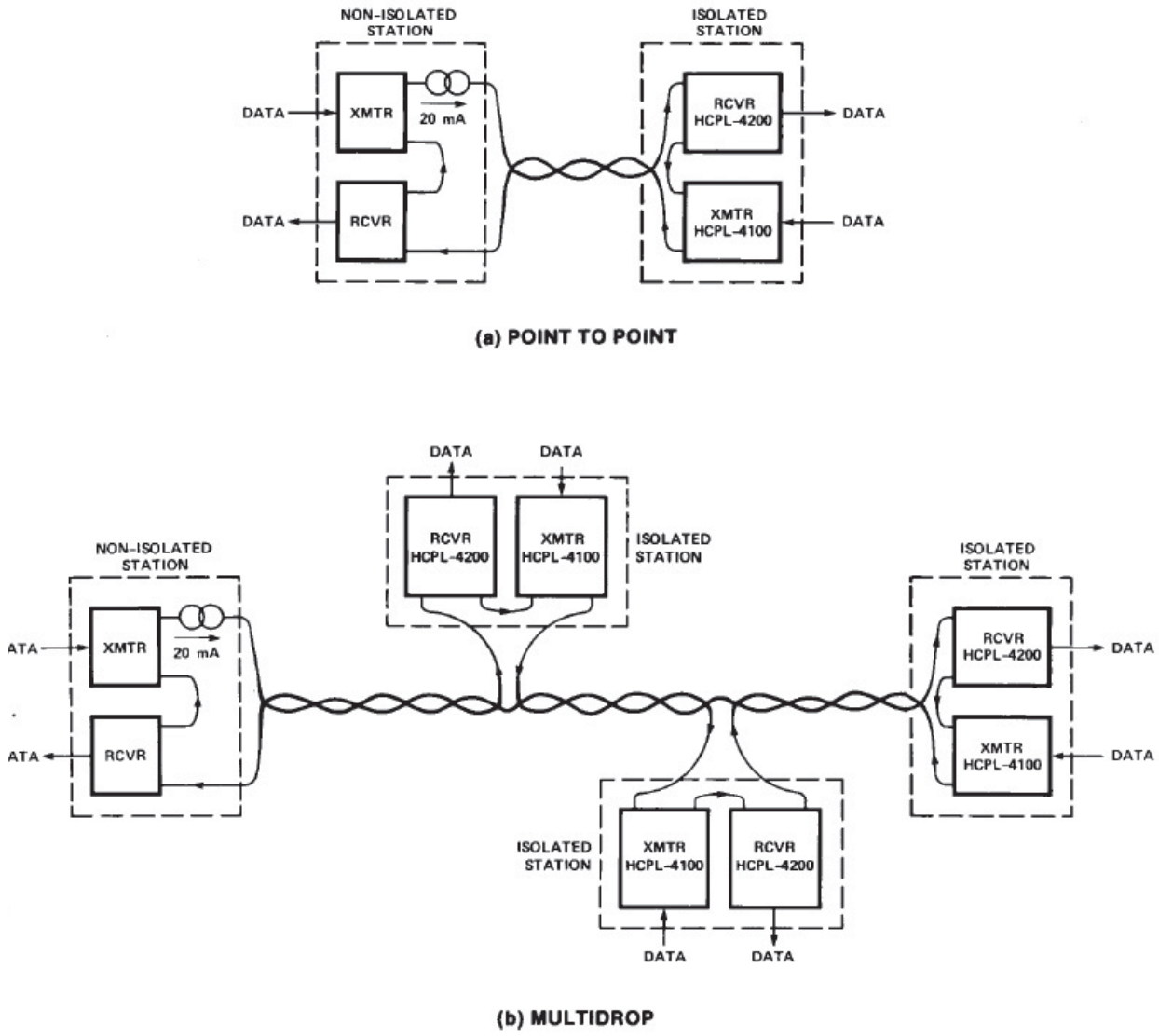


Figure 17. Half Duplex Current Loop System Configurations for (a) Point to Point, (b) Multidrop.