

FGD3040G2-F085C FGB3040G2-F085C

EcoSPARK[®] 2 Ignition IGBT 300 mJ, 400 V, N-Channel Ignition IGBT

Features

- SCIS Energy = 300 mJ at $T_J = 25^\circ\text{C}$
- Logic Level Gate Drive
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Application

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage ($I_C = 1\text{ mA}$)	400	V
BV_{ECS}	Emitter to Collector Voltage – Reverse Battery Condition ($I_C = 10\text{ mA}$)	28	V
$ESCIS_{25}$	ISCIS = 14.2 A, L = 3.0 mHy, RGE = 1 K Ω , $T_C = 25^\circ\text{C}$ (Note 1)	300	mJ
$ESCIS_{150}$	ISCIS = 10.8 A, L = 3.0 mHy, RGE = 1 K Ω , $T_C = 150^\circ\text{C}$ (Note 2)	170	mJ
IC_{25}	Collector Current Continuous at $V_{GE} = 5.0\text{ V}$, $T_C = 25^\circ\text{C}$	41	A
IC_{110}	Collector Current Continuous at $V_{GE} = 5.0\text{ V}$, $T_C = 110^\circ\text{C}$	25.6	A
V_{GEM}	Gate to Emitter Voltage Continuous	± 10	V
PD	Power Dissipation Total, $T_C = 25^\circ\text{C}$	150	W
	Power Dissipation Derating, $T_C > 25^\circ\text{C}$	1	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	300	$^\circ\text{C}$
T_{PKG}	Reflow Soldering according to JESD020C	260	$^\circ\text{C}$
ESD	HBM–Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV
	CDM–Electrostatic Discharge Voltage at 1 Ω	2	kV

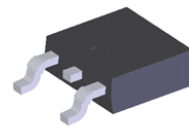
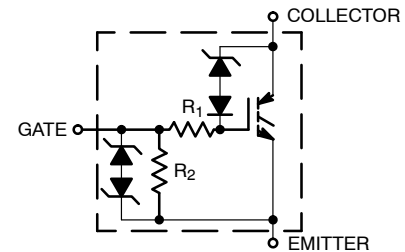
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self clamped inductive Switching Energy ($ESCIS_{25}$) of 300 mJ is based on the test conditions that is starting $T_J = 25^\circ\text{C}$, L = 3 mHy, ISCIS = 14.2 A, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.
2. Self Clamped inductive Switching Energy ($ESCIS_{150}$) of 170 mJ is based on the test conditions that is starting $T_J = 150^\circ\text{C}$, L = 3mHy, ISCIS = 10.8 A, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.

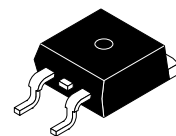


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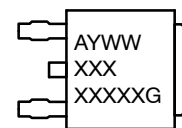


DPAK3
CASE 369AS



D²PAK-3
CASE 418AJ

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- XXXX = Device Code
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FGD3040G2-F085C

THERMAL RESISTANCE RATINGS

Characteristic	Symbol	Max	Units
Junction-to-Case – Steady State (Drain)	$R_{\theta JC}$	1	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
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OFF CHARACTERISTICS

BV_{CER}	Collector to Emitter Breakdown Voltage	$I_{CE} = 2\text{ mA}$, $V_{GE} = 0\text{ V}$, $R_{GE} = 1\text{ k}\Omega$, $T_J = -40\text{ to }150^\circ\text{C}$	370	400	430	V	
BV_{CES}	Collector to Emitter Breakdown Voltage	$I_{CE} = 10\text{ mA}$, $V_{GE} = 0\text{ V}$, $R_{GE} = 0$, $T_J = -40\text{ to }150^\circ\text{C}$	390	420	450	V	
BV_{ECS}	Emitter to Collector Breakdown Voltage	$I_{CE} = -75\text{ mA}$, $V_{GE} = 0\text{ V}$, $T_J = 25^\circ\text{C}$	28	-	-	V	
BV_{GES}	Gate to Emitter Breakdown Voltage	$I_{GES} = \pm 2\text{ mA}$	± 12	± 14	-	V	
I_{CER}	Collector to Emitter Leakage Current	$V_{CE} = 175\text{ V}$ $R_{GE} = 1\text{ k}\Omega$	$T_J = 25^\circ\text{C}$	-	-	25	μA
			$T_J = 150^\circ\text{C}$	-	-	1	mA
I_{ECS}	Emitter to Collector Leakage Current	$V_{EC} = 24\text{ V}$	$T_J = 25^\circ\text{C}$	-	-	1	mA
			$T_J = 150^\circ\text{C}$	-	-	40	
R_1	Series Gate Resistance		-	120	-	Ω	
R_2	Gate to Emitter Resistance		10K	-	30K	Ω	

ON CHARACTERISTICS

$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 6\text{ A}$, $V_{GE} = 4\text{ V}$, $T_J = 25^\circ\text{C}$	-	1.15	1.25	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 10\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^\circ\text{C}$	-	1.35	1.50	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 15\text{ A}$, $V_{GE} = 5\text{ V}$, $T_J = 150^\circ\text{C}$	-	1.68	1.85	V

DYNAMIC CHARACTERISTICS

$Q_{G(ON)}$	Gate Charge	$I_{CE} = 10\text{ A}$, $V_{CE} = 12\text{ V}$, $V_{GE} = 5\text{ V}$	-	21	-	nC	
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	$I_{CE} = 1\text{ mA}$ $V_{CE} = V_{GE}$	$T_J = 25^\circ\text{C}$	1.3	1.5	2.2	V
			$T_J = 150^\circ\text{C}$	0.75	1.2	1.8	
V_{GEP}	Gate to Emitter Plateau Voltage	$V_{CE} = 12\text{ V}$, $I_{CE} = 10\text{ A}$	-	2.8	-	V	

SWITCHING CHARACTERISTICS

$t_{d(ON)R}$	Current Turn-On Delay Time-Resistive	$V_{CE} = 14\text{ V}$, $R_L = 1\ \Omega$, $V_{GE} = 5\text{ V}$, $R_G = 470\ \Omega$, $T_J = 25^\circ\text{C}$	-	0.9	4	μs
t_{rR}	Current Rise Time-Resistive		-	1.9	7	
$t_{d(OFF)L}$	Current Turn-Off Delay Time-Inductive	$V_{CE} = 300\text{ V}$, $L = 1\text{ mH}$, $V_{GE} = 5\text{ V}$, $R_G = 470\ \Omega$, $I_{CE} = 6.5\text{ A}$, $T_J = 25^\circ\text{C}$	-	4.8	10	
t_{fL}	Current Fall Time-Inductive		-	2.0	15	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Package	Shipping [†]
FGD3040G2-F085C	DPAK (Pb-Free)	2500 Units / Tape & Reel
FGB3040G2-F085C	D ² PAK (Pb-Free)	800 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

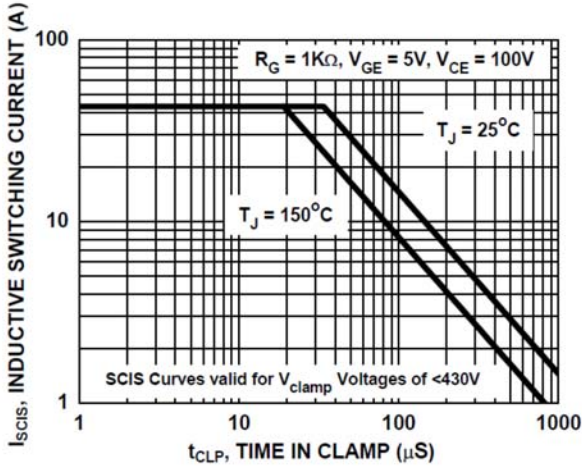


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

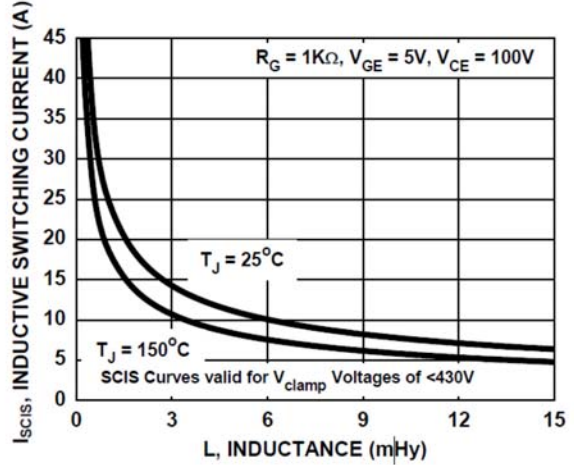


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

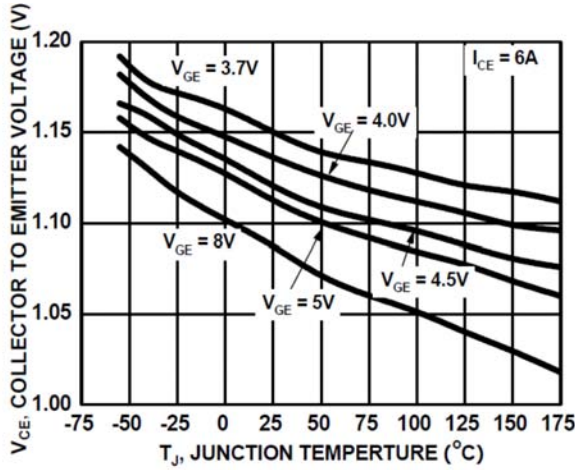


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

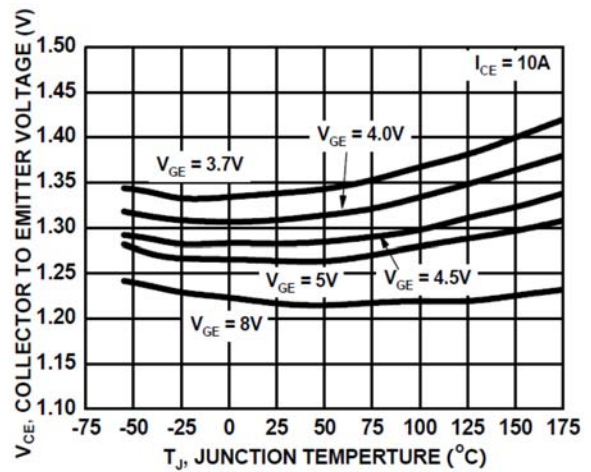


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

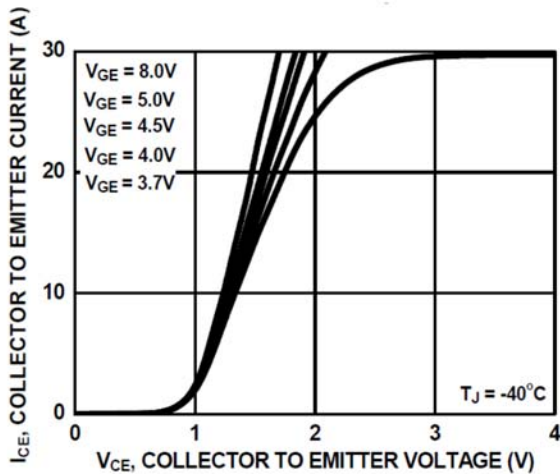


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

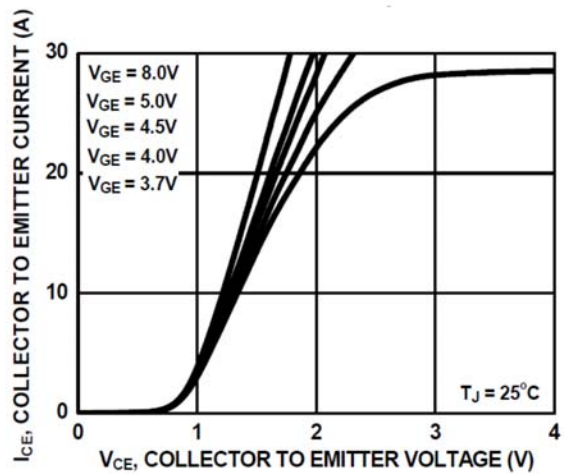


Figure 6. Collector to Emitter On-State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS (continued)

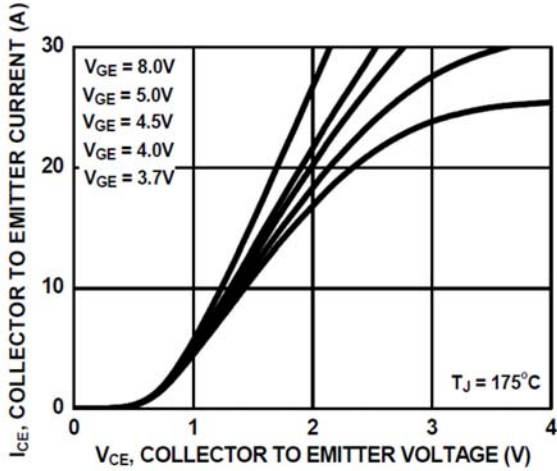


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

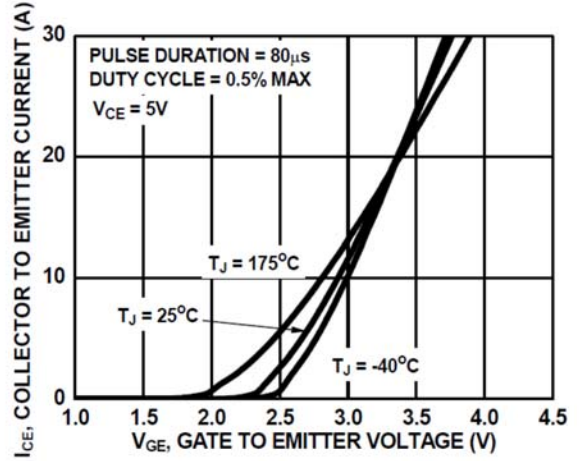


Figure 8. Transfer Characteristics

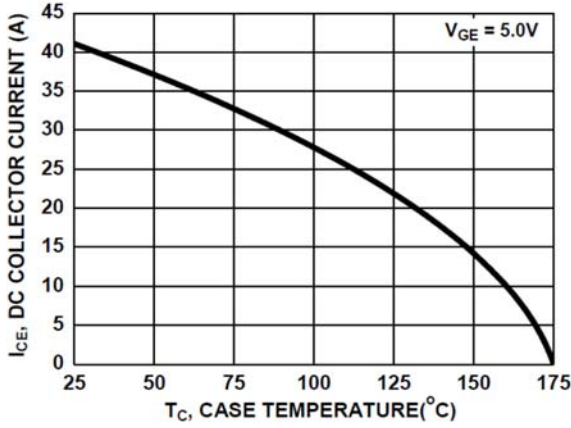


Figure 9. DC Collector Current vs. Case Temperature

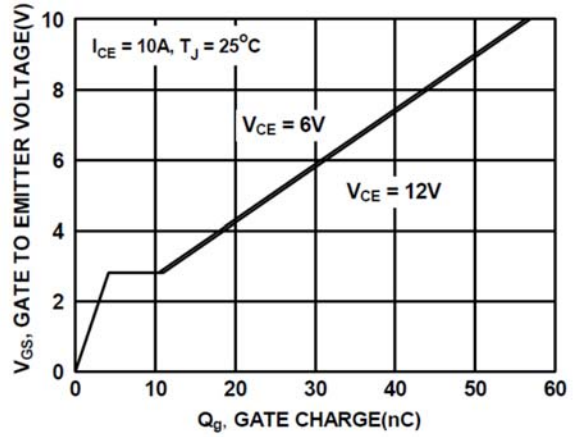


Figure 10. Gate Charge

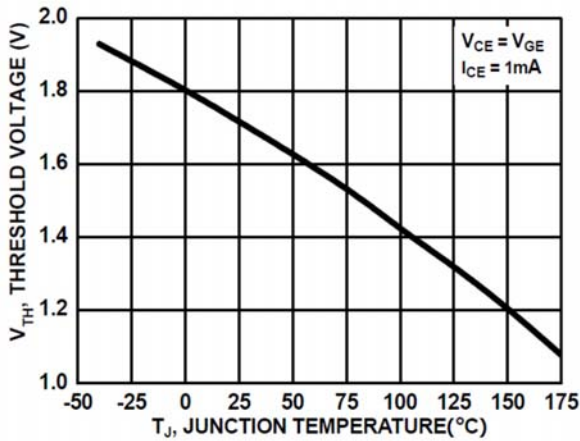


Figure 11. Threshold Voltage vs. Junction Temperature

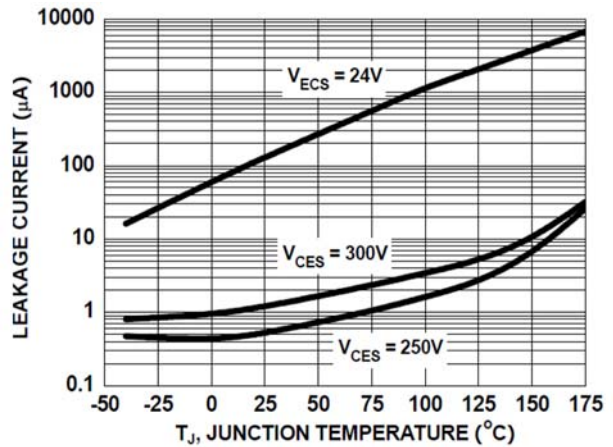


Figure 12. Leakage Current vs. Junction Temperature

FGD3040G2-F085C

TYPICAL CHARACTERISTICS (continued)

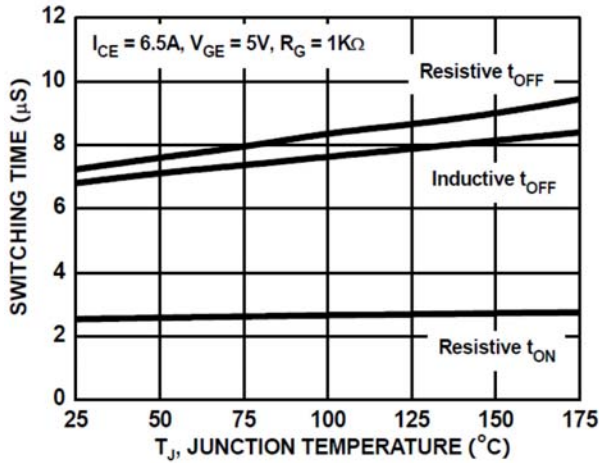


Figure 13. Switching Time vs. Junction Temperature

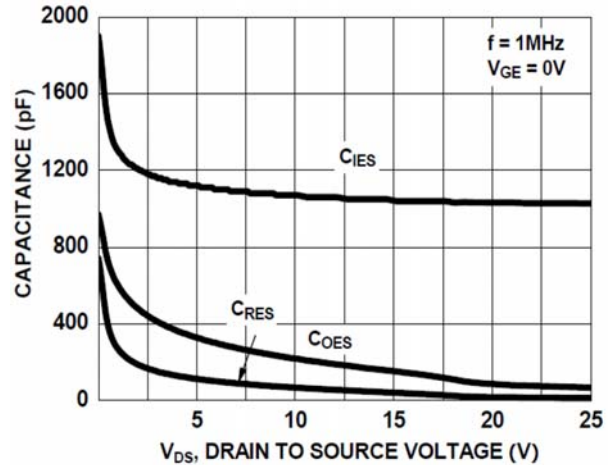


Figure 14. Capacitance vs. Collector to Emitter

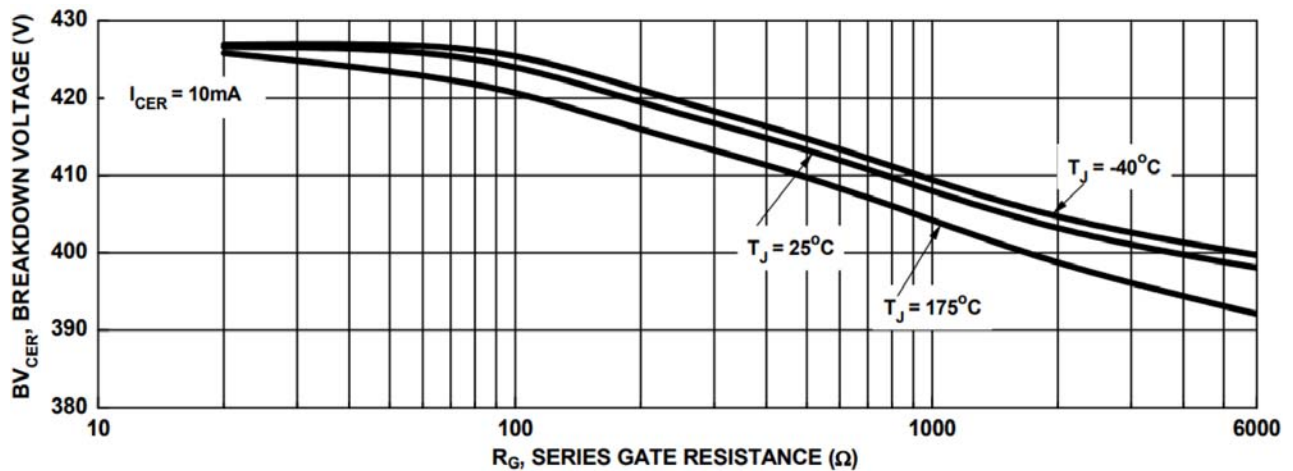


Figure 15. Break Down Voltage vs. Series Resistance

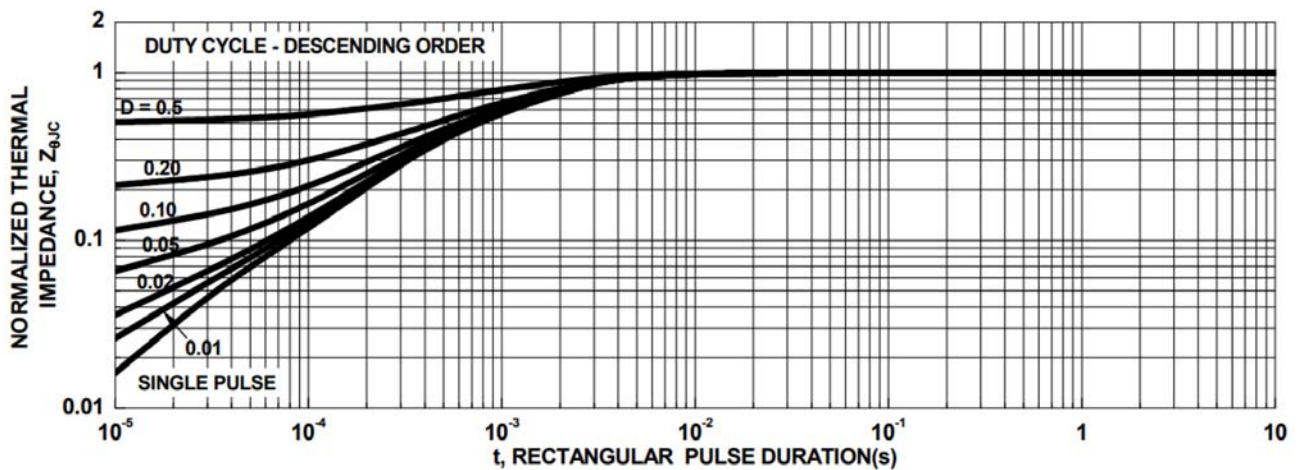


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TEST CIRCUIT AND WAVEFORMS

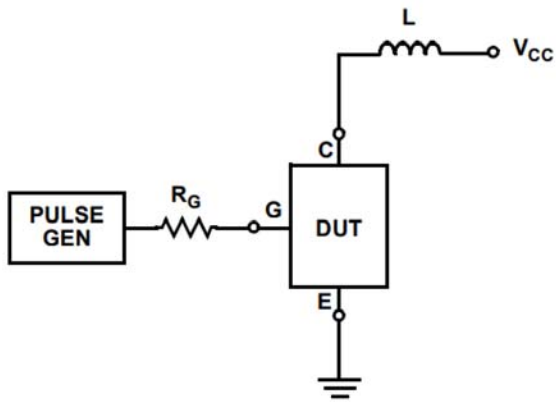


Figure 17. Inductive Switching Test Circuit

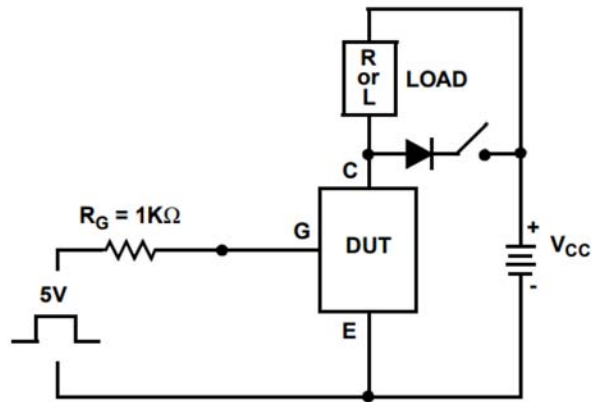


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

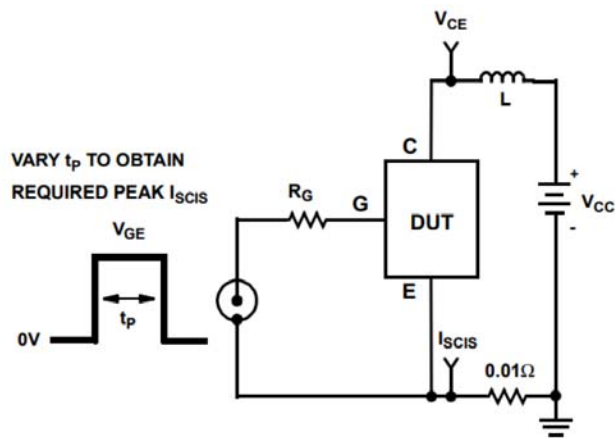


Figure 19. Energy Test Circuit

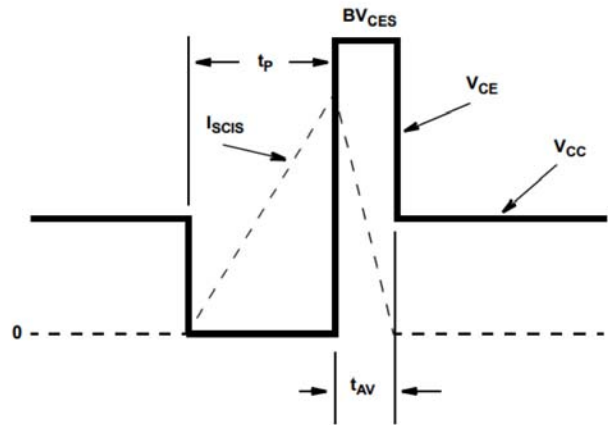
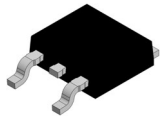


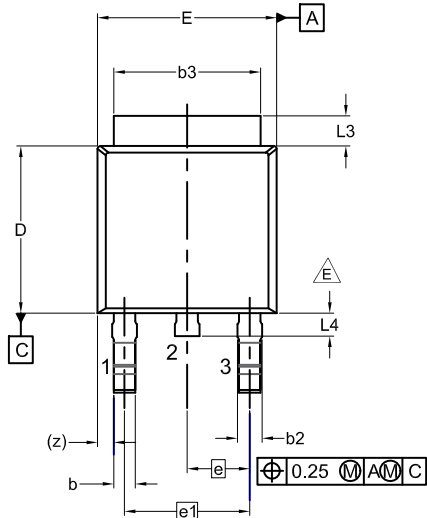
Figure 20. Energy Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

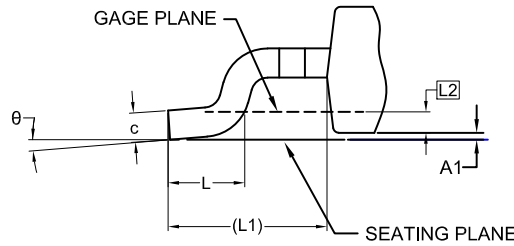


DPAK3 (TO-252 3 LD) CASE 369AS ISSUE A

DATE 28 SEP 2022

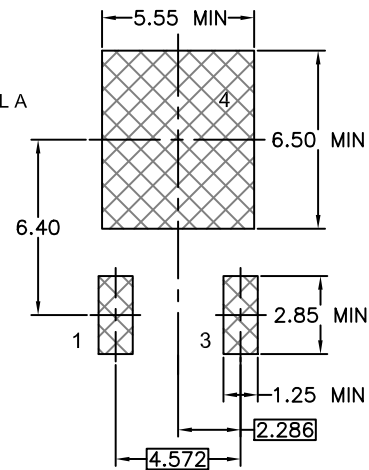
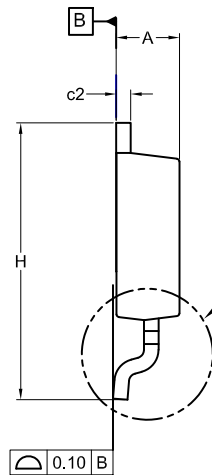
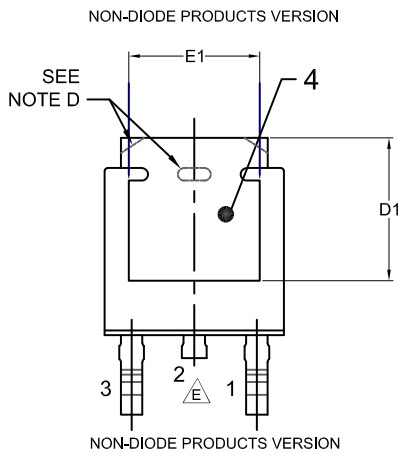


- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
θ	0°	--	10°



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

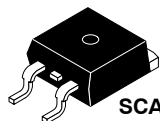
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



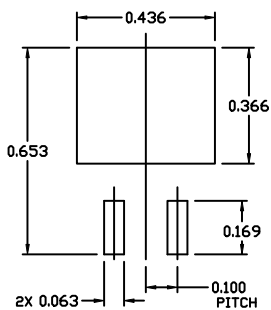
SCALE 1:1

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

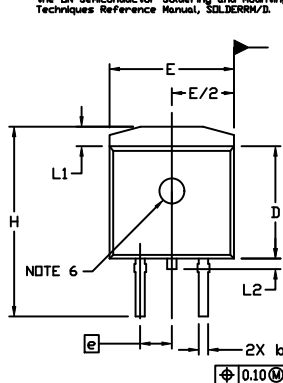
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

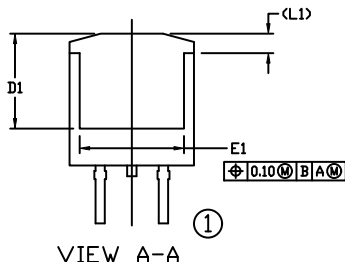
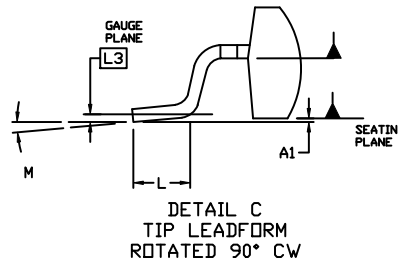
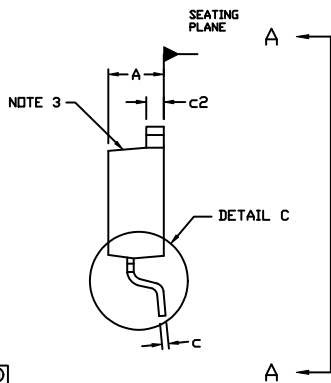
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



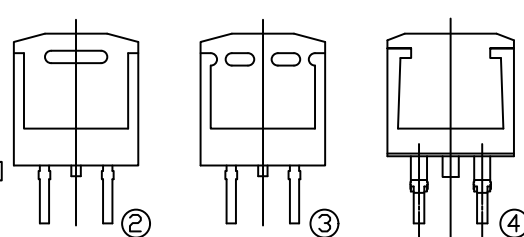
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

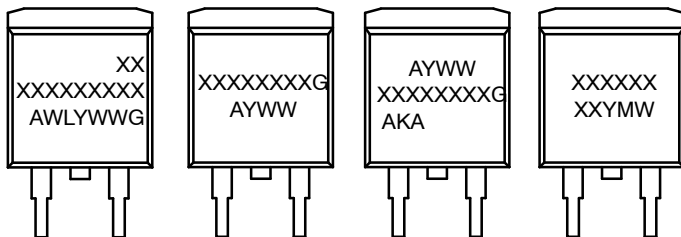


VIEW A-A



VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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