October 2001

# FDG6335N

## 20V N-Channel PowerTrench® MOSFET

### General Description

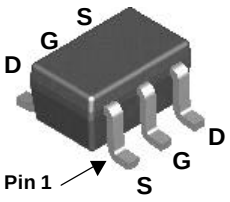
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized use in small switching regulators, providing an extremely low $R_{DS(ON)}$ and gate charge ($Q_G$) in a small package.

### Applications

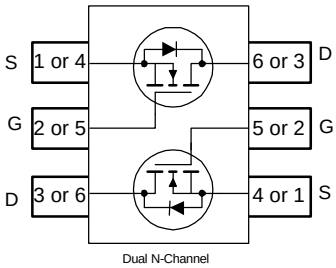
- DC/DC converter
- Power management
- Loadswitch

### Features

- 0.7 A, 20 V. $R_{DS(ON)}$ = 300 mΩ @ $V_{GS}$ = 4.5 V
  $R_{DS(ON)}$ = 400 mΩ @ $V_{GS}$ = 2.5 V
- Low gate charge (1.1 nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- Compact industry standard SC70-6 surface mount package




SC70-6




Dual N-Channel

The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

## Absolute Maximum Ratings $T_A$=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | ± 12 | V |
| $I_D$ | Drain Current – Continuous (Note 1) | 0.7 | A |
| | – Pulsed | 2.1 | |
| $P_D$ | Power Dissipation for Single Operation (Note 1) | 0.3 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | –55 to +150 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 415 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| .35 | FDG6335N | 7'' | 8mm | 3000 units |

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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 14 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | | | 1 | µA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 12 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –12 V, $V_{DS}$ = 0 V | | | –100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 0.6 | 1.1 | 1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | –2.8 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 0.7 A<br>$V_{GS}$ = 2.5 V, $I_D$ = 0.6 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 0.7 A, $T_J$=125°C | | 180<br>293<br>247 | 300<br>400<br>442 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | 1 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 0.7 A | | 2.8 | | S |
| Dynamic Characteristics | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 113 | | pF |
| $C_{oss}$ | Output Capacitance | | | 34 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 16 | | pF |
| Switching Characteristics (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 6 Ω | | 5 | 10 | ns |
| $t_r$ | Turn–On Rise Time | | | 7 | 15 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 9 | 18 | ns |
| $t_f$ | Turn–Off Fall Time | | | 1.5 | 3 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 10 V, $I_D$ = 0.7 A, $V_{GS}$ = 4.5 V | | 1.1 | 1.4 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 0.24 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 0.3 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 0.25 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.25 A (Note 2) | | 0.74 | 1.2 | V |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W when mounted on a minimum pad .

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

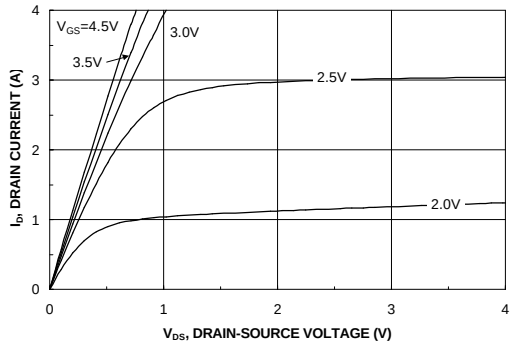


Figure 1. On-Region Characteristics.

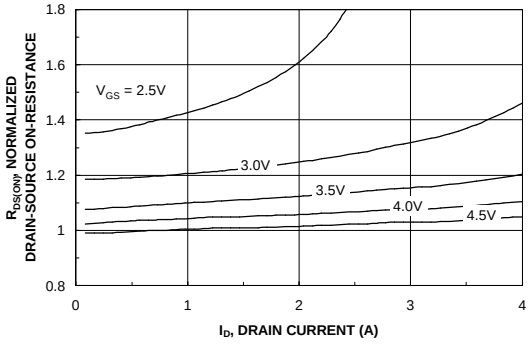


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

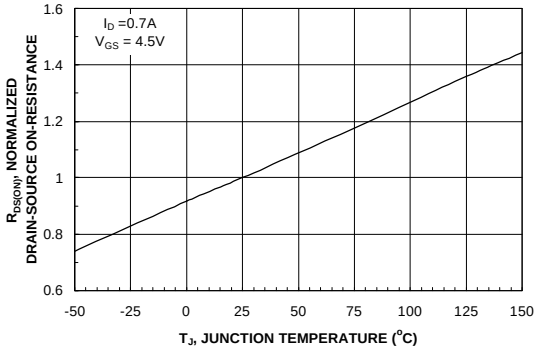


Figure 3. On-Resistance Variation with Temperature.

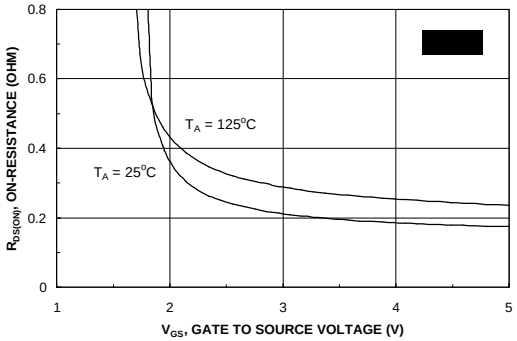


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

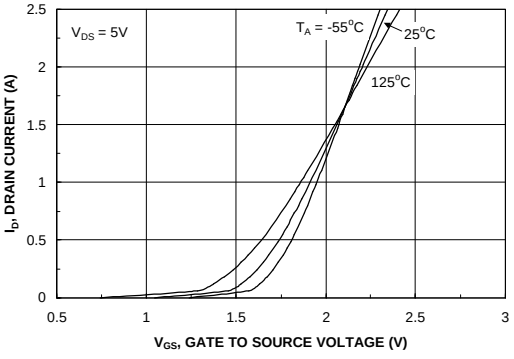


Figure 5. Transfer Characteristics.

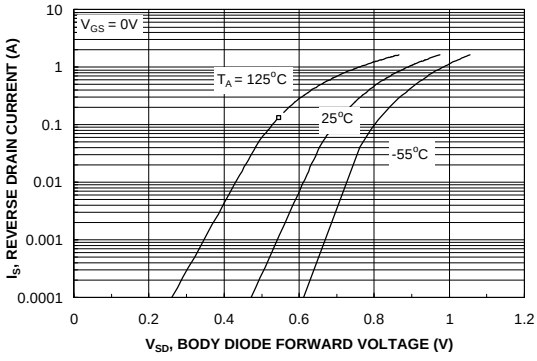


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

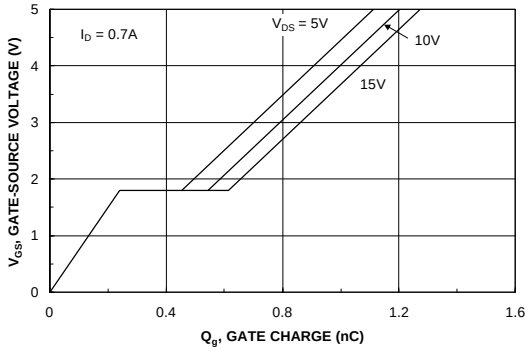


Figure 7. Gate Charge Characteristics.

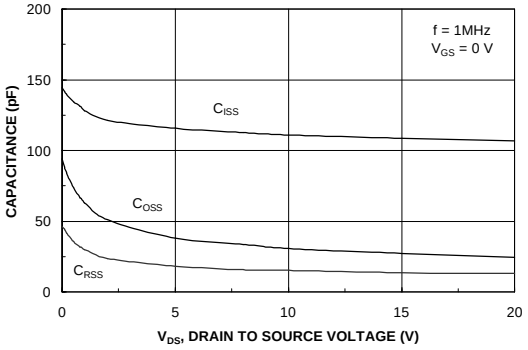


Figure 8. Capacitance Characteristics.

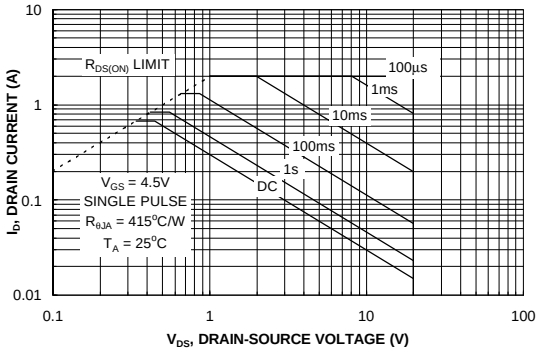


Figure 9. Maximum Safe Operating Area.

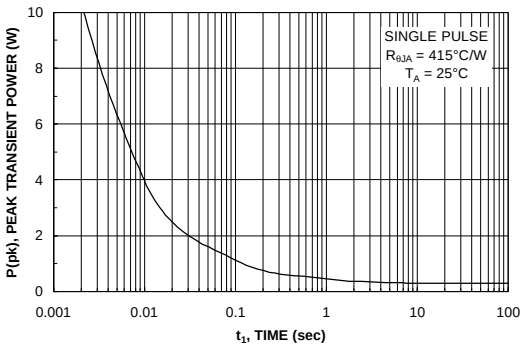


Figure 10. Single Pulse Maximum Power Dissipation.

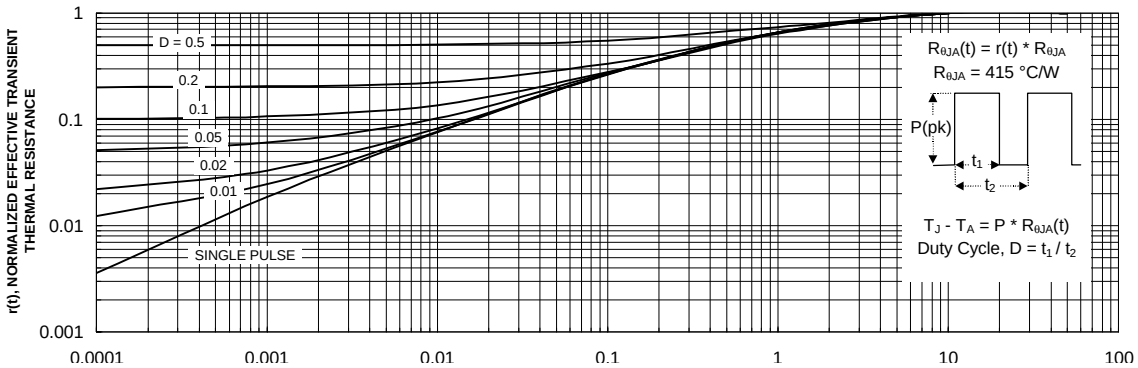


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.
Transient thermal response will change depending on the circuit board design.

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