15 W 5 V charger reference design with 700 V CoolMOS™ P7

EVAL_15W_5V_FLYB_P7 using IPS70R1K4P7S, ICE2QS03G, BSC067N06LS3 G

About this document

Scope and purpose

This document introduces a 15 W high efficiency USB charger reference design with a 5 V output voltage using the QR PWM IC ICE2QS03G with CoolMOS™ IPS70R1K4P7S (IPAK SL) and a secondary side synchronous rectification IC with OptiMOS™ BSC067N06LS3 G (SuperSO8) in a small form factor, high efficiency and various protections for a highly reliable system.

Additionally, it will show the benefits 700 V CoolMOS™ P7 can offer in charger designs in comparison to the existing 650 V CoolMOS™ CE technology, leading to higher efficiency and lower mold compound temperature.

This document will start by describing the general structure of the 15 W charger and will conclude by benchmarking the difference. It can be viewd as an update to the existing application note AN_201411_PL21_002 and therefore only describes the controller, OptiMOS™ and reference board sections in general and will concentrate on the performance advantage of 700 V CoolMOS™ P7 in this design.

Intended audience

This document is intended for designers and engineers who wish to design a high efficiency, very small form factor universal 15 W 5 V AC-DC adapter with Infineon CoolMOS™ P7 series, OptiMOS™, QR PWM IC ICE2QS03G and synchronous rectification.

Table of contents

1 Reference board

This document contains a list of features, power supply specifications, schematic, Bill of Materials (BOM) (component list) and transformer construction documentation. Furthermore, operating characteristics such as the performance curve of IPS70R1K4P7S compared to IPS65R1K5CE are included.

1.1 Pictures and outer dimensions

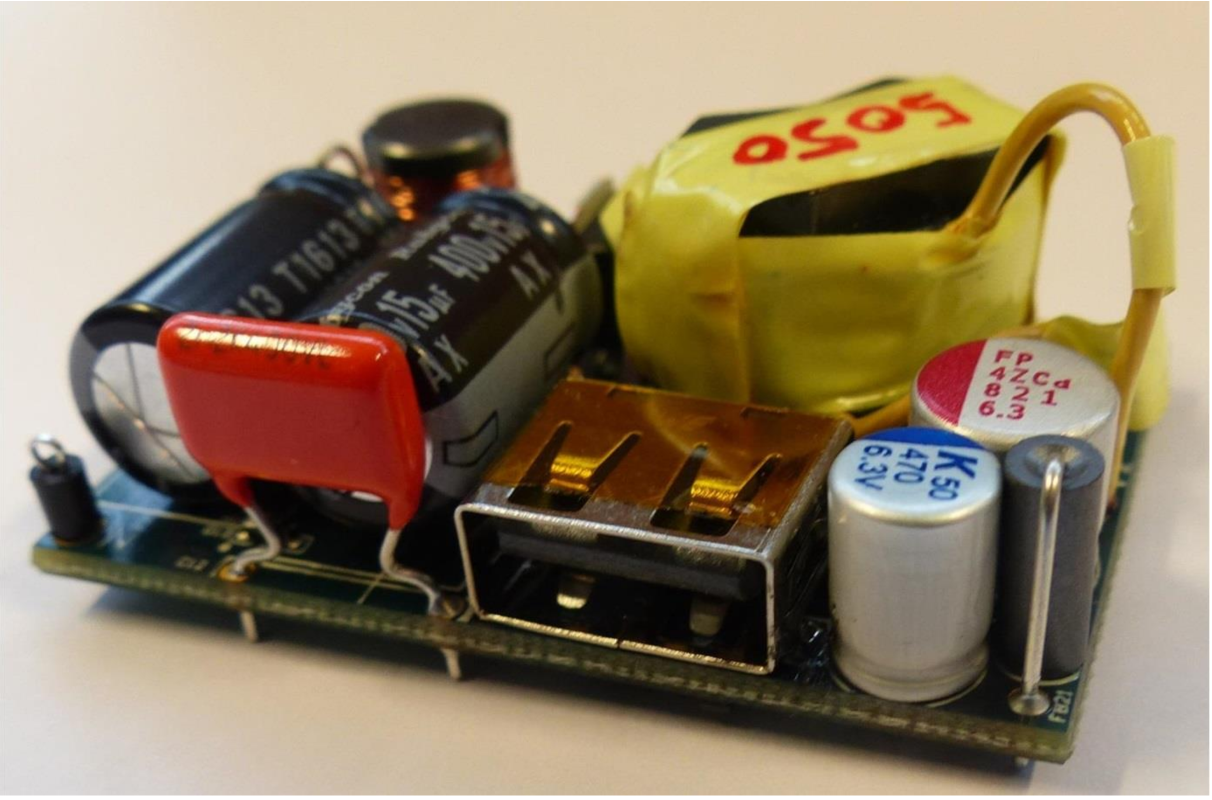


Figure 1 Demoboard perspective view EVAL_15W_5V_FLYB_P7

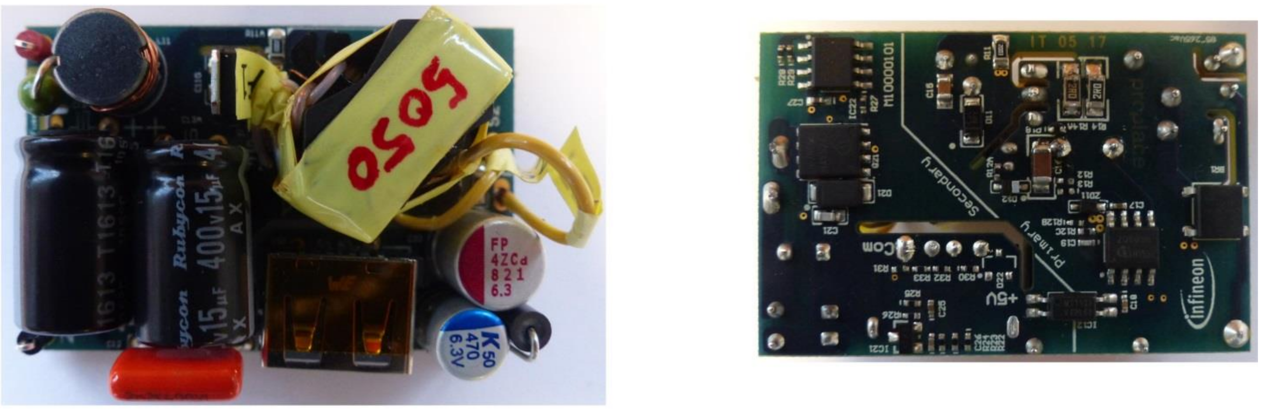


Figure 2 Demoboard top and bottom view EVAL_15W_5V_FLYB_P7

1.2 Specifications

Table 1 Specifications of EVAL_15W_5V_FLYB_P7

Input voltage	85 VAC ~ 265 VAC
Input frequency	50 ~ 60 Hz
Output voltage	5 V
Output current	3 A
Output power	15 W
Switching frequency	55 – 110 kHz
Efficiency	> 89% at 115 VACand 230 VAC(@ full load)

1.3 Circuit diagram

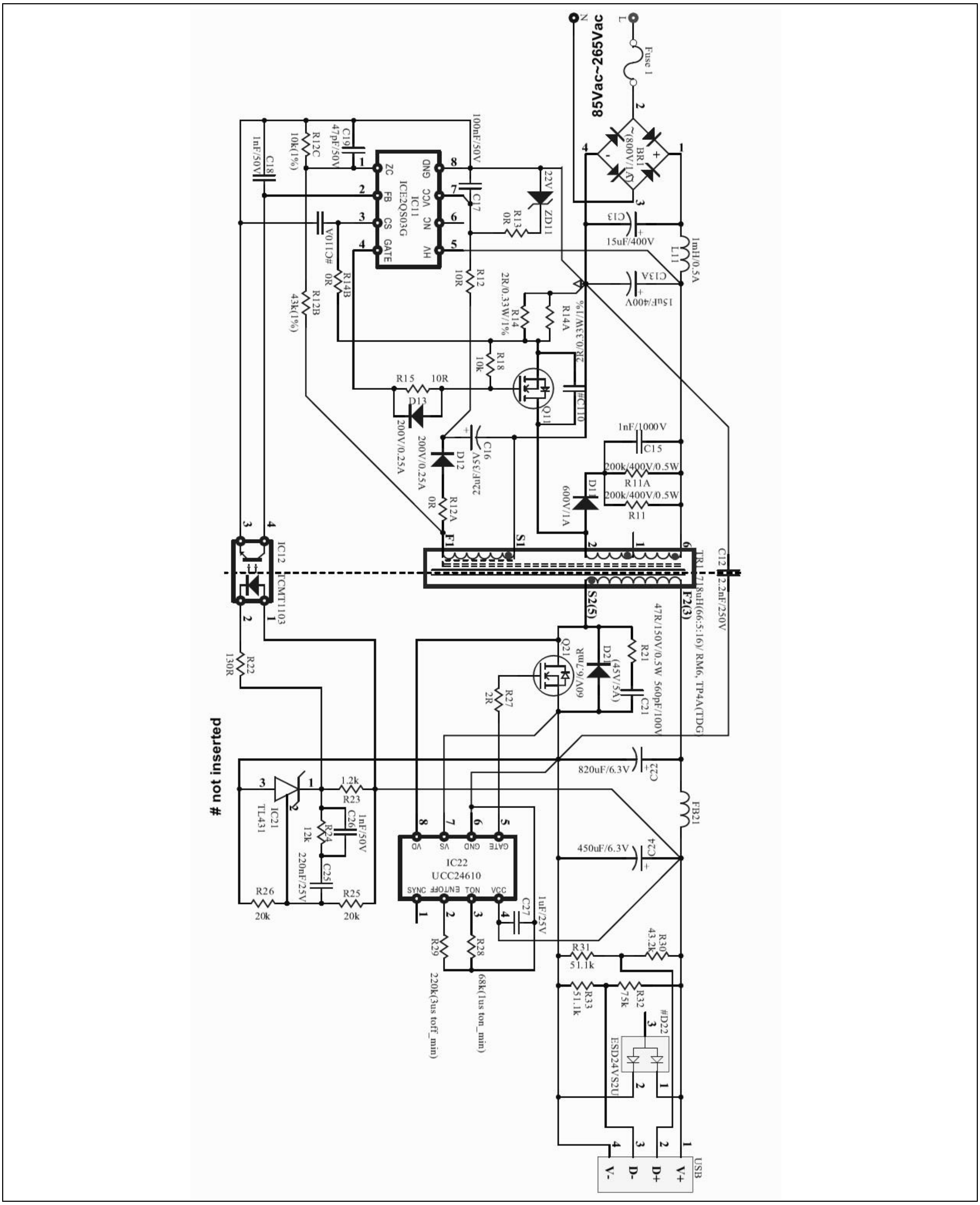


Figure 3 **Schematic of EVAL_15W_5V_FLYB_P7**

1.4 PCB layout

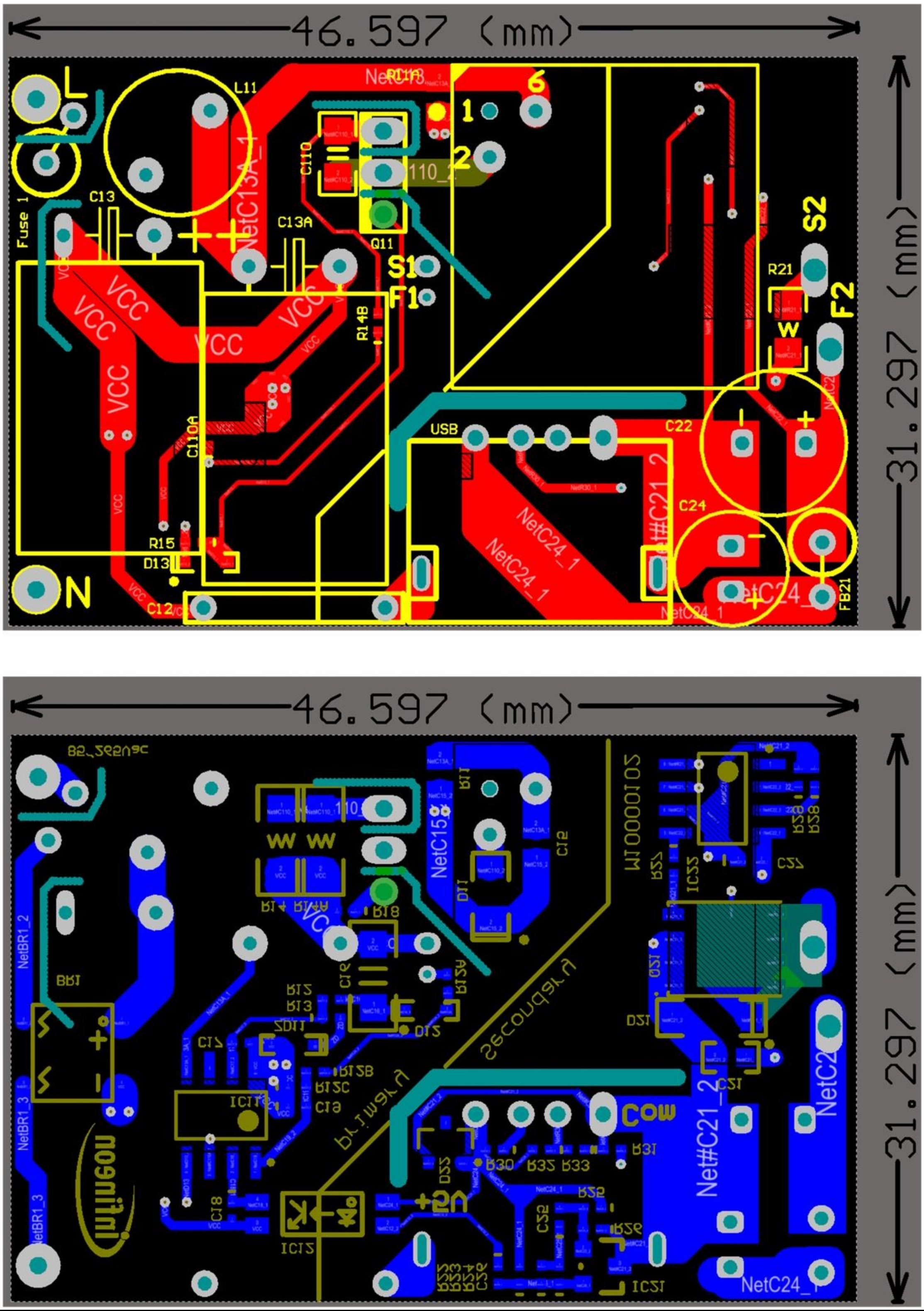


Figure 4 Top side copper (upper picture) and bottom side copper (lower picture)

1.5 BOM

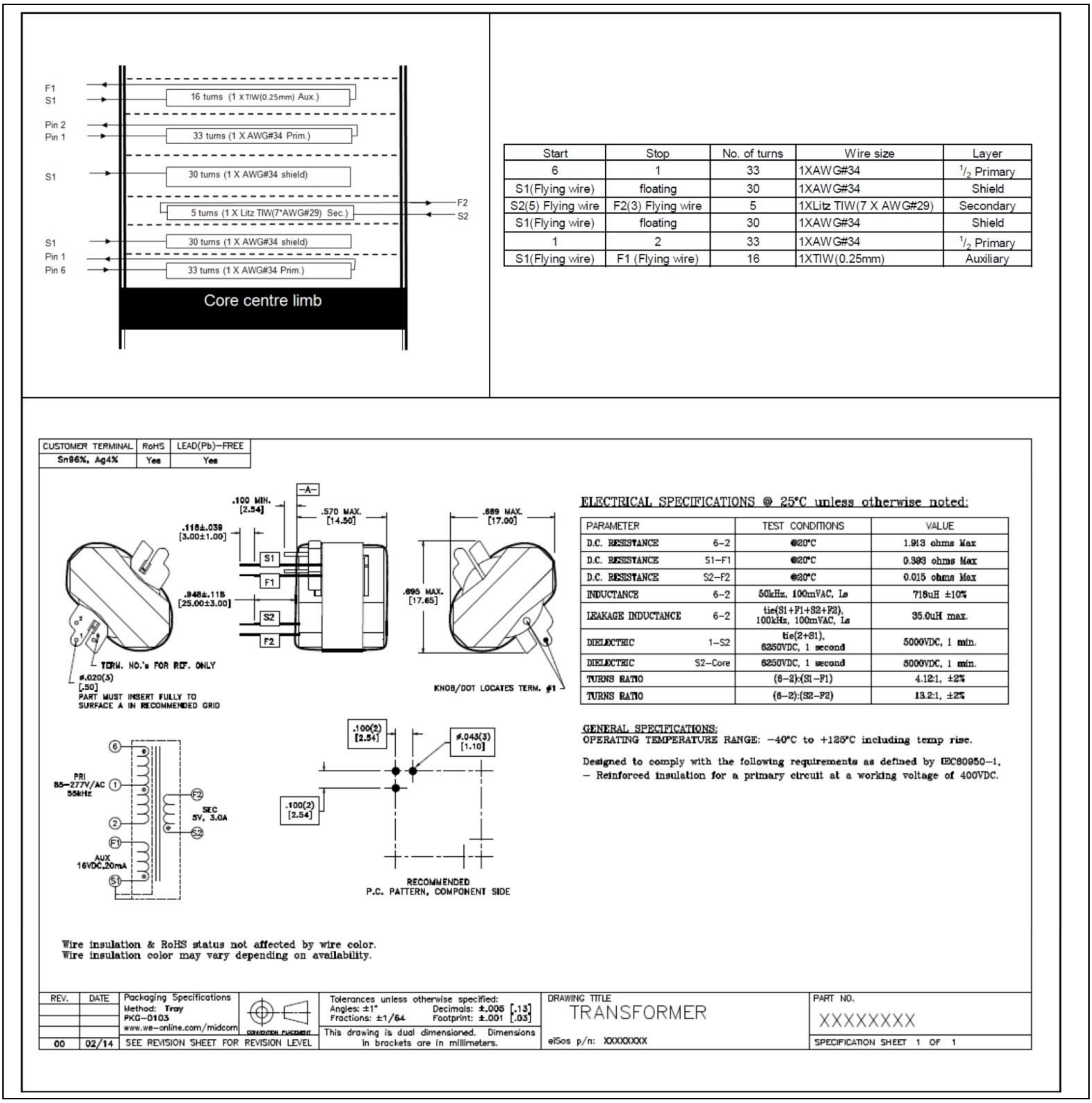
No.	Designator	Description	Footprint	Part Number	Manufacturer	Quantity
1	BR1	800V/1A	SOP-4	D1UBA80-7062	SHINDENGEN	1
2	C12	2.2nF/250V	MKT2/13/10_0M8	DE1E3KL222MC4BNA1S	MURATA	1
3	C13,C13A	15µF/400V	RB10H(10x16)	400AX15M10X16	RUBYCON	2
4	C15	1nF/1000V	0805	C0805X102KDRACTU		1
5	C16	22µF/35V	1206	C3216X5R1V226M		1
6	C17	100nF/50V	0402	GRM155R71H104KE14D	MURATA	1
7	C18, C26	1nF/50V	0402	GRM155R71H102KA01D	MURATA	2
8	C19	47pF/50V	0402	GRM1555C1H470JA01D	MURATA	1
9	C21	560pF/100V	0603	GRM1885C2A561JA01D	MURATA	1
10	C22	820µF/6.3V	8.0mm diameter	RL80J821MDN1KX	NICHICON	1
11	C24	470µF/6.3V	6.3mm diameter	A750EK477M0JAAE018	KEMET	1
12	C25	220nF/25V	0402	GRM155C81E224KE01D	MURATA	1
13	C27	1µF/25V	0402	GRM155R61E105KA12D	MURATA	1
14	D11	600V/1A	Sub SMA	ES1JL		1
15	D12, D13	200V/0.25A	SOD323	BAS21-03W	INFINEON	2
16	D21	45V/5A	DO-221AC (slim SMA)	VSSAF5L45-M3/6A		1
17	F1	250V/1A	AXIAL0.4_V 3mm	0263001.HAT1L		1
18	FB21	FAIR RITE	AXIAL0.4_V 3mm	2743002112		1
19	IC11	ICE2QS03G	SO-8	ICE2QS03G	INFINEON	1
20	IC12	TCMT1103	optocoupler half pitch mini flat package	TCMT1103		1
21	IC21	TL431	SOT-23	TL431BFDT		1
22	IC22	UCC24610	SO-8	UCC24610		1
23	L	connector	Connector	5000RED		1
24	L11	1mH/0.5A	CH8	768772102	WURTH ELECTRONICS	1
25	N	Connector N(2.5)	Connector(2.5)	5001BLACK		1
26	Q11	650V/1R	TO251(IPAK)	IPS70R1K4P7S	INFINEON	1
27	Q21	60V/6.7mR	INF-PG-TDSON81	BSC067N06LS3G	INFINEON	1
28	R11, R11A	200k/400V/0.5W	0805	ERJ-P06F2003V		2
29	R12, R15	10R	0402			2
30	R12A, R13, R14B	0R	0402			3
31	R12B	43k/1%	0402			1
32	R12C	10k/1%	0402			1
33	R14, R14A	2R/0.33W/1%	1206	ERJ8BQF2R0V		2
34	R18	10k	0402			1
35	R21	47R/0.5W	0805	ERJP6WF47R0V		1
36	R22	130R	0402			1
37	R23	1.2k	0402			1
38	R24	12k	0402			1
39	R25, R26	20k	0402			2
40	R27	2R	0402			1
41	R28	68k	0402			1
42	R29	220k	0402			1
43	R30	43.2k	0402			1
44	R31, R33	51.1k	0402			1
45	R32	75k	0402			1
46	TR1	718µH(66:5:16); RM6(TP4A)	TR_RM6_THT6Pin			1
47	USB Port	USBPORT	USB2 Short(Horizontal)	JL-CAF-001		1
48	ZD11	22V Zener	SOD323	UDZS22B		1

1.6 Transformer construction

Core and material: RM6 TP4A

Bobbin: RM6 with 3 pin

Primary Inductance: Lp = 718 µH (±10 %), measured between pin 2 and pin 6



Start	Stop	No. of turns	Wire size	Layer
6	1	33	1XAWG#34	1/2 Primary
S1(Flying wire)	floating	30	1XAWG#34	Shield
S2(5) Flying wire	F2(3) Flying wire	5	1XLitz TIW(7 X AWG#29)	Secondary
S1(Flying wire)	floating	30	1XAWG#34	Shield
1	2	33	1XAWG#34	1/2 Primary
S1(Flying wire)	F1 (Flying wire)	16	1XTIW(0.25mm)	Auxiliary

ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	6–2	@20°C	1.913 ohms Max
D.C. RESISTANCE	S1–F1	@20°C	0.393 ohms Max
D.C. RESISTANCE	S2–F2	@20°C	0.015 ohms Max
INDUCTANCE	6–2	50kHz, 100mVAC, Ls	716uH ±10%
LEAKAGE INDUCTANCE	6–2	tie(S1+F1+S2+F2), 100kHz, 100mVAC, Ls	35.0uH max.
DIELECTRIC	1–S2	tie(2+S1), 6250VDC, 1 second	5000VDC, 1 min.
DIELECTRIC	S2–Core	6250VDC, 1 second	5000VDC, 1 min.
TURNS RATIO		(6–2):(S1–F1)	4.12:1, ±2%
TURNS RATIO		(6–2):(S2–F2)	13.2:1, ±2%

Figure 5 Transformer structure

1.7 Additional information related to components of the design

To understand the control approach and obtain additional information on the components used, refer to AN_201411_PL21_002. This application note contains a detailed circuit description, circuit operation and the protection features of the controller.

2 Test results

This section of the application note will concentrate on benchmarking of the IPS70R1K4P7S against the IPS65R1K5CE that is the main focus of this document.

2.1 Efficiency

Measurement tolerance: 0.1%

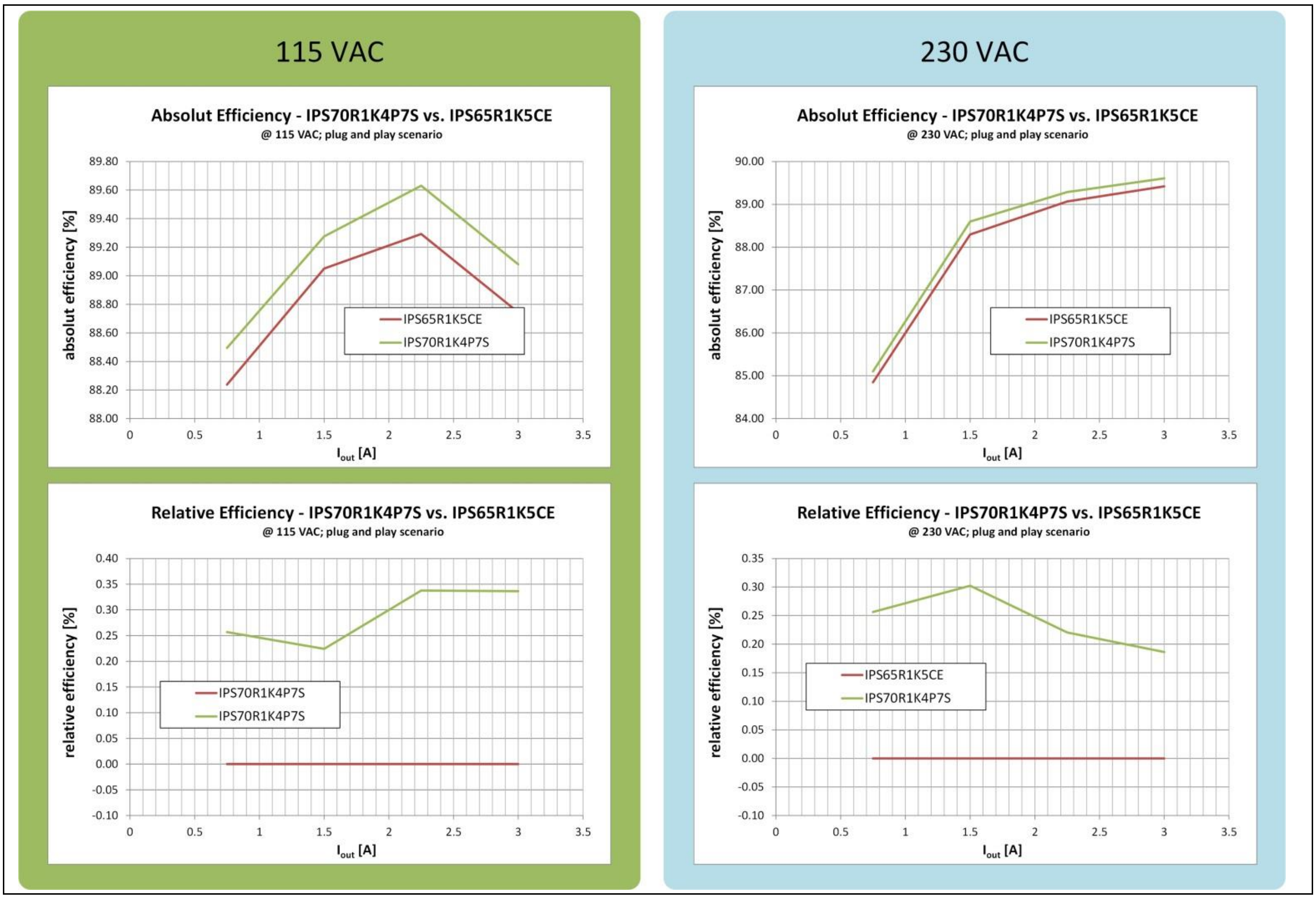


Figure 6 Efficiency comparison

As clearly shown in Figure 6, the IPS70R1K4P7S outperforms the IPS65R1K5CE over the whole load range at 115 VAC and 230 VAC input voltage. This behavior also improves the relevant average efficiency of 100%, 75%, 50% and 25% load points leading to an increase of 0.3% at low input voltage and around 0.25% at higher line operation.

2.2 Thermals

Measurement tolerance: 1°C

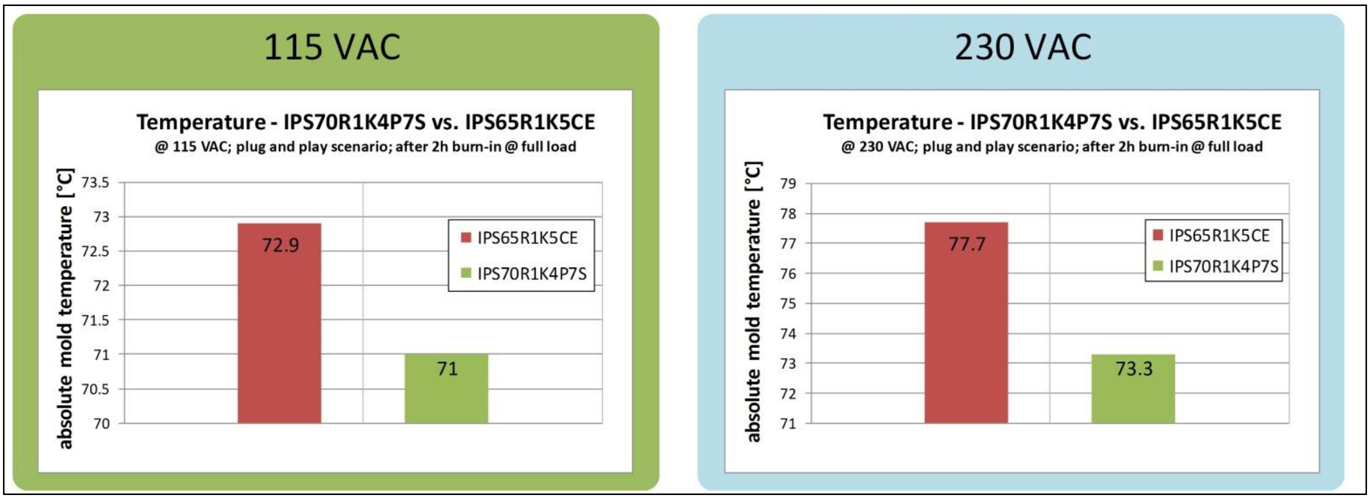


Figure 7 Mold compound temperature comparison

One of the biggest challenges in low power charger/adapters is the thermal behavior of the high voltage MOSFET on the primary side. This benchmarking shows that IPS70R1K4P7s exhibit in both operating conditions (low line and high line) a dramatic reduction of mold compound temperature under the same test condition. These values are measured with a thermal camera at 25°C ambient temperature after 2 hours burn-in at full load operation. There is an advantage for the IPS70R1K4P7S of around 2°C at 115 V AC and around 4.5°C at 230 VAC input voltage.

It is shown that at 115 VAC input voltage the thermal benefit of 700 V CoolMOS™ P7 is not as pronounced as at higher input voltage. This behavior is based on the E_{OSS} differences between P7 and CE technology where the E_{oss} difference is more pronounced at higher drain source voltage. This will be described in the following chapter of this application note.

3 Performance increase due to 700 V CoolMOS™ P7

Now, the question may arise: "Why does 700 V CoolMOS™ P7" outperform the competitor?" This section of the application note will concentrate on the most interesting value proposition besides higher efficiency and lower thermals but which is interlinked in order to achieve higher efficiency and introduce more safety in peak current controlled designs.

3.1 Energy stored in output capacitance (E_{oss})

E_{oss} is one of the main contributors to losses during the turn-on of the MOSFET. This is the energy which translates into losses during the turn-on at a certain V_{DS} voltage. In QR Flyback converters there are no E_{on} losses as there is no overlap between I_D and V_{DS} as the current throught the main transformer is 0 A. Nevertheless, additional losses are generated at every turn-on based on the amount of energy stored in the output capacitance.

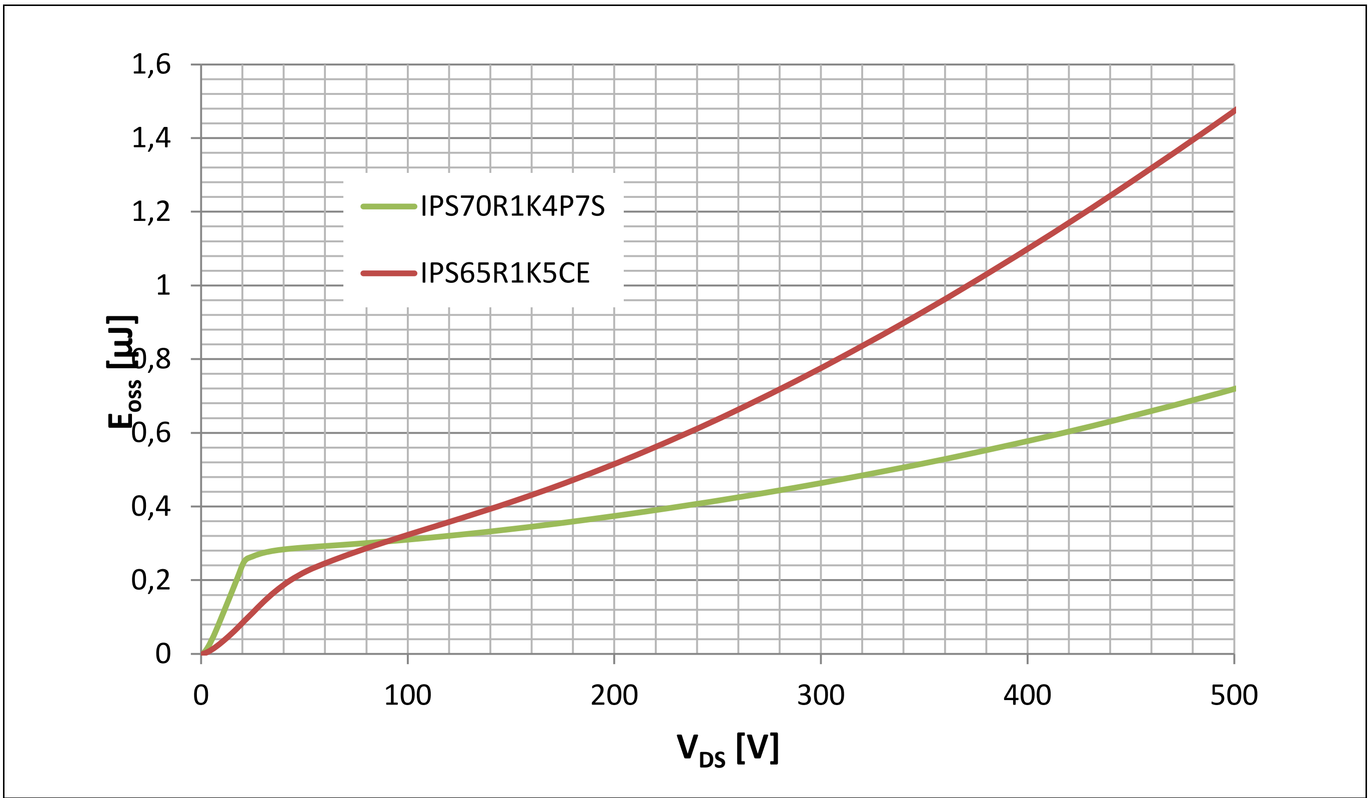


Figure 8 E_{oss} comparison of 1400 mΩ devices

From the diagram it is seen that 700 V CoolMOS™ P7 offers the lowest E_{oss} starting from 80 V V_{DS}. Typically it is not possible to have a real ZVS turn-on of the MOSFET as there would be a need to increase the reflected voltage from the secondary side to the primary side tremendously. This would also increase the bulk voltage and the drain source voltage peak during turn off. Therefore turn-on V_{DS} at low line is typically between 50 V and 150 V and at high line 200 V to 300 V, resulting in around 30% lower turn-on losses than for IPS65R1K5CE.

As these additional losses are present at every turn on, 700 V CoolMOS™ P7 offers the opportunity to move to higher switching frequencies.

With respect to low line operation, the drawback of higher E_{oss} is reduced by the temperature dependency of the IPS70R1K4P7S which is due to the much reduced E_{off} losses and described in the next chapter.

3.2 Temperature dependency of the on-state resistance

In the lower power market the conduction losses also have an influence on the efficiency and the thermal behavior of the overall system, especially at lower input voltages such as 90 VAC or 115 VAC. In this case, 700 V CoolMOS™ P7 offers a significant value proposition. Due to the MOSFET structure, 700 V CoolMOS™ P7 offers the lowest $R_{DS(on)}$ change driven by increasing junction temperature. The following diagram illustrates this behavior.

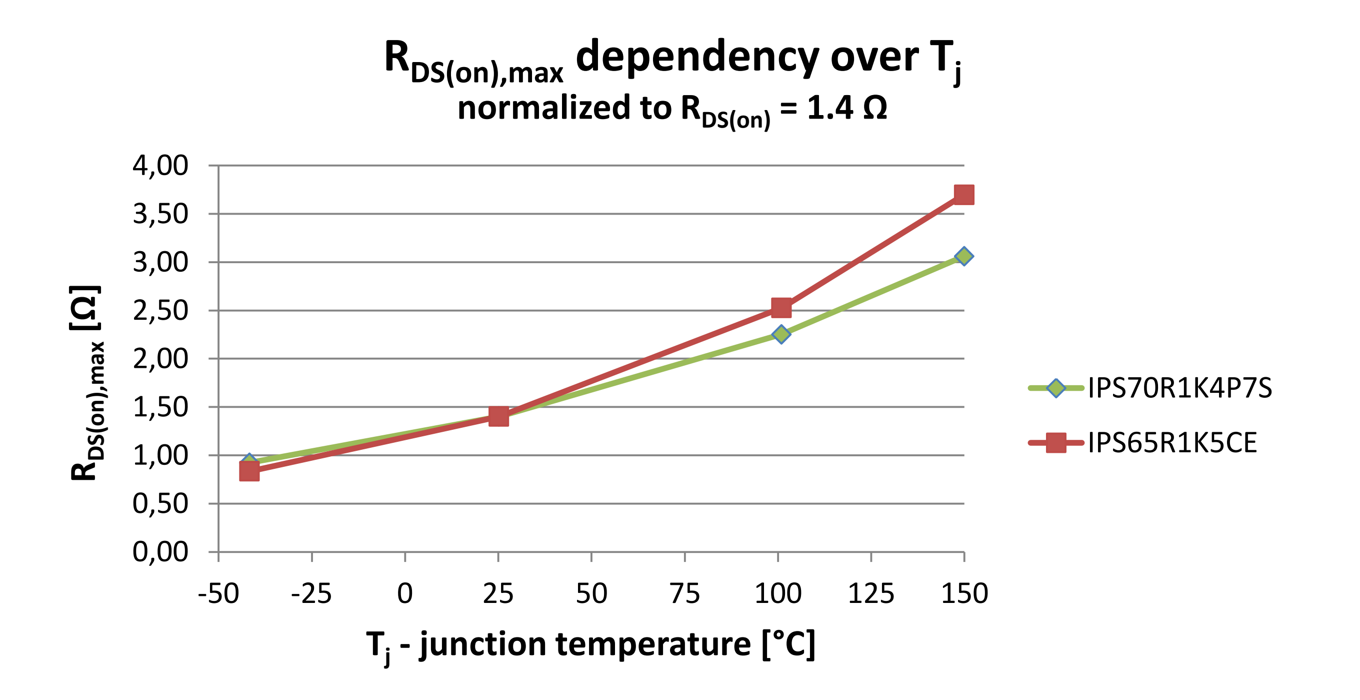


Figure 9 $R_{DS(on)}$ behavior over junction temperature

At 150°C junction temperature, the 700 V CoolMOS™ P7 shows around 21% lower maximum $R_{DS(on)}$ compared to Infineon's CoolMOS™ CE family. This key parameter results in the reduction of the MOSFET conduction losses in any design.

3.3 Improved transfer characteristics

Around 95% of all Flyback converters use peak current control. This means that the controller sends the turn-off signal to the gate driver at a certain value of current running through primary inductance of main transformer and MOSFET. There is a well known failure mode in charger and adapter applications when the gate source voltage is dropping (for example during burst mode operation) and the MOSFET is not able to carry enough current to reach the peak current. In this case, the MOSFET is operating in the linear region and the MOSFET does not turn off resulting in destruction of the application. In addition, 700 V CoolMOS™ P7 can offer a very narrow $V_{GS(th)}$ (gate source threshold voltage) window from 2.5 V to 3.5 V with a typical value of 3.0 V.

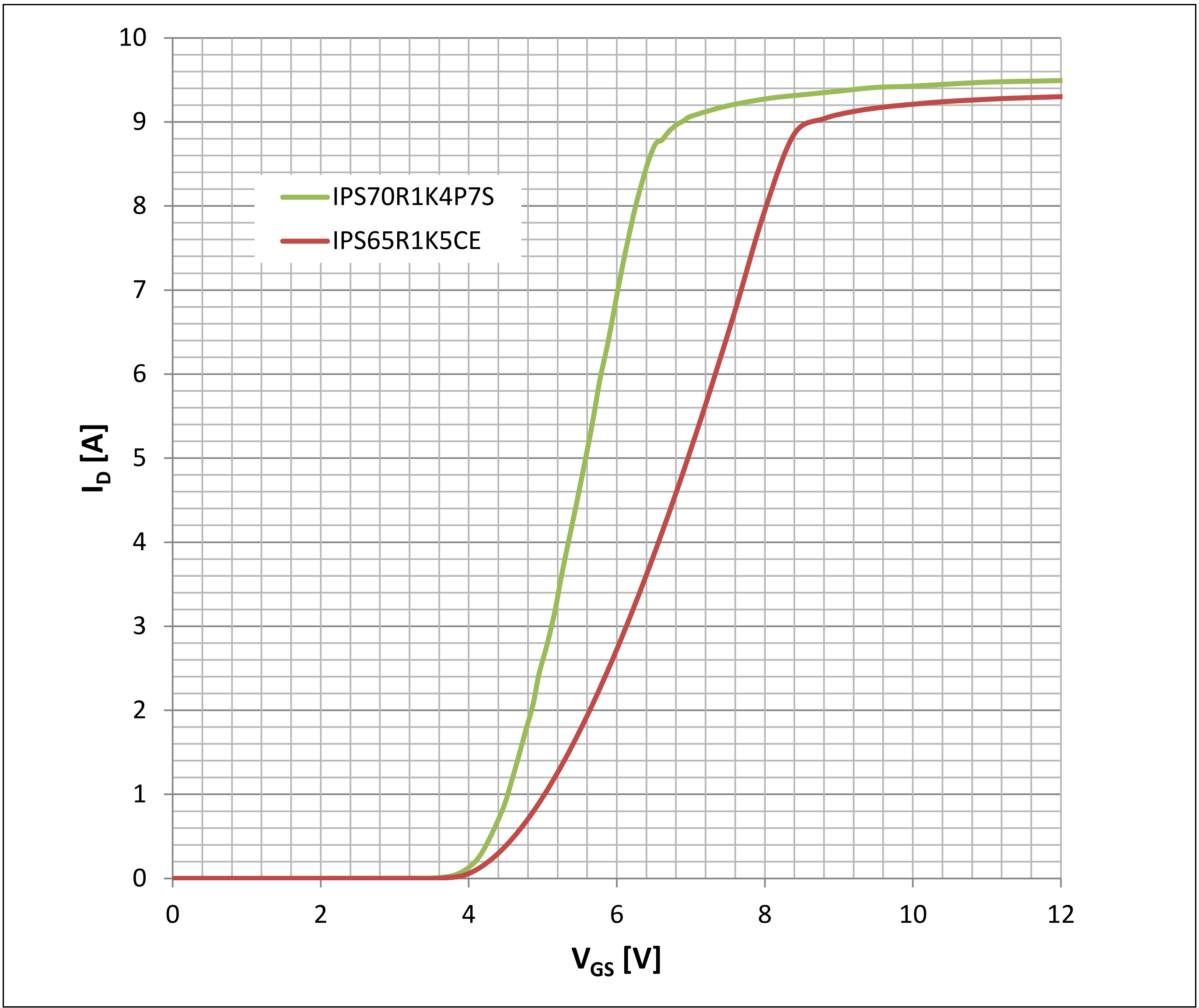


Figure 10 Transfer characteristics comparison of 1400 mΩ devices at 25°C

700 V CoolMOS™ P7 shows the best in class transconductance behavior due to the unmatched current capability at low gate source voltage. This leads to the opportunity to reduce the gate source voltage intentionally in order to minimize the overall driving losses as well as the opportunity to meet new no load operation requirements.

4 Conclusion

700 V CoolMOS™ P7 is an enabler for higher switching frequency applications in order to reduce the overall magnetic content of the applications, resulting in a smaller form factors and higher power densities.

700 V CoolMOS™ P7 shows its best performance at high line operation due to the E_{oss} behavior, but shows also good performance during low line operation due to the temperature dependency of $R_{DS(on)}$.

Last but not least, the typical $V_{GS(th)}$ and the slope of the transfer characteristics give 700 V CoolMOS™ P7 one additional factor in order to reduce failures on peak current controlled designs.

Revision history

Major changes since the last revision

Page or Reference	Description of change

Edition 2017-03-15

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_201702_PL52_014