EMIF04-1502M8

4-line IPAD™
low capacitance EMI filter and ESD protection in micro QFN package

Features

- EMI asymmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consumption: 1.7 mm x 1.5 mm
- Very thin package: 0.6 mm max
- High efficiency in ESD suppression on input pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging
- Lead-free package

Complies with following standards:

- IEC 61000-4-2 level 4 input pins
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3A (all pins)

Applications

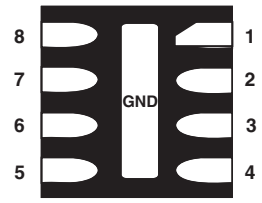
Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU boards

Description

The EMIF04-1502M8 is a 4-line, highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the input pins.



Micro QFN 1.7 mm x 1.5 mm (bottom view)

Figure 1. Pin configuration (top view)

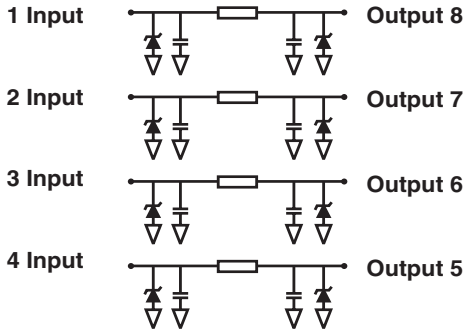
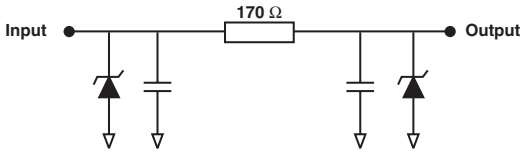


Figure 2. Basic cell configuration



Typical line capacitance = 14 pF @ 2.5 V

TM: IPAD is a trademark of STMicroelectronics

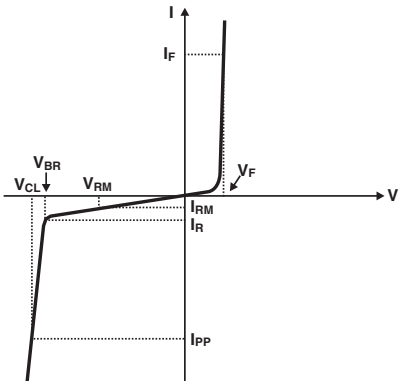
1 Characteristics

Table 1. Absolute ratings (limiting values at T_{amb} = 25° C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{PP}	ESD IEC 61000-4-2 air discharge on input pins ESD IEC 61000-4-2 contact discharge on input pins ESD IEC 61000-4-2 contact discharge on output pins	15 8 4	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V per line			100	nA
$R_{I/O}$	Tolerance ± 10%	153	170	187	Ω
C_{line}	V_{LINE} = 2.5 V dc, V_{OSC} = 30 mV, F = 1 MHz	12	14	16.5	pF

Figure 3. S21 attenuation measurement

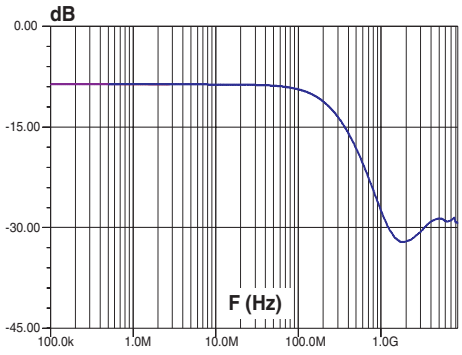


Figure 4. Analog cross talk measurements

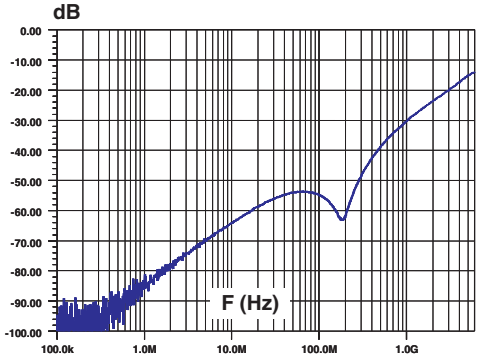


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

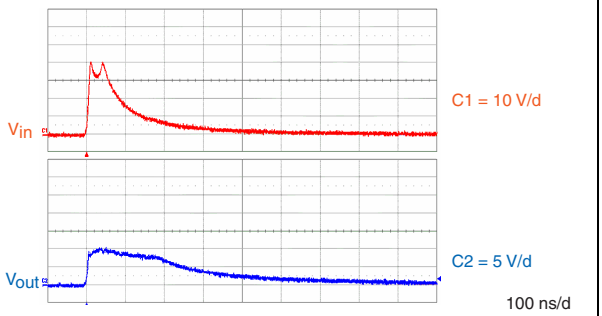


Figure 6. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

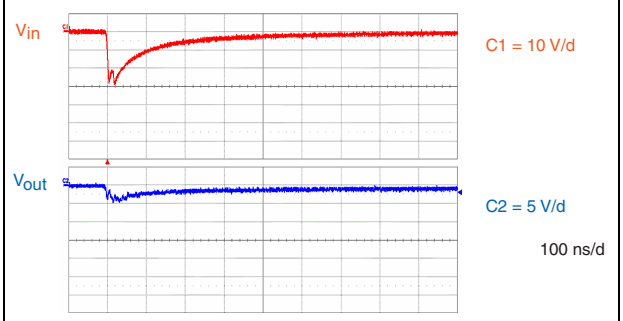
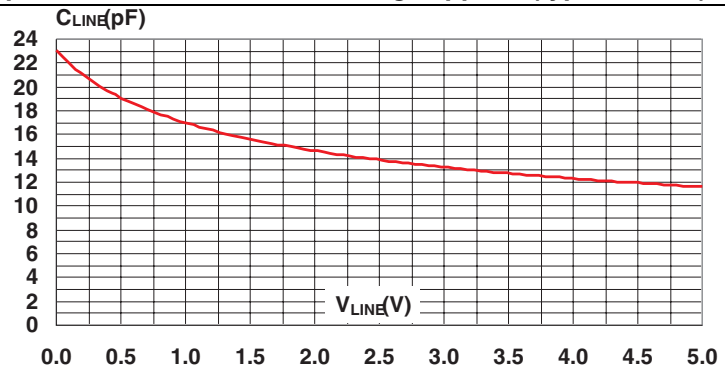
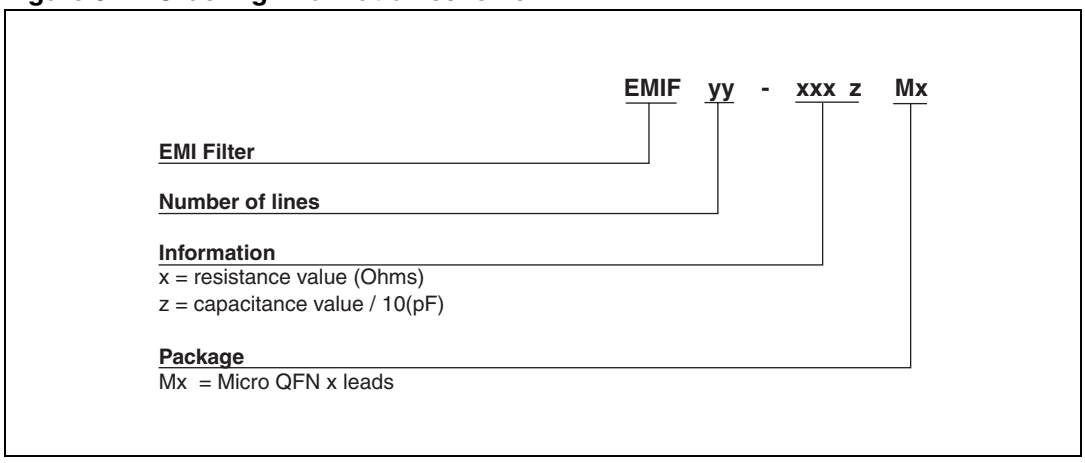


Figure 7. Line capacitance versus reverse voltage applied (typical value)



2 Ordering information scheme

Figure 8. Ordering information scheme

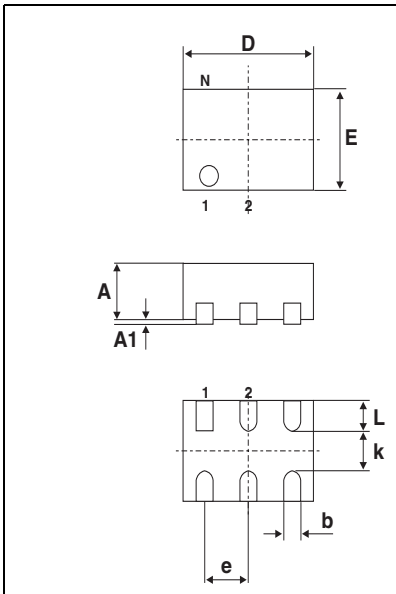


3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Table 3. QFN 1.7 x 1.5 package dimensions



Ref	Dimensions					
	Millimeters			inches		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.50	0.55	0.60	0.20	0.22	0.24
A1	0.00	0.02	0.05	0.00	0.01	0.02
b	0.15	0.18	0.25	0.06	0.07	0.10
D		1.70			0.67	
D2	0.9	1.00	1.10	0.35	0.39	0.43
E		1.50			0.59	
E2	0.30	0.40	0.50	0.12	0.16	0.24
e		0.40			0.16	
k	0.20			0.08		
L	0.25	0.30	0.35	0.10	0.12	0.14

Figure 9. Footprint

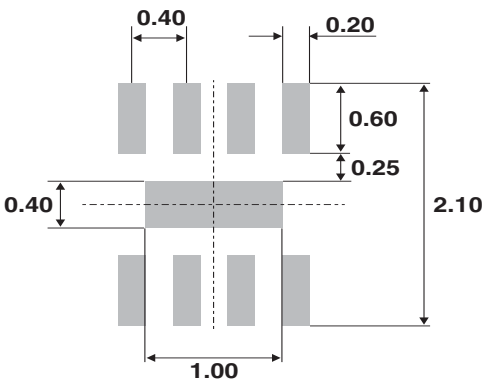


Figure 10. Marking

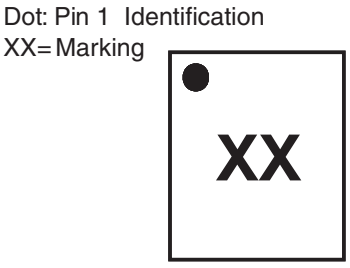
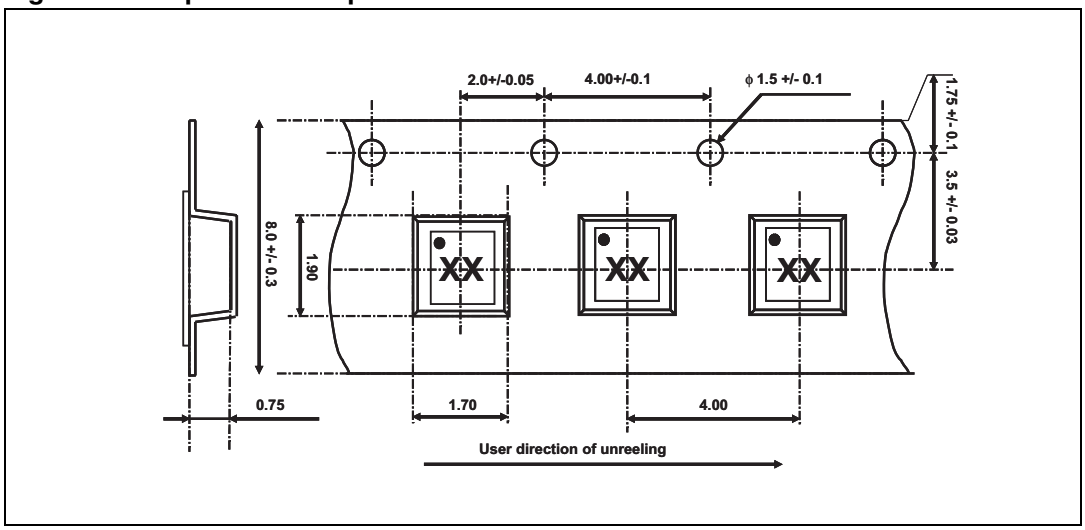


Figure 11. Tape and reel specification



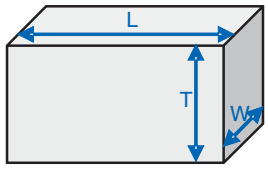
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 12. Stencil opening dimensions



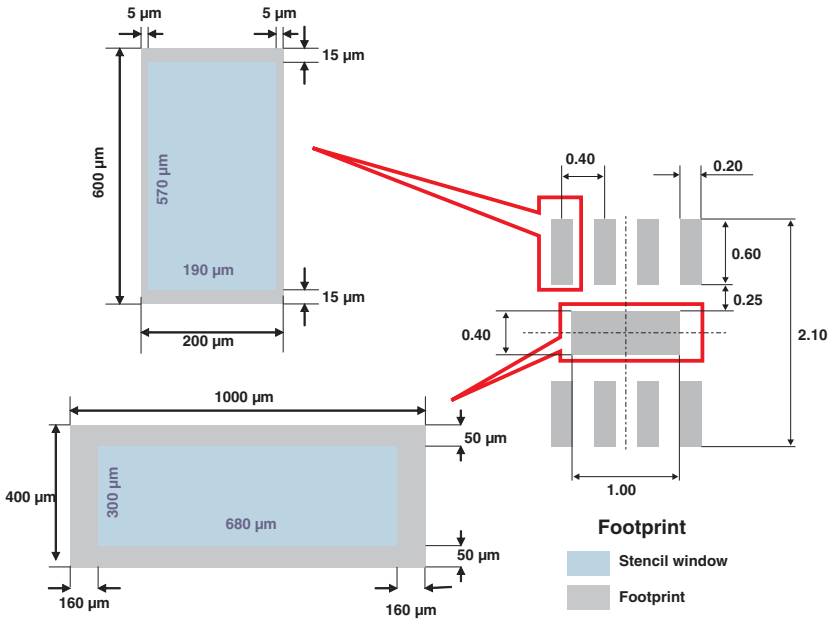
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 13. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

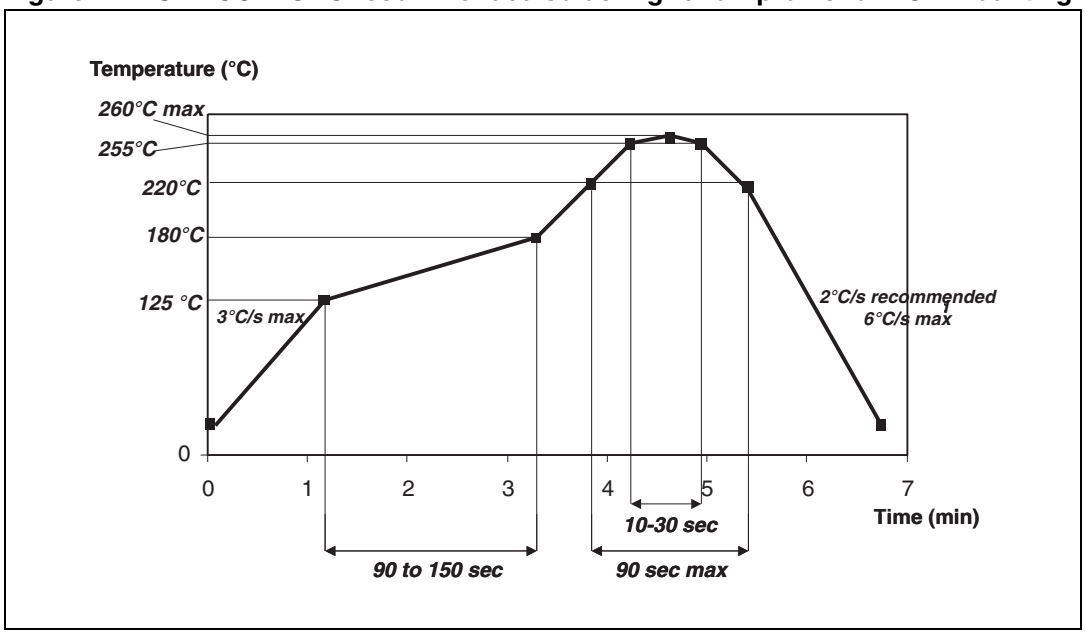
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF04-1502M8	G4(1)	Micro QFN	4 mg	3000	Tape and reel (7”)

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
12-Dec-2005	1	Initial release.
03-Jul-2006	2	Reformatted to current standard. Changed Figure 1 to show improved results.
01-Feb-2007	3	Added note on marking rotation in section 3. Package information.
26-Feb-2007	4	Pins range corrected on Micro QFN bottom view picture on page 1.
04-Feb-2008	5	Reformatted to current standards. Updated ECOPACK statement. Updated *Section 4: Recommendation on PCB assembly*.

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