National Semiconductor

July 29, 2009

DS90LT012AQ

Automotive LVDS Differential Line Receiver

General Description

The DS90LT012AQ is a single CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise, and high data rates. The devices are designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Swing (LVDS) technology

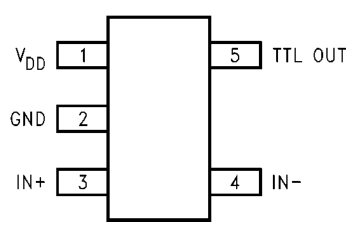
The DS90LT012AQ accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The DS90LT012AQ includes an input line termination resistor for point-to-point applications.

The DS90LT012AQ and companion LVDS line driver DS90LV011AQ provide a new alternative to high power PECL/ECL devices for high speed interface applications.

Features

- AECQ-100 Grade 1
- -40 to +125°C temperature range operation
- Compatible with ANSI TIA/EIA-644-A Standard
- >400 Mbps (200 MHz) switching rates
- 100 ps differential skew (typical)
- 3.5 ns maximum propagation delay
- Integrated line termination resistor (100Ω typical)
- Single 3.3V power supply design
- Power down high impedance on LVDS inputs
- LVDS inputs accept LVDS/CML/LVPECL signals
- Pinout simplifies PCB layout
- Low Power Dissipation (10mW typical @ 3.3V static)
- SOT-23 5-lead package

Connection Diagram



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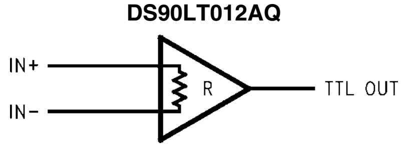
(Top View)
Order Number DS90LT012AQMF
See NS Package Number MF05A

Truth Table

INPUTS	OUTPUT
[IN+] – [IN–]	**TTL OUT**
$V_{ID} \geq 0V$	H
$V_{ID} \leq -0.1V$	L
Full Fail-safe OPEN/SHORT or Terminated	H

Functional Diagram



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Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +4V
Input Voltage (IN+, IN−)	−0.3V to +3.9V
Output Voltage (TTL OUT)	−0.3V to (V_{DD} + 0.3V)
Output Short Circuit Current	−100mA
Maximum Package Power Dissipation @ +25°C	
MF Package	794mW
Derate MF Package	7.22 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	138.5°C/W
θ_{JC}	107.0°C/W
Lead Temperature Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+135°C
ESD Rating	
HBM (Note 1)	>8 kV
MM (Note 2)	>250V
CDM (Note 3)	>1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.0	+3.3	+3.6	V
Operating Free Air Temperature (T_A)	−40	25	+125	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 5, 6)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} dependant on V_{DD}		IN+, IN−		−30	0	mV
V_{TL}	Differential Input Low Threshold				−100	−30		mV
V_{CM}	Common-Mode Voltage	V_{DD} = 3.0V to 3.6V, V_{ID} = 100mV			0.10		2.35	V
I_{IN}	Input Current	V_{IN} = +2.8V	V_{DD} = 3.6V or 0V		−10	±1	+10	μA
		V_{IN} = 0V			−10	±1	+10	μA
		V_{IN} = +3.6V	V_{DD} = 0V		−20		+20	μA
I_{IND}	Differential Input Current	V_{IN+} = +0.4V, V_{IN-} = +0V			3	3.9	4.4	mA
		V_{IN+} = +2.4V, V_{IN-} = +2.0V						
R_T	Integrated Termination Resistor					100		Ω
C_{IN}	Input Capacitance	IN+ = IN− = GND				3		pF
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		TTL OUT	2.4	3.1		V
		I_{OH} = −0.4 mA, Inputs terminated			2.4	3.1		V
		I_{OH} = −0.4 mA, Inputs shorted			2.4	3.1		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.3	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 7)			−15	−50	−100	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.7		V
I_{DD}	No Load Supply Current	Inputs Open		V_{DD}		5.4	9	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 6, 8, 9, 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15 pF	1.0	1.8	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High	V_{ID} = 200 mV	1.0	1.7	3.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$ (Note 11)	(*Figure 1* and *Figure 2*)	0	100	400	ps
t_{SKD3}	Differential Part to Part Skew (Note 12)		0	0.3	1.0	ns
t_{SKD4}	Differential Part to Part Skew (Note 13)		0	0.4	2.5	ns
t_{TLH}	Rise Time			350	800	ps
t_{THL}	Fall Time			175	800	ps
f_{MAX}	Maximum Operating Frequency (Note 14)			250		MHz

Note 4: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 5: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified (such as V_{ID}).

Note 6: All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.

Note 7: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 8: These parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.

Note 9: C_L includes probe and jig capacitance.

Note 10: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3 ns for IN±.

Note 11: t_{SKD1} is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.

Note 12: t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.

Note 13: t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max – Min| differential propagation delay.

Note 14: f_{MAX} generator input conditions: $t_r = t_f$ < 1 ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35 peak to peak). Output criteria: 60%/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.4V), load = 15 pF (stray plus probes).

Parameter Measurement Information

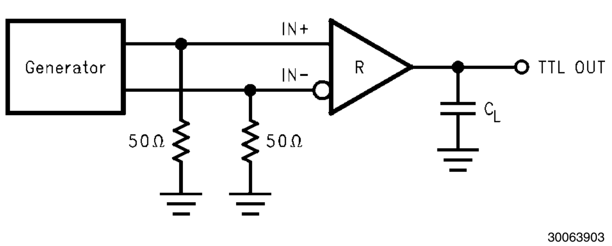


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

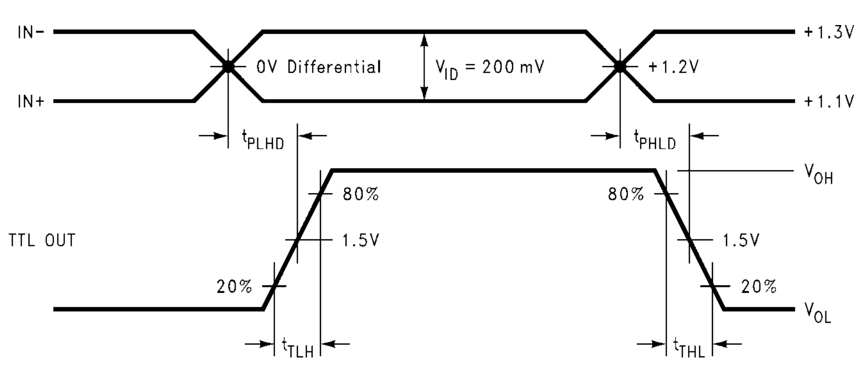


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

Typical Applications

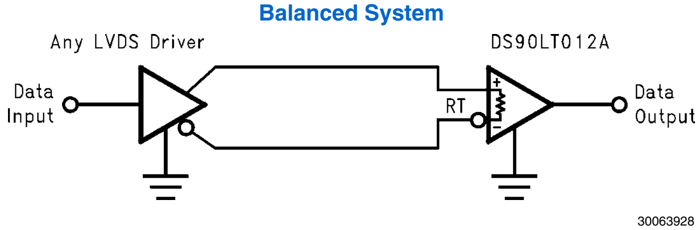


FIGURE 3. Point-to-Point Application (DS90LT012AQ)

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-003), AN-808, AN-977, AN-971, AN-916, AN-805, AN-903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 3*. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. The internal termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LT012AQ differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to V_{DD}, but exceeding V_{DD} will turn on the ESD protection circuitry which will clamp the bus voltages.

POWER DECOUPLING RECOMMENDATIONS

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1μF and 0.001μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10μF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC BOARD CONSIDERATIONS

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

DIFFERENTIAL TRACES

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

TERMINATION

The DS90LT012AQ integrates the terminating resistor for point-to-point applications. The resistor value will be between 90Ω and 133Ω.

THRESHOLD

The LVDS Standard (ANSI/TIA/EIA-644-A) specifies a maximum threshold of ±100mV for the LVDS receiver. The DS90LT012AQ supports an enhanced threshold region of

−100mV to 0V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in *Figure 4*. The typical DS90LT012AQ LVDS receiver switches at about −30mV. Note that with V_{ID} = 0V, the output will be in a HIGH state. With an external fail-safe bias of +25mV applied, the typical differential noise margin is now the difference from the switch point to the bias point. In the example below, this would be 55mV of Differential Noise Margin (+25mV − (−30mV)). With the enhanced threshold region of −100mV to 0V, this small external fail-safe biasing of +25mV (with respect to 0V) gives a DNM of a comfortable 55mV. With the standard threshold region of ±100mV, the external fail-safe biasing would need to be +25mV with respect to +100mV or +125mV, giving a DNM of 155mV which is stronger fail-safe biasing than is necessary for the DS90LT012AQ. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

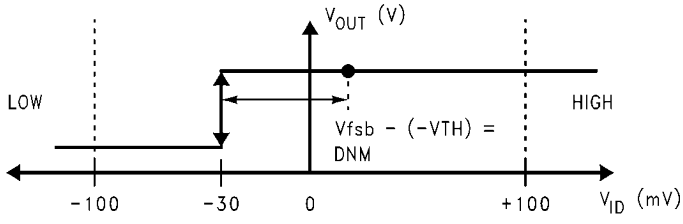


FIGURE 4. VTC of the DS90LT012AQ LVDS Receiver

FAIL SAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to VDD thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194, “Failsafe Biasing of LVDS Interfaces” for more information.

PROBING LVDS TRANSMISSION LINES

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

CABLES AND CONNECTORS, GENERAL COMMENTS

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

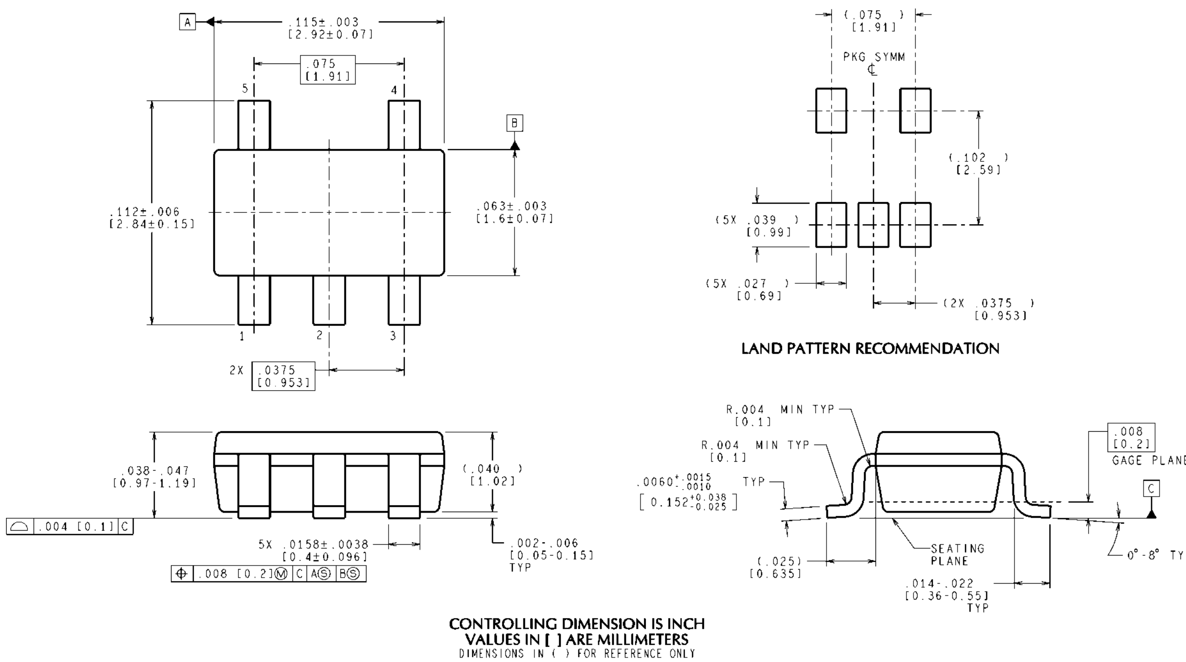
Pin Descriptions

Package Pin Number SOT23	Pin Name	Description
4	IN−	Inverting receiver input pin
3	IN+	Non-inverting receiver input pin
5	TTL OUT	Receiver output pin
1	V_{DD}	Power supply pin, +3.3V ± 0.3V
2	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40°C to +125°C	MF05A	DS90LT012AQMF

Physical Dimensions inches (millimeters) unless otherwise noted



MF05A (Rev D)

5-Lead SOT23, JEDEC MO-178, 1.6mm
Order Number DS90LT012AQMF
NS Package Number MF05A

Notes

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