Rev 0; 5/04

DALLAS SEMICONDUCTOR MAXIM

Dual, NV, Variable Resistors with User EEPROM

DS3902

General Description

The DS3902 features a dual, nonvolatile (NV), low temperature-coefficient, variable digital resistor with 256 user-selectable positions. The DS3902 can operate over a wide supply range of 2.4V to 5.5V, and communication with the device is achieved through an I²C™-compatible serial interface. Internal address settings allow the DS3902 slave address to be programmed to one of 128 possible addresses. The low cost and the small size of the DS3902 make it an ideal replacement for conventional mechanical-trimming resistors.

Applications

Optical Transceivers

Optical Transponders

Instrumentation and Industrial Controls

RF Power Amps

Audio Power-Amp Biasing

Replacement for Mechanical Variable Resistors and DIP Switches

Features

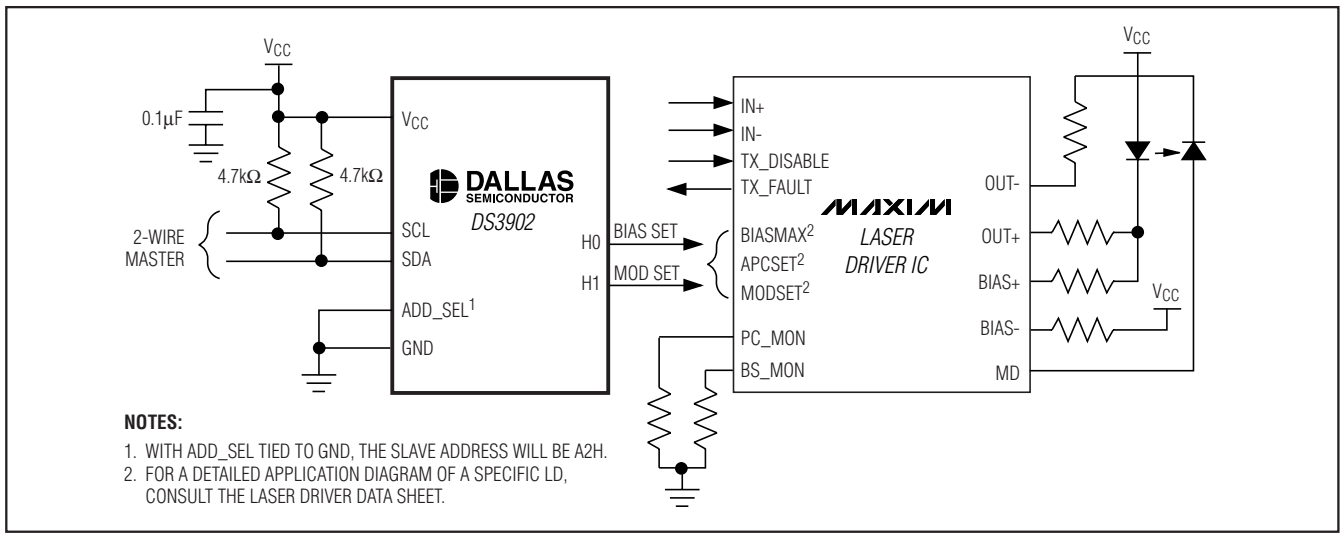
- **Dual 256-Position Linear Digital Resistors**
- **Available as 50kΩ/30kΩ or 50kΩ/15kΩ**
- **Resistor Settings Stored in NV Memory**
- **Low Temperature Coefficient**
- **I²C-Compatible Serial Interface**
- **Wide Operating Voltage (2.4V to 5.5V)**
- **Software Write Protection**
- **User-EEPROM Memory**
- **Programmable Slave Address**
- **Operating Temperature Range: -40°C to +95°C**
- **Small 8-Pin µSOP Package**

Ordering Information

PART	RESISTOR VALUES (R0, R1)	TOP BRAND	PIN-PACKAGE
DS3902U-530	30kΩ, 50kΩ	3902A	8 µSOP
DS3902U-515	15kΩ, 50kΩ	3902B	8 µSOP

**Add /T&R for Tape & Reel orders.*

Typical Operating Circuit



NOTES:

1. WITH ADD_SEL TIED TO GND, THE SLAVE ADDRESS WILL BE A2H.
2. FOR A DETAILED APPLICATION DIAGRAM OF A SPECIFIC LD, CONSULT THE LASER DRIVER DATA SHEET.

Pin Configuration appears at end of data sheet.

Dual, NV, Variable Resistors with User EEPROM

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, SDA, SCL, H0, and H1 Relative to Ground .....-0.5V to +6.0V
Voltage Range on ADD_SEL Relative to Ground .....-0.5V to (V_{CC} + 0.5V), not to exceed 6.0V
Resistor Current 3mA

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +95°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.4		+5.5	V
Input Logic 1 (SDA, SCL, ADD_SEL)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL, ADD_SEL)	V_{IL}		-0.3		+0.3 x V_{CC}	V
Resistor Inputs	H0, H1		-0.3		+5.5	V
Resistor Current	I_{RES}				3	mA

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{STBY}	(Note 2)			200	µA
Input Leakage	I_L		-1		+1	µA
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V
	V_{OL2}	6mA sink current	0		0.6	

ANALOG RESISTOR CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resistance Tolerance		T_A = +25°C	-20		+20	%
Position 0 Resistance				160	250	Ω
Absolute Linearity		(Note 3)	-1		+1	LSB
Relative Linearity		(Note 4)	-0.75		+0.75	LSB
Temperature Coefficient		At position FFh. (Notes 5, 6)	-300		+300	ppm/°C
High-Impedance Resistor Current	I_{RHIZ}	H0, H1 = V_{CC}	-1		+1	µA

AC ELECTRICAL CHARACTERISTICS (Figure 1)

(V_{CC} = +2.4V to +5.5V, T_A = -40°C to +95°C, unless otherwise noted. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 7)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			µs
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 8)	20 + 0.1 x C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 8)	20 + 0.1 x C_B		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 8)			400	pF
EEPROM Write Time	t_{WR}	(Note 9)			10	ms
Input Capacitance	C_I			5		pF
Startup Time	t_{ST}	(Note 6)			2	ms

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Writes		+70°C (Note 6)	50,000			

Note 1: All voltages referenced to ground.

Note 2: I_{STBY} specified for the inactive state measured with SDA = SCL = V_{CC}, ADD_SEL = GND, and with H0 and H1 floating.

Note 3: Absolute linearity is the difference of measured value from expected value at resistor position. Expected value is from the measured minimum position to measured maximum position.

Note 4: Relative linearity is the deviation of an LSB resistor setting change vs. the expected LSB change. Expected LSB slope of the straight line is the typical operating curves from the measured minimum position to measured maximum position.

Note 5: See the *Typical Operating Characteristics* section.

Note 6: Guaranteed by design.

Note 7: Timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard mode.

Note 8: C_B—total capacitance of one bus line in picofarads.

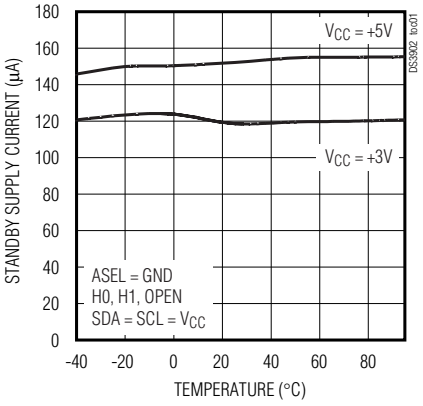
Note 9: EEPROM write begins after a STOP condition occurs.

Dual, NV, Variable Resistors with User EEPROM

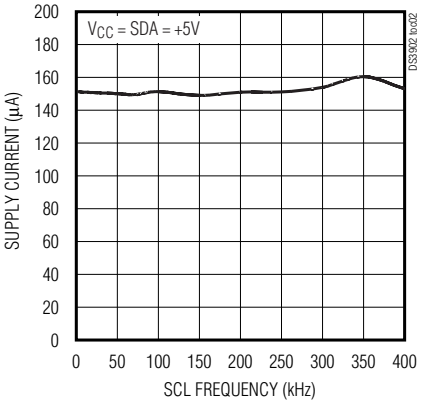
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

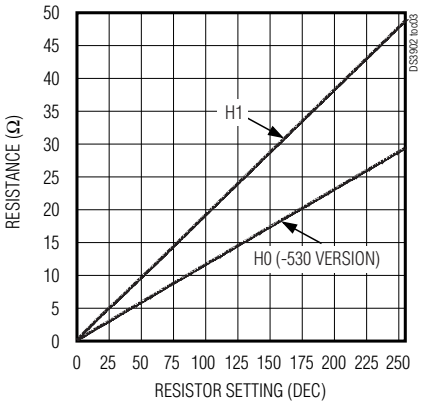
STANDBY SUPPLY CURRENT vs. TEMPERATURE



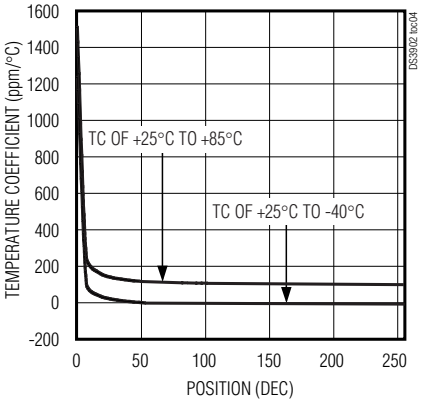
SUPPLY CURRENT vs. SCL FREQUENCY



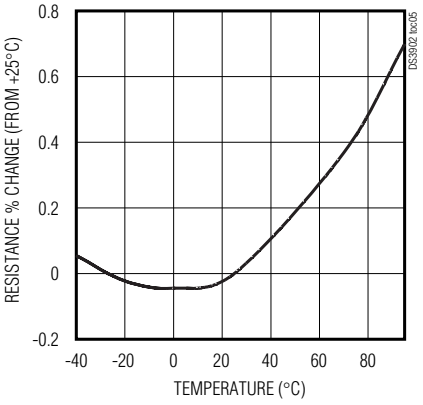
RESISTANCE vs. RESISTOR SETTING



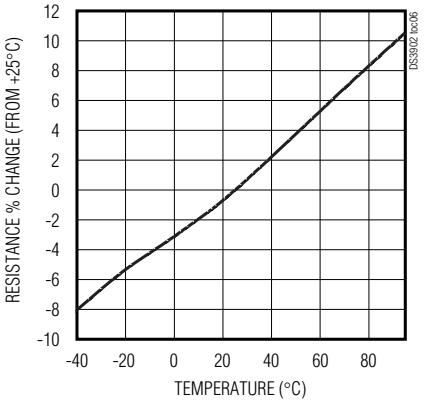
TEMPERATURE COEFFICIENT vs. POSITION



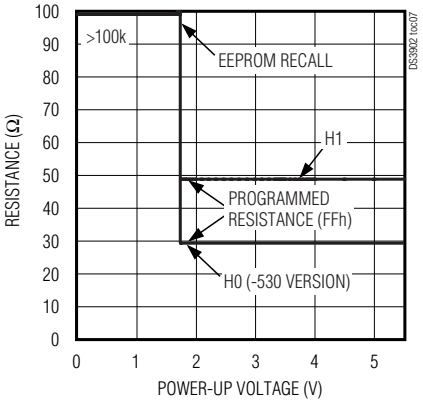
POSITION FFh RESISTANCE PERCENT CHANGE FROM +25°C vs. TEMPERATURE



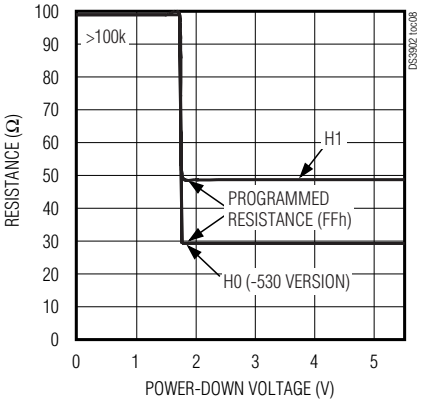
POSITION 00h RESISTANCE PERCENT CHANGE FROM +25°C vs. TEMPERATURE



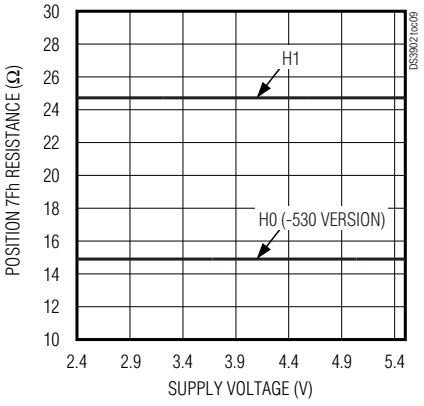
H0, H1 RESISTANCE vs. POWER-UP VOLTAGE



H0, H1 RESISTANCE vs. POWER-DOWN VOLTAGE



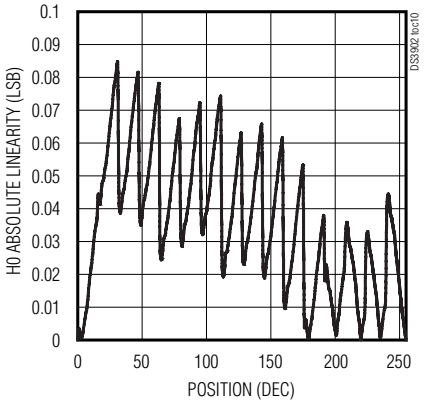
POSITION 7Fh RESISTANCE vs. SUPPLY VOLTAGE



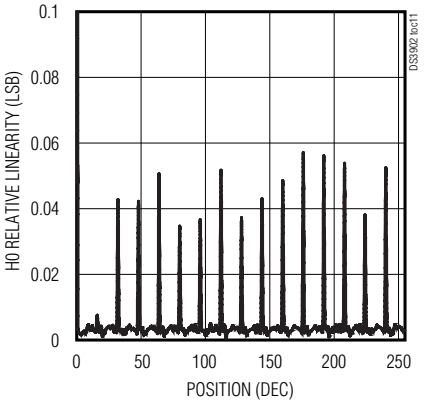
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

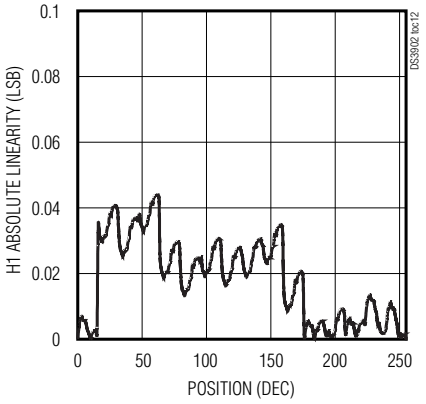
H0 ABSOLUTE LINEARITY vs. POSITION



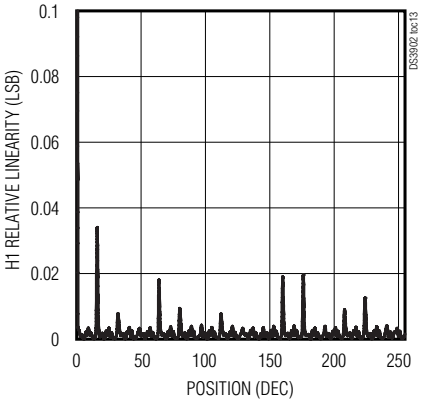
H0 RELATIVE LINEARITY vs. POSITION



H1 ABSOLUTE LINEARITY vs. POSITION



H1 RELATIVE LINEARITY vs. POSITION



Dual, NV, Variable Resistors with User EEPROM

Pin Description

PIN	NAME	FUNCTION
1	H0	Resistor 0 High Terminal
2	SDA	I²C Serial-Data Open-Drain Input/Output
3	SCL	I²C Serial-Clock Input
4	GND	Ground
5	ADD_SEL	Address Select
6	H1	Resistor 1 High Terminal
7	N.C.	No Connection
8	V_{CC}	Power-Supply Voltage

Detailed Description

The block diagram of the DS3902 is shown in the *Block Diagram* section. Detailed descriptions of major components follow.

Memory Map

A memory map of the DS3902 is shown in Table 1.

Resistors

The DS3902 contains two, 256-position (plus High-Z), NV, variable digital resistors. Pins H0 and H1 are the high terminals of Resistor 0 and Resistor 1, respectively. The low terminals of both resistors are tied to ground internally. The resistors are programmed using the I²C serial interface (see the Resistor 0 and Resistor 1 regis-

Block Diagram

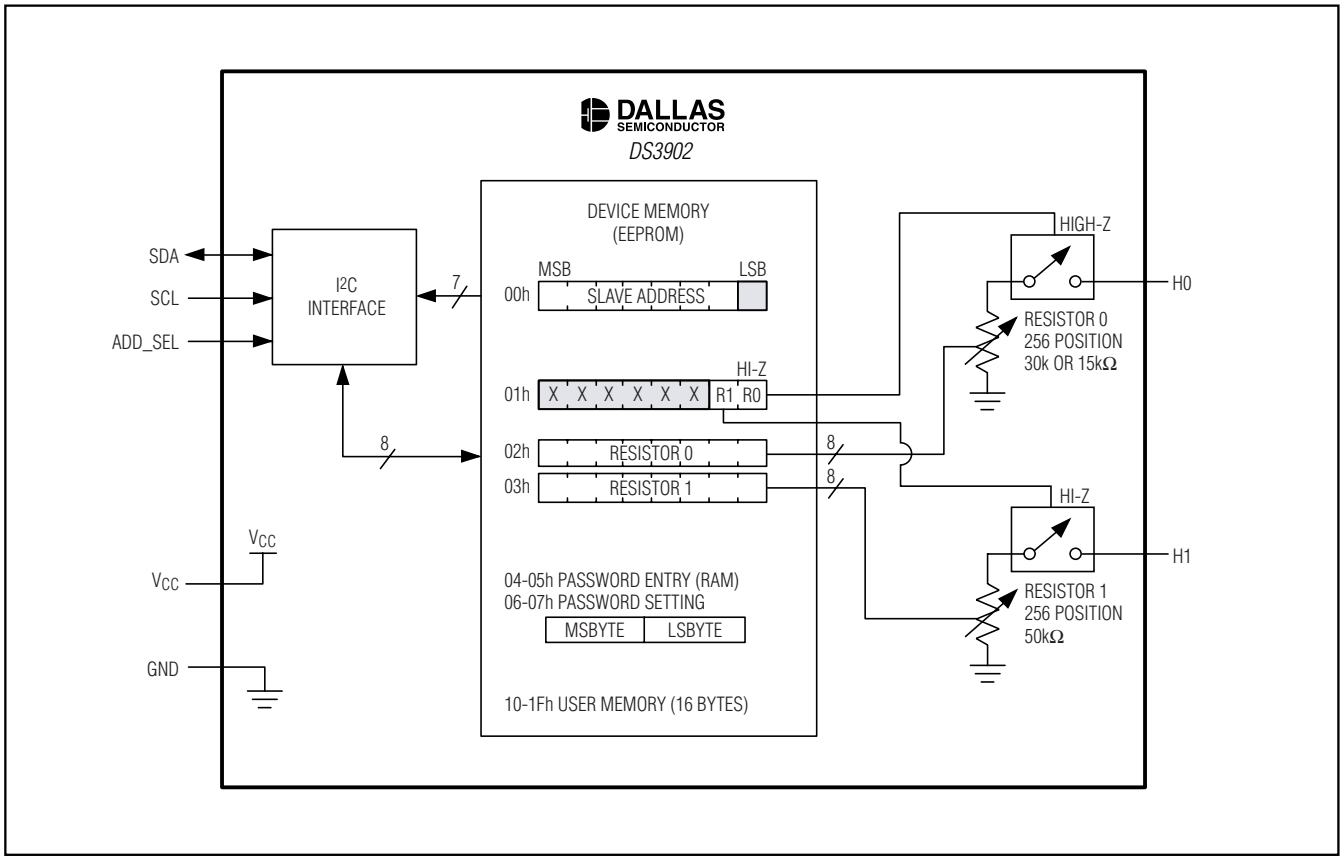


Table 1. Memory Map

DESCRIPTION	ADDR	BINARY MSB							LSB	FACTORY DEFAULT	ACCESS W/O PW	ACCESS W/PW	TYPE
Slave Address	00h	SLAVE ADDRESS							X	A0h	R	R/W	EEPROM
Configuration	01h	X	X	X	X	X	X	R1	R0	00h	R	R/W	EEPROM
Resistor 0	02h	b7	b6	b5	b4	b	b2	b1	b0	7Fh	R	R/W	EEPROM
Resistor 1	03h	b7	b6	b5	b4	b3	b2	b1	b0	7Fh	R	R/W	EEPROM
Password Entry	04h	PW MSB								FFh	W	W	RAM
	05h	PW LSB								FFh			
Password Setting	06h	PW MSB								FFh	—	R/W	EEPROM
	07h	PW LSB								FFh			
No Memory	08h–0Fh	—								—	—	—	—
User Memory	10h–1Fh	16 BYTES OF GENERAL PURPOSE EEPROM								ALL FFh	R	R/W	EEPROM

X = Don't care.

ters in the Memory Map). The Configuration register contains a bit (R0 and R1) for each resistor to enable the High-Z state. When one of the High-Z bits is written to a '1', the corresponding resistor goes High-Z. When written back to a '0', the resistor goes back to the programmed resistance. Writing the Resistor 0 or Resistor 1 register to 00h, sets the respective resistor to its minimum position (and minimum resistance). This value can be found in the *Analog Resistor Characteristics* electrical table. Writing Resistor 0 or Resistor 1 to FFh, sets the resistor to its maximum resistance. The nominal resistance (in ohms) of the resistors can be found in the ordering information table at the beginning of this data sheet.

When the DS3902 is powered up, the resistors are both set to High-Z instantaneously while the settings stored in EEPROM are recalled.

Slave Address & ADD_SEL Pin

The I²C slave address of the DS3902 depends on the state of the ADD_SEL pin. If this pin is low, then the slave address is A2h. If the ADD_SEL pin is high, then the slave address is determined by the value stored in EEPROM at address 00h. Refer to the *Memory Map* to see the factory default of the slave address. The seven most significant bits are used (the LSB is not used because it is in the bit position of the R/$\overline{W}$ bit) to allow the slave address to be programmed to one of 128 possible addresses. The I²C interface is described in detail in a later section.

Software Write Protection

Software write protection is enabled by creating a two byte password and writing it to the Password Setting register (06h to 07h). When write protected, all memory locations can be read, but only the Password Entry register (04h to 05h) can be written. When the correct password is entered, then the memory can be written to. Refer to the *Memory Map* to see which registers can be read/written with and without the password (PW). When shipped from the factory, the password setting is FFFFh. Likewise, every time the device is powered-up the Password Entry register (which is RAM, not EEPROM) defaults to FFFFh, giving full access to the device. If write protection is not desired, then leave the Password Setting at the factory default and ignore the Password Entry register.

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, START, and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic high states. When the bus is idle it often initiates a low-power mode for slave devices.

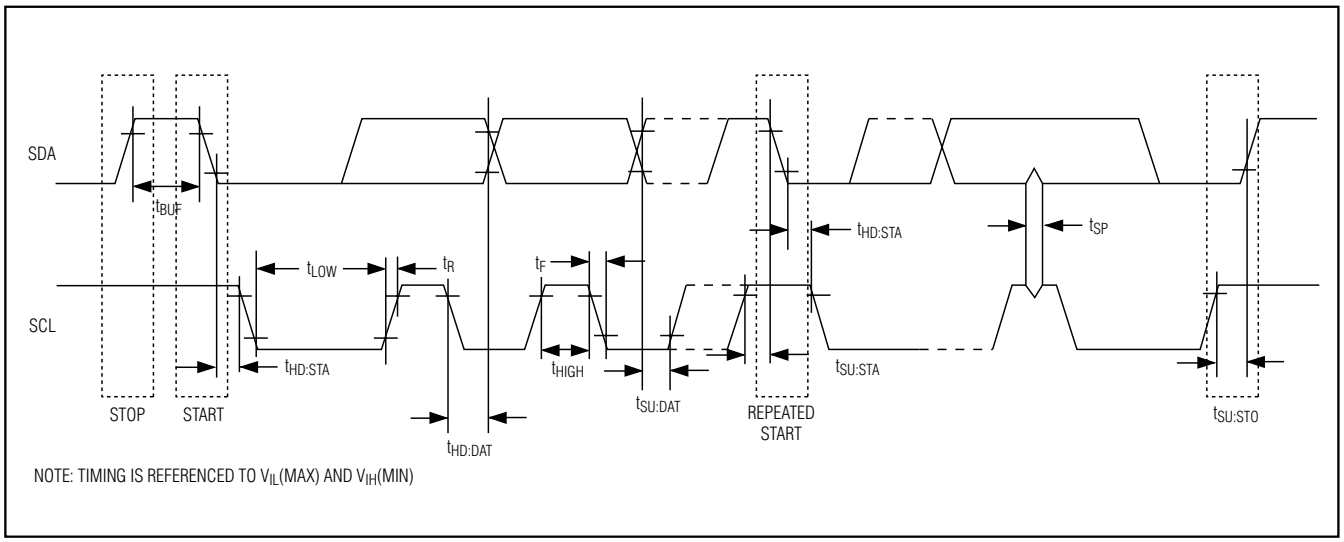


Figure 1. I²C Timing Diagram

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See the timing diagram for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See the timing diagram for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it immediately initiates a new data transfer following the current one. Repeated STARTS are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (see Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 1) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 1) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8-bits of information transferred from the master to the slave (MSB first) plus a 1-bit acknowledgement from the slave to the master. The 8-bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (MSB first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave addressing byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7-bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3902's slave address depends on the state of the ADD_SEL pin. If ADD_SEL is low, then the slave address byte is A2h, where the LSB is the R/$\overline{W}$ bit. If the R/$\overline{W}$ bit is 0 (such as in A2h), then master indicates it will write data to the slave. If R/$\overline{W}$ = 1 (A3h in this case), the master will read data from the slave. If an incorrect slave address is written, the DS3902 will assume the master is communicating with another I²C device and ignore the communication until the next START condition is sent.

On the other hand, if the ADD_SEL pin is a logic high, then the slave address byte is determined by the Slave Address register saved in EEPROM (address 00h). The LSB of the register is not used since it is in the bit location of the R/$\overline{W}$ bit. Refer to the *Slave Address and ADD_SEL Pin* section for more information.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data and generate a STOP condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 2 data bytes and generates a STOP condition.

The DS3902 is capable of writing 1 or 2 bytes (1 page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 2-byte page. Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row. Each row begins on even memory addresses.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, and then wait for the bus free or EEPROM write time to elapse. Then the master may generate a new START condition, write the slave address byte (R/$\overline{W}$ = 0), and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time an EEPROM page is written, the DS3902 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeated addressing the DS3902, which allows the next page to be written as soon as the DS3902 is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_W to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur, the DS3902 will write the whole EEPROM memory page even if only a single byte on the page was modified. Writes that do not modify all 2-bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page one byte at a time will wear the EEPROM out two times faster than writing the entire page at once. The DS3902's EEPROM write cycles are specified in the Nonvolatile Memory Characteristics table. The specification shown is at the worst case temperature. It is capable of handling approximately 10x that many writes at room temperature.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Dual, NV, Variable Resistors with User EEPROM

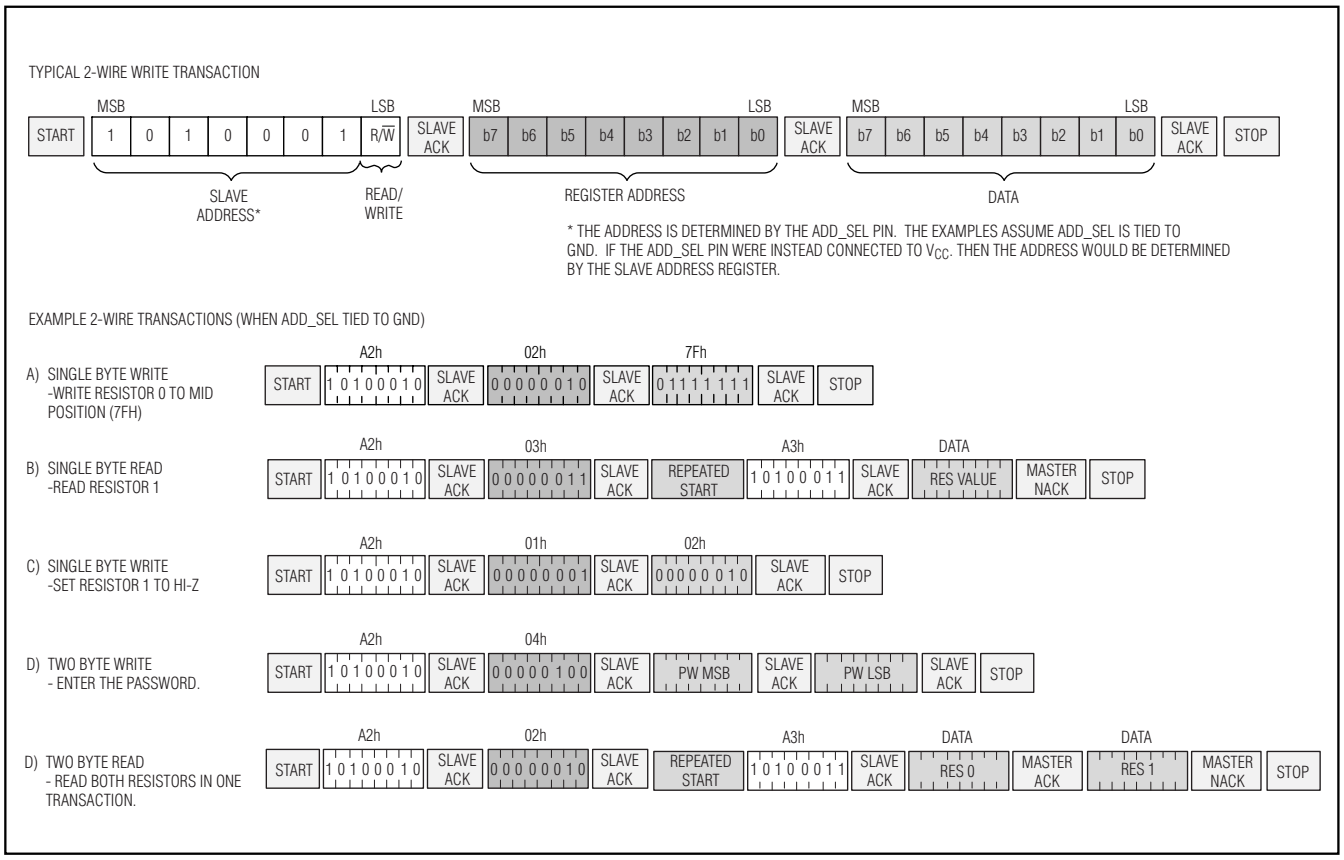


Figure 2. I²C Communication Examples

See Figure 2 for a read example using the repeated START condition to specify the starting memory location.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it NACKs to indicate the end of the transfer and generates a stop condition. This can be done with or without modifying the address counter's location before the read cycle.

Application Information

Using the Resistors as a Switch

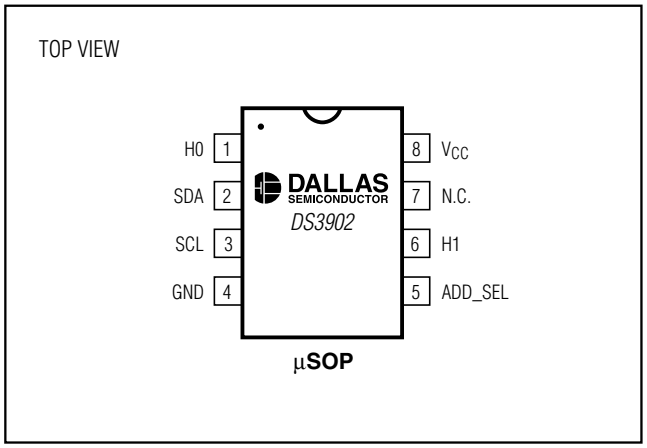
By taking advantage of the resistor's high-impedance state, the resistors can be used as a digitally controlled switch. Setting the resistor to position 0 is equivalent to a logic low level. By using an external pull-up resistor, a logic high level can be generated by setting the resistor to the High-Z state.

Power Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor is used on the IC power supply pins. Typical values of decoupling capacitors are 0.01µF and 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the IC to minimize lead inductance.

Dual, NV, Variable Resistors with User EEPROM

Pin Configuration



Chip Topology

TRANSISTOR COUNT: 11252

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.