DRV5021 Low-Voltage, Unipolar, Digital-Switch Hall Effect Sensor

1 Features

- Digital Unipolar-Switch Hall Sensor
- 2.5-V to 5.5-V Operating V_{CC} Range
- Magnetic Sensitivity Options (B_{OP}, B_{RP}):
  - DRV5021A1: 2.9 mT, 1.8 mT
  - DRV5021A2: 9.2 mT, 7.0 mT
  - DRV5021A3: 17.9 mT, 14.1 mT
- Fast 30-kHz Sensing Bandwidth
- Open-Drain Output Capable of 20 mA
- Optimized Low-Voltage Architecture
- Integrated Hysteresis to Enhance Noise Immunity
- Operating Temperature Range: –40°C to +125°C
- Standard Industry Package:
  - Surface-Mount SOT-23

2 Applications

- Home Appliances
- Industrial Valves, Solenoids
- Limit Switches
- General Proximity Sensing
- Brushed DC Motor Feedback
- Docking Detection
- Door Open and Close Detection
- Pulse Counting

3 Description

The DRV5021 device is a low-voltage, digital-switch, Hall effect sensor for high-speed applications. Operating from a 2.5-V to 5.5-V power supply, the device senses magnetic flux density, and gives a digital output based on predefined magnetic thresholds.

This device senses magnetic fields perpendicular to the face of the package. When the applied magnetic flux density exceeds the magnetic operate point (B_{OP}) threshold, the open-drain output of the device drives a low voltage. When the flux density decreases to less than the magnetic release point (B_{RP}) threshold, the output goes to high impedance. The hysteresis resulting from the separation of B_{OP} and B_{RP} helps prevent output errors caused by input noise. This configuration makes system designs more robust against noise interference.

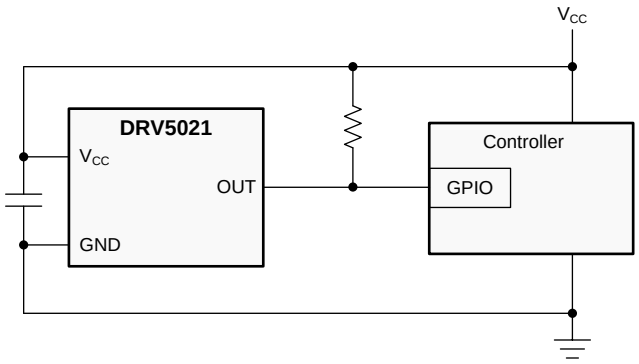
The device operates consistently across a wide ambient temperature range of –40°C to +125°C.

Device Information(1)

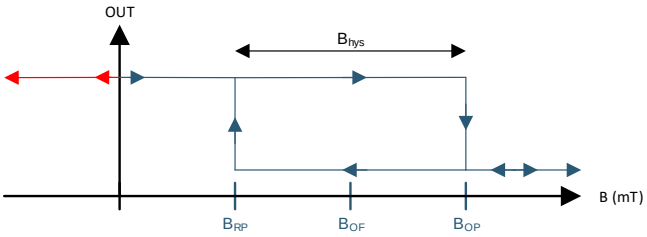
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5021	SOT-23 (3)	2.90 mm × 1.30 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Schematic



Magnetic Response



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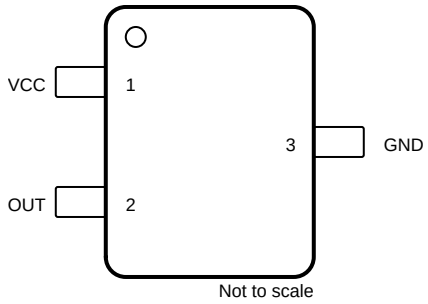
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2018	*	Initial release.

5 Pin Configuration and Functions

DBZ Package
3-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DBZ		
GND	3	GND	Ground pin
OUT	2	Output	Hall sensor open-drain output. The open drain requires a pullup resistor.
V_{CC}	1	Power	2.5-V to 5.5-V power supply. Bypass this pin to the GND pin with a 0.1-μF (minimum) ceramic capacitor rated for V_{CC}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VCC)	–0.3	6.0	V
Output voltage (OUT)	–0.3	6.0	V
Output current (OUT)		30	mA
Magnetic flux density, B_{MAX}		Unlimited	T
Operating junction temperature, T_J	–40	140	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage range	2.5	5.5	V
V_O	Output pin voltage	0	5.5	V
I_{OUT}	Output sinking current	0	20	mA
T_A	Operating ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV5021 SOT-23 (DBZ) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	356	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	128	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94	°C/W
Y_{JT}	Junction-to-top characterization parameter	11.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	92	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

for V_{CC} = 2.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{CC}	Operating supply current			2.3	2.8	mA
t_{ON}	Power-on time			40	70	µs
t_d	Propagation delay time(1)	B = B_{RP} – 10 mT to B_{OP} + 10 mT in 1 µs		13	25	µs
I_{OZ}	High-impedance output leakage current	5.5 V applied to OUT, while OUT is high-impedance			100	nA
V_{OL}	Low-level output voltage	I_{OUT} = 20 mA		0.15	0.4	V
$R_{DS(on)}$	Output FET resistance	I_{OUT} = 5 mA, V_{CC} = 3.3 V		8		Ω

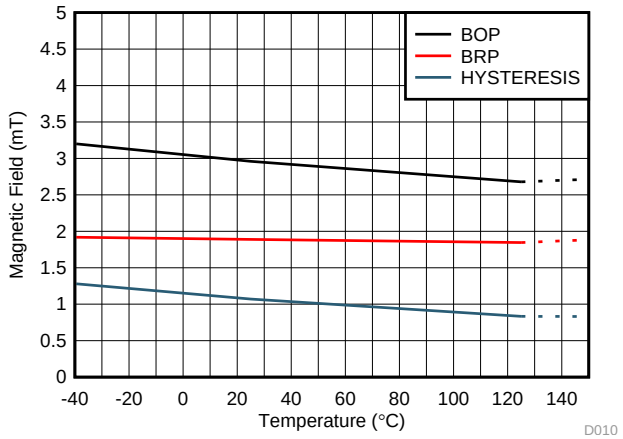
(1) See the *Propagation Delay* section for more information.

6.6 Magnetic Characteristics

for V_{CC} = 2.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

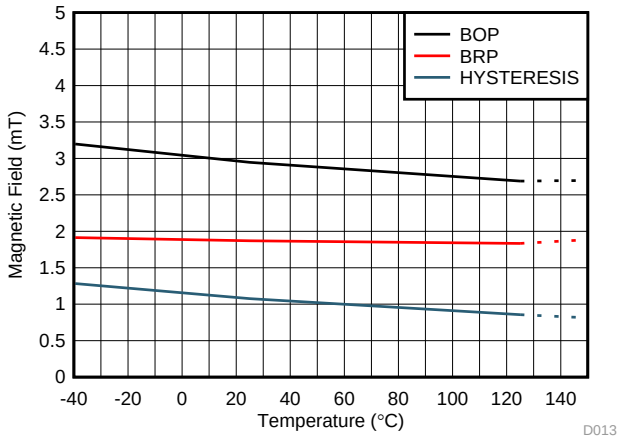
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DRV5021A1, DRV5021A2, DRV5021A3						
f_{BW}	Sensing bandwidth			30		kHz
DRV5021A1						
B_{OP}	Magnetic threshold Operate Point		1.4	2.9	4.4	mT
B_{RP}	Magnetic threshold Release Point		0.4	1.8	3.0	mT
B_{HYS}	Magnetic hysteresis: $\lvert B_{OP} - B_{RP} \rvert$		0.2	1.1	2.5	mT
DRV5021A2						
B_{OP}	Magnetic threshold Operate Point		5.5	9.2	12.5	mT
B_{RP}	Magnetic threshold Release Point		3.6	7.0	9.5	mT
B_{HYS}	Magnetic hysteresis: $\lvert B_{OP} - B_{RP} \rvert$		1.1	2.2	4.5	mT
DRV5021A3						
B_{OP}	Magnetic threshold Operate Point		9.5	17.9	22.7	mT
B_{RP}	Magnetic threshold Release Point		6.7	14.1	18.5	mT
B_{HYS}	Magnetic hysteresis: $\lvert B_{OP} - B_{RP} \rvert$		1.6	3.8	6.0	mT

6.7 Typical Characteristics



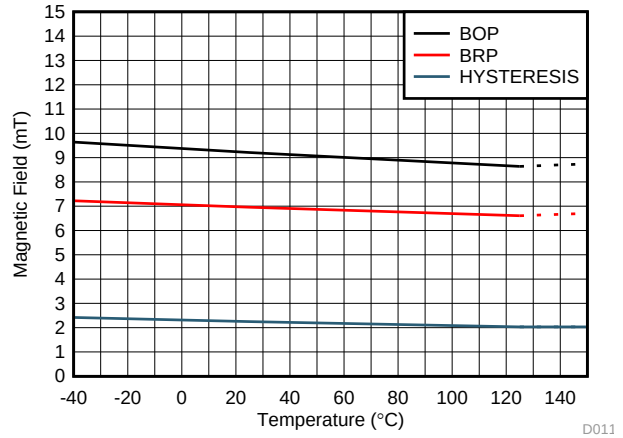
DRV5021A1, V_{CC} = 3.3 V

Figure 1. Magnetic Threshold vs Temperature



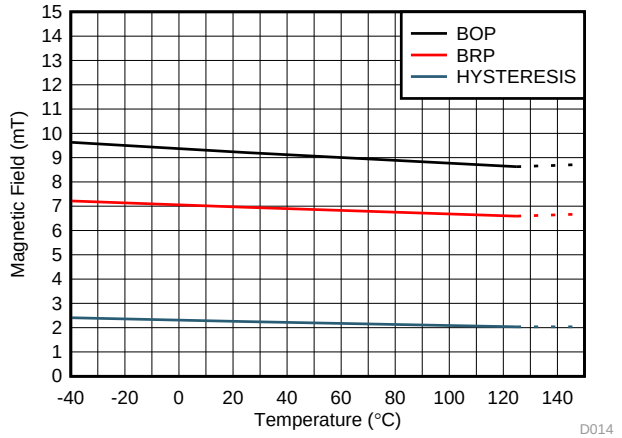
DRV5021A1, V_{CC} = 5.0 V

Figure 2. Magnetic Threshold vs Temperature



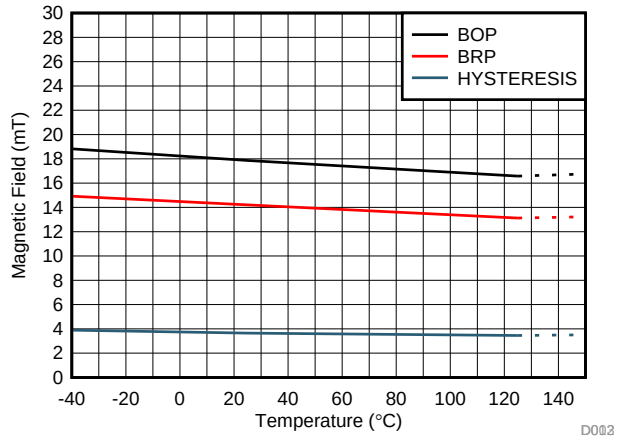
DRV5021A2, V_{CC} = 3.3 V

Figure 3. Magnetic Threshold vs Temperature



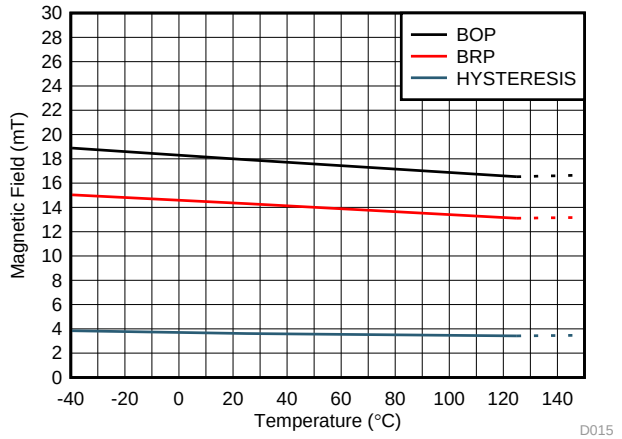
DRV5021A2, V_{CC} = 5.0 V

Figure 4. Magnetic Threshold vs Temperature



DRV5021A3, V_{CC} = 3.3 V

Figure 5. Magnetic Threshold vs Temperature



DRV5021A3, V_{CC} = 5.0 V

Figure 6. Magnetic Threshold vs Temperature

Typical Characteristics (continued)

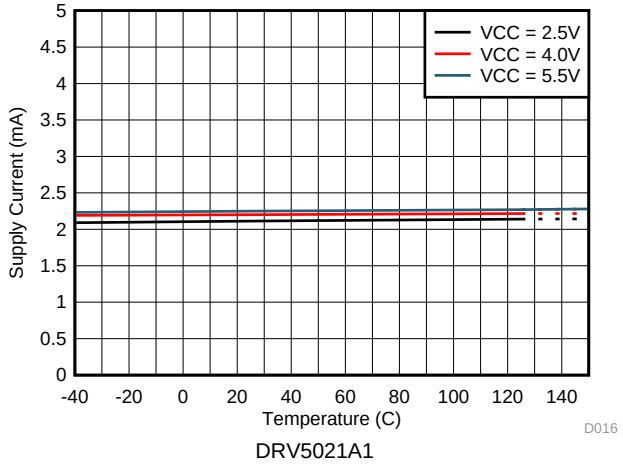


Figure 7. Supply Current vs Temperature

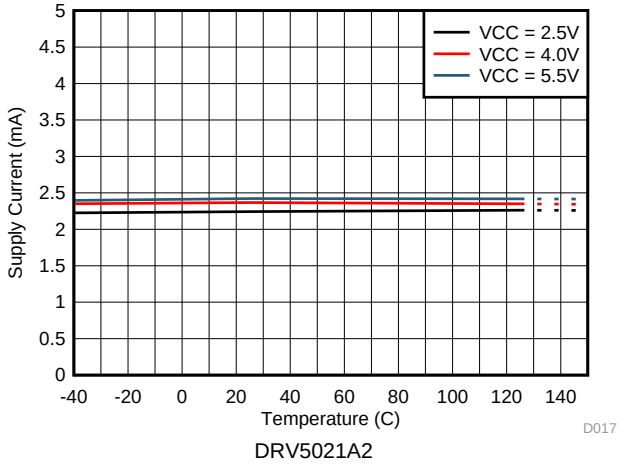


Figure 8. Supply Current vs Temperature

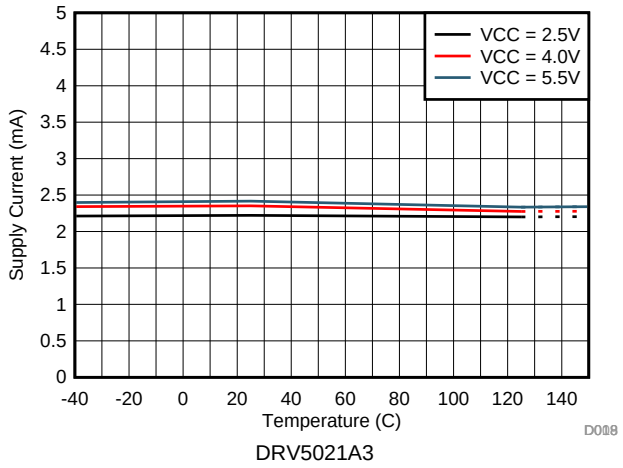


Figure 9. Supply Current vs Temperature

7 Detailed Description

7.1 Overview

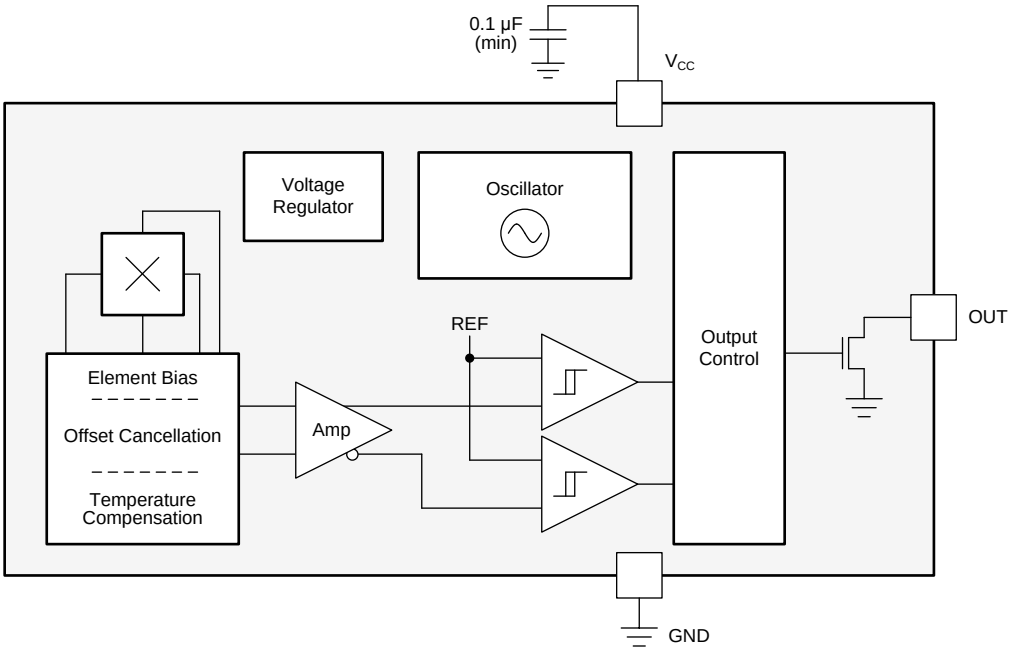
The DRV5021 device is a spinning-current Hall sensor with a digital output for magnetic-sensing applications. The DRV5021 can be powered with a supply voltage between 2.5 V and 5.5 V.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field. The output state depends on the magnetic field perpendicular to the package.

A strong south pole near the marked side of the package causes the output to pull low. A weak south pole, the absence of a field, or any north pole makes the output high impedance. Hysteresis is included in between the operate point and the release point to prevent toggling near the magnetic threshold.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC}, or to a different voltage supply. This feature allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

As shown in Figure 10, the DRV5021 is sensitive to the magnetic field component that is perpendicular to the top of the package.

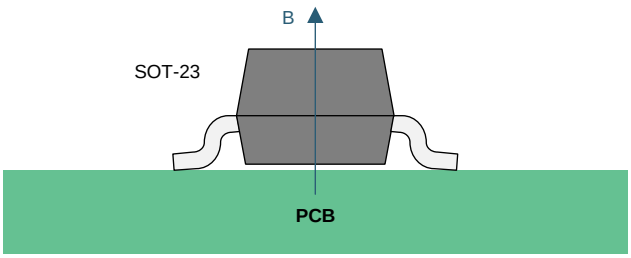


Figure 10. Direction of Sensitivity

Feature Description (continued)

Figure 11 shows that a positive magnetic field is defined as a south pole near the marked side of the package.

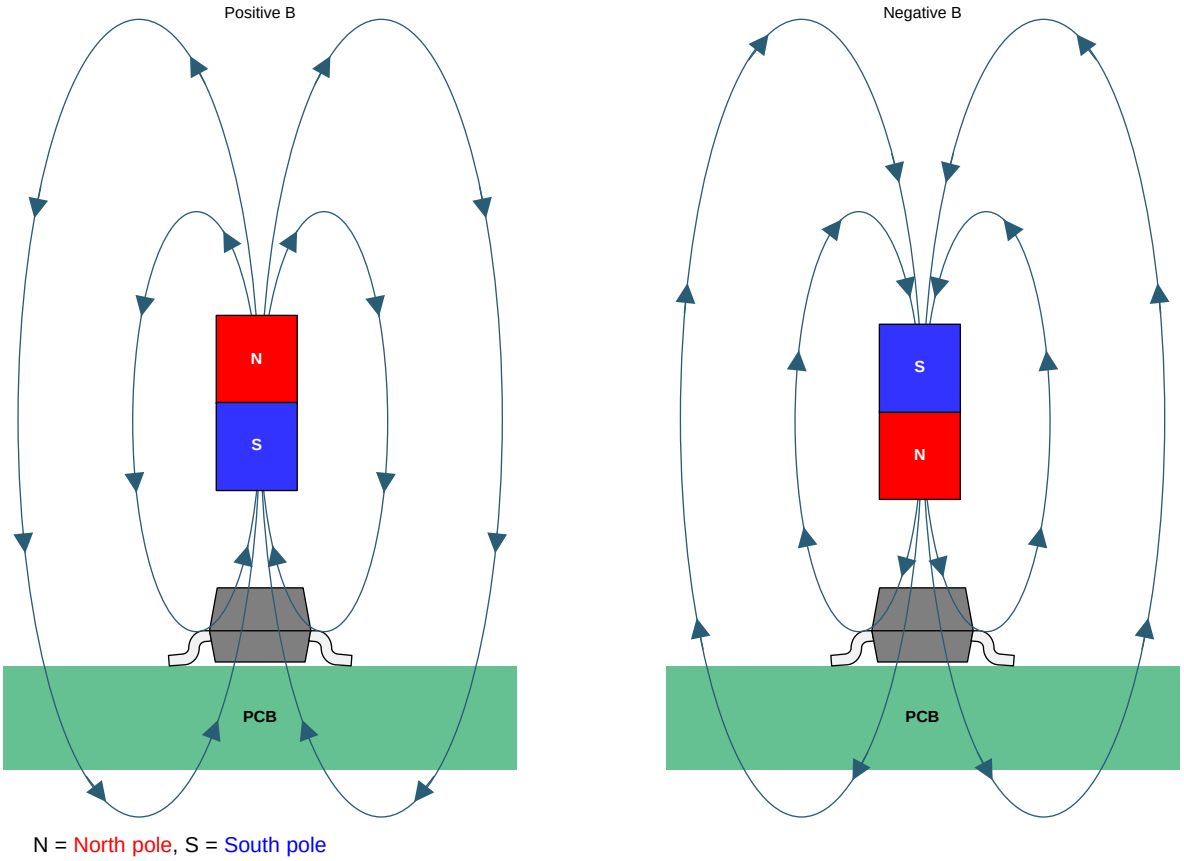


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the device output is indeterminate. If the field strength is greater than B_{OP}, then the output is pulled low. If the field strength is less than B_{RP}, then the output is released.

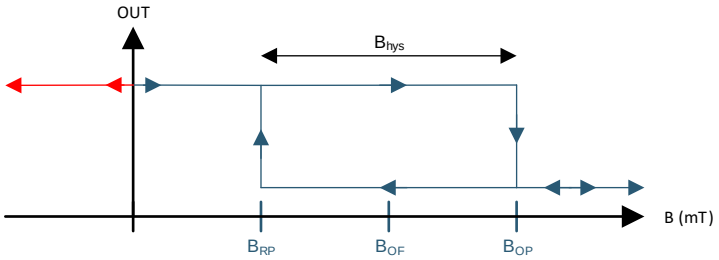


Figure 12. Output State

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5021, t_{on} must elapse before the OUT pin is valid. In case 1 (Figure 13) and case 2 (Figure 14), the output is defined assuming that magnetic field $B_{APPLIED} > B_{OP}$, and $B_{APPLIED} < B_{RP}$, respectively.

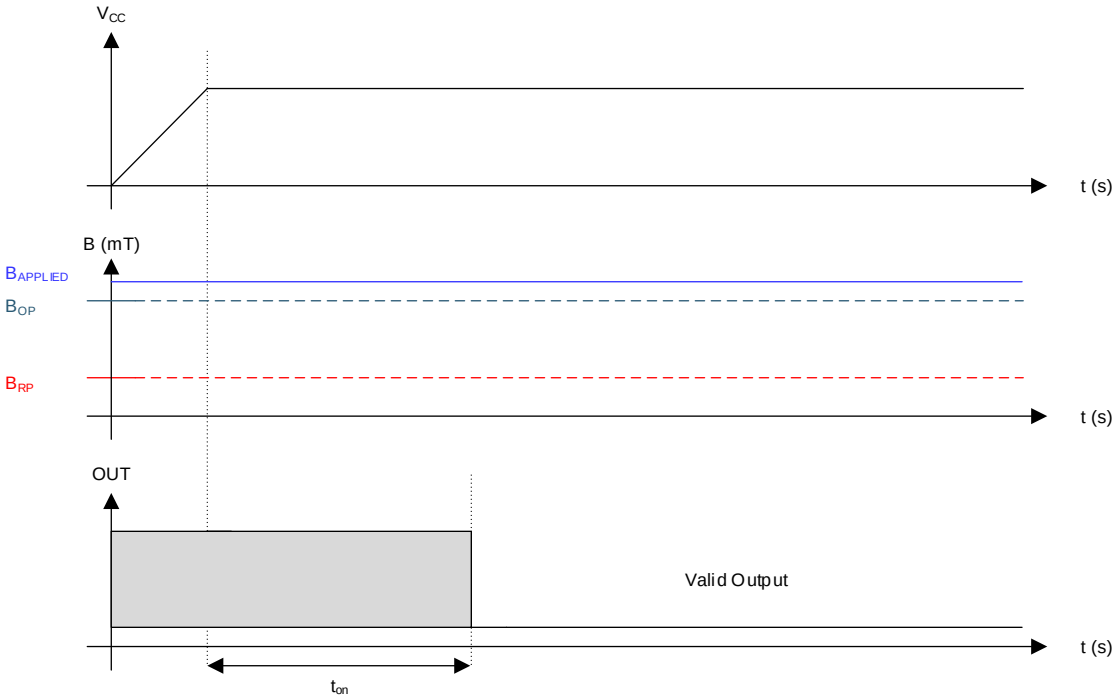


Figure 13. Case 1: Power On When B > B_{OP}

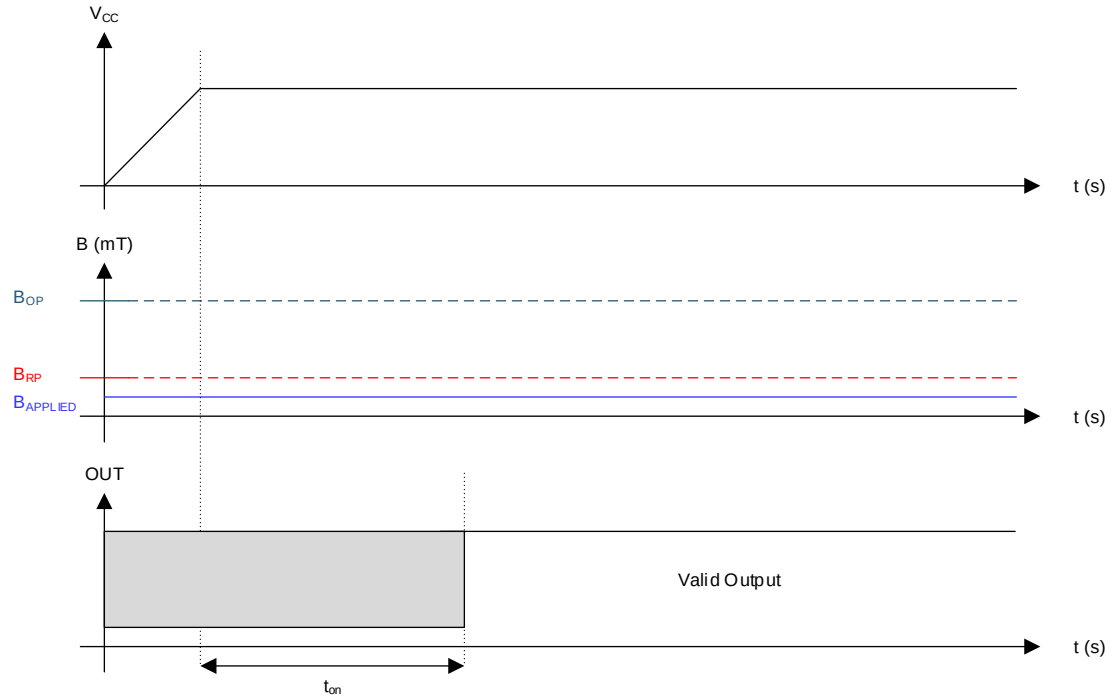


Figure 14. Case 2: Power On When B < B_{RP}

Feature Description (continued)

If the device is powered on with $B_{RP} < B_{APPLIED} < B_{OP}$, then the device output remains in indeterminate state until the magnetic field changes. After the change in magnetic field results in a condition that meets either $B_{OP} < B_{APPLIED}$ or $B_{RP} > B_{APPLIED}$, the output turns to valid state after t_d time elapses. Case 3 (Figure 15) and case 4 (Figure 16) show examples of this behavior.

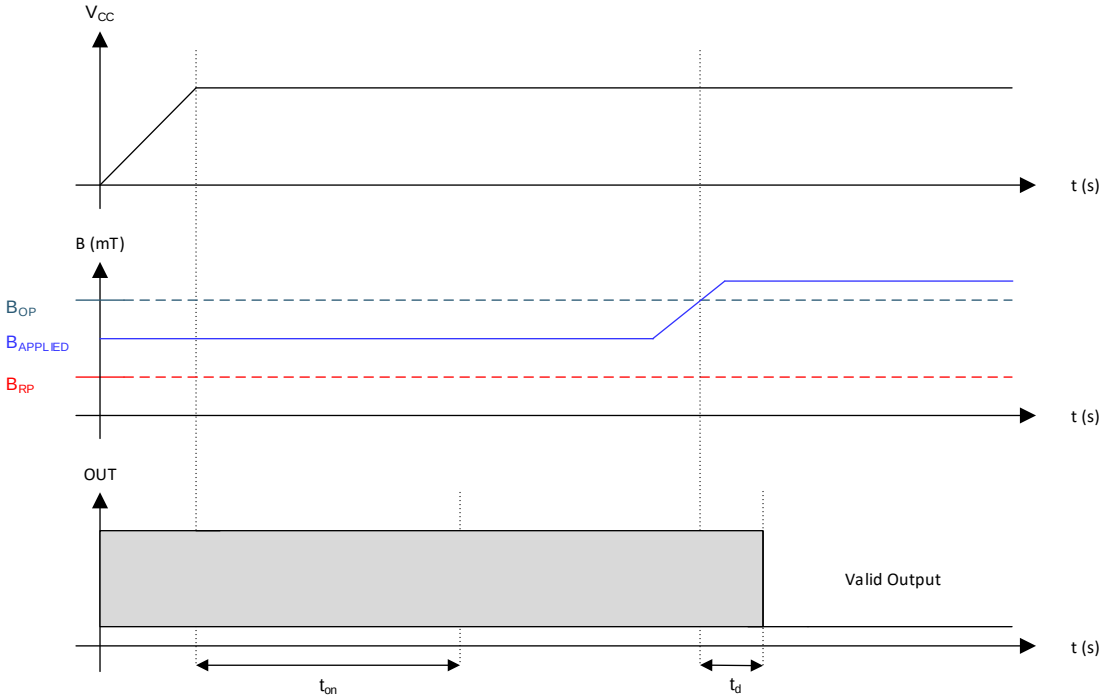


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

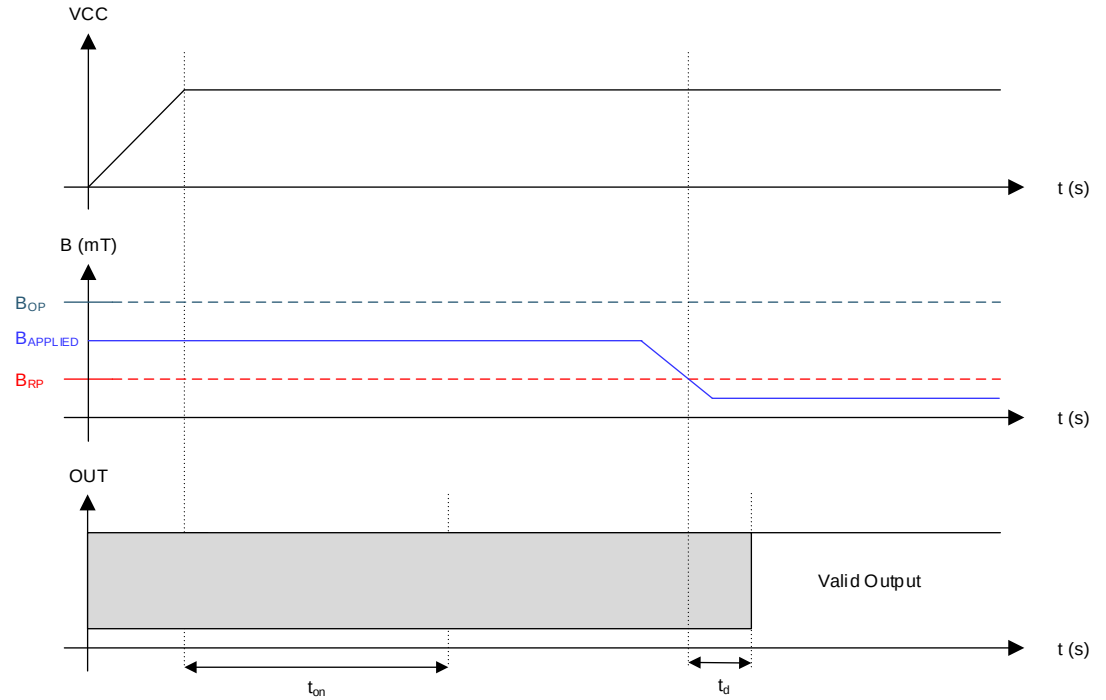


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

Feature Description (continued)

7.3.4 Hall Element Location

The sensing element inside the device is in the center of both packages when viewed from the top. Figure 17 shows the tolerances and side-view dimensions.

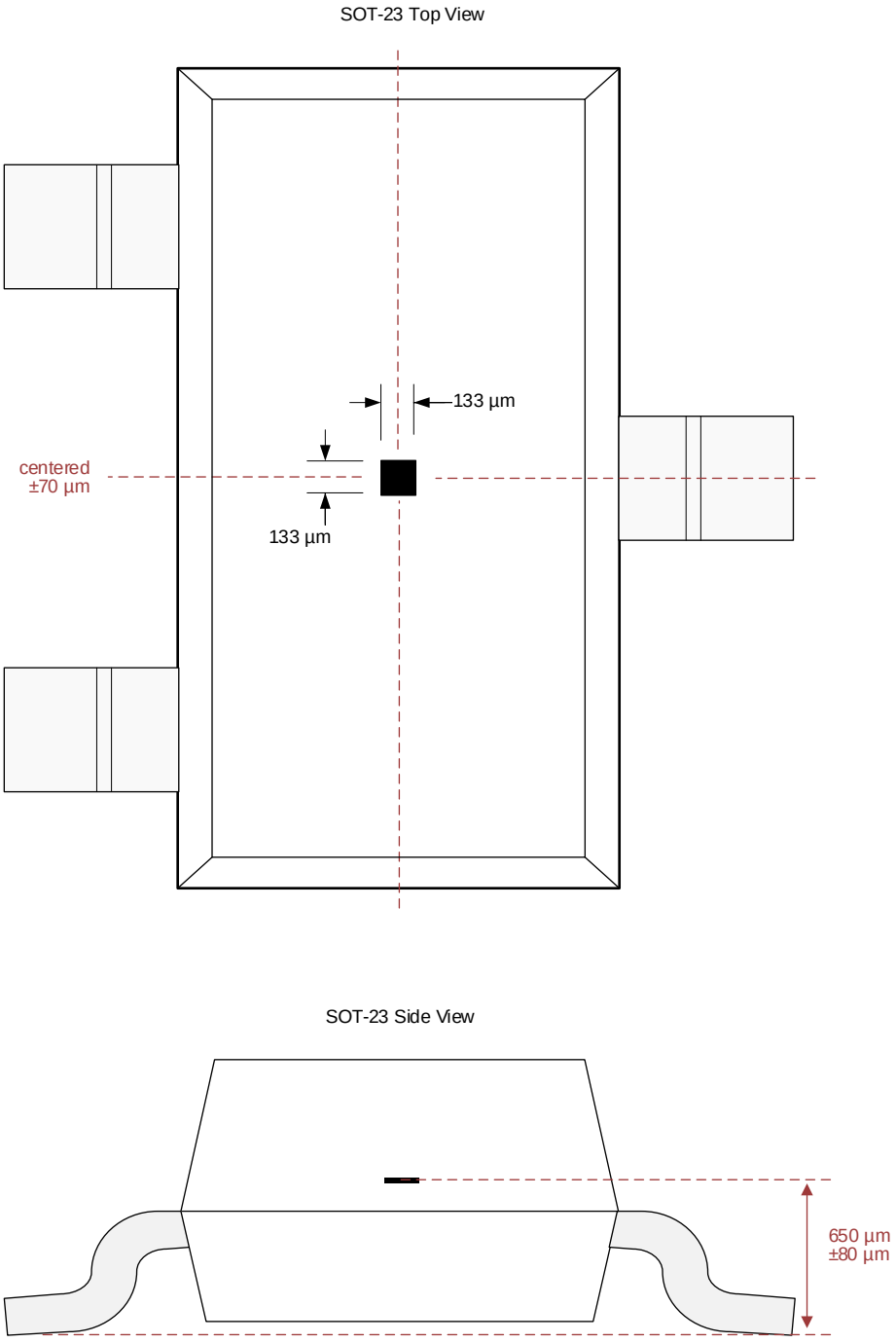


Figure 17. Hall Element Location

Feature Description (continued)

7.3.5 Propagation Delay

The DRV5021 samples the Hall element at a nominal sampling period of 16.67 µs to detect the presence of a magnetic north or south pole. At each sampling point, the device takes the average of the current sampled value and immediately preceding sampled value of the magnetic field. If this average value crosses the B_{OP} or B_{RP} threshold, the device output changes according to the transfer function.

Figure 18 shows the DRV5021 propagation delay analysis in the proximity of a magnetic south pole. The Hall element of the DRV5021 experiences an increasing magnetic field as the magnetic south pole approaches near the device. At time t_2, the average magnetic field is (B_2 + B_1) / 2, which is less than the B_{OP} threshold of the device. At time t_3, the actual magnetic field has crossed the B_{OP} threshold. However, the average (B_3 + B_2) / 2 is still less than the B_{OP} threshold. Thus, the device waits for next sample time, t_4, to start the output transition through the analog signal chain. The propagation delay, t_d, is measured as the delay from the time the magnetic field crosses the B_{OP} threshold to the time output transitions.

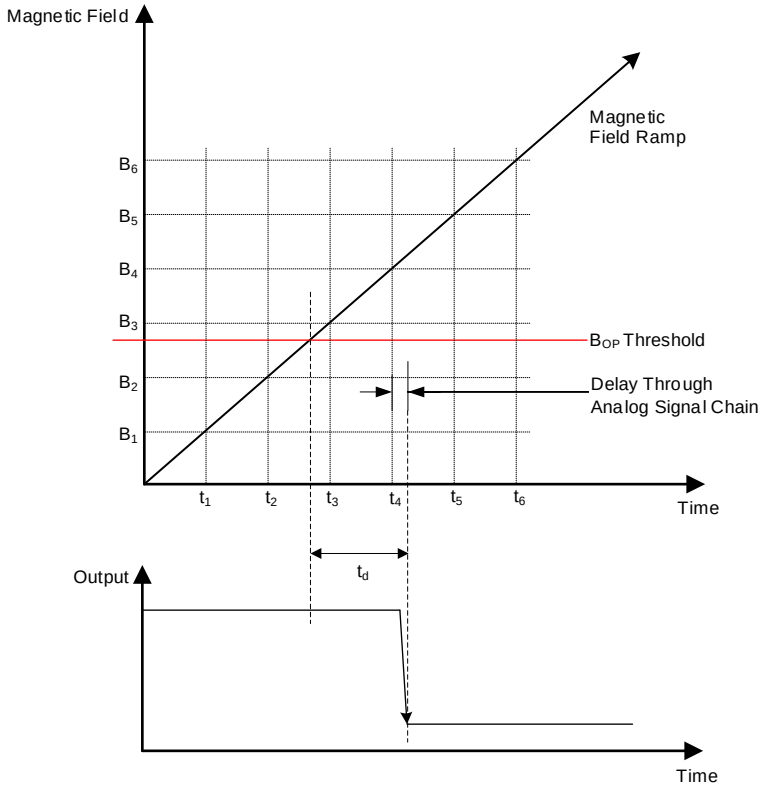


Figure 18. Propagation Delay

Feature Description (continued)

7.3.6 Output Stage

The DRV5021 output stage uses an open-drain NMOS transistor that is rated to sink up to 20 mA of current. For proper operation, calculate the value of pullup resistor R1 using Equation 1.

$$\frac{V_{ref}\,max}{20\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better; however, faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, the value of R1 must be > 500 Ω in order to make sure that the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC}. The allowable voltage range of this pin is specified in the *Recommended Operating Conditions*.

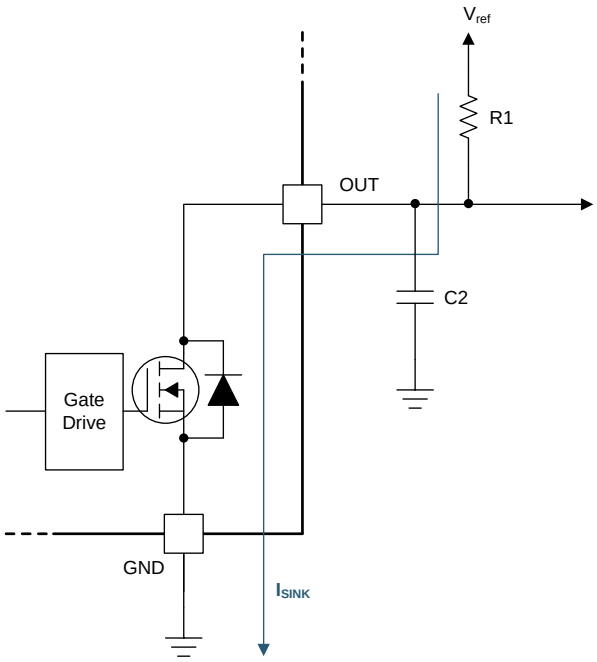


Figure 19. Open-Drain Output

Select a value for C2 based on the system bandwidth specifications shown in Equation 2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

7.4 Device Functional Modes

The DRV5021 device is active only when V_{CC} is between 2.5 V and 5.5 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5021 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Proximity Sensing Circuit

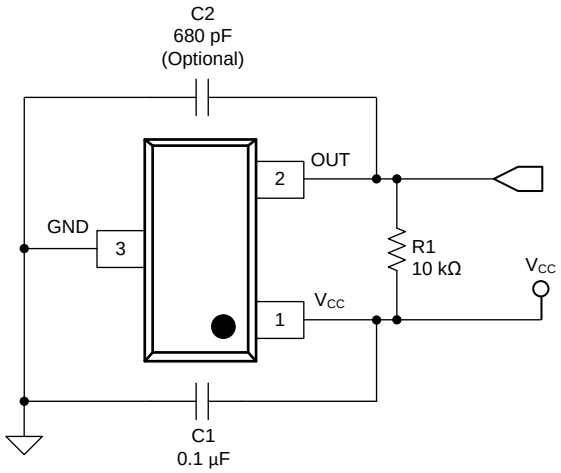


Figure 20. Proximity Sensing Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 V to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 2 shows the external components needed to create this design example.

Table 2. External Components

COMPONENT	CONNECTED BETWEEN		RECOMMENDED
C1	V_{CC}	GND	A 0.1-µF ceramic capacitor rated for V_{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	V_{CC} (1)	Requires a pullup resistor

(1) Pullup resistor may be connected to a voltage source other than V_{CC}; see the *Recommended Operating Conditions* for the valid range of the output pin voltage.

8.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ V_{ref} ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\,max}{20\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ V}{20\ mA} \le R1 \le \frac{3.2\ V}{100\ \mu A} \tag{4}$$

Therefore:

$$170\ \Omega \le R1 \le 32\ k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

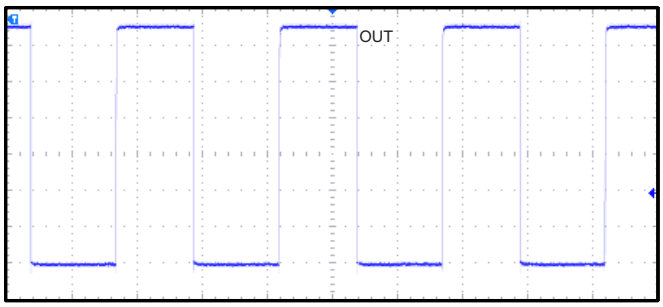
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ kHz < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

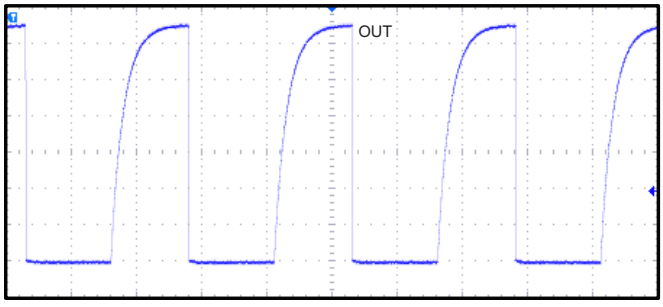
For R1 = 10 kΩ and C2 = 680 pF, the corner frequency for the low-pass filter is 23.4 kHz.

8.2.1.3 Application Curves



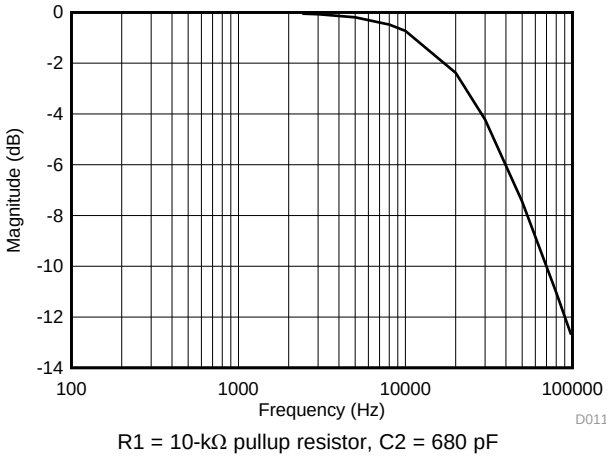
R1 = 10-kΩ pullup resistor, no C2 capacitor

Figure 21. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup, C2 = 680 pF

Figure 22. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup resistor, C2 = 680 pF

Figure 23. Low-Pass Filtering

8.2.2 Alternative Two-Wire Application

For systems that require a minimal wire count, connect the device output to V_{CC} through a resistor, and sense the total supplied current near the controller. Use a shunt resistor or other circuitry to sense the current.

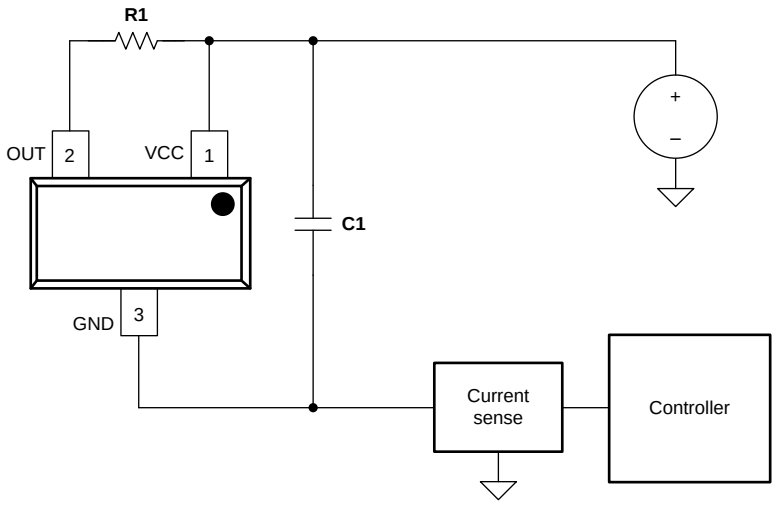


Figure 24. 2-Wire Application

8.2.2.1 Design Requirements

Table 3 lists the related design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	5 V
OUT resistor	R1	1 kΩ
Bypass capacitor	C1	0.1 µF
Current when B < B_{RP}	$I_{RELEASE}$	About 2.3 mA
Current when B > B_{OP}	$I_{OPERATE}$	About 7.3 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 2.3 mA).

When the output pulls low, a parallel current path is added, equal to V_{CC} / (R1 + $r_{DS(on)}$). Using 5 V and 1 kΩ, the parallel current is approximately 5 mA, making the total current approximately 7.3 mA.

Local bypass capacitor C1 must be at least 0.1 µF. Use a larger value capacitor if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5021 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 5.5 V. A 0.1-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5021 device as possible.

10 Layout

10.1 Layout Guidelines

Place the bypass capacitor near the DRV5021 device for efficient power delivery with minimal inductance. Place the external pullup resistor near the microcontroller input to provide the most stable voltage at the input. Alternatively, an integrated pullup resistor within the GPIO of the microcontroller can be used.

Generally, PCB copper planes underneath the DRV5021 have no effect on magnetic flux, and do not interfere with device performance because copper is not a ferromagnetic material. However, If nearby system components contain iron or nickel, they may redirect magnetic flux in unpredictable ways.

10.2 Layout Example

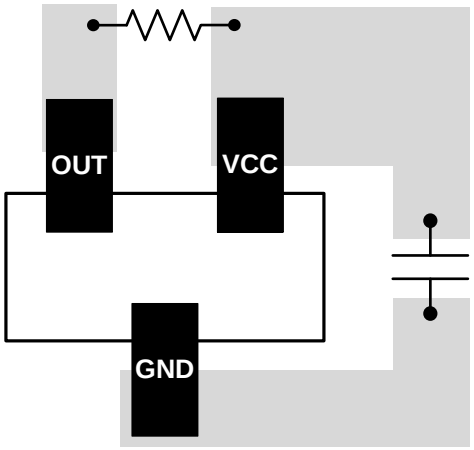


Figure 25. DRV5021 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instrument, *HALL-ADAPTER-EVM* User's Guide
- Texas Instrument, *Understanding and Applying Hall Effect Sensor Datasheets* Application Report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5021A1QDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21A1	Samples
DRV5021A1QDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21A1	Samples
DRV5021A2QDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21A2	Samples
DRV5021A2QDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21A2	Samples
DRV5021A3QDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21A3	Samples
DRV5021A3QDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	21A3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

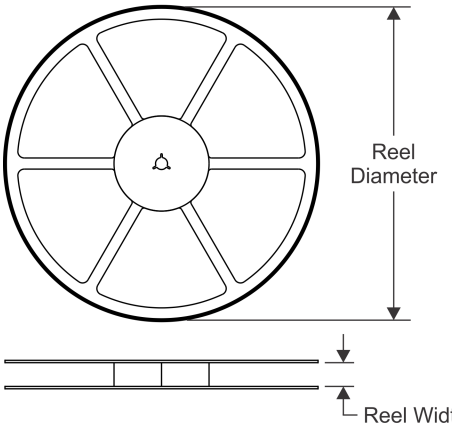
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

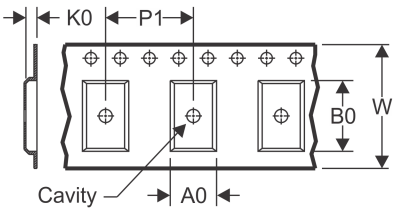
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

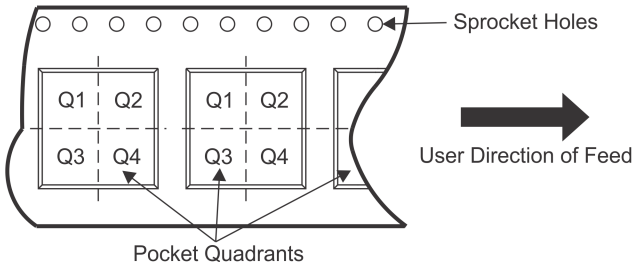


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

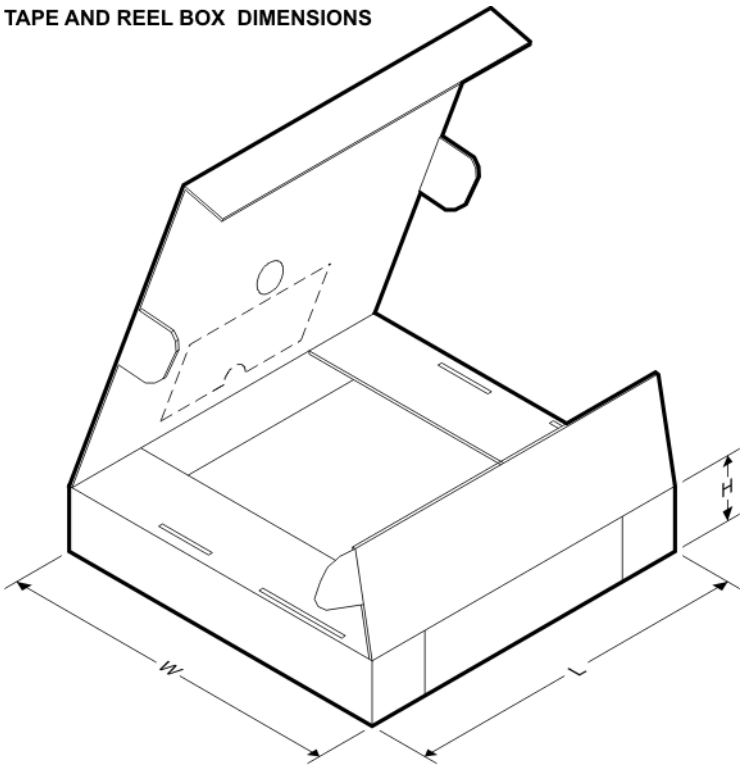
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5021A1QDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5021A1QDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5021A2QDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5021A2QDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5021A3QDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5021A3QDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



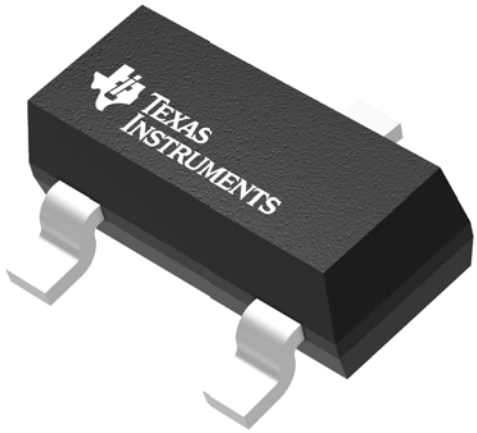
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5021A1QDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5021A1QDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
DRV5021A2QDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5021A2QDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
DRV5021A3QDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5021A3QDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



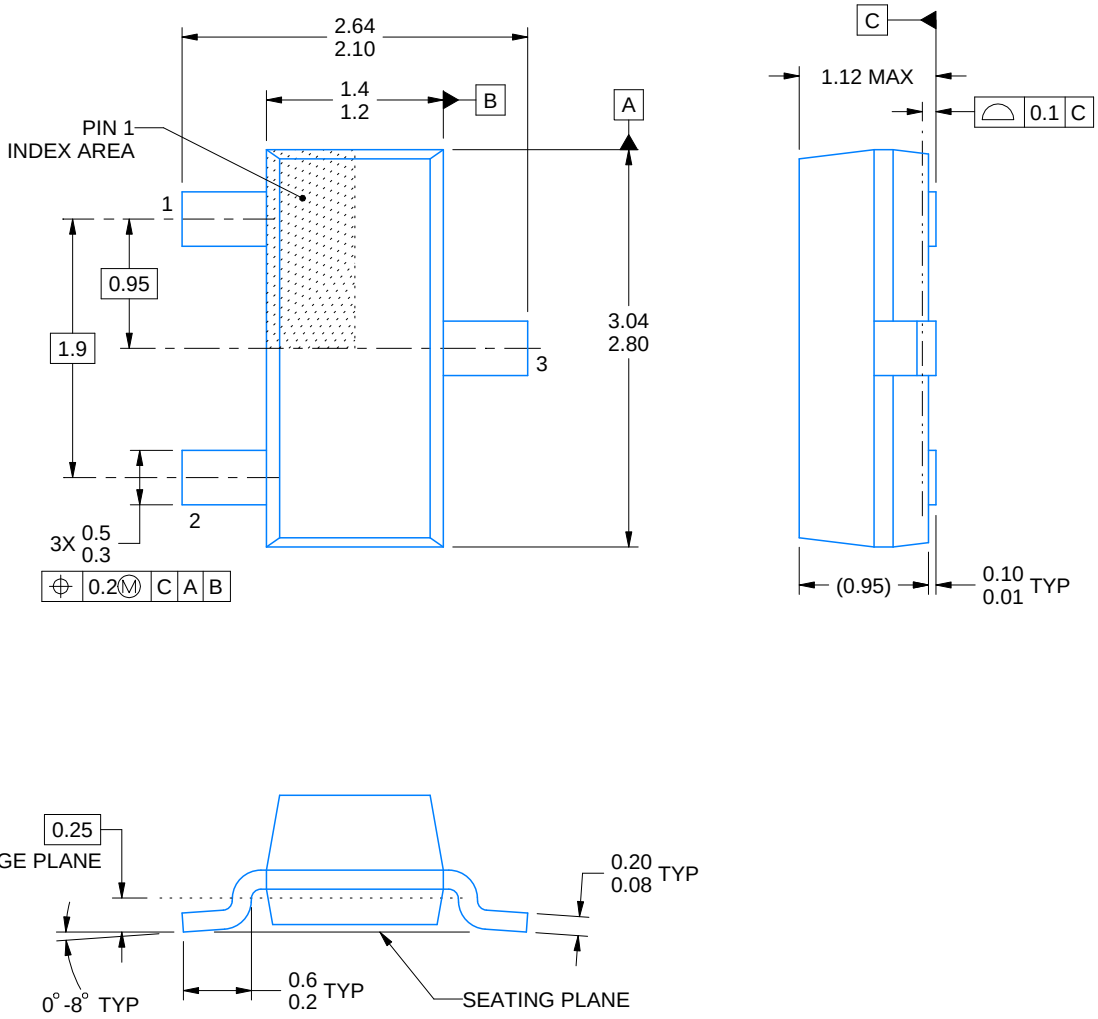
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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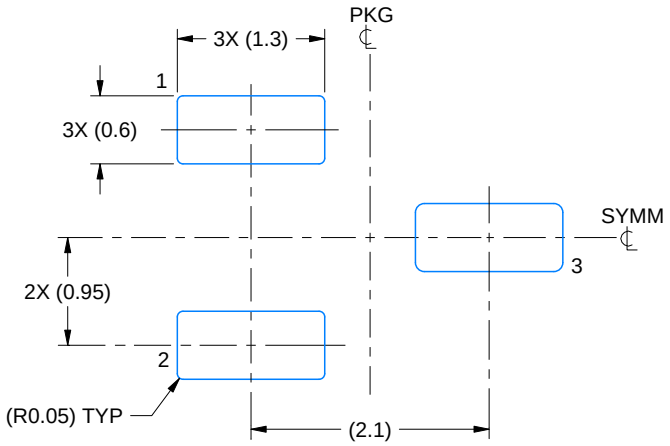
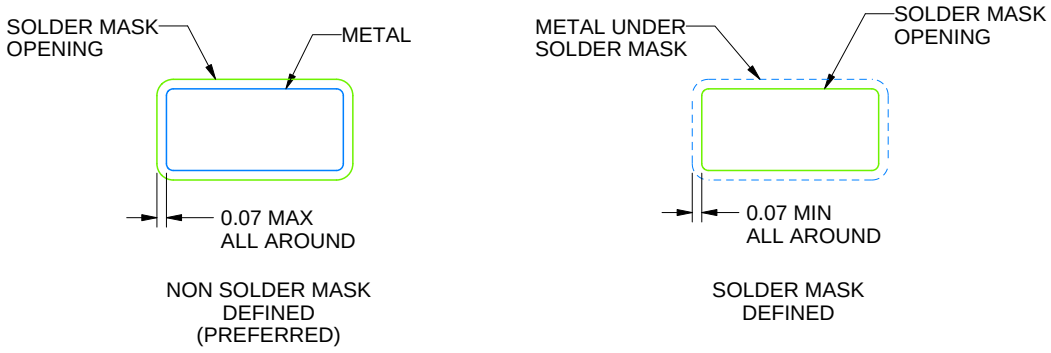
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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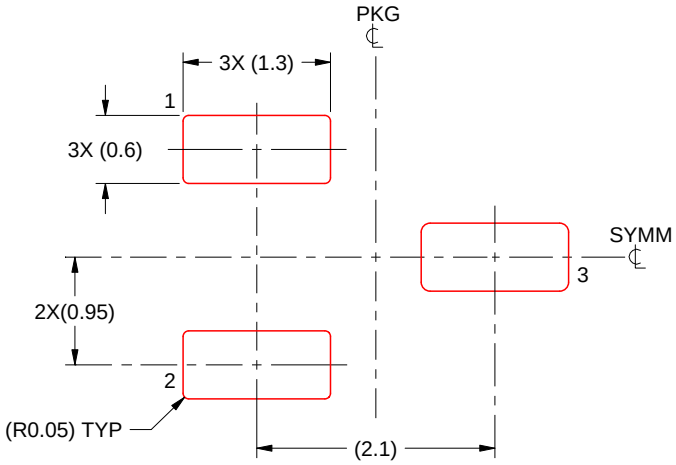
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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