

## Features

- All outputs skew <100 ps typical (250 max.)
- 15 to 80 MHz output operation
- Zero input to output delay
- 50% duty cycle outputs
- Outputs drive 50Ω terminated lines
- Low operating current
- 24-pin SOIC package
- Jitter:<200 ps peak to peak, <25 ps RMS

## Functional Description

The CY7B9910 and CY7B9920 Low Skew Clock Buffers offer low skew system clock distribution. These multiple output clock drivers optimize the timing of high performance computer systems. Each of the eight individual drivers can drive terminated transmission lines with impedances as low as 50Ω. They deliver minimal and specified output skews and full swing logic levels (CY7B9910 TTL or CY7B9920 CMOS).

The completely integrated PLL enables “zero delay” capability. External divide capability, combined with the internal PLL, allows distribution of a low frequency clock that is multiplied by virtually any factor at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

## Block Diagram Description

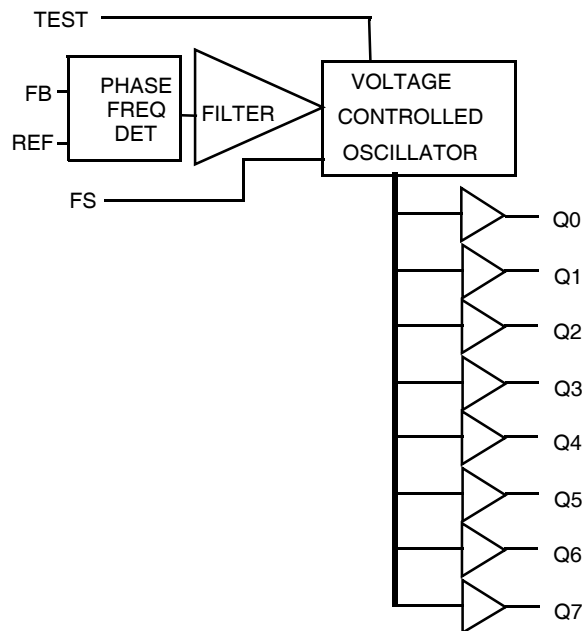
### Phase Frequency Detector and Filter

The Phase Frequency Detector and Filter blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase Locked Loop (PLL) that tracks the incoming REF signal.

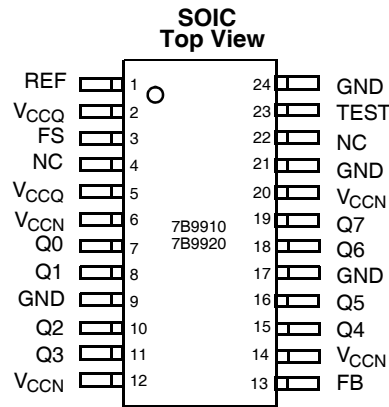
### VCO

The VCO accepts analog control inputs from the PLL filter block and generates a frequency. The operational range of the VCO is determined by the FS control pin.

## Logic Block Diagram



## Pin Configuration



## Pin Definitions

| Signal Name           | IO  | Description   |
|-----------------------|-----|---|
| REF                   | I   | Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured. |
| FB                    | I   | PLL feedback input (typically connected to one of the eight outputs).   |
| FS <sup>[1,2,3]</sup> | I   | Three level frequency range select.   |
| TEST                  | I   | Three level select. See <a href="#">TEST MODE</a> .   |
| Q[0..7]               | O   | Clock outputs.  |
| V <sub>CCN</sub>      | PWR | Power supply for output drivers.  |
| V <sub>CCQ</sub>      | PWR | Power supply for internal circuitry.  |
| GND                   | PWR | Ground.   |

## Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910 and CY7B9920 to operate as described in [Block Diagram Description](#). For testing purposes, any of the three level inputs can have a removable jumper to ground or be tied LOW through a 100W resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected and input levels supplied to REF directly control all outputs. Relative output-to-output functions are the same as in normal mode.

### Notes

- For all three state inputs, HIGH indicates a connection to VCC, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to VCC/2.
- The level to be set on FS is determined by the "normal" operating frequency (f<sub>NOM</sub>) of the VCO (see [Logic Block Diagram](#)). The frequency appearing at the REF and FB inputs are f<sub>NOM</sub> when the output connected to FB is undivided. The frequency of the REF and FB inputs are f<sub>NOM</sub>/X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
- When the FS pin is selected HIGH, the REF input must not transition upon power up until VCC reached 4.3V.

## Maximum Ratings

Operating outside these boundaries may affect the performance and life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

Output Current into Outputs (LOW)..... 64 mA

Static Discharge Voltage..... >2001V  
(MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C        | 5V ± 10%        |
| Industrial | -40°C to +85°C      | 5V ± 10%        |

**Electrical Characteristics** Over the Operating Range

| Parameter        | Description  | Test Conditions  | CY7B9910                    |                             | CY7B9920                    |                             | Unit |
|------------------|--|--|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------|
|                  |  |  | Min                         | Max                         | Min                         | Max                         |      |
| V <sub>OH</sub>  | Output HIGH Voltage                                      | V <sub>CC</sub> = Min, I <sub>OH</sub> = -16 mA  | 2.4                         |                             |                             |                             | V    |
|                  |  | V <sub>CC</sub> = Min, I <sub>OH</sub> = -40 mA  |                             |                             | V <sub>CC</sub> -0.75       |                             |      |
| V <sub>OL</sub>  | Output LOW Voltage                                       | V <sub>CC</sub> = Min, I <sub>OL</sub> = 46 mA   |                             | 0.45                        |                             |                             | V    |
|                  |  | V <sub>CC</sub> = Min, I <sub>OL</sub> = 46 mA   |                             |                             |                             | 0.45                        |      |
| V <sub>IH</sub>  | Input HIGH Voltage (REF and FB inputs only)              |  | 2.0                         | V <sub>CC</sub>             | V <sub>CC</sub> - 1.35      | V <sub>CC</sub>             | V    |
| V <sub>IL</sub>  | Input LOW Voltage (REF and FB inputs only)               |  | -0.5                        | 0.8                         | -0.5                        | 1.35                        | V    |
| V <sub>IHH</sub> | Three Level Input HIGH Voltage (Test, FS) <sup>[4]</sup> | Min ≤ V <sub>CC</sub> ≤ Max  | V <sub>CC</sub> - 1V        | V <sub>CC</sub>             | V <sub>CC</sub> - 1V        | V <sub>CC</sub>             | V    |
| V <sub>IMM</sub> | Three Level Input MID Voltage (Test, FS) <sup>[4]</sup>  | Min ≤ V <sub>CC</sub> ≤ Max  | V <sub>CC</sub> /2 - 500 mV | V <sub>CC</sub> /2 + 500 mV | V <sub>CC</sub> /2 - 500 mV | V <sub>CC</sub> /2 + 500 mV | V    |
| V <sub>ILL</sub> | Three Level Input LOW Voltage (Test, FS) <sup>[4]</sup>  | Min ≤ V <sub>CC</sub> ≤ Max  | 0.0                         | 1.0                         | 0.0                         | 1.0                         | V    |
| I <sub>IH</sub>  | Input HIGH Leakage Current (REF and FB inputs only)      | V <sub>CC</sub> = Max, V <sub>IN</sub> = Max   |                             | 10                          |                             | 10                          | μA   |
| I <sub>IL</sub>  | Input LOW Leakage Current (REF and FB inputs only)       | V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.4V  | -500                        |                             | -500                        |                             | μA   |
| I <sub>IHH</sub> | Input HIGH Current (Test, FS)                            | V <sub>IN</sub> = V <sub>CC</sub>  |                             | 200                         |                             | 200                         | μA   |
| I <sub>IMM</sub> | Input MID Current (Test, FS)                             | V <sub>IN</sub> = V <sub>CC</sub> /2   | -50                         | 50                          | -50                         | 50                          | μA   |
| I <sub>ILL</sub> | Input LOW Current (Test, FS)                             | V <sub>IN</sub> = GND  |                             | -200                        |                             | -200                        | μA   |
| I <sub>OS</sub>  | Output Short Circuit Current <sup>[5]</sup>              | V <sub>CC</sub> = Max, V <sub>OUT</sub> = GND (25°C only)  |                             | -250                        |                             | N/A                         | mA   |
| I <sub>CCQ</sub> | Operating Current Used by Internal Circuitry             | V <sub>CCN</sub> = V <sub>CCQ</sub> = Max All Input Selects Open   | Com'I                       | 85                          |                             | 85                          | mA   |
|                  |  |  | Mil/Ind                     |                             | 90                          |                             | 90   |
| I <sub>CCN</sub> | Output Buffer Current per Output Pair <sup>[6]</sup>     | V <sub>CCN</sub> = V <sub>CCQ</sub> = Max<br>I <sub>OUT</sub> = 0 mA<br>Input Selects Open, f <sub>MAX</sub> |                             | 14                          |                             | 19                          | mA   |
| PD               | Power Dissipation per Output Pair <sup>[7]</sup>         | V <sub>CCN</sub> = V <sub>CCQ</sub> = Max<br>I <sub>OUT</sub> = 0 mA<br>Input Selects Open, f <sub>MAX</sub> |                             | 78                          |                             | 104 <sup>[5]</sup>          | mW   |

**Notes**

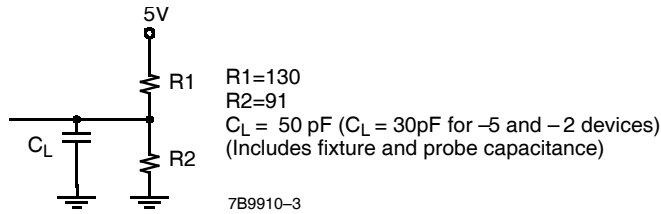
- These inputs are normally wired to V<sub>CC</sub>, GND, or left unconnected (actual threshold voltages vary as a percentage of V<sub>CC</sub>). Internal termination resistors hold unconnected inputs at V<sub>CC</sub>/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t<sub>LOCK</sub> time before all data sheet limits are achieved.
- Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B9920 outputs are not short circuit protected.
- Total output current per output pair is approximated by the following expression that includes device current plus load current:  
 CY7B9910:  
 $I_{CCN} = [(4 + 0.11F) + (((835 - 3F)/Z) + (.0022FC))N] \times 1.1$   
 CY7B9920:  
 $I_{CCN} = [(3.5 + .17F) + (((1160 - 2.8F)/Z) + (.0025FC))N] \times 1.1$   
 Where  
 F = frequency in MHz  
 C = capacitive load in pF  
 Z = line impedance in ohms  
 N = number of loaded outputs; 0, 1, or 2  
 FC = F < C.
- Total power dissipation per output pair is approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:  
 CY7B9910:  
 $PD = [(22 + 0.61F) + (((1550 - 2.7F)/Z) + (.0125FC))N] \times 1.1$   
 CY7B9920:  
 $PD = [(19.25 + 0.94F) + (((700 + 6F)/Z) + (.017FC))N] \times 1.1$ . See note 3 for variable definition.

## Capacitance

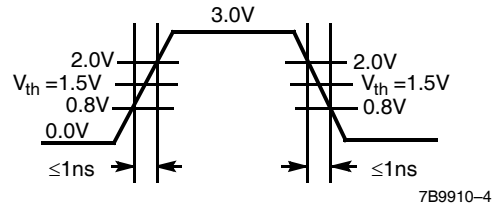
Tested initially and after any design or process changes that may affect these parameters.

| Parameter       | Description       | Test Conditions  | Max | Unit |
|-----------------|-------------------|--|-----|------|
| C <sub>IN</sub> | Input Capacitance | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 10  | pF   |

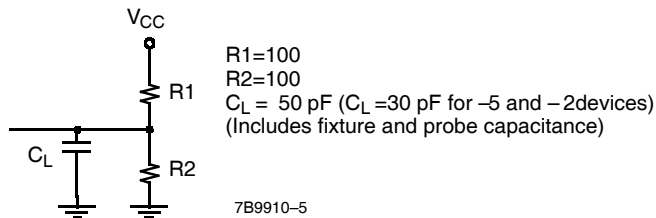
## AC Test Loads and Waveforms



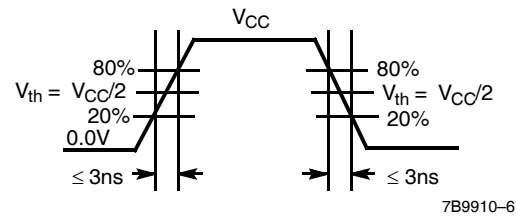
**TTL AC Test Load (CY7B9910)**



**TTL Input Test Waveform (Cy7B9910)**



**CMOS AC Test Load (CY7B9920)**



**CMOS Input Test Waveform (CY7B9920)**

## Switching Characteristics

Over the Operating Range <sup>[11]</sup>

| Parameter          | Description  | CY7B9910-2 <sup>[8]</sup>      |     |       | CY7B9920-2 <sup>[8]</sup> |     |       | Unit |                    |
|--------------------|--|--------------------------------|-----|-------|---------------------------|-----|-------|------|--------------------|
|                    |  | Min                            | Typ | Max   | Min                       | Typ | Max   |      |                    |
| f <sub>NOM</sub>   | Operating Clock Frequency in MHz                   | FS = LOW <sup>[1, 2]</sup>     | 15  |       | 30                        | 15  |       | MHz  |                    |
|                    |  | FS = MID <sup>[1, 2]</sup>     | 25  |       | 50                        | 25  |       |      |                    |
|                    |  | FS = HIGH <sup>[1, 2, 3]</sup> | 40  |       | 80                        | 40  |       |      | 80 <sup>[12]</sup> |
| t <sub>RPWH</sub>  | REF Pulse Width HIGH                               | 5.0                            |     |       | 5.0                       |     |       | ns   |                    |
| t <sub>RPWL</sub>  | REF Pulse Width LOW                                | 5.0                            |     |       | 5.0                       |     |       | ns   |                    |
| t <sub>SKEW</sub>  | Zero Output Skew (All Outputs) <sup>[13, 14]</sup> |                                | 0.1 | 0.25  |                           | 0.1 | 0.25  | ns   |                    |
| t <sub>DEV</sub>   | Device-to-Device Skew <sup>[14, 15]</sup>          |                                |     | 0.75  |                           |     | 0.75  | ns   |                    |
| t <sub>PD</sub>    | Propagation Delay, REF Rise to FB Rise             | -0.25                          | 0.0 | +0.25 | -0.25                     | 0.0 | +0.25 | ns   |                    |
| t <sub>ODCV</sub>  | Output Duty Cycle Variation <sup>[16]</sup>        | -0.65                          | 0.0 | +0.65 | -0.65                     | 0.0 | +0.65 | ns   |                    |
| t <sub>ORISE</sub> | Output Rise Time <sup>[17, 18]</sup>               | 0.15                           | 1.0 | 1.2   | 0.5                       | 2.0 | 2.5   | ns   |                    |
| t <sub>OFALL</sub> | Output Fall Time <sup>[17, 18]</sup>               | 0.15                           | 1.0 | 1.2   | 0.5                       | 2.0 | 2.5   | ns   |                    |
| t <sub>LOCK</sub>  | PLL Lock Time <sup>[19]</sup>                      |                                |     | 0.5   |                           |     | 0.5   | ms   |                    |
| t <sub>JR</sub>    | Cycle-to-Cycle Output Jitter                       | Peak to Peak                   |     |       | 200                       |     |       | 200  | ps                 |
|                    |  | RMS                            |     |       | 25                        |     |       | 25   | ps                 |

| Parameter          | Description  |                                | CY7B9910-5 |      |      | CY7B9920-5 |      |                    | Unit |
|--------------------|--|--------------------------------|------------|------|------|------------|------|--------------------|------|
|                    |  |                                | Min        | Typ  | Max  | Min        | Typ  | Max                |      |
| f <sub>NOM</sub>   | Operating Clock Frequency in MHz                   | FS = LOW <sup>[1, 2]</sup>     | 15         |      | 30   | 15         |      | 30                 | MHz  |
|                    |  | FS = MID <sup>[1, 2]</sup>     | 25         |      | 50   | 25         |      | 50                 |      |
|                    |  | FS = HIGH <sup>[1, 2, 3]</sup> | 40         |      | 80   | 40         |      | 80 <sup>[12]</sup> |      |
| t <sub>RPWH</sub>  | REF Pulse Width HIGH                               |                                | 5.0        |      |      | 5.0        |      |                    | ns   |
| t <sub>RPWL</sub>  | REF Pulse Width LOW                                |                                | 5.0        |      |      | 5.0        |      |                    | ns   |
| t <sub>SKEW</sub>  | Zero Output Skew (All Outputs) <sup>[13, 14]</sup> |                                |            | 0.25 | 0.5  |            | 0.25 | 0.5                | ns   |
| t <sub>DEV</sub>   | Device-to-Device Skew <sup>[8, 15]</sup>           |                                |            |      | 1.0  |            |      | 1.0                | ns   |
| t <sub>PD</sub>    | Propagation Delay, REF Rise to FB Rise             |                                | -0.5       | 0.0  | +0.5 | -0.5       | 0.0  | +0.5               | ns   |
| t <sub>ODCV</sub>  | Output Duty Cycle Variation <sup>[16]</sup>        |                                | -1.0       | 0.0  | +1.0 | -1.0       | 0.0  | +1.0               | ns   |
| t <sub>ORISE</sub> | Output Rise Time <sup>[17, 18]</sup>               |                                | 0.15       | 1.0  | 1.5  | 0.5        | 2.0  | 3.0                | ns   |
| t <sub>OFALL</sub> | Output Fall Time <sup>[17, 18]</sup>               |                                | 0.15       | 1.0  | 1.5  | 0.5        | 2.0  | 3.0                | ns   |
| t <sub>LOCK</sub>  | PLL Lock Time <sup>[19]</sup>                      |                                |            |      | 0.5  |            |      | 0.5                | ms   |
| t <sub>JR</sub>    | Cycle-to-Cycle Output Jitter                       | Peak to Peak <sup>[8]</sup>    |            |      | 200  |            |      | 200                | ps   |
|                    |  | RMS <sup>[8]</sup>             |            |      | 25   |            |      | 25                 | ps   |

**Notes**

8. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
9. CMOS output buffer current and power dissipation specified at 50 MHz reference frequency.
10. Applies to REF and FB inputs only.
11. Test measurement levels for the CY7B9910 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B9920 are CMOS levels (VCC/2 to VCC/2). Test conditions assume signal transition times of 2ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
12. Except as noted, all CY7B9920-2 and -5 timing parameters are specified to 80 MHz with a 30 pF load.
13. t<sub>SKEW</sub> is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B9910) or VCC/2 (CY7B9920).
14. t<sub>SKEW</sub> is defined as the skew between outputs.
15. t<sub>DEV</sub> is the output-to-output skew between any two outputs on separate devices operating under the same conditions (VCC, ambient temperature, air flow, and so on).
16. t<sub>ODCV</sub> is the deviation of the output from a 50% duty cycle.
17. Specified with outputs loaded with 30 pF for the CY7B99X0-2 and -5 devices and 50 pF for the CY7B99X0-7 devices. Devices are terminated through 50Ω to 2.06V (CY7B9910) or VCC/2 (CY7B9920).
18. t<sub>ORISE</sub> and t<sub>OFALL</sub> measured between 0.8V and 2.0V for the CY7B9910 or 0.8VCC and 0.2VCC for the CY7B9920.
19. t<sub>LOCK</sub> is the time that is required before synchronization is achieved. This specification is valid only after VCC is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t<sub>PD</sub> is within specified limits.

## Switching Characteristics

Over the Operating Range<sup>[11]</sup> (continued)

| Parameter          | Description  |                               | CY7B9910-7 |     |      | CY7B9920-7 |     |                    | Unit |
|--------------------|--|-------------------------------|------------|-----|------|------------|-----|--------------------|------|
|                    |  |                               | Min        | Typ | Max  | Min        | Typ | Max                |      |
| f <sub>NOM</sub>   | Operating Clock Frequency in MHz                   | FS = LOW <sup>[1, 2]</sup>    | 15         |     | 30   | 15         |     | 30                 | MHz  |
|                    |  | FS = MID <sup>[1, 2]</sup>    | 25         |     | 50   | 25         |     | 50                 |      |
|                    |  | FS = HIGH <sup>1, 2, 3]</sup> | 40         |     | 80   | 40         |     | 80 <sup>[12]</sup> |      |
| t <sub>RPWH</sub>  | REF Pulse Width HIGH                               |                               | 5.0        |     |      | 5.0        |     |                    | ns   |
| t <sub>RPWL</sub>  | REF Pulse Width LOW                                |                               | 5.0        |     |      | 5.0        |     |                    | ns   |
| t <sub>SKEW</sub>  | Zero Output Skew (All Outputs) <sup>[13, 14]</sup> |                               |            | 0.3 | 0.75 |            | 0.3 | 0.75               | ns   |
| t <sub>DEV</sub>   | Device-to-Device Skew <sup>[8, 15]</sup>           |                               |            |     | 1.5  |            |     | 1.5                | ns   |
| t <sub>PD</sub>    | Propagation Delay, REF Rise to FB Rise             |                               | -0.7       | 0.0 | +0.7 | -0.7       | 0.0 | +0.7               | ns   |
| t <sub>ODCV</sub>  | Output Duty Cycle Variation <sup>[16]</sup>        |                               | -1.2       | 0.0 | +1.2 | -1.2       | 0.0 | +1.2               | ns   |
| t <sub>ORISE</sub> | Output Rise Time <sup>[17, 18]</sup>               |                               | 0.15       | 1.5 | 2.5  | 0.5        | 3.0 | 5.0                | ns   |
| t <sub>OFALL</sub> | Output Fall Time <sup>[17, 18]</sup>               |                               | 0.15       | 1.5 | 2.5  | 0.5        | 3.0 | 5.0                | ns   |
| t <sub>LOCK</sub>  | PLL Lock Time <sup>[19]</sup>                      |                               |            |     | 0.5  |            |     | 0.5                | ms   |
| t <sub>JR</sub>    | Cycle-to-Cycle Output Jitter                       | Peak to Peak <sup>[8]</sup>   |            |     | 200  |            |     | 200                | ps   |
| t <sub>JR</sub>    |  | RMS <sup>[8]</sup>            |            |     | 25   |            |     | 25                 | ps   |

## AC Timing Diagrams

Figure 1. AC Timing Diagrams

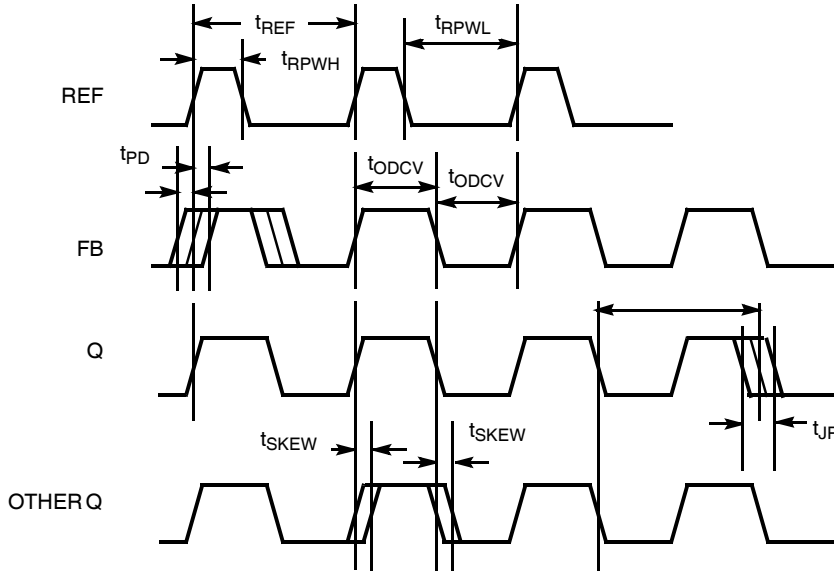
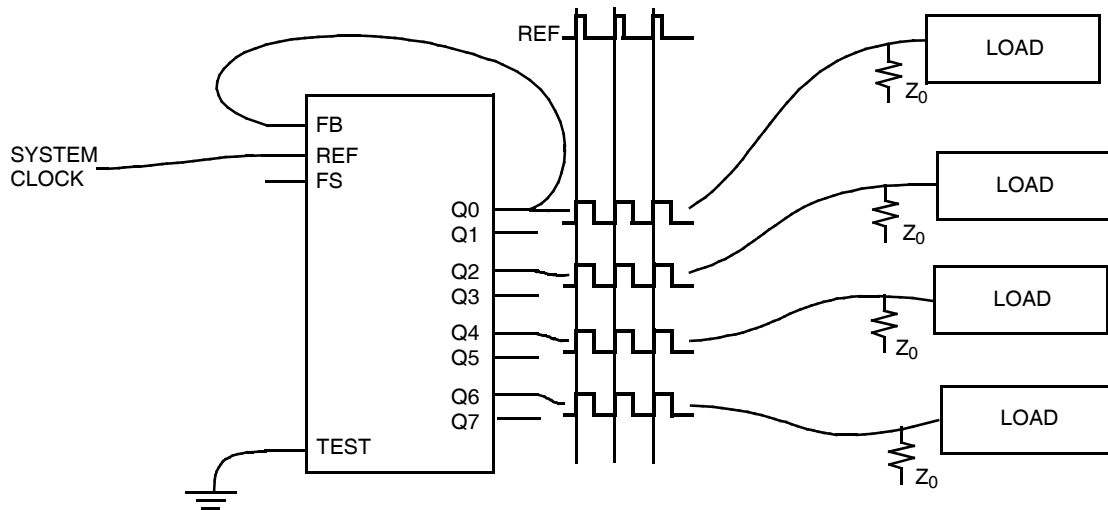


Figure 2. Zero Skew and Zero Delay Clock Driver



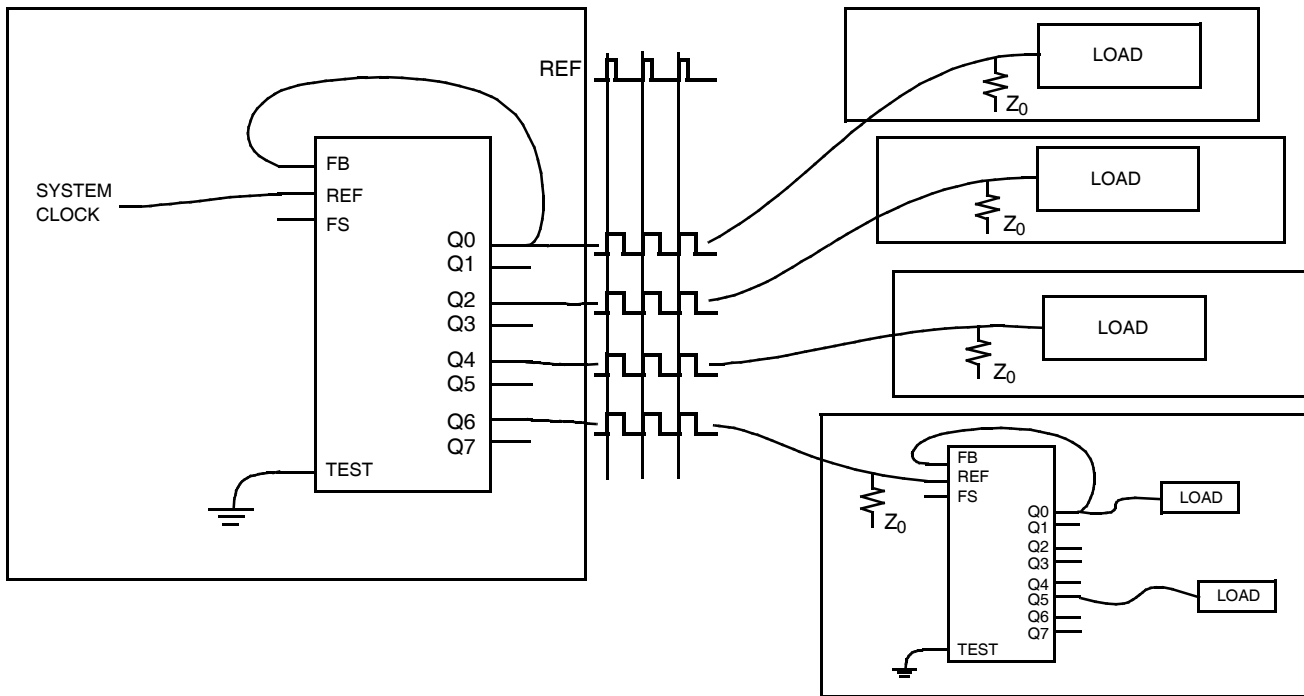


### Operational Mode Descriptions

Figure 2 shows the device configured as a zero skew clock buffer. In this mode the 7B9910/9920 is used as the basis for a low skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input is tied to any output and the operating frequency range is selected with the FS pin. The low skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), enables efficient printed circuit board design.

Figure 1 shows the CY7B9910/9920 connected in series to construct a zero skew clock distribution tree between boards. Cascaded clock buffers accumulates low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in series.

**Figure 3. Board-to-Board Clock Distribution**

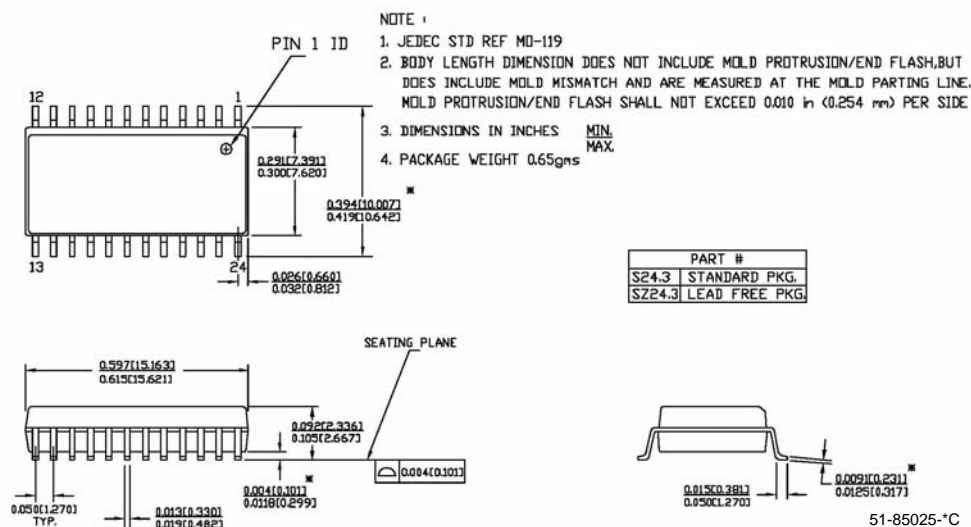


### Ordering Information

| Accuracy (ps)  | Ordering Code                | Package Type                           | Operating Range |
|----------------|------------------------------|--|-----------------|
| 250            | CY7B9910-2SC                 | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9910-2SCT                | 24-Pb Small Outline IC - Tape and Reel | Commercial      |
|                | CY7B9920-2SC <sup>[20]</sup> | 24-Pb Small Outline IC                 | Commercial      |
| 500            | CY7B9910-5SC                 | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9910-5SCT                | 24-Pb Small Outline IC - Tape and Reel | Commercial      |
|                | CY7B9910-5SI                 | 24-Pb Small Outline IC                 | Industrial      |
|                | CY7B9910-5SIT                | 24-Pb Small Outline IC - Tape and Reel | Industrial      |
|                | CY7B9920-5SC                 | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9920-5SCT                | 24-Pb Small Outline IC - Tape and Reel | Commercial      |
|                | CY7B9920-5SI                 | 24-Pb Small Outline IC                 | Industrial      |
| 750            | CY7B9910-7SC                 | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9910-7SI <sup>[20]</sup> | 24-Pb Small Outline IC                 | Industrial      |
|                | CY7B9920-7SC <sup>[20]</sup> | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9920-7SI <sup>[20]</sup> | 24-Pb Small Outline IC                 | Industrial      |
| <b>Pb-Free</b> |                              |  |                 |
| 250            | CY7B9910-2SXC                | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9910-2SXCT               | 24-Pb Small Outline IC - Tape and Reel | Commercial      |
| 500            | CY7B9910-5SXC                | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9910-5SXCT               | 24-Pb Small Outline IC - Tape and Reel | Commercial      |
|                | CY7B9910-5SXI                | 24-Pb Small Outline IC                 | Industrial      |
|                | CY7B9910-5SXIT               | 24-Pb Small Outline IC - Tape and Reel | Industrial      |
| 750            | CY7B9910-7SXC                | 24-Pb Small Outline IC                 | Commercial      |
|                | CY7B9910-7SXCT               | 24-Pb Small Outline IC - Tape and Reel | Commercial      |

### Package Diagram

Figure 4. 24-Pin (300 Mil) Molded SOIC S13



Note  
20. Not recommended for new design.

## Document History

| Document Title: CY7B9910/CY7B9920 Low Skew Clock Buffer<br>Document Number: 38-07135 |         |            |                 |  |
|--|---------|------------|-----------------|--|
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
| **   | 110244  | 10/28/01   | SZV             | Change from Specification number: 38-00437 to 38-07135   |
| *A   | 1199925 | See ECN    | DPF/AESA        | Added Pb-free parts in Ordering Information<br>Added Note 20: Not recommended for the new design |
| *B   | 1353343 | See ECN    | AESA            | Change status to final   |

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