# CY62167DV30 MoBL®

# 16-Mbit (1M x 16) Static RAM

## Features

- Thin small outline package (TSOP I) Configurable as 1M x 16 or as 2M x 8 SRAM
- Wide voltage range: 2.2 V – 3.6 V
- Ultra-low active power: Typical active current: 2 mA at f = 1 MHz
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}_1$, $CE_2$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed / power
- Available in Pb-free and non Pb-free 48-ball very fine ball grid array (VFBGA) and 48-pin TSOP I package

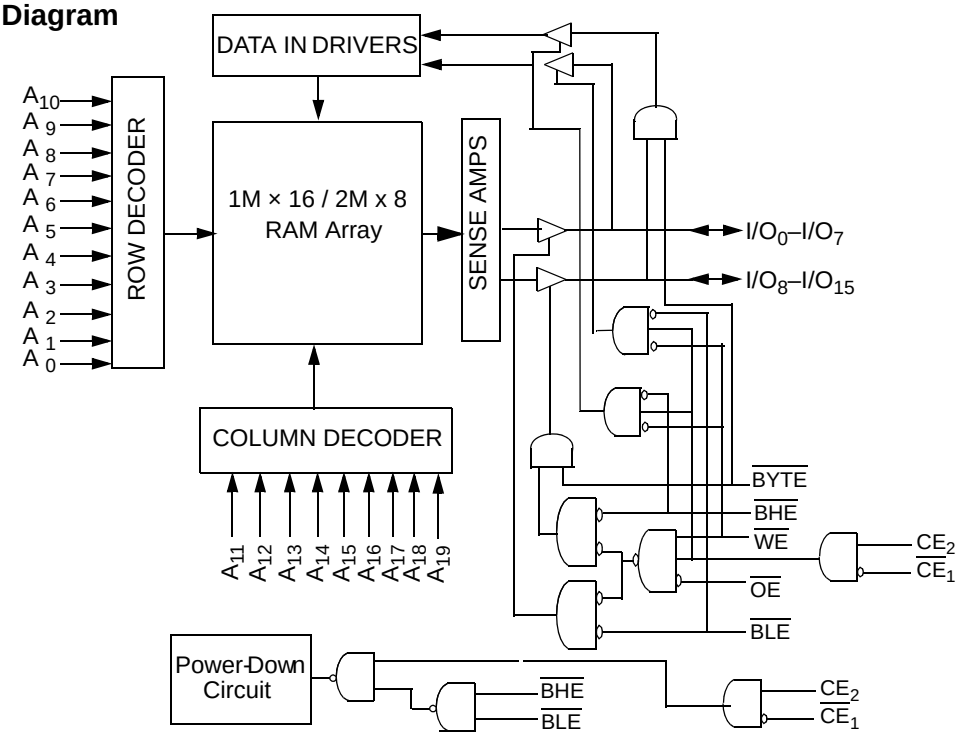
## Functional Description[1]

The CY62167DV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins ($I/O_0$ through $I/O_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, $CE_2$ HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$), is written into the location specified on the address pins ($A_0$ through $A_{19}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{19}$).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on $I/O_8$ to $I/O_{15}$. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

### Logic Block Diagram




**Note**

1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

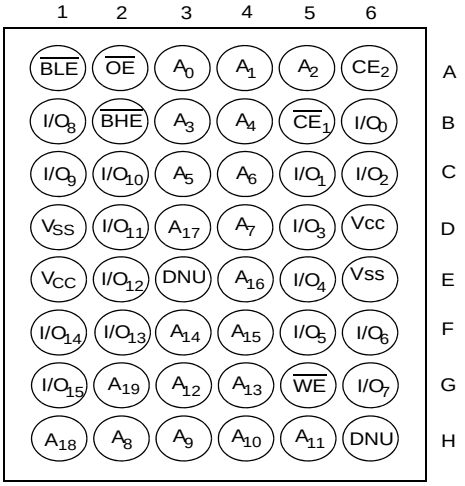
## Contents

## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Operating $I_{CC}$(mA) | | | | Standby $I_{SB2}$(µA) | |
| | | | | | f = 1MHz | | f = $f_{Max}$ | | | |
| | Min | Typ[2] | Max | | Typ[2] | Max | Typ[2] | Max | Typ[2] | Max |
| CY62167DV30LL | 2.2 | 3.0 | 3.6 | 55 | 2 | 4 | 15 | 30 | 2.5 | 22 |
| | | | | 70 | | | 12 | 25 | | |

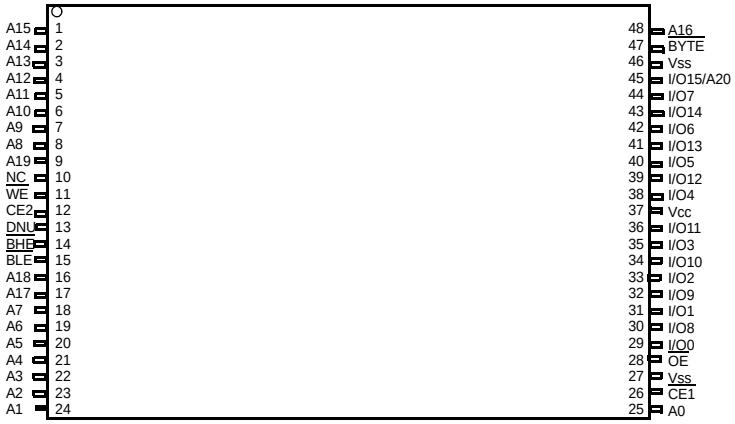
## Pin Configuration

**Figure 1. 48- ball VFBGA Top View**[3, 4, 5]




**48-Pin TSOP I (Forward) (1M x 16/ 2M x 8)**[6]

**Top View**




**Notes**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ.)}$, $T_A$ = 25 °C.
3. NC pins are not connected on the die.
4. DNU pins have to be left floating.
5. Ball H6 for the FBGA package can be used to upgrade to a 32M density.
6. The BYTE pin in the 48-TSOP I package has to be tied to $V_{CC}$ to use the device as a 1M X 16 SRAM. The 48-TSOPI package can also be used as a 2M X 8 SRAM by tying the BYTE signal to $V_{SS}$. In the 2M x 8 configuration, Pin 45 is A20, while BHE, BLE and I/O8 to I/O14 pins are not used (DNU).

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.2 V to $V_{CC}$ + 0.3 V

DC voltage applied to outputs in High-Z state[7, 8] ..... –0.2 V to $V_{CC}$ + 0.3 V

DC input voltage[7, 8] ..... –0.2 V to $V_{CC}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$[9] |
|---|---|---|---|
| CY62167DV30LL | Industrial | –40 °C to +85 °C | 2.20 V to 3.60 V |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | CY62167DV30-55 | | | CY62167DV30-70 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[10] | Max | Min | Typ[10] | Max | |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –0.1 mA | $V_{CC}$ = 2.20 V | 2.0 | – | – | 2.0 | – | – | V |
| | | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 2.70 V | 2.4 | | | 2.4 | | | |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 0.1 mA | $V_{CC}$ = 2.20 V | – | – | 0.4 | | – | 0.4 | V |
| | | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 2.70 V | | | | | | | |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ = 2.2 V to 2.7 V | | 1.8 | – | $V_{CC}$ +0.3 V | 1.8 | – | $V_{CC}$ +0.3V | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | 2.2 | | | 2.2 | | | |
| $V_{IL}$ | Input LOW voltage | $V_{CC}$ = 2.2 V to 2.7 V | | –0.3 | – | 0.6 | –0.3 | – | 0.6 | V |
| | | $V_{CC}$= 2.7 V to 3.6 V | | | | 0.8 | | | 0.8 | |
| $I_{IX}$ | Input leakage current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | – | +1 | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | | –1 | – | +1 | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating supply current | $V_{CC}$ = $V_{CC(max)}$ $I_{OUT}$ = 0 mA CMOS levels | f = $f_{Max}$ = $1/t_{RC}$ | – | 15 | 30 | – | 12 | 25 | mA |
| | | | f = 1 MHz | | 2 | 4 | | 2 | 4 | |
| $I_{SB1}$ | Automatic Power-down current — CMOS inputs | $\overline{CE_1}$ ≥ $V_{CC}$ – 0.2 V or $CE_2$ ≤ 0.2 V, $V_{IN}$ ≥ $V_{CC}$ – 0.2 V, $V_{IN}$ ≤ 0.2 V, f = $f_{Max}$ (Address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$), $V_{CC}$ = 3.60 V | | – | 2.5 | 22 | – | 2.5 | 22 | µA |
| $I_{SB2}$ | Automatic Power-down current — CMOS Inputs | $\overline{CE_1}$ ≥ $V_{CC}$ – 0.2 V or $CE_2$ ≤ 0.2 V $V_{IN}$ ≥ $V_{CC}$ – 0.2 V or $V_{IN}$ ≤ 0.2V, f = 0, $V_{CC}$ = 3.60 V | | – | 2.5 | 22 | – | 2.5 | 22 | µA |

**Notes**

7. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
8. $V_{IH(max)}$ = $V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
9. Full Device AC operation requires linear $V_{CC}$ ramp from 0 to $V_{CC(min.)}$ and $V_{CC}$ must be stable at $V_{CC(min)}$ for 500 µs.
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C

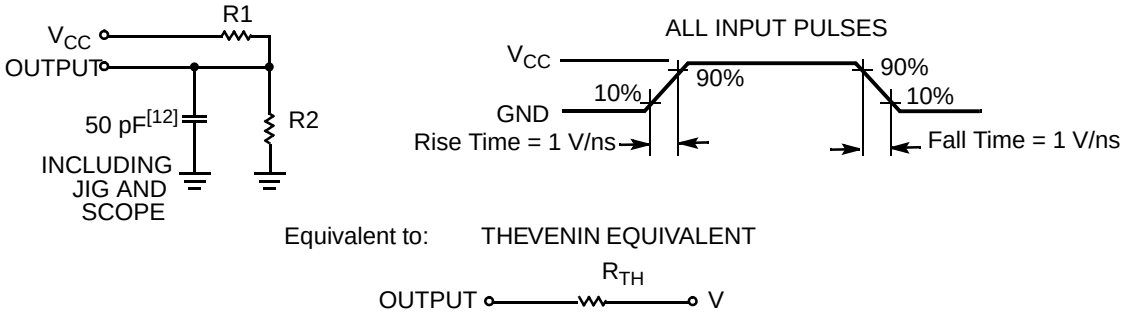
## Capacitance

| Parameter[11] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 8 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter[11] | Description | Test Conditions | VFBGA | TSOP I | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (Junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board | 55 | 60 | °C / W |
| $\Theta_{JC}$ | Thermal resistance (Junction to case) | | 16 | 4.3 | °C / W |

## AC Test Loads and Waveforms



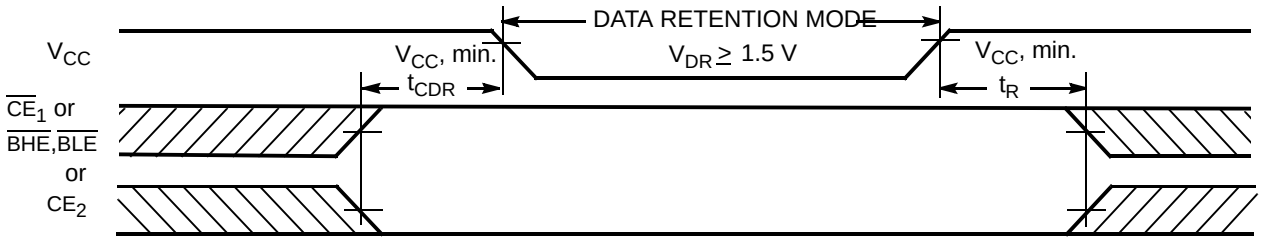

| Parameters | 2.5 V | 3.0 V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | | Min | Typ[12] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data retention | | | 1.5 | – | – | V |
| $I_{CCDR}$ | Data retention current | $V_{CC}$= 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$V or $V_{IN} \leq 0.2$ V | | – | – | 10 | µA |
| $t_{CDR}$[11] | Chip deselect to data retention time | | | 0 | – | – | ns |
| $t_R$[13] | Operation recovery time | | CY62167DV30LL-55 | 55 | – | – | ns |
| | | | CY62167DV30LL-70 | 70 | | | |

**Notes**
11. Tested initially and after any design or process changes that may affect these parameters.
12. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C
13. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)}$ ≥ 100 µs or stable at $V_{CC(min.)}$ ≥ 100 µs.

## Data Retention Waveform[14]




## Switching Characteristics Over the Operating Range

| Parameter[15] | Description | 55 ns | | 70 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read cycle time | 55 | – | 70 | – | ns |
| $t_{AA}$ | Address to data valid | – | 55 | – | 70 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE_1}$ LOW and $CE_2$ HIGH to data valid | – | 55 | – | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 25 | – | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to LOW Z[16] | 5 | – | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[16, 17] | – | 20 | – | 25 | ns |
| $t_{LZCE}$ | $\overline{CE_1}$ LOW and $CE_2$ HIGH to Low Z[16] | 10 | – | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE_1}$ HIGH and $CE_2$ LOW to High Z[16, 17] | – | 20 | – | 25 | ns |
| $t_{PU}$ | $\overline{CE_1}$ LOW and $CE_2$ HIGH to Power-up | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE_1}$ HIGH and $CE_2$ LOW to Power-down | – | 55 | – | 70 | ns |
| $t_{DBE}$ | BLE/BHE LOW to data valid | – | 55 | – | 70 | ns |
| $t_{LZBE}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[16] | 10 | – | 10 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$/$\overline{BHE}$ HIGH to HIGH Z[16, 17] | – | 20 | – | 25 | ns |
| **Write Cycle**[18] | | | | | | |
| $t_{WC}$ | Write cycle time | 55 | – | 70 | – | ns |
| $t_{SCE}$ | $\overline{CE_1}$ LOW and $CE_2$ HIGH to write end | 40 | – | 60 | – | ns |
| $t_{AW}$ | Address set-up to write end | 40 | – | 60 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address set-up to write start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 40 | – | 45 | – | ns |
| $t_{BW}$ | $\overline{BLE}$/$\overline{BHE}$ LOW to write end | 40 | – | 60 | – | ns |
| $t_{SD}$ | Data set-up to write end | 25 | – | 30 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[16, 17] | – | 20 | – | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[16] | 10 | – | 10 | – | ns |

**Notes**

14. $\overline{BHE}$.$\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
15. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the “AC Test Loads and Waveforms” section.
16. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
17. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
18. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$, and $CE_2$ = $V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

## Switching Waveforms

**Figure 2. Read Cycle 1 (Address Transition Controlled)[19, 20]**

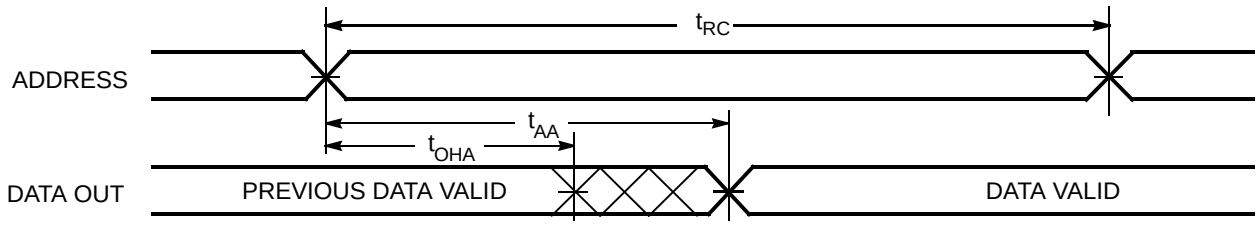
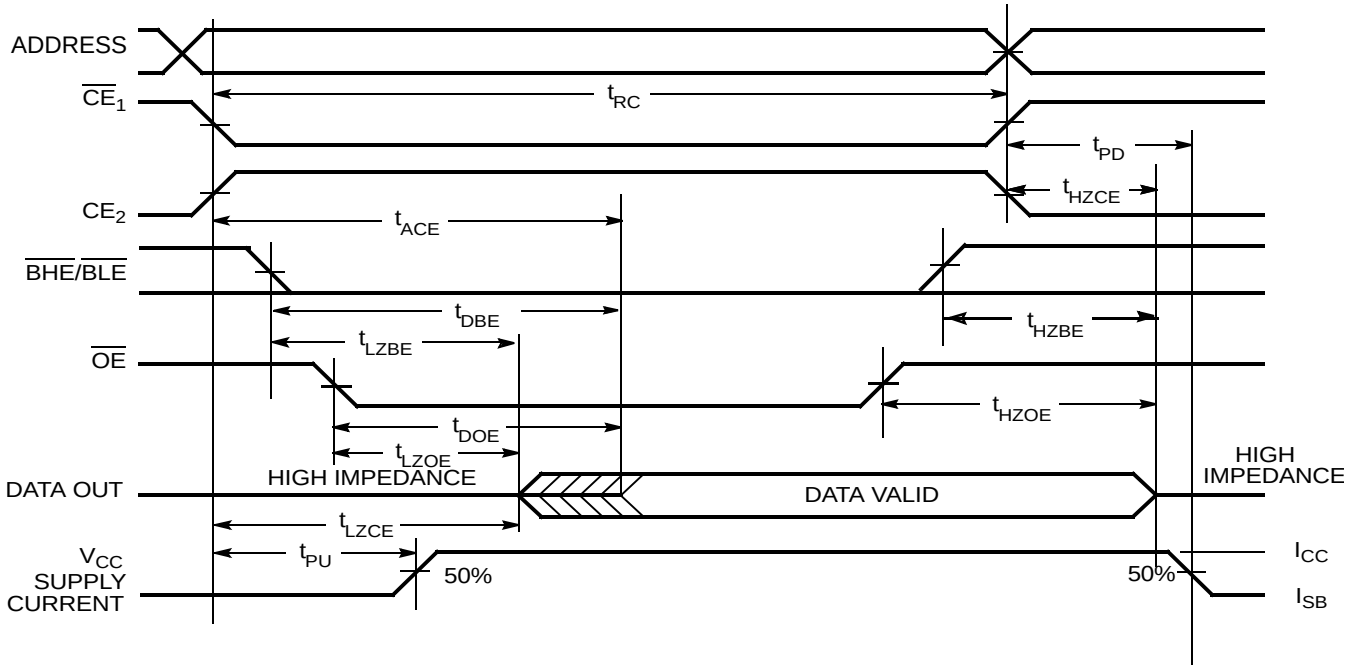


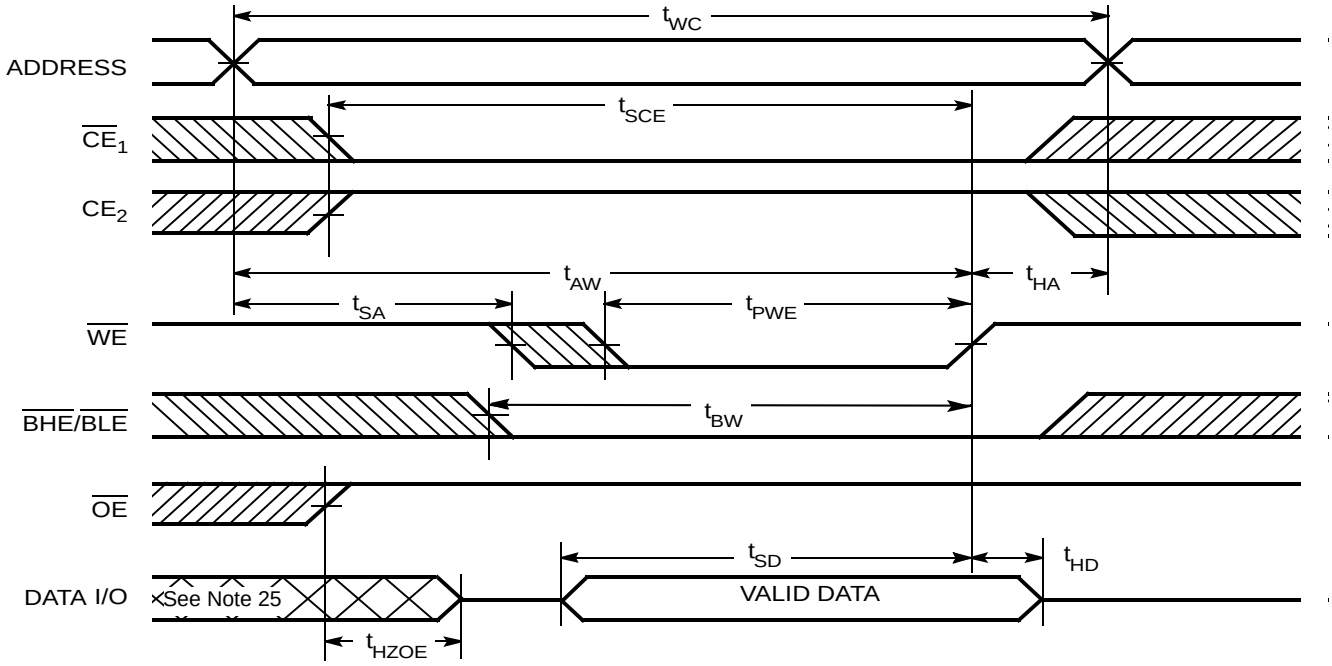

**Figure 3. Read Cycle 2 ($\overline{OE}$ Controlled)[20, 21]**




**Notes**
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and $CE_2$ transition HIGH.

## Switching Waveforms (continued)

**Figure 4. Write Cycle 1 ($\overline{WE}$ Controlled)**[22, 23, 24]




**Notes**

22. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$, and $CE_2$ = $V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.
23. Data I/O is high-impedance if $\overline{OE}$ = $V_{IH}$.
24. If $\overline{CE_1}$ goes HIGH and $CE_2$ goes LOW simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high-impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Figure 5. Write Cycle 2 ($\overline{CE_1}$ or $CE_2$ Controlled)[26, 27, 28]**

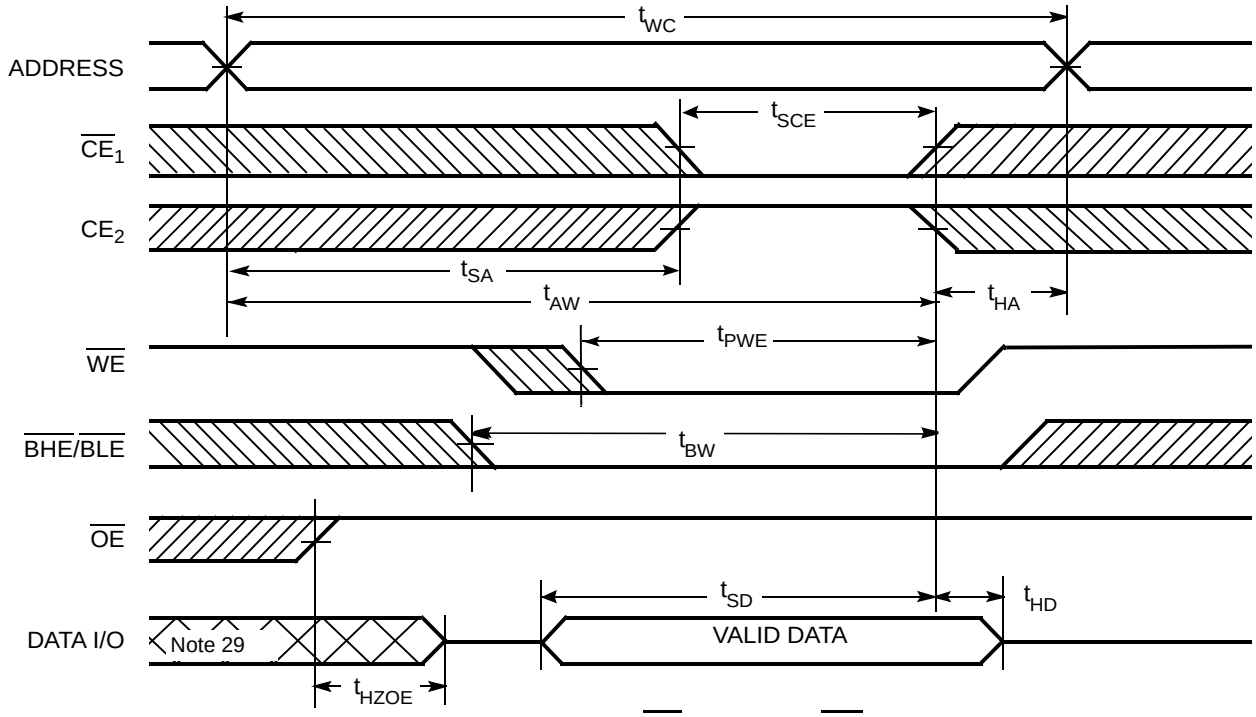
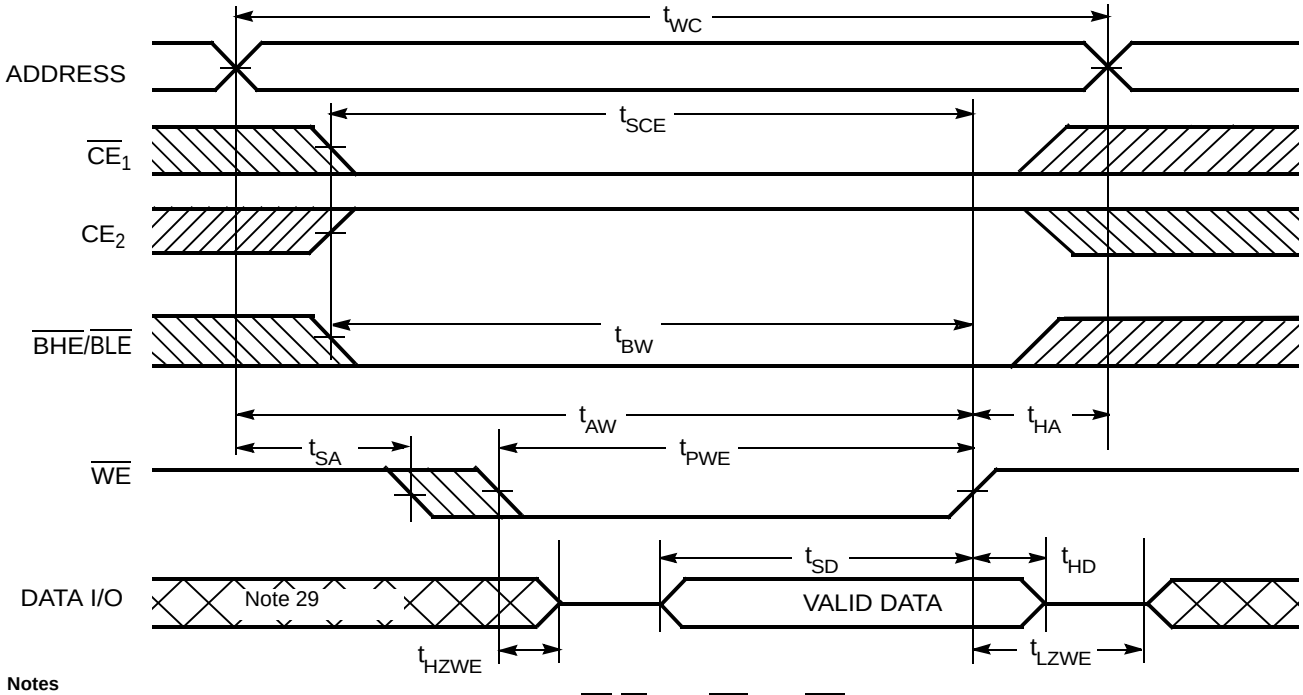



**Figure 6. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[28]**

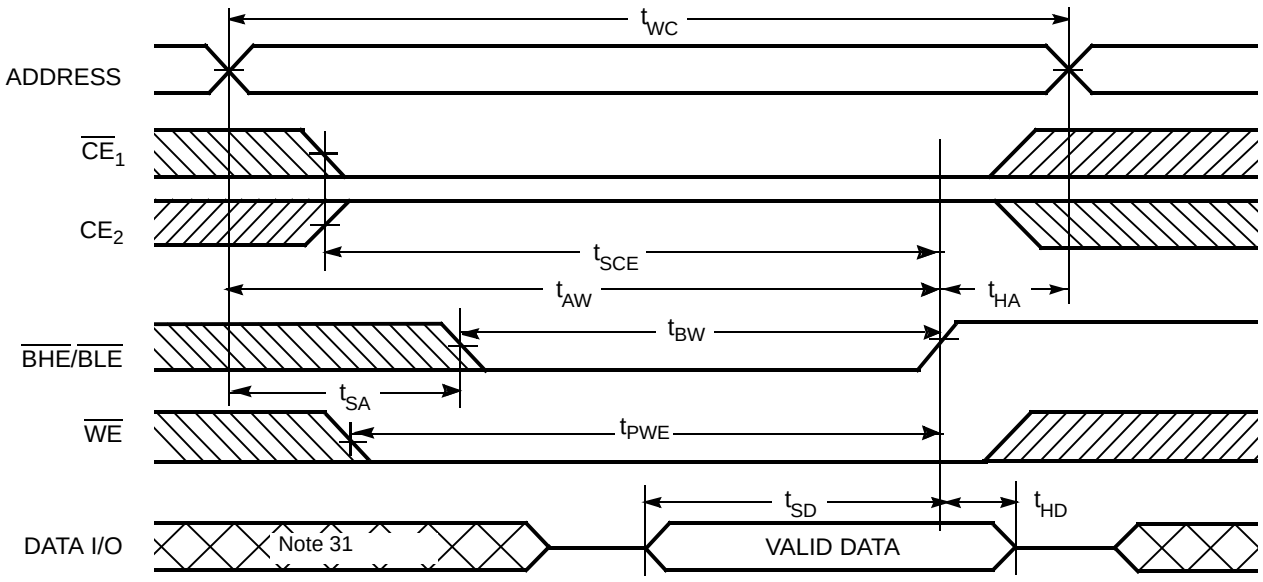



**Notes**

26. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$, and $CE_2$ = $V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.
27. Data I/O is high-impedance if $\overline{OE}$ = $V_{IH}$
28. If $\overline{CE_1}$ goes HIGH and $CE_2$ goes LOW simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high-impedance state.
29. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Figure 7. Write Cycle 4 (BHE/BLE Controlled, OE LOW)[30]**




**Notes**
30. If $\overline{CE_1}$ goes HIGH and $CE_2$ goes LOW simultaneously with $\overline{WE}$ = $V_{IH}$, the output remains in a high-impedance state
31. During this period, the I/Os are in output state and input signals should not be applied.

## Truth Table

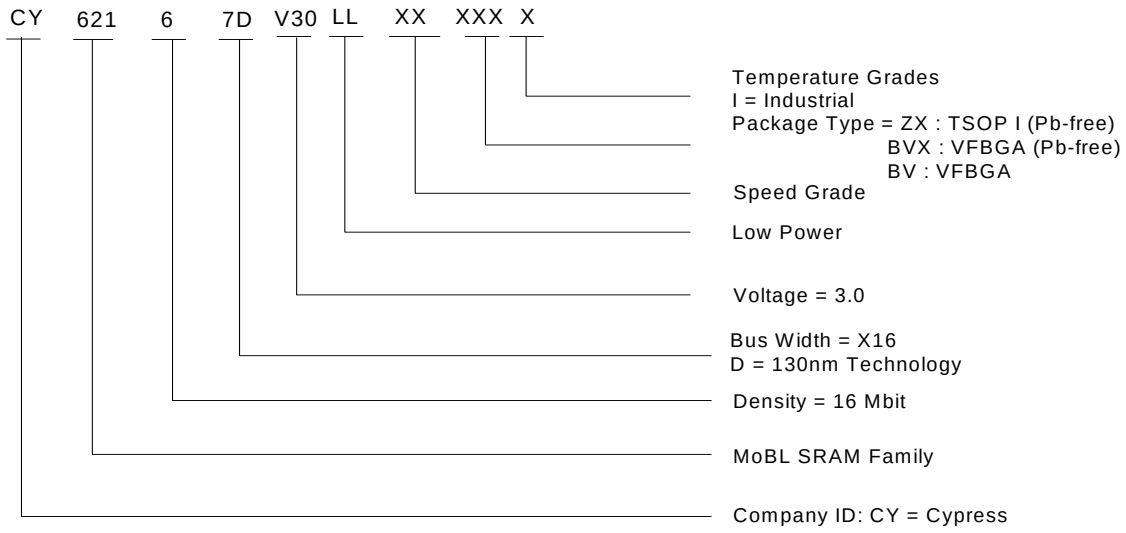
| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X | L | X | X | X | X | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X | X | X | X | H | H | High Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | H | L | L | L | Data out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | H | L | High Z ($I/O_8$–$I/O_{15}$); Data out ($I/O_0$–$I/O_7$) | Read | Active ($I_{CC}$) |
| L | H | H | L | L | H | Data out ($I/O_8$–$I/O_{15}$); High Z ($I/O_0$–$I/O_7$) | Read | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data in ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | H | L | X | H | L | High Z ($I/O_8$–$I/O_{15}$); Data in ($I/O_0$–$I/O_7$) | Write | Active ($I_{CC}$) |
| L | H | L | X | L | H | Data in ($I/O_8$–$I/O_{15}$); High Z ($I/O_0$–$I/O_7$) | Write | Active ($I_{CC}$) |
| L | H | H | H | L | H | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | H | L | High Z | Output disabled | Active ($I_{CC}$) |
| L | H | H | H | L | L | High Z | Output disabled | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62167DV30LL-55BVI | 51-85178 | 48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) | Industrial |
| | CY62167DV30LL-55BVXI | | 48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) (Pb-free) | |
| | CY62167DV30LL-55ZXI | 51-85183 | 48-pin TSOP I (12 x 18.4 x 1 mm) (Pb-free) | |
| 70 | CY62167DV30LL-70BVI | 51-85178 | 48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) | |

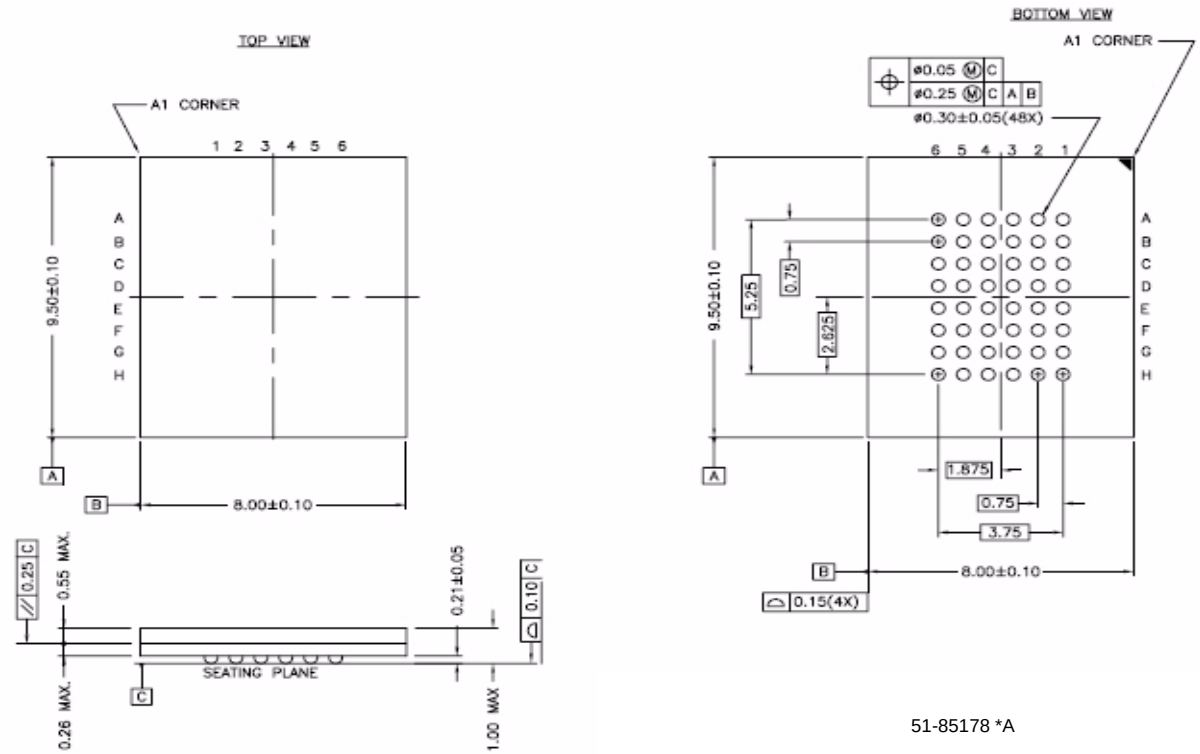
Please contact your local Cypress sales representative for availability of these parts

### Ordering Code Definition



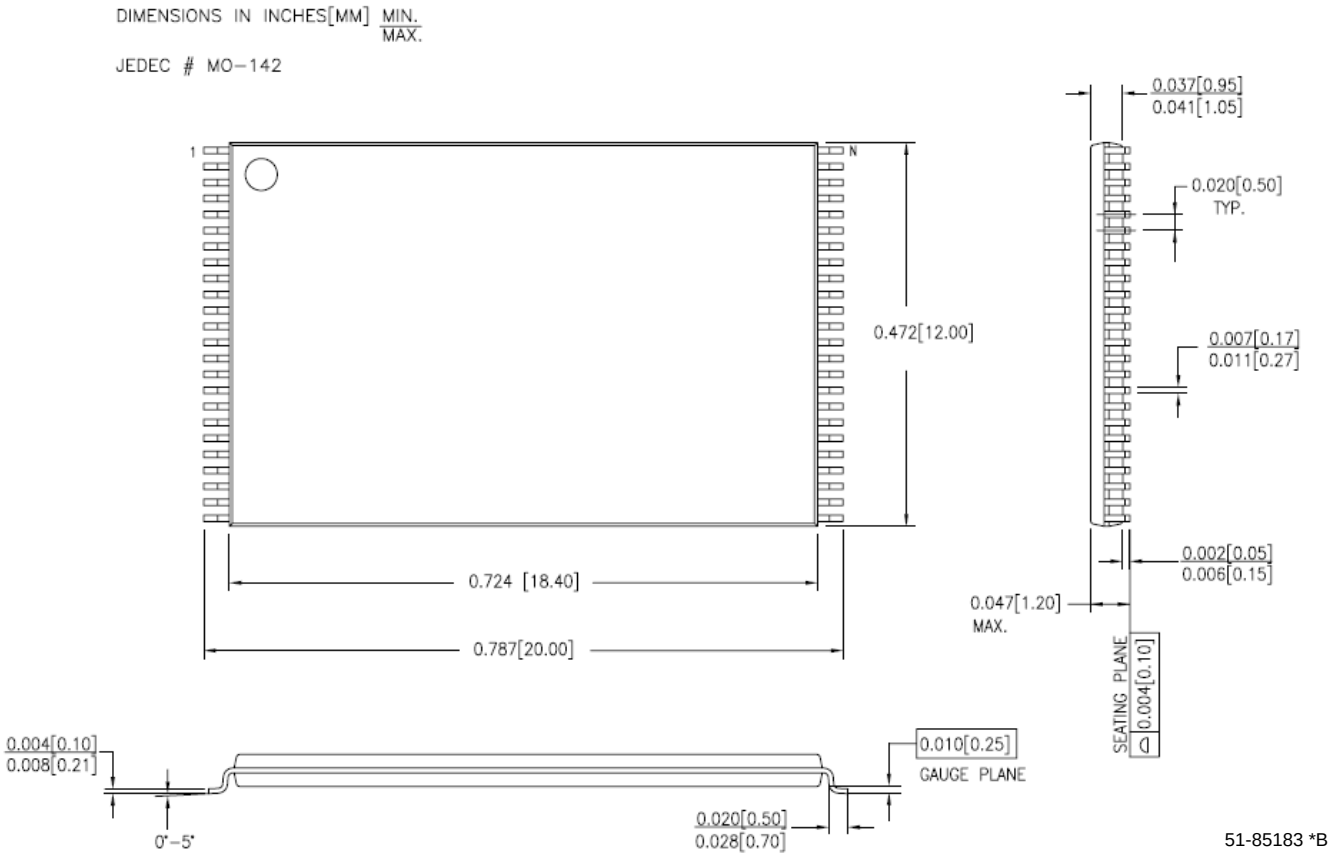
## Package Diagrams

**48-ball VFBGA (8 x 9.5 x 1 mm) (51-85178)**




51-85178 *A

**48-pin TSOP I (12 x 18.4 x 1 mm) (51-85183)**



## Acronyms

| Acronym | Description |
|---|---|
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| SRAM | static random access memory |
| VFBGA | very fine ball grid array |
| TSOP | thin small outline package |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| µA | microamperes |
| mA | milliampere |
| MHz | megahertz |
| ns | nanoseconds |
| pF | picofarads |
| V | volts |
| Ω | ohms |
| W | watts |

## Document History Page

| Document Title: CY62167DV30 MoBL®, 16-Mbit (1M x 16) Static RAM<br>Document Number: 38-05328 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 118408 | 09/30/02 | GUG | New Data Sheet |
| *A | 123692 | 02/11/03 | DPM | Changed Advanced to Preliminary<br>Added package diagram |
| *B | 126555 | 04/25/03 | DPM | Minor change: Changed Sunset Owner from DPM to HRT |
| *C | 127841 | 09/10/03 | XRJ | Added 48 TSOP I package |
| *D | 205701 | | AJU | Changed $\overline{\text{BYTE}}$ pin usage description for 48 TSOPI package |
| *E | 238050 | See ECN | KKV/AJU | Replaced 48-ball VFBGA package diagram; Modified Package Name in Ordering Information table from BV48A to BV48B |
| *F | 304054 | See ECN | PCI | Added 45-ns Speed Bin in AC, DC and Ordering Information tables<br>Added Footnote #12 on page #4<br>Added Pb-free packages on page # 10 |
| *G | 492895 | See ECN | VKN | Modified datasheet to explain x8 configurability<br>Removed L power bin from the product offering<br>Updated Ordering Information Table |
| *H | 2896036 | 03/19/2010 | AJU | Removed 45-ns. Removed inactive parts from Ordering Information.<br>Updated Packaging Information<br>Updated links in Sales, Solutions, and Legal Information. |
| *I | 3067267 | 11/08/2010 | RAME | Updated datasheet as per new template<br>Added Ordering Code Definition, Acronyms and Units of Measure.<br>Updated all tablenotes to footnote.<br>Package diagram updated 51-85178 from ** to *A |

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